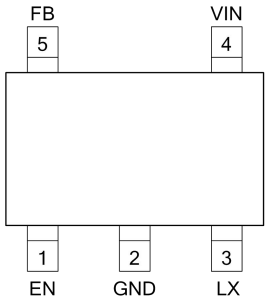
WD1039EB

High Efficiency 2A continuous, 2.5A peak, 1MHz Synchronous Step Down Regulator

Http//:www.sh-willsemi.com

SOT-23-5L



SOT-23-5L

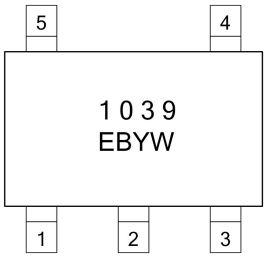
Descriptions

The WD1039EB is a high efficiency, synchronous step down DC-DC convertor optimized for battery powered portable applications. It supports up to 2A continuous 2.5A peak output current. With a wide input voltage range of 2.7V to 5.5V, the device supports applications powered by single Li-ion battery with extended voltage range, two and three alkaline cell, 3.3V and 5V input voltage range. The WD1039EB operates at 1MHz fixed switching frequency with Pulse-Width-Modulation (PWM) and enters Pulse-Skipping-Modulation (PSM) operation at light load current to maintain high efficiency over the entire load current range. 100% duty cycle capability provides low dropout operation, extending battery life in portable systems.

The switching frequency is internally set at 1MHz, allowing the use of tiny surface mount inductor and input/output capacitors.

The WD1039EB is available in SOT-23-5L package. Standard product is Pb-free and Halogen -free.

Pin configuration (Top view)



SOT-23-5L

1039 = Device code
EB = Package code
Y = Year code
W = Week code

Marking

Features

- Input voltage range : 2.7~5.5V
- Continue output current : 2A continuous
  2.5A peak
- Switching frequency : 1MHz (Typ.)
- Efficiency : Up to 96%
- Feedback reference voltage : 0.6V
- 100% duty cycle for low dropout operation
- Adjustable Output Voltage

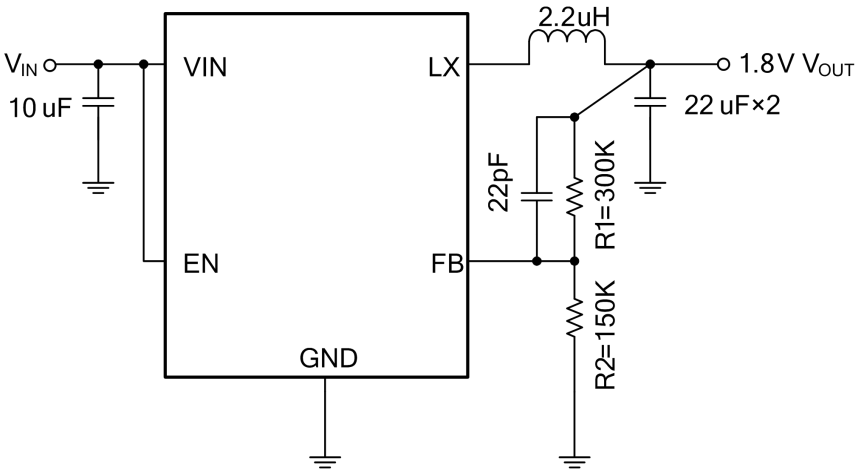
Applications

- Cellphones
- PADs
- STBs

Order information

Device	Package	Shipping
WD1039EB-5/TR	SOT-23-5L	3000/Reel&Tape

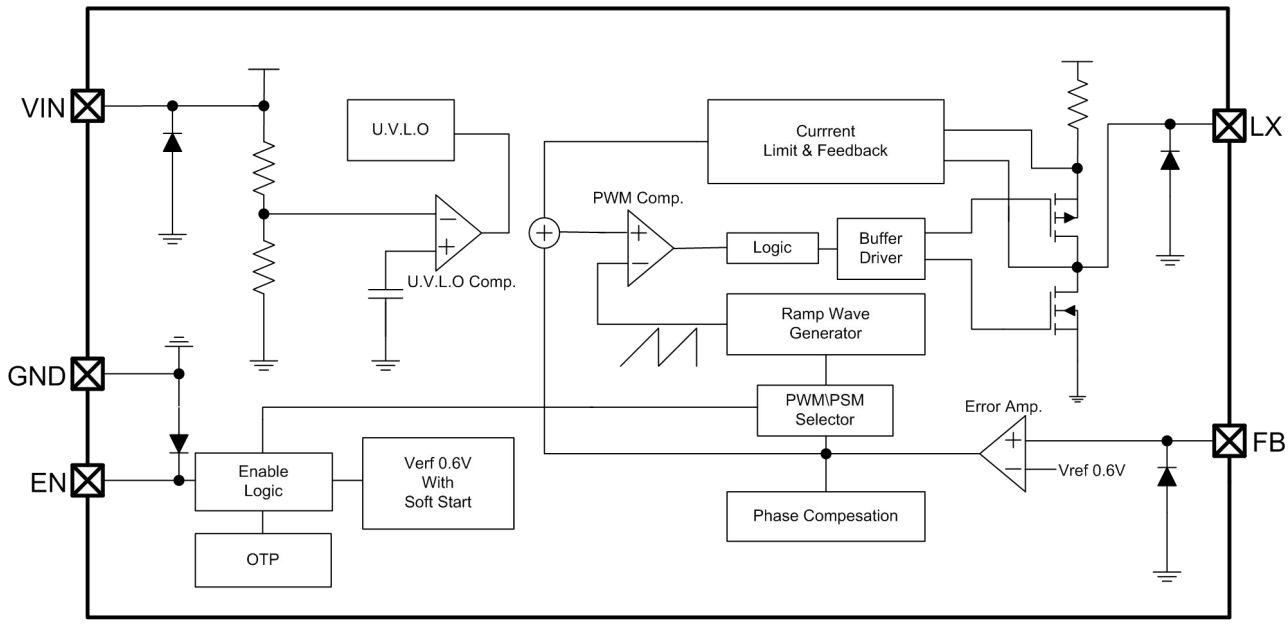
Typical applications



Pin descriptions

Symbol	Pin Number	Descriptions
EN	1	Enable, Active High
GND	2	Ground
LX	3	Switching signal output
VIN	4	Input Voltage
FB	6	Feedback

Block diagram



Absolute maximum ratings

Parameter	Symbol	Value	Unit
VIN pin voltage range	V_{IN}	-0.3～6.5	V
EN, FB pin voltage range	-	-0.3～V_{IN}	V
SW pin voltage range (DC)	-	-0.3～V_{IN}	V
Power Dissipation – SOT-23-5L (Note 1)	P_D	0.5	W
Junction to Ambient Thermal Resistance – SOT-23-5L (Note 1)	$R_{\theta JA}$	250	°C/W
Junction temperature	T_J	150	°C
Lead temperature(Soldering, 10s)	T_L	260	°C
Operating ambient temperature	Topr	-40 ~ 85	°C
Storage temperature	Tstg	-55 ~ 150	°C
ESD Ratings	HBM	8000	V
	MM	400	V

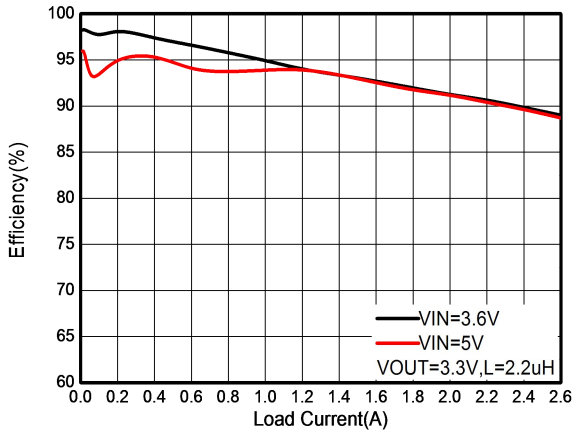
These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note 1: Surface mounted on FR-4 Board using 1 square inch pad size, dual side, 1oz copper

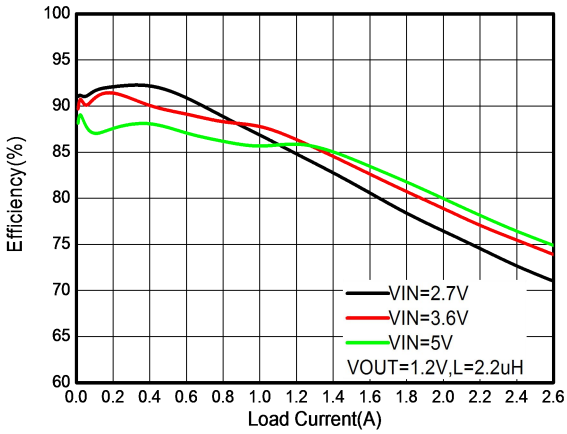
Electronics Characteristics (Ta=25°C, V_{IN}=3.6V, V_{EN}=V_{IN}, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		2.7		5.5	V
Operating Supply Current	I_Q	V_{FB} = 60%, I_{OUT} = 0A		340		uA
Standby Supply Current	I_Q	V_{FB} = 105%, I_{OUT} = 0A		80		uA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, V_{IN}=4.2V			1	uA
Feedback reference Voltage	V_{FB}		0.588	0.60	0.612	V
Line Regulation	$\triangle_{LINE}$	V_{IN} = 2.7V to 5.5V I_{OUT} =10mA		0.05	1	%/V
Load Regulation	$\triangle_{LOAD}$	I_{OUT} = 10mA to 1A		1.4		%
Inductor Limit Current	I_{LIM}	V_{IN} = 3.6V, V_{OUT} = 90%*V_{OUT}	2.6			A
Oscillator Frequency	f_{OSC}	V_{FB} or V_{OUT} in regulation	0.8	1	1.2	MHz
		V_{FB} or V_{OUT} to GND		250		KHz
$R_{DS(ON)}$ of P-Channel FET	R_{PFET}	I_{SW} = 100mA, V_{IN}=3.6V		0.12		Ω
$R_{DS(ON)}$ of N-Channel FET	R_{NFET}	I_{SW} = −100mA, V_{IN}=3.6V		0.08		Ω
Feedback Leakage Current	I_{FB}				±30	nA
SW Leakage Current	I_{LSW}	V_{IN} = 5V, V_{SW} = 0V or 5V			±1	uA
EN Rising Threshold	V_{ENH}		1.4			V
EN falling Threshold	V_{ENL}				0.4	V
EN Leakage Current	I_{EN}	V_{IN} = 5V, V_{EN} = 0V or VIN			1	uA
Over Temperature Protection	T_{OTP}			165		°C
OTP Hysteresis				30		°C
Discharge Resistance	R_{LOW}	V_{IN} = 5V, V_{EN} = 0V		200		Ω

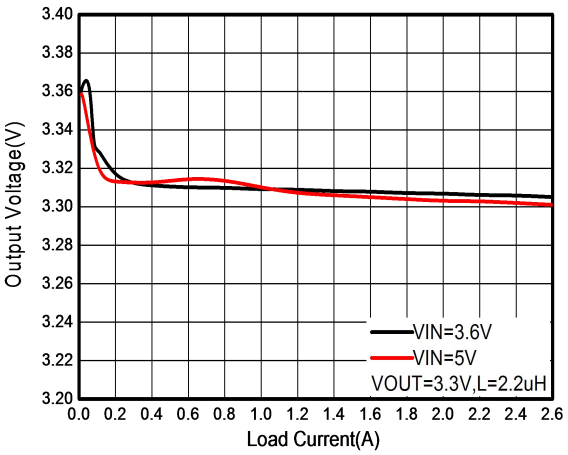
Typical Characteristics (Ta=25°C, V_{IN}=3.6V, unless otherwise noted)



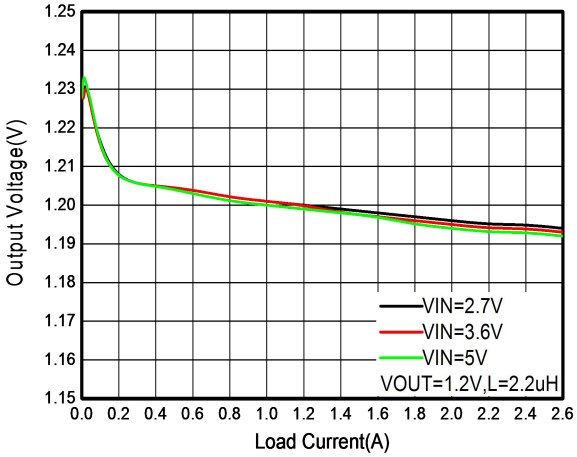
Efficiency vs. Load Current



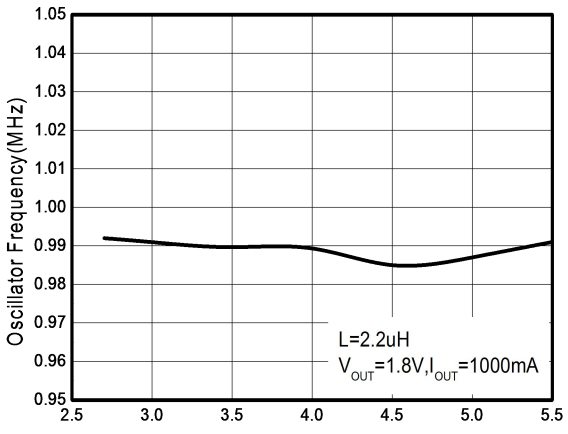
Efficiency vs. Load Current



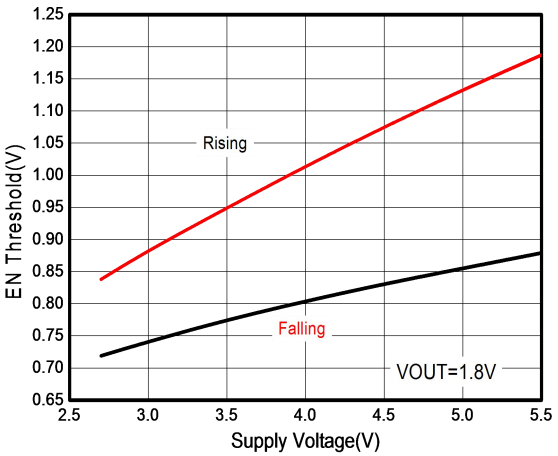
Output Voltage vs. Load Current



Output Voltage vs. Load Current

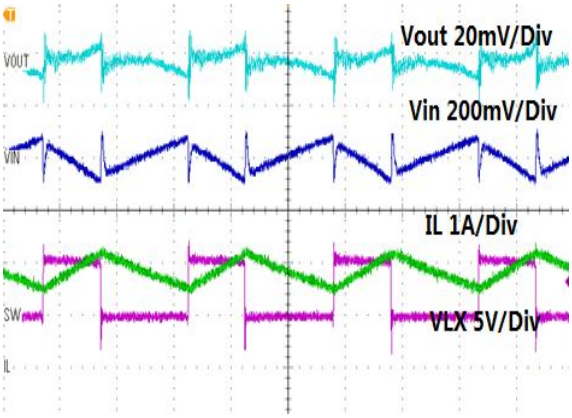


Oscillator Frequency vs Input Voltage



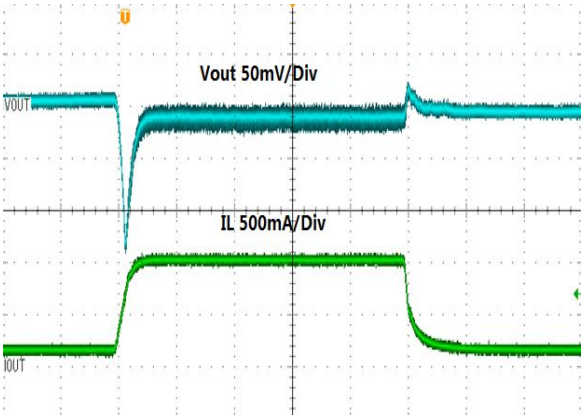
EN Threshold vs. Input Voltage

Output Ripple
（Vin=5V，Vout=1.8V，I_{LOAD}=1.8A）



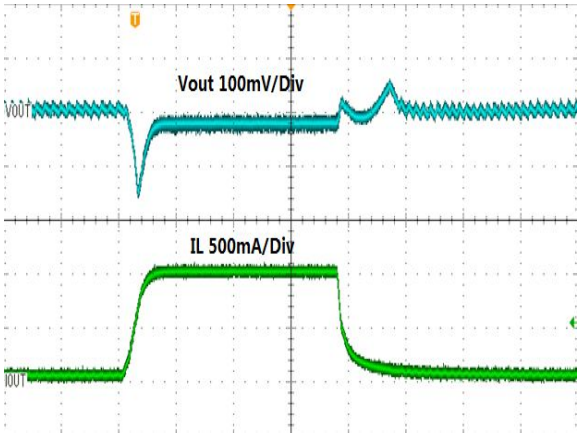
400ns/div

Load Transient
（Vin=5V，Vout=1.8V，I_{LOAD}=0.14~1A）



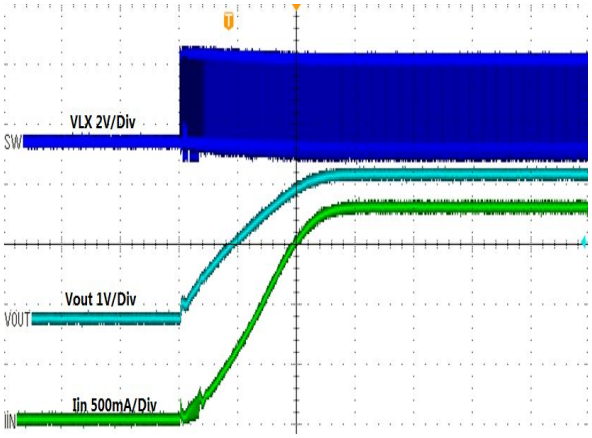
80us/div

Load Transient
（Vin=3.6V，Vout=1.8V，I_{LOAD}=0.04~1A）



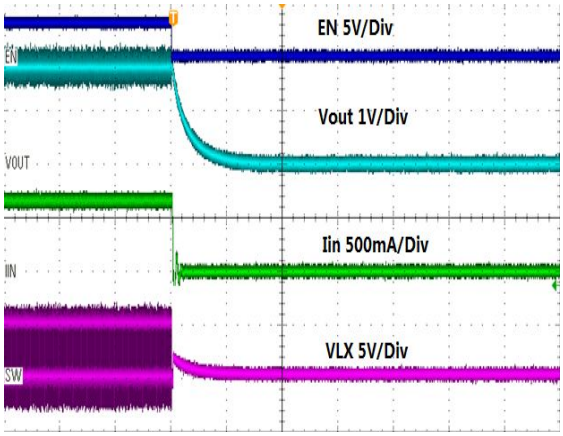
80us/div

Turn on from Enable
（Vin=4.2V，Vout=2.4V，I_{LOAD}=2A）



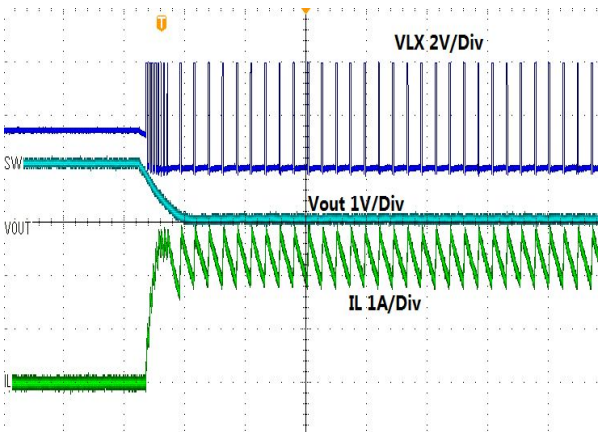
400us/div

Turn off from Enable
（Vin=3.6V，Vout=1.8V，I_{LOAD}=1.8A）



80us/div

Vout short to GND transient
（Vin=4V）



20us/div

Operation Information

PWM Control Mode

The WD1039EB step-down converter operates with typically 1MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. Both the main P-channel MOSFET and synchronous N-channel MOSFET switches are internal. During PWM operation, the converter uses a current-mode control scheme to achieve good line and load transient response. At the beginning of each clock cycle initiated by the clock signal, the main switch is turned on. The current flows from the input capacitor via the main switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turn off the switch. After a dead time, which prevents shoot-through current, the synchronous switch is turned on and the inductor current ramps down. The current flows from the inductor and the output capacitor to the load. It returns back to the inductor through the synchronous switch.

The next cycle is initiated by the clock signal again turning off the synchronous switch and turning on the main switch.

Pulse Skipping Mode (PSM)

At light loads, the inductor current may reach zero or reverse on each pulse. The synchronous switch is turned off by the current reversal comparator, I_{RCMP}, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At very light loads, the WD1039EB will automatically skip pulses in pulse skipping mode (PSM) operation to maintain output regulation.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 250KHz. This frequency fold back ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 1MHz when V_{FB} rises above 0V.

Dropout Operation

The device starts to enter 100% duty-cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the main switch is turned on 100% for one or more cycles. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Shutdown Mode

Drive EN to GND to place the WD1039EB in shutdown mode. In shutdown mode, the reference, control circuit, main switch, and synchronous switch turn off and the output becomes high impedance. Input current falls to 0.1μA (Typ.) during shutdown mode.

Over Temperature Protection (OTP)

As soon as the junction temperature (T_J) exceeds 165°C (Typ.), the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFET are turned off.

Application Information

External component selection for the application circuit depends on the load current requirements. Certain tradeoffs between different performance parameters can also be made.

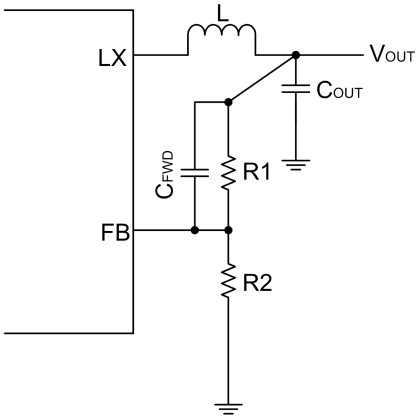
Output Voltage Setting

The output voltage can be calculated as:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in figure as below. To minimize the current through the feedback divider network, R1 should be larger than 100kΩ. The sum of R1 and R2 should not exceed 1 MΩ, to keep the network robust against noise. An external feed forward capacitor C_{FWD}, is required for optimum load transient response. The value of C_{FWD} should be in the range between 22pF and 33pF.

Route the FB line away from noise sources, such as the inductor or the LX line.



Inductor Selection

The WD1039EB high switching frequency allows the use of a physically small inductor. The inductor ripple current is determined by

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where △I_L is the peak-to-peak inductor ripple current and f is the switching frequency. The inductor peak-to-peak current ripple is typically set to be 40% of the maximum dc load current. Using this guideline and solving for L,

$$L = \frac{V_{OUT}}{f(40\% I_{LOAD(MAX)})}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

It is important to ensure that the inductor is capable of handling the maximum peak inductor current, I_{LPK}, determined by

$$I_{LPK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field EMI requirements than on what the WD1039EB requires to operate.

Input Capacitor Selection

Capacitor ESR is a major contributor to input ripple in high-frequency DC-DC converters. Ordinary aluminum electrolytic capacitors have high ESR and should be avoided. Low-ESR tantalum or polymer capacitors are better and provide a compact solution for space constrained surface mount designs. Ceramic capacitors have the lowest overall ESR. The input filter capacitor reduces peak currents and noise at the input voltage source. Connect a low ESR bulk capacitor to the input. Select this bulk capacitor to meet the input ripple requirements and voltage rating rather than capacitance value. Use the following equation to calculate the maximum RMS input current:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}}\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

Output Capacitor Selection

Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1-\frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

At nominal load current, the device operates in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V = V_{OUT} \times \frac{1-\frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right)$$

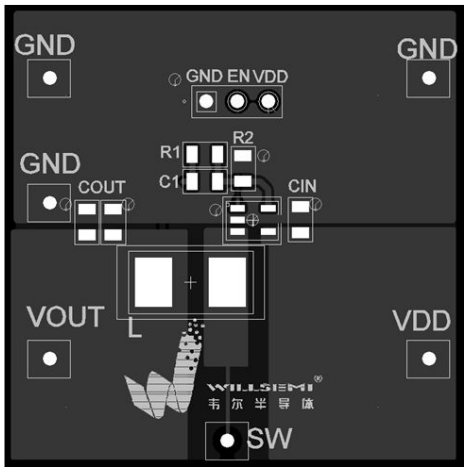
At light load currents, the converter operates in pulse skipping mode, and the output voltage ripple is dependent on the capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PSM operation and tighten dc output accuracy in PSM operation.

PC Board Layout Considerations

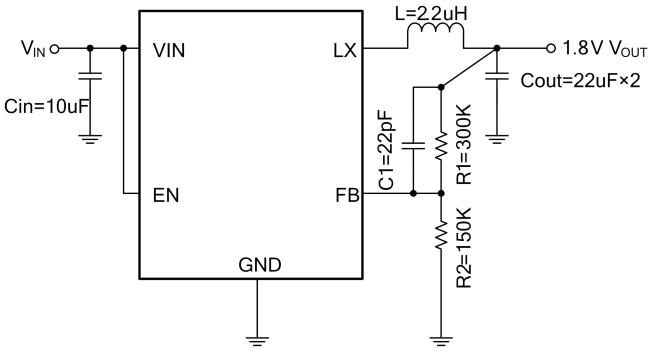
A good circuit board layout aids in extracting the most performance from the WD1039EB. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance.

The evaluation board layout is optimized for the WD1039EB. Use this layout for best performance. If this layout needs changing, use the following guidelines:

1. Use separate analog and power ground planes. Connect the sensitive analog circuitry (such as voltage divider components) to analog ground; connect the power components (such as input and output bypass capacitors) to power ground. Connect the two ground planes together near the load to reduce the effects of voltage dropped on circuit board traces. Locate C_{IN} as close to the V_{IN} pin as possible, and use separate input bypass capacitors for the analog.
2. Route the high current path from C_{IN}, through L, to the SW and PGND pins as short as possible.
3. Keep high current traces as short and as wide as possible.
4. Place the feedback resistors as close as possible to the FB pin to prevent noise pickup.
5. Avoid routing high impedance traces, such as FB, near the high current traces and components or near the switch node (LX).
6. If high impedance traces are routed near high current and/or the SW node, place a ground plane shield between the traces.



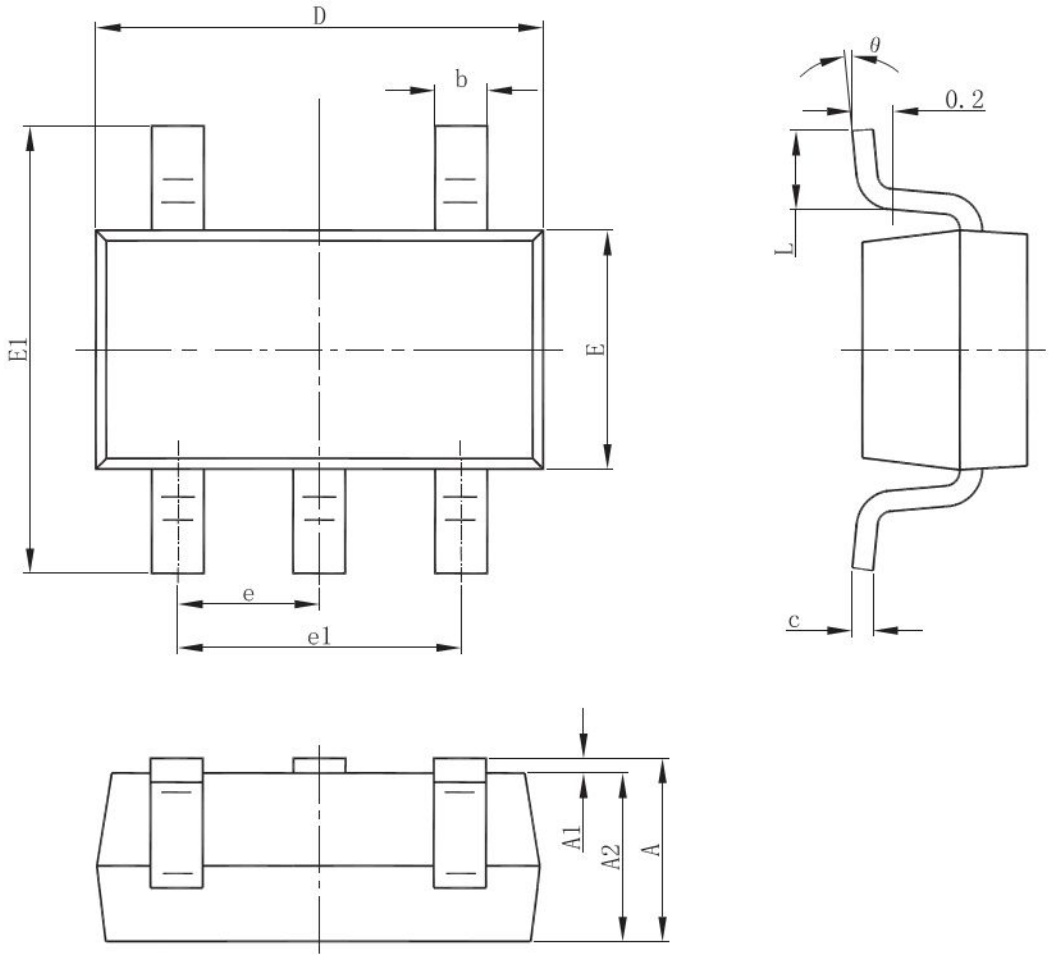
WD1039EB PCB Suggest Layout (Demo)



WD1039EB Demo Schematic

Package outline dimensions

SOT-23-5L



Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.050	-	1.250
A1	0.000	-	0.100
A2	1.050	-	1.150
b	0.300	0.400	0.500
c	0.100	-	0.200
D	2.820	2.900	3.020
E	1.500	1.600	1.700
E1	2.650	2.800	2.950
e	0.950 Typ.		
e1	1.800	1.900	2.000
L	0.300	-	0.600
θ	0°	-	8°