WD1050 SMD Controller/Formatter

FEATURES

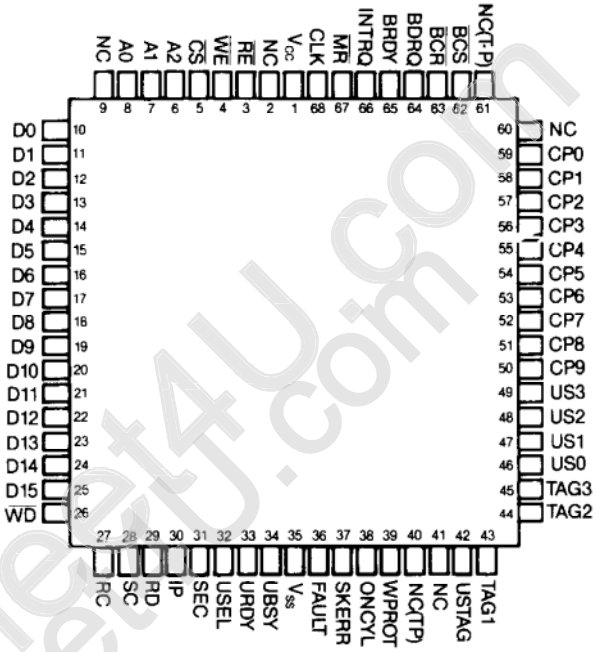
- 16 BIT HOST INTERFACE
- 9.677 MBITS/SEC DATA RATE
- SINGLE/MULTIPLE SECTOR TRANSFERS
- FIXED SECTOR FROMAT
- TTL COMPATIBLE INPUT/OUTPUT
- 68 PIN JEDEC TYPE C CHIP CARRIER PACKAGE
- COMPATIBLE WITH SMD, MMD, FHT, LMD, AND CMD FAMILIES
- SINGLE +5V SUPPLY

DESCRIPTION

The WD1050 SMD Controller/Formatter is an MOS/LSI device designed to interface an SMD compatible rigid disk drive to a Host processor. The device is compatible with all rigid disk drives adhering to Control Data Corporation's flat cable interface for SMD, MMD, FHT, FMD, LMD and CMD families (CDC specification 64712400 Rev H). It is TTL compatible on most inputs and outputs, with interface capability for 8 or 16 bit data buses.

The WD1050 contains a powerful set of Macro Commands for Read/Write and control functions. An internal 16 bit task file is used to process a selected command based upon parameter information in the file.

The WD1050 operates from a single +5V supply and is available in a 68 pin JEDEC Type C chip-carrier package.



PIN DESIGNATION

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
1	V_{CC}	V_{CC}	+5V ±5% power supply input
2	NO CONNECTION	NC	
3	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	Tri-state bi-directional line, used as an input when reading the task file and an output when the WD1050 is reading from the buffer.
4	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	Tri-state bi-directional line used as an input when writing to the task file and an output when the WD1050 is writing to the buffer.
5	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input enables both $\overline{WE}$ and $\overline{RE}$ signals as inputs.
6-8	ADDRESS 0-2	A_0A_2	These three inputs select a task file register to receive/transmit data.
9	NO CONNECTION	NC	
10-25	DATA BUS 0-15	D0-D15	Sixteen bit bi-directional bus used for transfer of commands, status, and data.
26	$\overline{\text{WRITE DATA}}$	$\overline{WD}$	Open drain, NRZ data output which is synchronized to the Servo Clock Input.
27	READ CLOCK	RCLK	Input clock from the drive which is synchronized with the Read Data input.
28	SERVO CLOCK	SCLK	A nominal 9.677 MHz clock input from the drive. This clock must be valid when Unit Ready (Pin 31) is active and Fault (Pin 34) is inactive.
29	READ DATA	RD	NRZ data input from the drive which must be synchronized to the Read Clock (Pin 25) input.
30	INDEX PULSE	IP	Active high input used to monitor the Index signal from the drive.
31	SECTOR	SEC	Active high input used to monitor sector pulses from the drive.
32	UNIT SELECTED	USEL	Active high input used to verify the selected drive.
33	UNIT READY	URDY	Active high input used to inform the WD1050 of a ready condition on a selected drive. If this line is made inactive during any command, command execution is terminated.
34	UNIT BUSY	UBSY	Active high input used to monitor drive status during a unit selection. If the unit had previously been selected and/or reserved prior to issuing a USTAG, the UBSY must be made active within one microsecond of the USTAG selection. This signal is used for dual-channel access applications and should be tied to ground when not used.
35	GROUND	V_{SS}	Ground.
36	FAULT	FAULT	Active high input used to detect a fault condition at the drive. Command execution is terminated if Fault is made active during any command. Only the Fault Clear Command may be issued while this line is asserted.

PIN NUMBER	NAME	SYMBOL	DESCRIPTION
37	SEEK ERROR	SKERR	Active high input used to detect a seek error at the drive.
38	ON CYLINDER	ONCYL	Active high input used to inform the WD1050 when the heads are settled and positioned over a cylinder.
39	WRITE PROTECT	WPROT	Active high input used to monitor the Write Protect signal from the drive.
40	NO CONNECTION	NC(TP)	Test Point.
41	NO CONNECTION	NC	
42	UNIT SELECT TAG	USTAG	Active high output used for selection of a unit on USO-US3 lines.
43-45	TAG1-TAG3	TAG1-TAG3	Active high outputs used to strobe specific data out on the Control Port Lines. Tag definitions are: TAG1 __ Cylinder address TAG2 __ Head/Volume select TAG3 __ Control Tag
46-49	UNIT SELECT 0-3	USO-US3	These four outputs reflect the contents of the unit address field of the task file and are used to select one of 16 drives.
50-59	CONTROL PORT BITS 9-0	CP9-CP0	Ten bit output bus used to issue tag parameters to the selected drive.
60	NO CONNECTION	NC	
61	NO CONNECTION	NC(TP)	Test Point.
62	$\overline{\text{BUFFER CHIP SELECT}}$	$\overline{\text{BCS}}$	Active low output used to enable reading or writing to the external buffer by the WD1050.
63	$\overline{\text{BUFFER COUNTER RESET}}$	$\overline{\text{BCR}}$	Active low output that is strobed prior to Read/Write Commands. Used to clear an external buffer counter.
64	BUFFER DATA REQUEST	BDRQ	This output is set to initiate data transfers to/from the external buffer.
65	BUFFER READY	BRDY	This input informs the WD1050 that the buffer is either full or empty.
66	INTERRUPT REQUEST	INTRQ	Active high output which is set at the completion of any command, providing the 'I' bit is also set in the command word. INTRQ is reset subsequent to a Status register read.
67	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	Active low input used to initialize the WD1050, usually after a power-UP condition.
68	CLOCK	CLK	2 MHz Master Clock is input.

FUNCTION DESCRIPTION

The WD1050 SMD Winchester Controller performs the necessary link between an 8 or 16 bit processor and an SMD compatible drive. The internal architecture of the WD1050 is shown in Figure 1. The major functional blocks are:

CONTROL UNIT

This section decodes commands, implements command execution sequencing, monitors the comparator and CRC logic, monitors status and issues control to the Host and Drive Interfaces. It also writes appropriate information to the Status register during command execution.

DATA I/O BUFFERS

A 16-bit bi-directional three-state bus (D15-D0) for data transfers between the Host CPU or data buffer and the HDC. (The higher order 8-bits of this bus [D15-D8] may be used for 8-bit data bus transfers between the Host CPU and the HDC).

HOST/BUFFER CONTROL

This section allows HDC register selection and communication by the CPU, issues interrupt requests, and provides Direct Buffer Access (DBA) transfers between the disk drive and the data buffer.

STATUS REGISTER

A 16-bit register reflecting operational status of the HDC and disk drive. This is a read-only register.

COMMAND REGISTER

A 16-bit field containing command information that dictates operational control sequencing of the Host and Drive Interfaces by the HDC. This is a write-only register.

DATA REGISTER

A 16-bit field used to assemble/disassemble words/bytes during data transfers. This register is internally interfaced to the HDC's Data I/O Buffers ('D' bus) and the HDC's Read Data Holding (RDH) register or Write Data Holding (WDH) register (as appropriate) during Host/drive data transfers. The contents of this register are compared to the appropriate Task File field as required by command execution.

CRC LOGIC

This logic is used to generate or check the 16-bit Cyclic Redundancy Check (CRC). The polynominal is:

$$G(x) = X^{16} + X^{12} + X^5 + 1$$

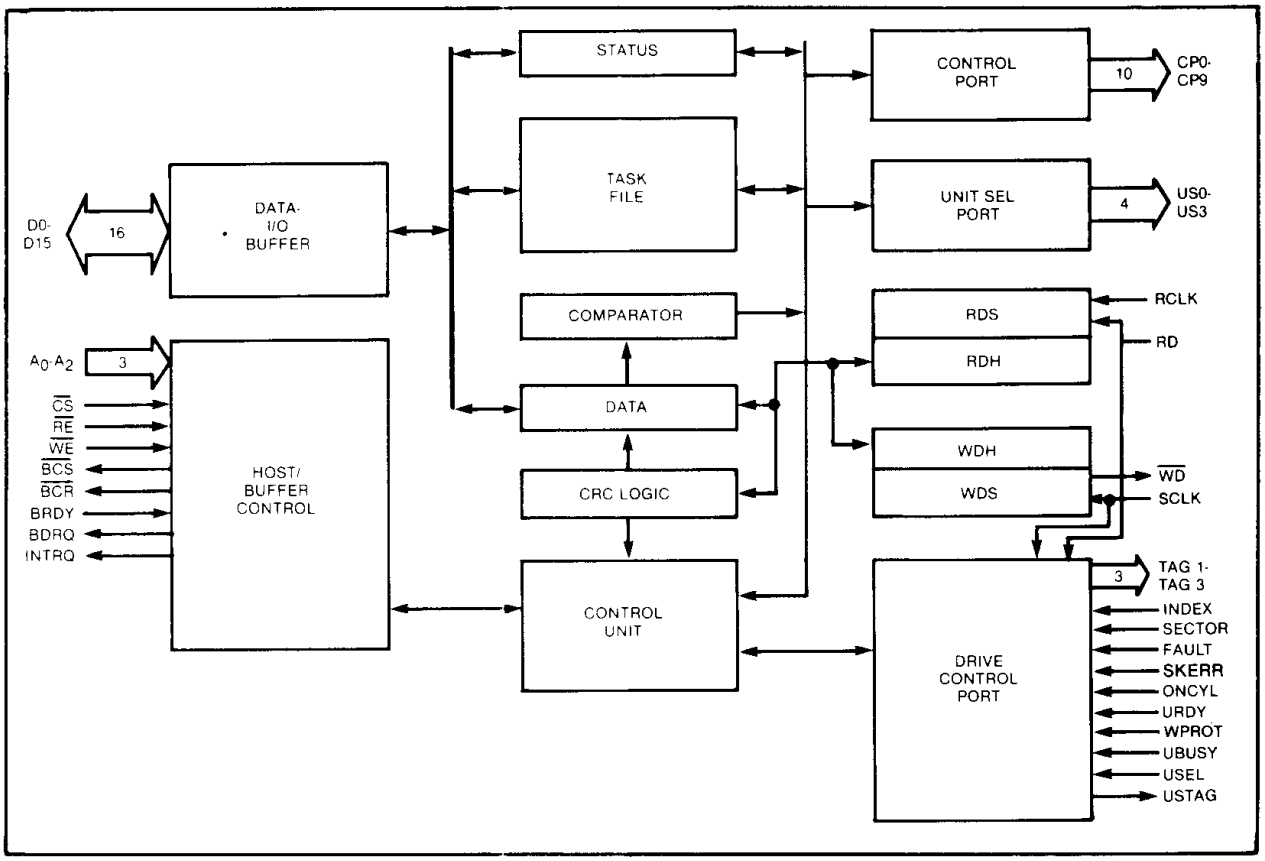


Figure 1. BLOCK DIAGRAM

The CRC includes all information beginning with the Sync character and ending with the CRC word. The CRC is preset to ones prior to a data transmission.

The CRC is implemented in parallel eight bits at a time as data is transferred between the HDC's Data register and the HDC's Read or Write Data Holding registers. The CRC word is transferred to the HDC's Data register and appended to the ID Field and Data Field (if enabled) during Format Sector or Write Data Commands.

COMPARATOR

A 16-bit comparator used to compare the appropriate HDC's Task File field with the respective byte(s) read from the disk.

READ DATA SHIFT REGISTER (RDS)

This 8-bit register shifts data read from Read Data (RD) input via the drives Read Clock (HDC's RCLK input).

READ DATA HOLDING REGISTER (RDH)

This 8-bit holding register assembles bytes from the Read Data Shift register and transfers them to the Data register.

WRITE DATA HOLDING REGISTER (WDH)

This 8-bit holding register receives bytes from the Data register and provides an eight bit parallel input to the HDC's Write Data Shift register (WDS).

WRITE DATA SHIFT REGISTER (WDS)

This 8-bit shift register converts the eight bit parallel input from the Write Data Holding register (WDH) into a serial bit stream issued to the HDC's Write Data ($\overline{WD}$) output via the drive's Servo Clock (HDC's SCLK input).

DRIVE CONTROL

This section monitors drive status, synchronizes the byte boundaries generated by the Servo Clock to the sync character read from the disk or the drive's Index or Sector pulse as appropriate, and issues control tags to the drive.

CONTROL PORT (CPO-9)

This 10-bit output is used to provide the drive with volume/head #, cylinder address, and control information in conjunction with outputs Tag 1 (cylinder address), Tag 2 (volume/head #), and Tag 3 (control). The contents of the appropriate HDC register or signals generated from the Control Unit are gated to the Control Port during command execution.

UNIT SELECT PORT (US0-3)

This 4-bit output port reflects the contents of the Unit Address register. The Unit Select Tag output selects the desired disk drive unit.

HOST INTERFACE

The primary interface between the Host processor and the WD1050 is through a 16-bit bi-directional bus. This bus is used to transfer status, parameter, and command information between the WD1050 and the Host, as well as data between the WD1050 and sector buffer. The external sector buffer is constructed with either FIFO memory or a RAM and binary counter. Since the WD1050 will make this bus active when accessing the sector buffer, a transceiver must be used to isolate this bus from the Host. Figure 2 shows a typical Host Interface using a RAM and Binary counter. The Sector Buffer may be one or more sectors in length, depending upon system requirements.

Whenever the WD1050 is not using the sector buffer, the Buffer Chip Select ($\overline{BCS}$) is high (disabled). This allows the Host to access the WD1050's Task File, read status, and issue commands. It also allows the Host to access data within the Sector Buffer. A separate RAM select line from the Host is used to access the data in memory. With each $\overline{RE}$ or $\overline{WE}$ strobe from the Host, the address counter is incremented on the trailing edge of $\overline{RE}$ or $\overline{WE}$, pointing to the next sequential memory location. Whenever the WD1050 changes the state of $\overline{BCS}$, the Buffer Counter Reset ($\overline{BCR}$) Line is strobed, causing the address counter to be reset to zero. The $\overline{RE}$ and $\overline{WE}$ lines become outputs from the WD1050 to allow access to the buffer only when $\overline{BCS}$ is low. Although 8-bit programming is allowed via the use of Address Line 0. the data path to and from the WD1050 must be 16 bits wide.

TASK FILE

The WD1050 contains five 16-bit registers called the Task File. These registers are used to set up parameter information prior to issuing a command. These registers are:

A2	A1	A0	15 REGISTER 0
0	0	0	HEAD/SECTOR ADDRESS
0	1	0	SECTOR COUNT/LENGTH & UNIT ADDRESS
1	0	0	CYLINDER REGISTER
1	1	0	COMMAND REGISTER (WRITE ONLY)
1	1	0	STATUS REGISTER (READ ONLY)

Each register in the Task File is accessed by selecting the proper address while CS (pin 4) is low, then strobing the $\overline{WE}$ or $\overline{RE}$ lines. All registers in the Task File are Read/Write except for the Command/Status register. The Command register can only be written to, while the Status register is a read-only register. The command and status registers have the same address.

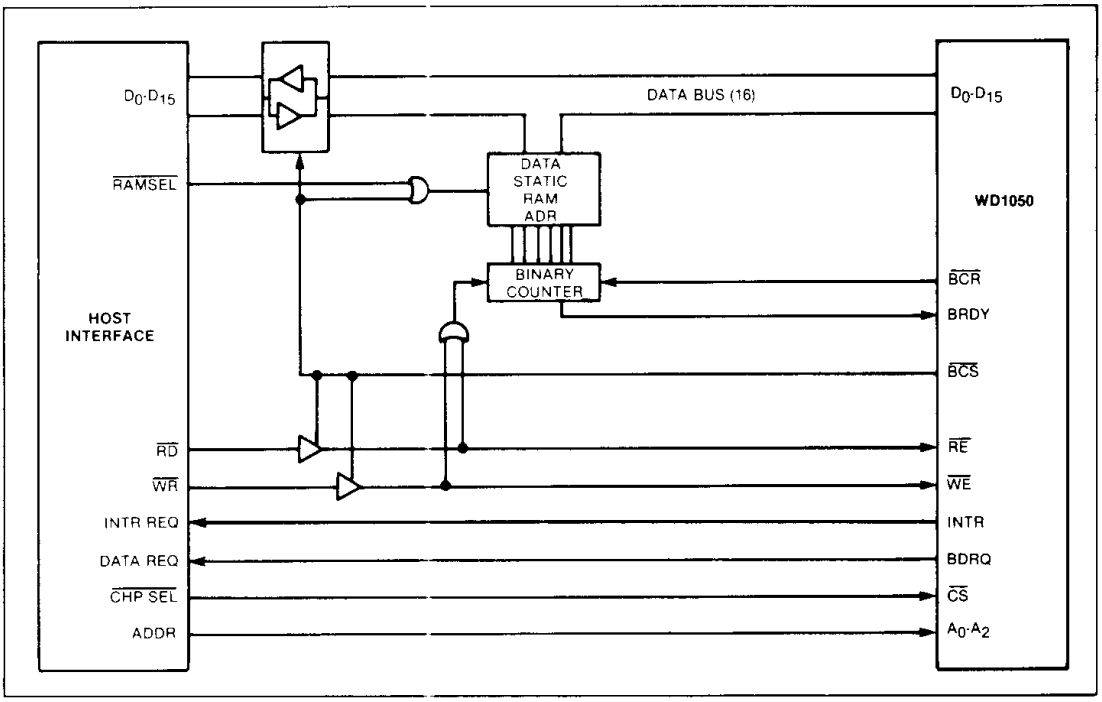


Figure 2. TYPICAL HOST INTERFACE

An 8-bit mode can also be used for accessing the Task File. Data is read/written on the most significant 8-bits of the Data bus (D15-D8). The upper byte is accessed with A_0 (pin 7) is high, and the lower byte is accessed when A_0 is low. The upper byte (A_0 = 1) must be accessed first, followed by the lower byte. This insures that data is transferred to the internal 16-bit bus properly, and that a command will execute after the full 16-bit word is written.

HEAD/SECTOR ADDRESS

This register holds the Head number and Sector Address fields:

15 — 8	7 — 0
HEAD NUMBER	SECTOR ADDR

The Sector Address byte (bits 7-0) holds the logical sector number used for comparison when searching for the specified ID field. The Head number byte (bits 15-8) holds the logical head number, and volume flag (where applicable). This 8 bit field is sent to the drive via the Control Port (CP7-0) when Tag 2 is issued. Note that all 8-bits of each byte are wrtten into the ID field during formats and are compared during other commands.

CYLINDER REGISTER

This register holds the 16-bit cylinder number:

15 — 0
CYLINDER REGISTER

The least significant 10-bits of this register (bits 9- 0) are transferred to the Control Port (CP9-0) when Tag 1 is issued. All sixteen bits of this register are written to the ID field during formats and are compared during other commands.

SECTOR COUNT/LENGTH & UNIT ADDRESS

This register holds the Sector Count, Sector Length and Unit Address fields:

15	14 — 8	7 — 4	3 — 0
M	SECTOR COUNT	LENGTH	UNIT

The four bit Unit Address field (bits 3-0) contains the physical Unit Address and is reflected at the drive via the Unit Select Port (US3-0). This port is used in conjunction with the Unit Select Tag (USTAG) output to select the desired drive.

The four bit sector length field is used to determine the number of bytes to be read/written from the disk. The allowable Sector Lengths are:

BITS 7	6	5	4	# OF BYTES IN DATA FIELD
1	0	0	0	128
0	1	0	0	256
0	0	1	0	512
0	0	0	1	1024

If the CE bit (CRC Enable) in the command word is zero, an additional 8 bytes are added to the above sector length (and the CRC bytes are not appended to the data field). These bytes can be used to append ECC codes to each sector.

The Sector Count Field, seven bits of which (bits 14-8) are used to control single/multiple record operation for commands where the LS (Logical Sector) Flag is set, is decremented by one for each sector encountered after the desired sector has been located on the disk. The Op Code Command is repeated until the contents of this field (bits 14-8) are equal to zero. For single sector operation, this field (bits 14-8) must equal "0000000". (This field [bits 14-8] is ignored for the Fault Clear Command).

For the Format Sector, Verify Sector, and commands where the LS flag is not set, the Sector Count Field (bits 14-8) must contain the desired physical sector location (i.e., the Sector Count number of sector pulses from the Index Pulse = physical sector location). This register is counted down to zero to determine the physical sector location for these commands. For physical sectored commands, bit 15 is used as a one bit field controlling single/multiple record operation. For bit 15 equal to '0', a single sector command is executed. For bit 15 equal to '1', these commands are repeated until the Index pulse is re-encountered, allowing multiple sector operations.

For logical sectoring, bit 15 of this register should equal '0'.

COMMAND REGISTER

This "write-only" register is used to load in the desired command:

15	0
COMMAND REGISTER	

The command register may be loaded whenever the Command-In-Process (CIP) status bit is low.

STATUS REGISTER

This "ready-only" register is used to monitor status and error conditions as the result of command execution or its format is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCS	CIP	UBSY	USEL	WPRT	URDY	OCYL	SKER	BCS	FLT	BDRQ	-	DFCE	DFNF	IDCE	IDNF

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (FLT) input.
7	Buffer Chip Select ($\overline{BSC}$)	This bit is an inverted copy of the Buffer Chip Select (BCS) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (SKER) input.
9	On Cylinder (ONCYL)	Reflects the status of the On Cylinder (ONCYL) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (URDY) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (USEL) input.
13	Unit Busy (UBSY)	Reflects the status of the Unit Busy (UBSY) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select (BCS) output. This bit also appears in Status Bit 7.

Note: That Status Register bits 13-8 are frozen upon premature command termination (as described in Command Execution, step 2). These bits are released to active monitoring and error bits 3-0 are reset low following a read of the Status register (or following programming of the Command register) when the Command register CIP bit is low and/or the INTR output is inactive.

INSTRUCTION SET

The WD1050 will execute eight commands. Prior to issuing a command, the Host must first setup the Task File with parameter information.

A command can only be accepted if the CIP bit in the status register is low.

COMMAND	MSB COMMAND REGISTER BITS LSB															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	D
Return to Zero	1	0	0	1	0	0	0	I	0	0	0	M	U	S	E	D
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	D
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	D
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	D
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	0	U	S	E	D
Format	1	1	1	0	R	P	O	I	Z	C	H	0	U	S	E	D
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	D

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head Change
L = Logical Sectoring	C = Cylinder Addr
P = Programmable Sectors	H = Head Selection
O = On Cylinder	M = Marginal Data Recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
D = Unit Deselect/LATE	S = Priority Sel/Servo Plus

COMMAND FLAG DESCRIPTION

BIT	NAME	DESCRIPTION
V	Verify	Compare The Head number and Cylinder Address word of the ID field with the appropriate Task File field when On Cylinder becomes active. The Sector Address byte in the ID Field is not compared, althought the CRC is checked. This flag is valed only for the Seek Cylinder Command.
R	Data Field CRC Enable	Data Field CRC is enabled. If the flag is not set, the condition of the DFCRC Status bit will not affect command execution; the data field is extended by four words (8 bytes), and the CRC bytes are not appended.
L	Logical Sectoring	Locate sector by matching the ID Field bytes read from the disk to the appropriate field in the HDC Task File. The Sector Count register in the Task File is used to indicate the additional number of sectors to be transferred for multiple sector commands. If L is not set, physical sectoring is implemented. The Task File Sector Count register is decremented to locate the desired physical sector from the Indes pulse. ID Field compares are made, but do not affect command execution.
P	Programmamble Sectors	The Head Number/Sector Address register is read from the buffer as each sector is encountered per command execution. (This allows an entire track to be formatted/verified with interleave sectors in one revolution of the disk). This flag is valid only for the Format Sector or Verify Sector Commands.
O	On Cylinder	For the Seek Cylinder Command, command completion requires activation of On Cylinder or Seek Error inputs. For other commands, On Cylinder is required before a read or write can occur.
I	Interrupt Enable	Enable the interrupt output (INTRQ) for activation upon completion or termination of command execution.

COMMAND FLAG DESCRIPTION

BIT	NAME	DESCRIPTION
Z	Volume/Head	Issue Tag 2 as required for volume/head change.
C	Cylinder	Issue Tag 1 as required for cylinder address selection. (Tag 1 will follow Tag 2 if the Z and C flags are both set).
H	Head	Issue Tag 2 as required for head selection. (Tag 2 will follow Tag 1 if the C and H flags are both set).
M	Marginal Data	Attempt a marginal data recovery. (marginal data recovery may be attempted only where a command requires reading from the drive). This bit controls the function of bits 3-0 (U, S, E, D). (See Note 1)
U	Unit Select/Servo Offset Minus	For M = 0 (or not applicable, set Unit Select Tag as required for unit selection. Unit Selected must become active for command execution to continue.
S	Priority Select/ Servo Offset Plus	For M = 0, issue priority select control as required to reserve the unit. See Note 2). For M = 1, issue servo offset plus control for marginal data recovery attempt.
E	Priority Release/ Data Strobe Early	For M = o, issue priority release control as required to release reserve of the unit. (See Note 2) For M = 1. issue data strobe early control for marginal data recovery attempt.
D	Unit Deselect/Data Strobe Late	For M - 0, reset Unit Select Tag at Completion of the command. For M - 1, issue data strobe late contron for marginal data recovery attempt.

Note 1: Certain marginnal data recovery features are not applicable depending on the particular drive type under control. (Refer to CDC Interface Specification 64712400).

Note 2: Priority select and release features are applicable only for dual channel drive applications.

COMMAND EXECUTION

Command work architecture has been designed to provide comprehensive control of the drive unit via programmable macro-level commands. For example, unit selection, cylinder seek, head selection, Op Code execution (of multiple records if desired), and unit deselection can be performed with a single command.

Command execution follows the following sequence (for 'M'flag = 0):

1. If the U flag is set, the Unit Select (US) Tag is activated. (The drive should select the unit specified by the Unit Select bus [US0-3] when the US Tag is activated.)

   If the S flag is also set, CP9 will be activated when the US Tag is activated (exclusively reserving the unit to that channel until released).

2. The following conditions must be met and maintained for command execution to continue:
   Unit Ready input active
   Unit Selected input active
   Unit Busy input not active

   If these comditions are not met, command execution is terminated with the appropriate bit set in the Status register.

   For all commands except the Fault Clear Command, the Fault input must also be inactive and remain inactive for command execution to continue.

3. For the Write Data and Format Commands, the Write Protect Status bit is checked; if true command execution is terminated.

4. For the Write Data Command, and the Format Verify Command with the P (programmable sector) flag set, the HDC activates BDRQ requesting the Host to provide the required data to the buffer.

5. If the Z flag is set (indicating a volume change), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed. (Applies only for drives with volume select.)

6. If the C flag is set (indicating a cylinder address seek), the Cylinder Address field of the Task File is issued to the Control Port (bits 9-0 respectively), and Tag 1 is pulsed.

NOTE:

For the Seek Cylinder Command, and for other commands where the On Cylinder flag is set, the On Cylinder input must be active before Tag 1 will be issued. (If the Seek Error input is active or becomes active before On Cylinder is active, execution is terminated with the Seek Error status recorded in the Status register).

7. If the H flag is set (indicating a head selection), the Head number field of the Task File is issued to the Control Port (Head field bits 15-8 to CP lines 7-0 respectively), and Tag 2 is pulsed.
8. For commands other than Seek Cylinder, O flag operation is as follows:

   If O is set, execution is suspended pending an active On Cylinder input.

   if O is not set, the command is executed regardless of the condition of On Cylinder.

   NOTE:

   Data transfer to/from the drive with On Cylinder inactive is allowed only under certain circumstances on specific drives. For example, on a drive with both fixed and moveable heads, it is possible to execute a Seek Cylinder Command with the C flag not set to the moveable heads (On Cylinder will drop). The fixed heads may then be given a Read Data command with the O flag not set. The Fixed head can then be read regardless of the condition of On Cylinder. (This is an overlap seek within a given unit between the fixed and moveable media). For valid read/write operation without an active On Cylinder, refer to the appropriate drive operating specification.

   For commands with C set and Seek Error received instead of On Cylinder, command execution is terminated.
9. For the Write Data Command, and the Format and Verify Commands with the P flat set, the BRDY input is inspected. Command execution is suspended pending reception of a low to high transtion on the BRDY input.

   NOTE:

   For commands where M is set, marginal data recovery control as described in the chart below is issued to the control port prior to the activation of Tag 3. Note that unit selection, channel reserve control, and unit deselection must be accomplished with a non-marginal data recovery command since the U, S, E, and D flags assume marginal data recovery control significance.

COMMAND FLAG IF MD IS SET	FEATURE	CONTROL PORT BIT ACTIVATED
U	Servo Offset Plus	2
S	Servo Offset Minus	3
E	Data Strobe Early	7
D	Data Strobe LATE	8

Location of the appropriate sector within the cylinder is common to all commands except Fault Clear and RTZ. One of two methods is used: logical sector search (for commands where the L flag is set) and physical sector locating (for the Format and Verify Commands and commands where the L bit is not set).

Logical sector search consists of reading the first encountered ID Field, comparing these bytes to the appropriate fields in the HDC's Task File, (including the sync byte) and checking the ID Field CRC bytes. When a valid compare with correct CRC are found, execution continues. If a valid compare with correct CRC are not found before four Index pulses are detected, the appropriate Status bits are set (IDNF and/or IDCE) and command execution is complete. For mulitple sector commands, The Sector Address field of the Task File is incremented between sectors and the Sector Count field is used to indicate the number of additional sectors for which the command is to be executed. A single sector sommand is executed for Sector Count = '00. . .00".

Physical sector locating is accomplished by decrementing the Sector Count field of the Task File by one for each Sector pulse encountered after the Index pulse is located until the Sector Count field = '0000000'. For Sector Count = '0000000', the command will be executed to the sector immediately following the Index pulse. The ID Field compares and the IDCE check are still made and the appropriate bit set in the Status register (if applicable), but command execution is not affected by an error condition. A single sector command is executed if bit 15 of the Sector Count/Sector Length/Unit Address register of the Task File is zero. If bit 15 is one, command execution is repeated until the Index pulse is re-encountered. Note that Status register error bits are not cleared between sectors (one's catching).

Tag 3 (Control Select) is activated for all commands except Seek Cylinder with the V flag not set.

When the appropriate Sector pulse is encountered, CPI (Read Gate) is activated and the HDC synchronizes to the first low to high transition on the Read Data (RD) input. This initiates the following three compares: the sync byte FE preceded by eight zeros, the upper and lower Cylinder Address, and the Head number and Sector Address. (The Sector Address compare is suppressed on the Seek Cylinder command). The ID FIELD CRC is then checked. CPI is deactivated and command execution follows.

FAULT CLEAR

CP4 (Fault Clear) is pulsed and this completes execution. This command is intended to clear the Fault output of the drive. The condition causing the fault within the drive should no longer exist when this command is issued.

RTZ (RETURN TO ZERO)

CP6 (RTZ) is pulsed and the Cylinder Address, Head number, and Sector Address fields of the Task File are all set to zero. This completes execution.

SEEK CYLINDER

Execution of this command is controlled completely by the command flags. If O is set, execution is suspended until On Cylinder (or Seek Error) is received. If the V flag is not set, receipt of On Cylinder completes execution. If C and V are both set, and On Cylinder is received, CPI (Read Data) is issued and the ID Field is inspected. The Sector Address compare is not made for this command.

NOTE:

If L is set (logical sectoring), execution is complete when ID Field is successfully found or when the 4th Index pulse is encountered. There is no multiple sector operation when L is set for this command. If L is not set (physical sectoring). the IDNF and IDCE Status bit are one's catching. (The entire track may be verified with multiple sector operation).

The V flag is ignored if the O flag is not set.

If the C flag is not set, this command may be used for Unit Select only functions.

READ ID FIELD

The Read ID Field command is provided to allow transfer of the ID Field formatted on the disk to the data buffer (i.e., $\overline{BCS}$ • D15-Do • $\overline{WE}$ pulses). The Sector Address field is not compared in this command.

If the L flag is set, the first encountered ID Field is transferred to the buffer. The following bytes are transfered: 00FE, Upper and Lower Cylinder Address, Head number, Sector Address, and two CRC bytes. Thus four $\overline{WE}$ pulses are issued.

If the L flag is not set, the physical sector is located and the corresponding ID Field is transferred to the buffer.

There are no retries with this command if ID Field compare errors result.

For the Read ID Field command, CP1 is reactivated, and the first low to high transition on the RD input initiates a compare for the Data Field sync character. If the compare does not match, the Data Field Not Found (DFNF) Status bit is set. The Data Field CRC (DFCE) Status bit is set if an error is detected. CP1 is then deactivated.

Note that the Data Field is not transferred with this command, but that the following eight bytes are transferred: 00, FE, Upper Cylinder Address, Lower Cylinder Address, Head #, Sector Address, and the two CRC bytes.

If the L flag is not set, multiple sector operation continues to the next INDX pulse without inspection BRDY.

For multiple sector operation, the Sector Address Field of the Task File is automatically incremented. If the L flag is set, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (i.e., buffer not full) execution is then repeated. If a low to high transition has occurred, (i.e., buffer is full) BSC is deactivated, BCR is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition of BRDY (i.e., buffer empty). BCR is then pulsed, and execution is repeated. If a Data Field CRC is detected, the command will not terminate.

READ DATA

After the appropriate sector has been located, Data Field operation is as described under the Read ID Field Command, except that the Data Field is transferred to the buffer. Note that only the Data Field data bytes are transferred with this command.

This completes execution for single sector commands and for multiple sector commands where the L and R flags are set. If a Data Field sync error (DFNF) or a Data Field CRC (DFCE) error has occurred, the command will be terminated.

For multiple sector commands where the R flag and/or L flag is not set, or for multiple sector commands where no Data Field error has occured, execution is repeated.

Note that if the R flag and/or the L flag is not set, the DFNF and DFCF Status bits are one's catching.

WRITE DATA

After the appropriate sector has been located, CPO (Write Gate) is activated. Thirteen bytes of zeros (two Write Splice bytes and eleven PL0 Sync bytes) are written followed by the sync character. The Data Field is then written to the disk from the data buffer (i.e., $\overline{BCS}$ • D15-D0 • $\overline{Re}$ pulses). The CRC bytes and two bytes of zeros (End of Record) are appended to the Data Field and written to the disk.

For multiple sector operation, the BRDY input is inspected following each sector's transfer. If a low to high transition has not occurred (i.e., buffer empty), $\overline{BCS}$ is deactivated, $\overline{BCR}$ is pulsed, and BDRQ is activated. Execution is suspended pending a low to high transition on BRDY (i.e., buffer full). $\overline{BCR}$ is then pulsed, and execution is repeated.

FORMAT SECTOR

Physical sectoring only applies to the Format Sector Command. Upon reception of the appropriate Sector pulse, CP0 (Write Gate) is activated. Twenty seven bytes of zeros (16 Head Scatter bytes and eleven PL0 Sync bytes), and the sync character are written to the disk from the HDC's Task File, and the resultant CRC is appended. Thirteen bytes of zeros are written (two Write Splice bytes and eleven PL0 sync bytes) followed by the sync character. The Data Field (Format Character E5 repeated) is then written. If the R bit is set, then the two CRC bytes are appended; if

R is not set, eight additional E5's are added to the data field. Zeros are written until the next Sector or Index pulse is encountered.

For single sector operations CP0 is then deactivated. For multiple sector operation, CP0 remains active, and execution is repeated until the Index pulse is again encountered.

If the P flag is set, the HDC will fetch the Head Number / Sector Address from the data buffer prior to encountering each ID Field. Thus, by filling the data buffer with the desired Head Number / Sector Address information, the HDC can format an entire track with any given programmed sector interleave in one revolution.

If the P Flag is not set, the contents of the Sector Address field of the Task File will be incremented by one between sectors.

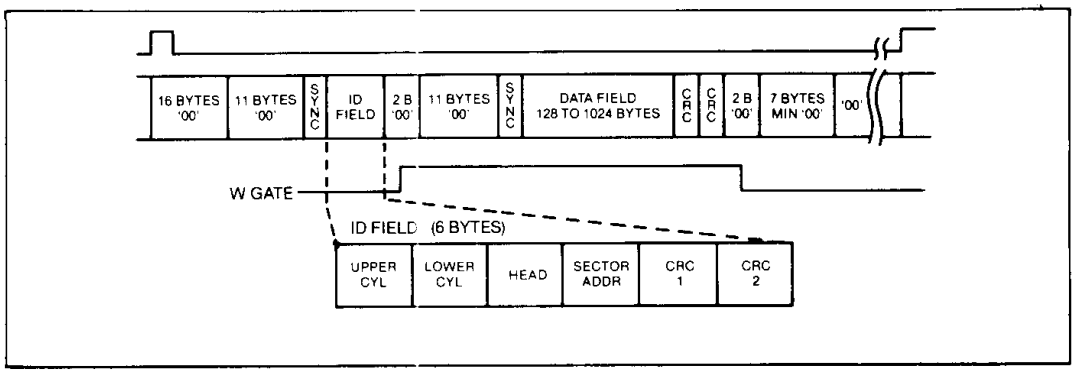
The BCS output will remain active for the duration of this command.

VERIFY SECTOR

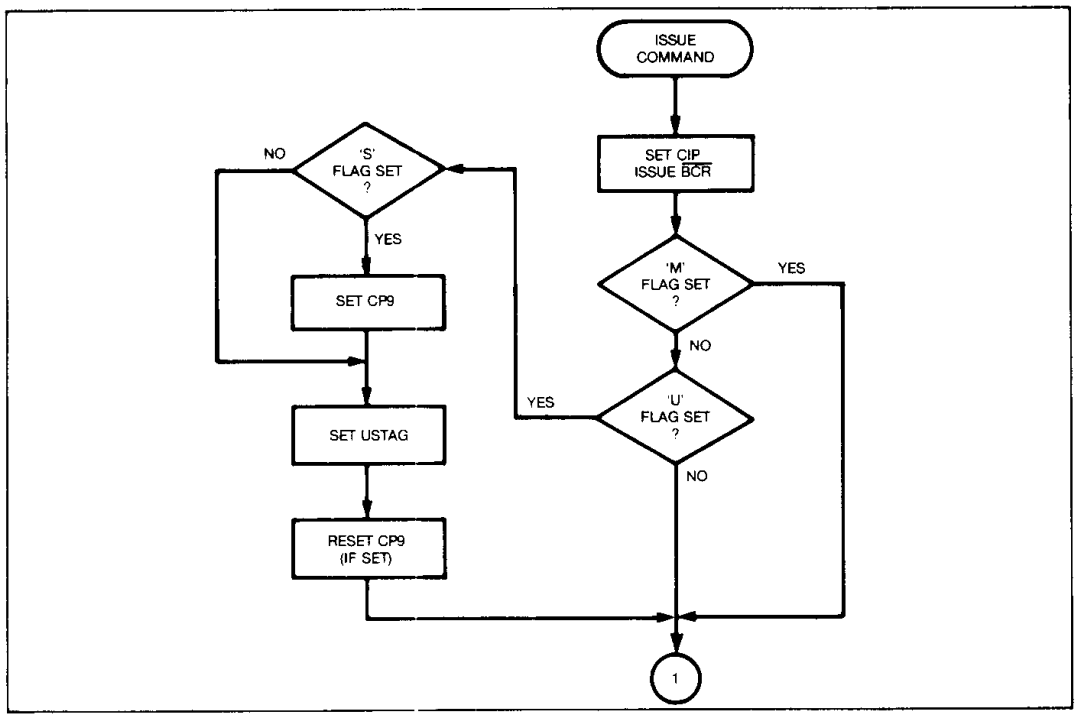
This command allows verification of sector format without transfer of data. Sector addressing is identical to that described for the Format Sector Command. The IDNF, IDCE, DFND and DFCE bits are set if errors are found (all bits are one's catching for multiple sector operation). With multiple sector operation, an entire track can be verified in a single revolution.

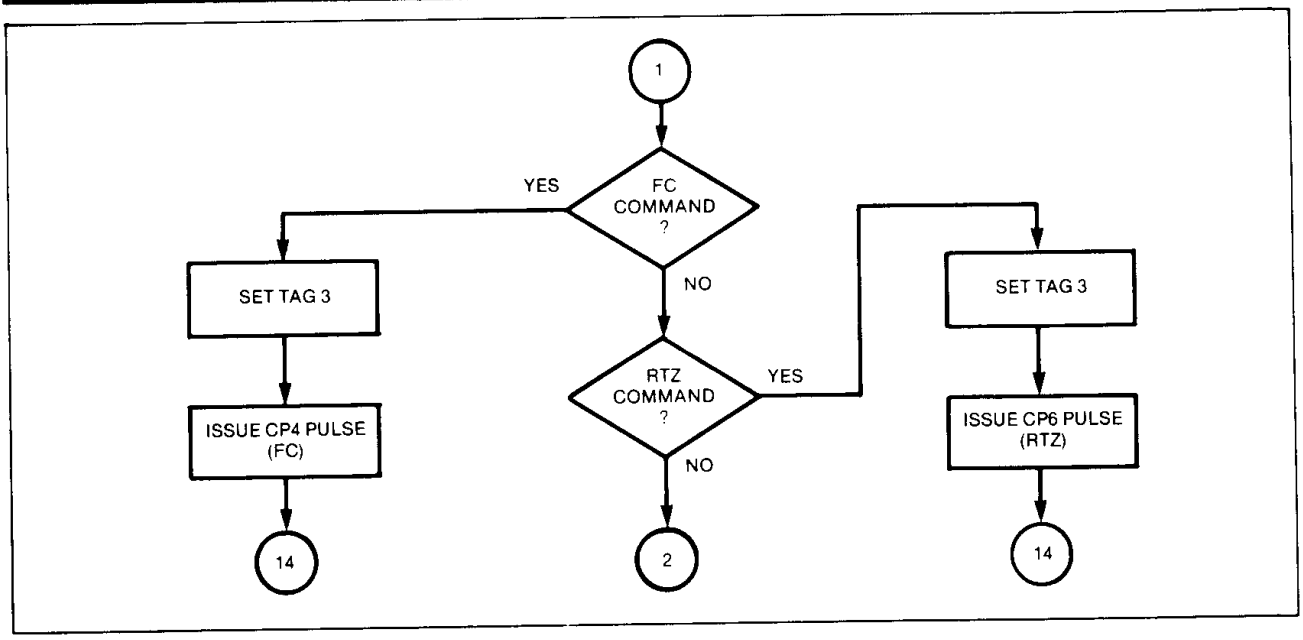
NOTE:

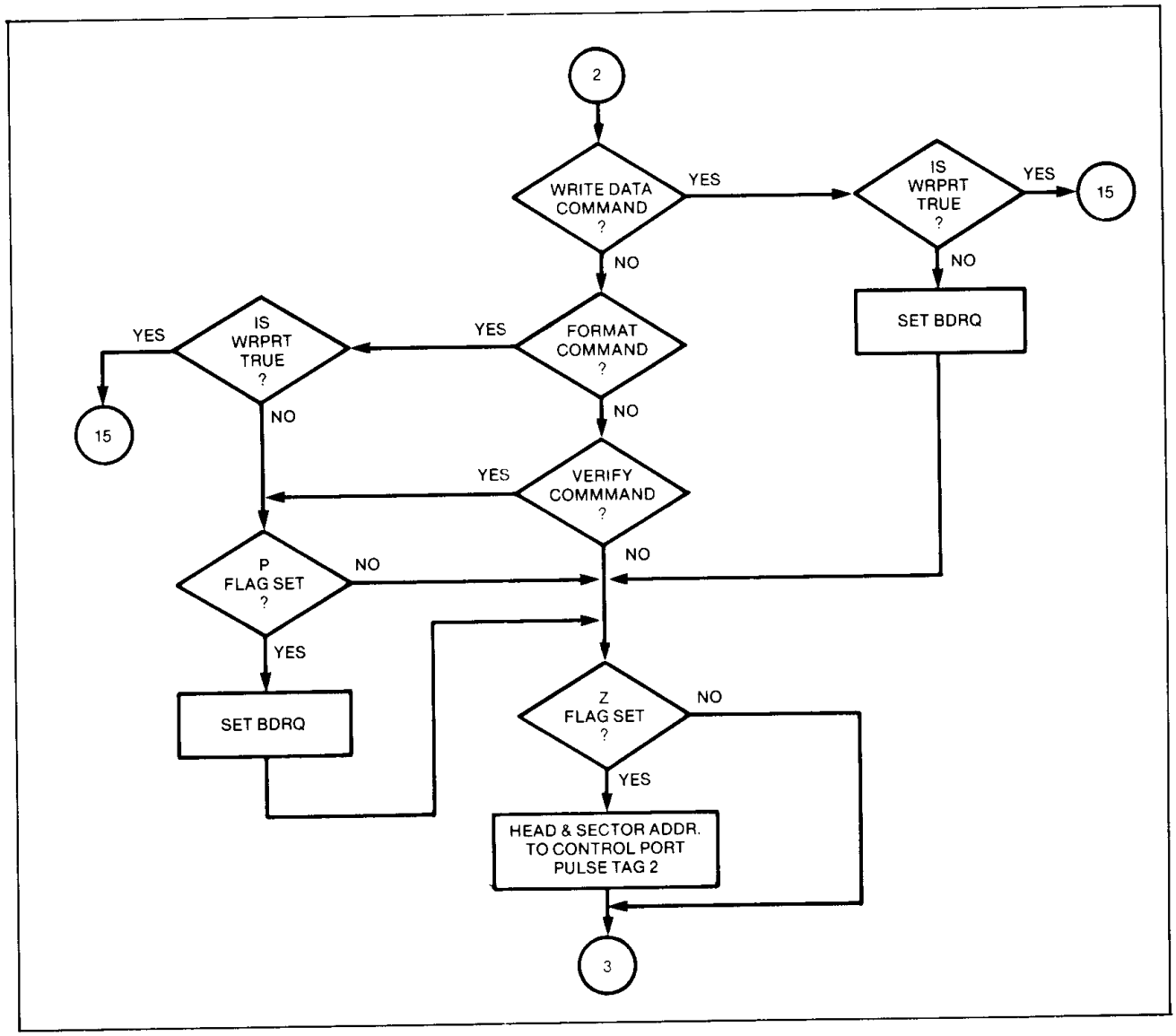
When used with the Lark drive, the validity of the DFCE bit is not guaranteed with this command if it immediately follows a FORMAT of the sector.

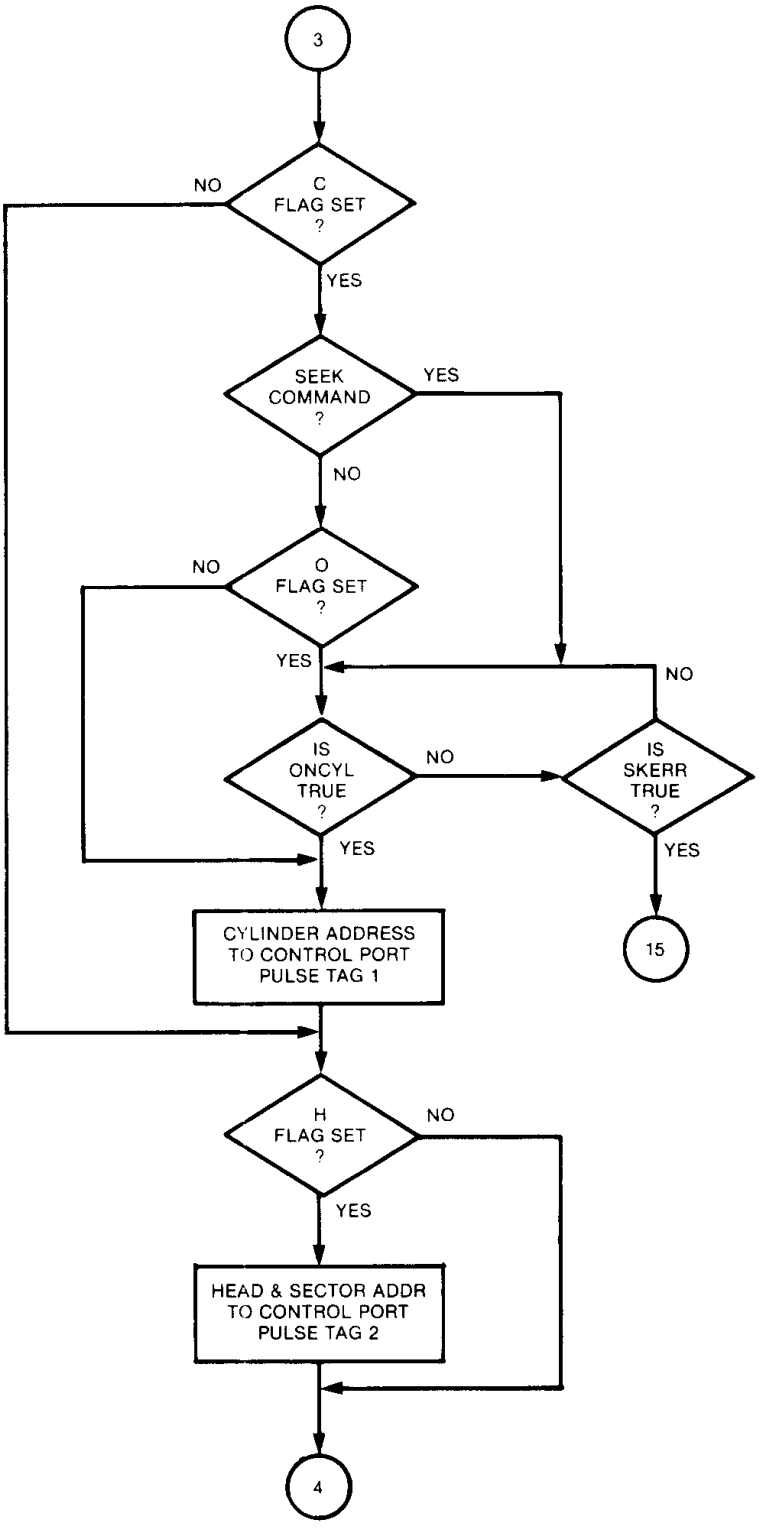


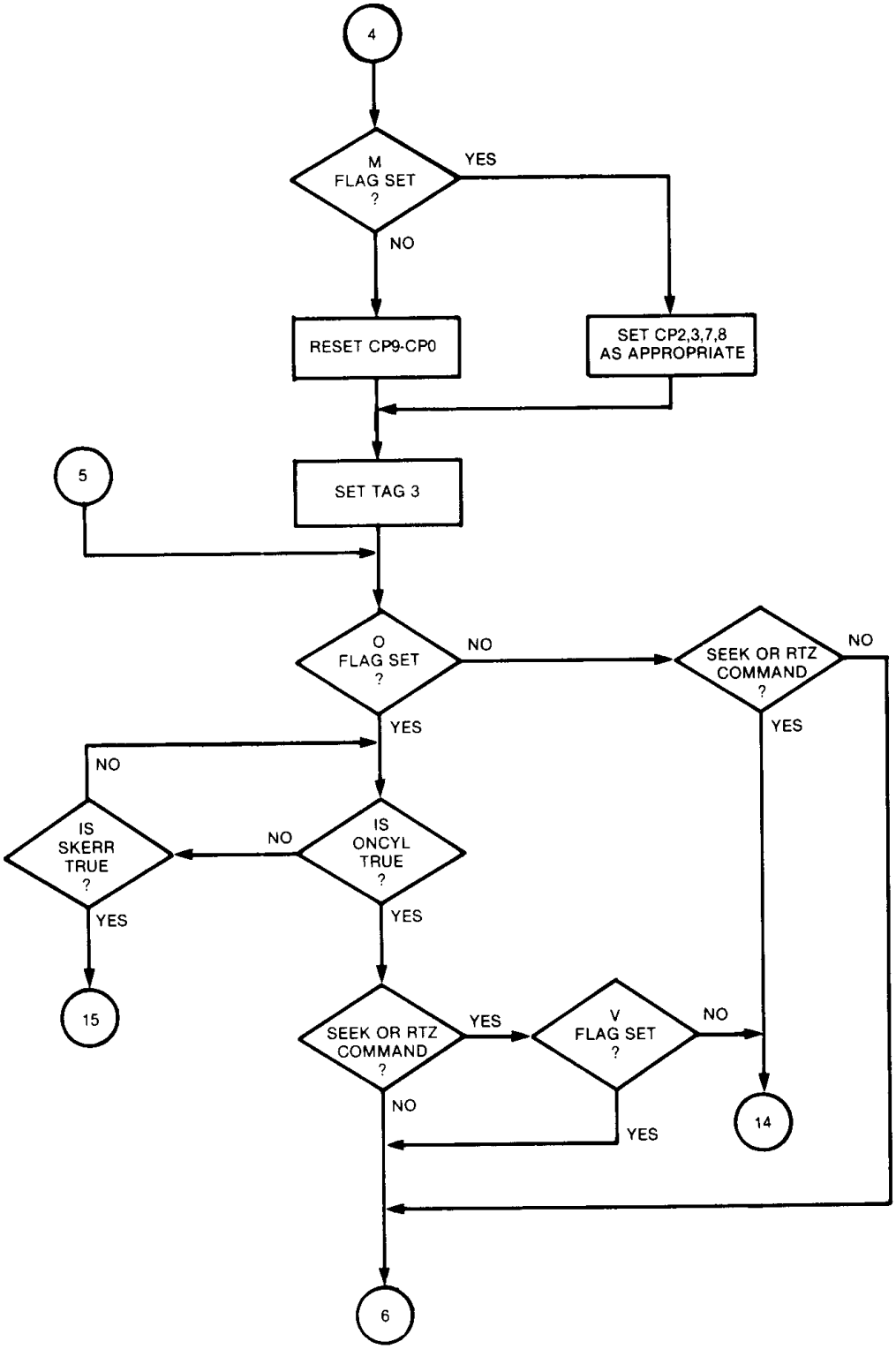
FIXED SECTOR FORMAT

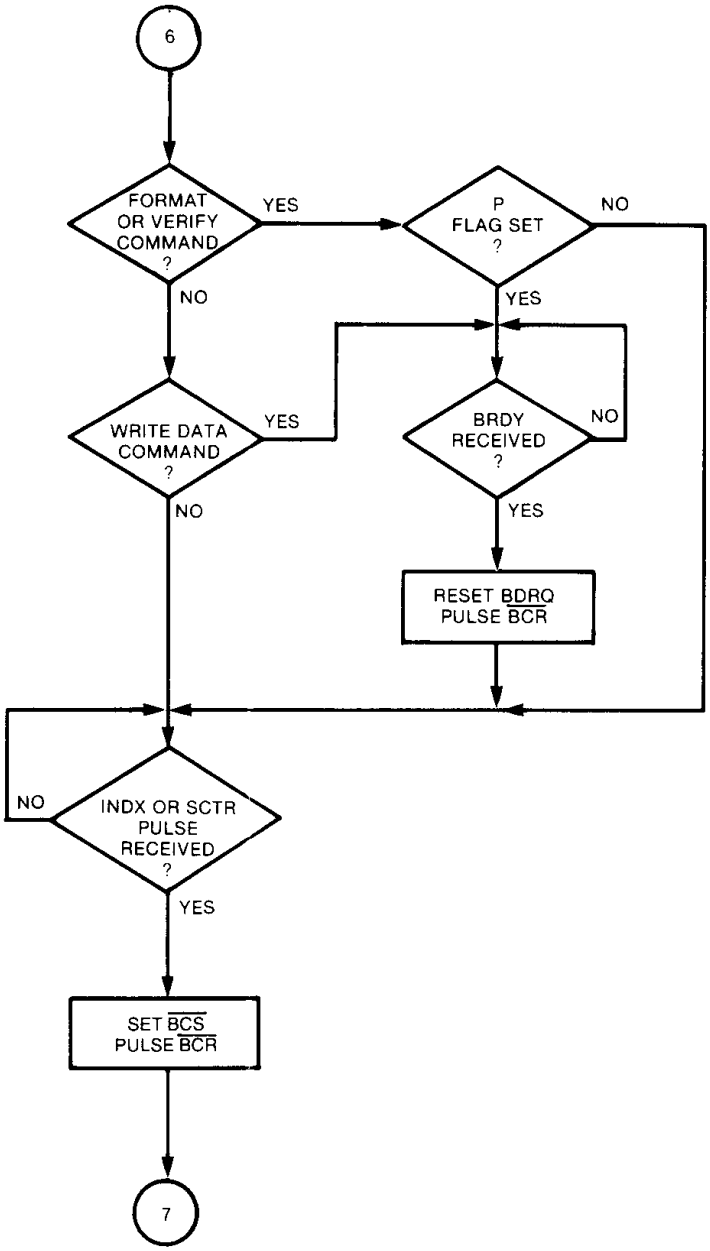


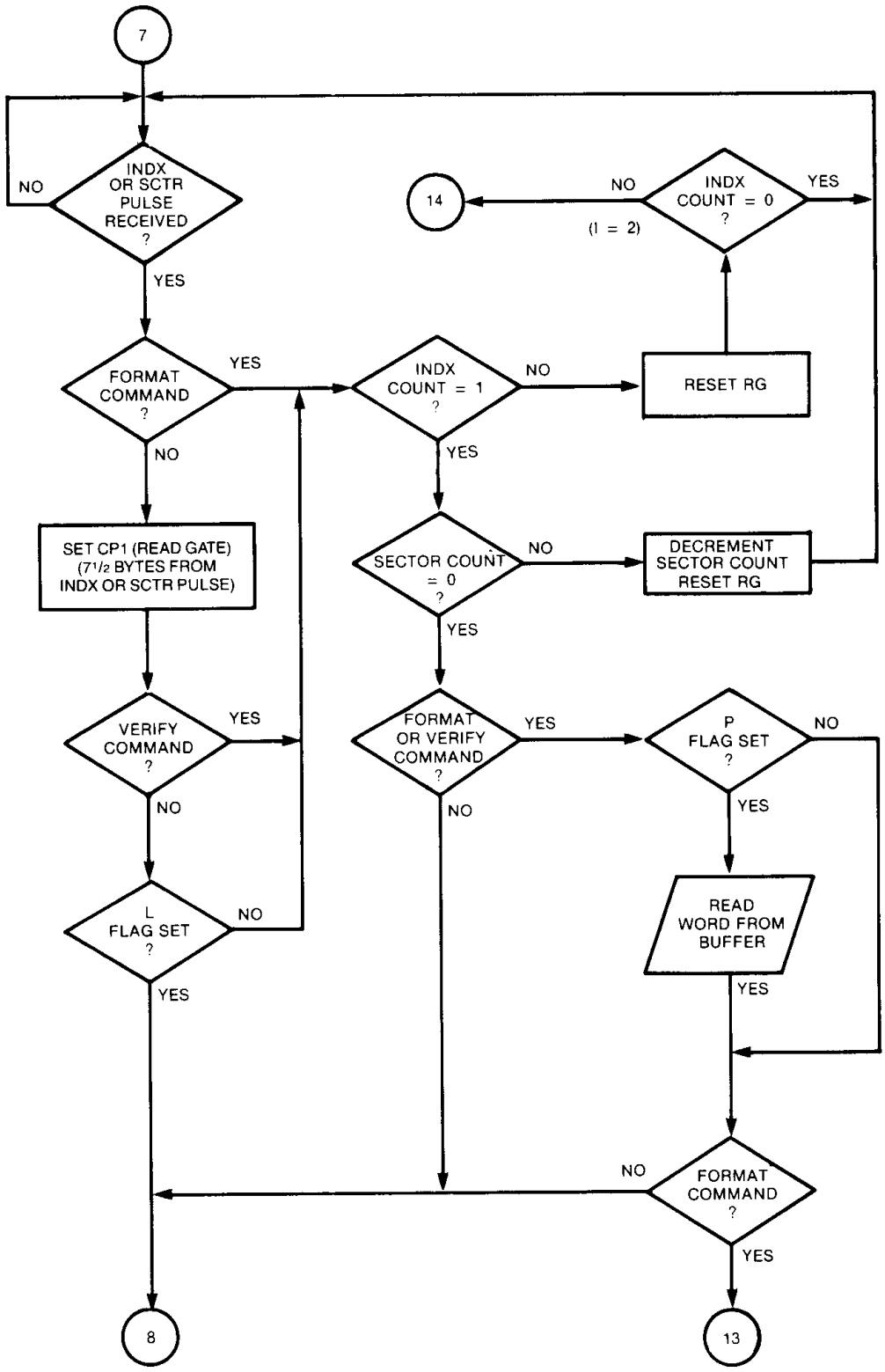

1
FC COMMAND ?
YES
NO
SET TAG 3
ISSUE CP4 PULSE (FC)
14
RTZ COMMAND ?
YES
NO
2
SET TAG 3
ISSUE CP6 PULSE (RTZ)
14

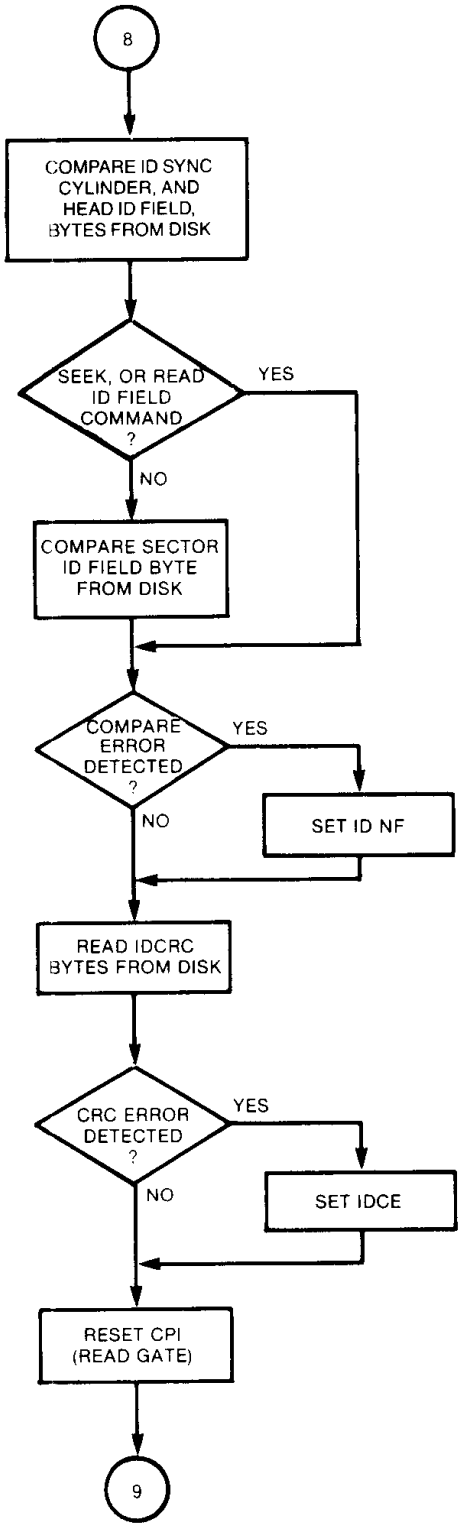

2
WRITE DATA COMMAND ?
YES
NO
IS WRPRT TRUE ?
YES
15
NO
SET BDRQ
FORMAT COMMAND ?
YES
IS WRPRT TRUE ?
YES
15
NO
NO
VERIFY COMMMAND ?
YES
P FLAG SET ?
NO
YES
SET BDRQ
NO
Z FLAG SET ?
YES
HEAD & SECTOR ADDR. TO CONTROL PORT PULSE TAG 2
3

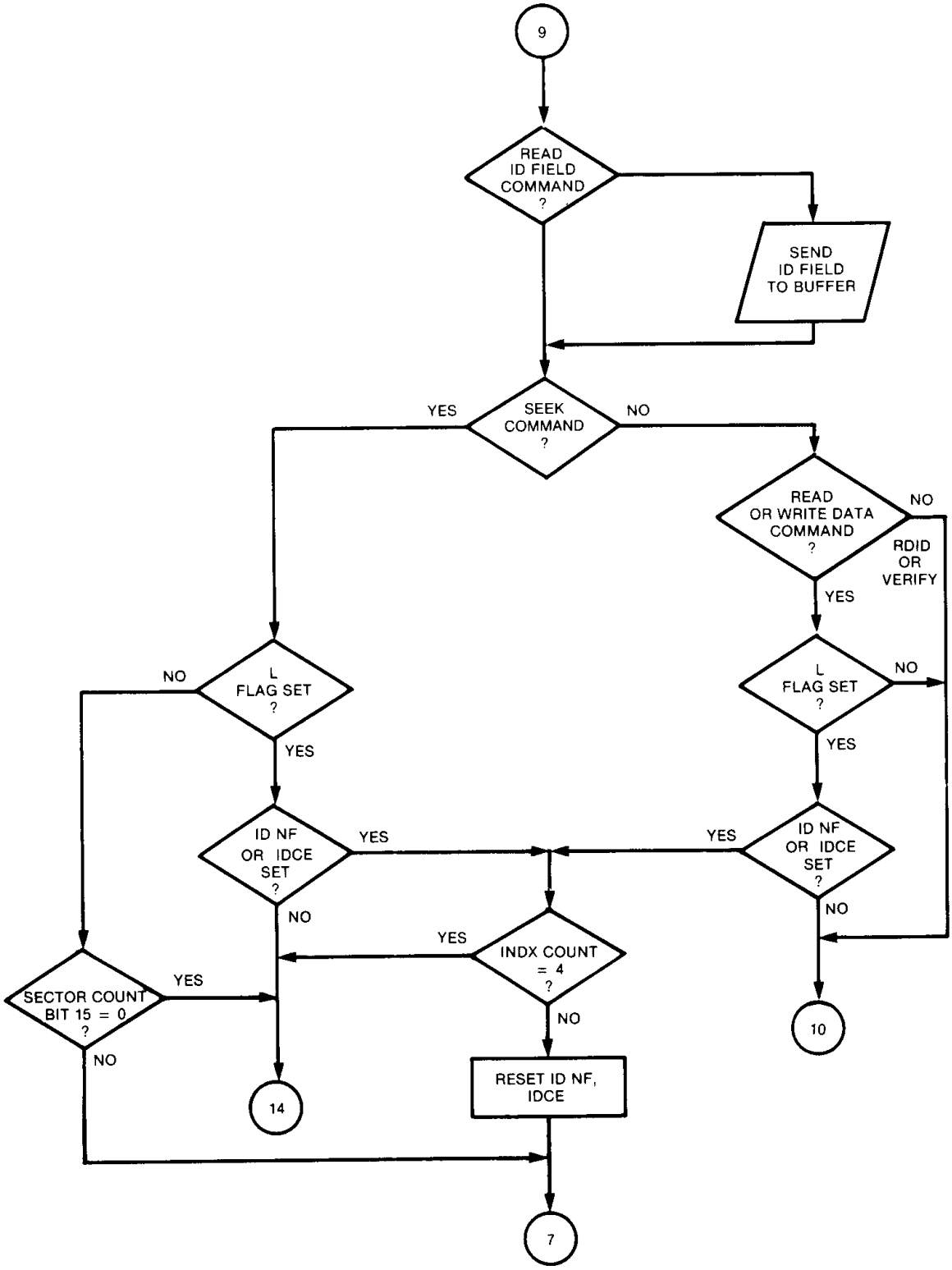

3
C FLAG SET ?
NO
YES
SEEK COMMAND ?
YES
NO
O FLAG SET ?
NO
YES
NO
IS ONCYL TRUE ?
NO
IS SKERR TRUE ?
YES
YES
15
CYLINDER ADDRESS TO CONTROL PORT PULSE TAG 1
H FLAG SET ?
NO
YES
HEAD & SECTOR ADDR TO CONTROL PORT PULSE TAG 2
4


4
M FLAG SET ?
YES
NO
RESET CP9-CP0
SET CP2,3,7,8 AS APPROPRIATE
5
SET TAG 3
O FLAG SET ?
NO
SEEK OR RTZ COMMAND ?
NO
YES
YES
NO
IS SKERR TRUE ?
NO
IS ONCYL TRUE ?
YES
YES
15
SEEK OR RTZ COMMAND ?
YES
V FLAG SET ?
NO
NO
YES
14
6

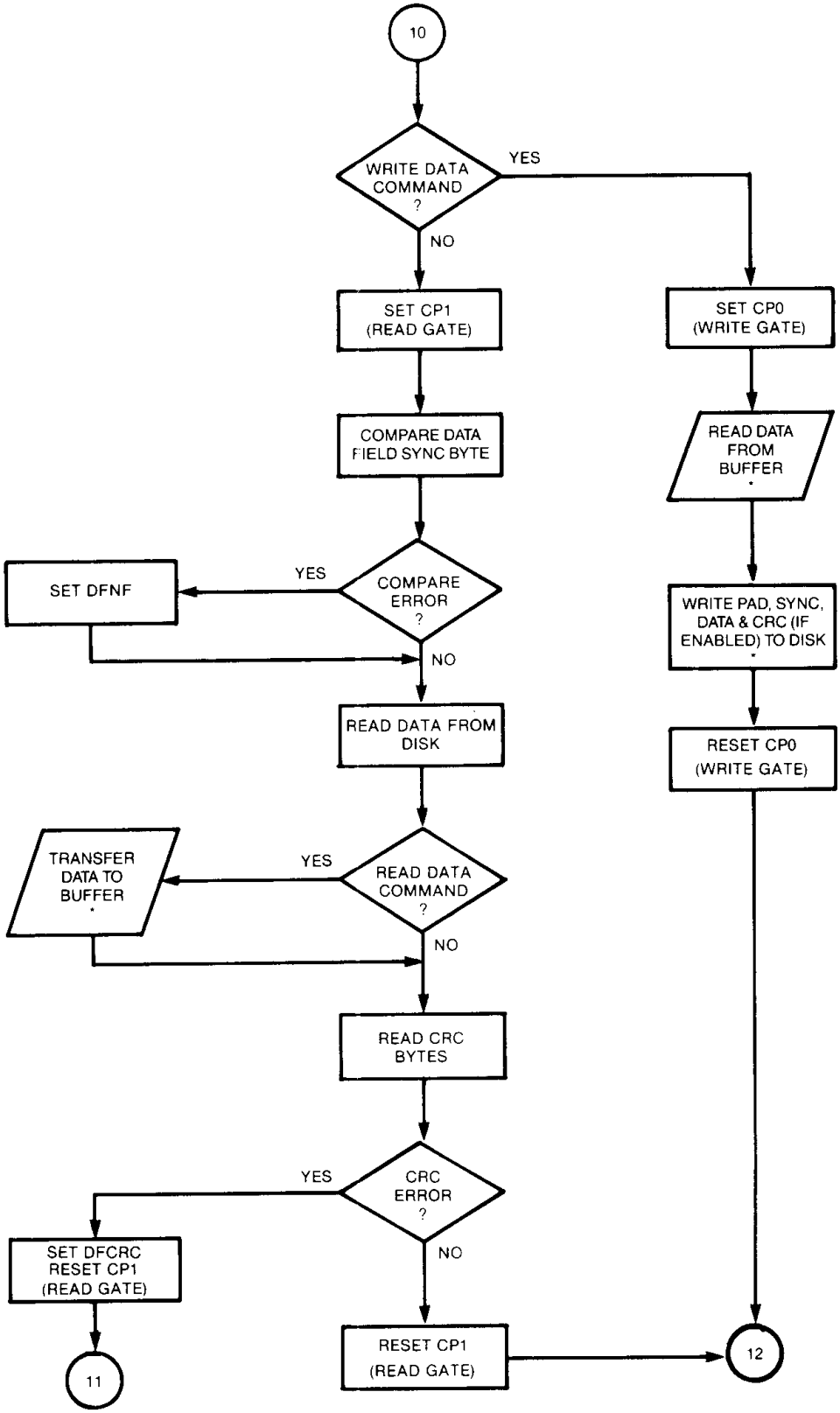

6
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
WRITE DATA COMMAND ?
YES
NO
BRDY RECEIVED ?
NO
YES
RESET BDRQ PULSE BCR
NO
INDX OR SCTR PULSE RECEIVED ?
YES
SET BCS PULSE BCR
7

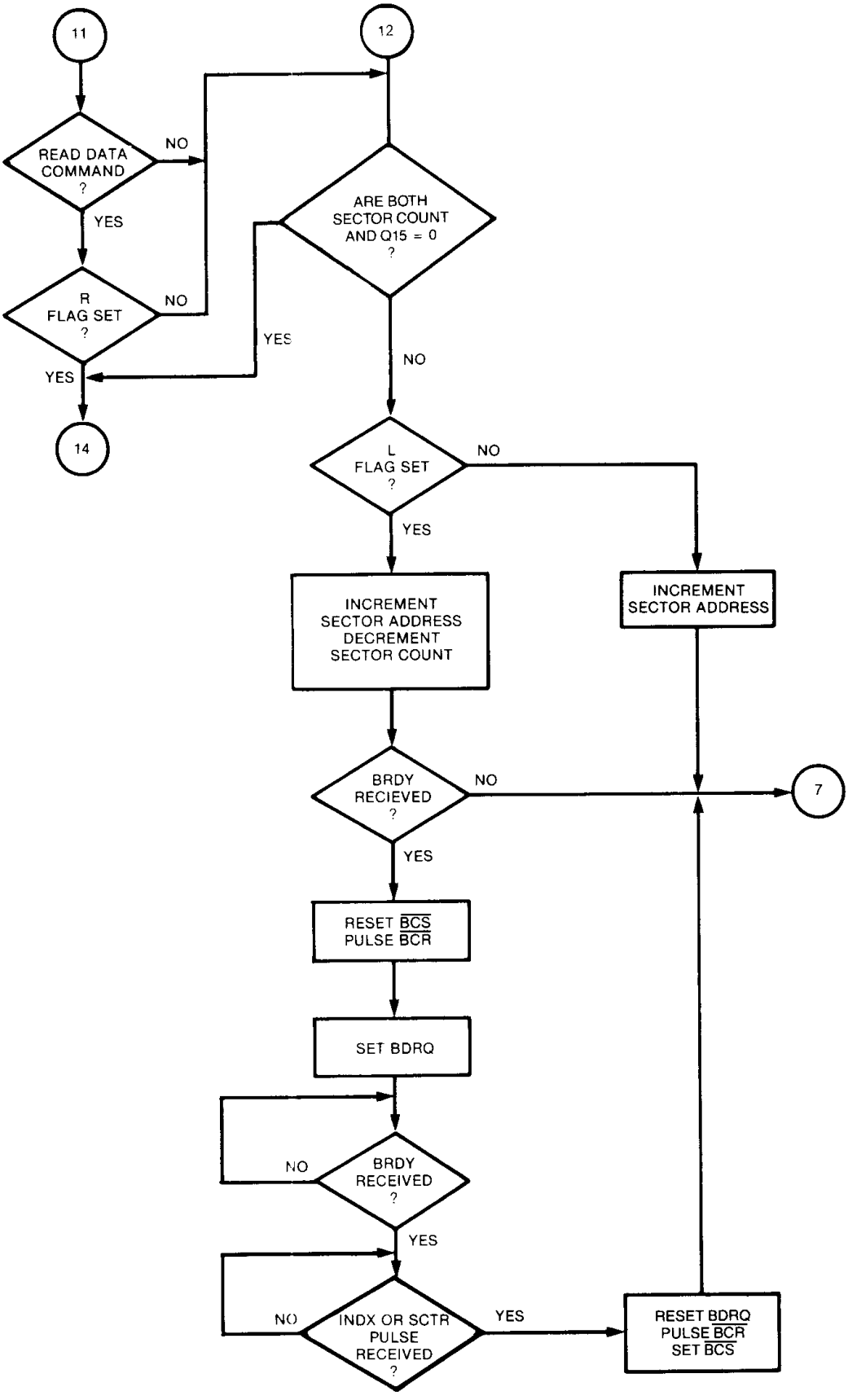

7
INDX OR SCTR PULSE RECEIVED ?
NO
YES
FORMAT COMMAND ?
YES
NO
SET CP1 (READ GATE) (7 1/2 BYTES FROM INDX OR SCTR PULSE)
VERIFY COMMAND ?
YES
NO
L FLAG SET ?
NO
YES
8
INDX COUNT = 1 ?
NO
YES
RESET RG
SECTOR COUNT = 0 ?
NO
YES
DECREMENT SECTOR COUNT RESET RG
FORMAT OR VERIFY COMMAND ?
YES
NO
P FLAG SET ?
NO
YES
READ WORD FROM BUFFER
YES
FORMAT COMMAND ?
NO
YES
13
14
INDX COUNT = 0 ?
NO
(1 = 2)
YES


8
COMPARE ID SYNC CYLINDER, AND HEAD ID FIELD, BYTES FROM DISK
SEEK, OR READ ID FIELD COMMAND ?
YES
NO
COMPARE SECTOR ID FIELD BYTE FROM DISK
COMPARE ERROR DETECTED ?
YES
NO
SET ID NF
READ IDCRC BYTES FROM DISK
CRC ERROR DETECTED ?
YES
NO
SET IDCE
RESET CPI (READ GATE)
9

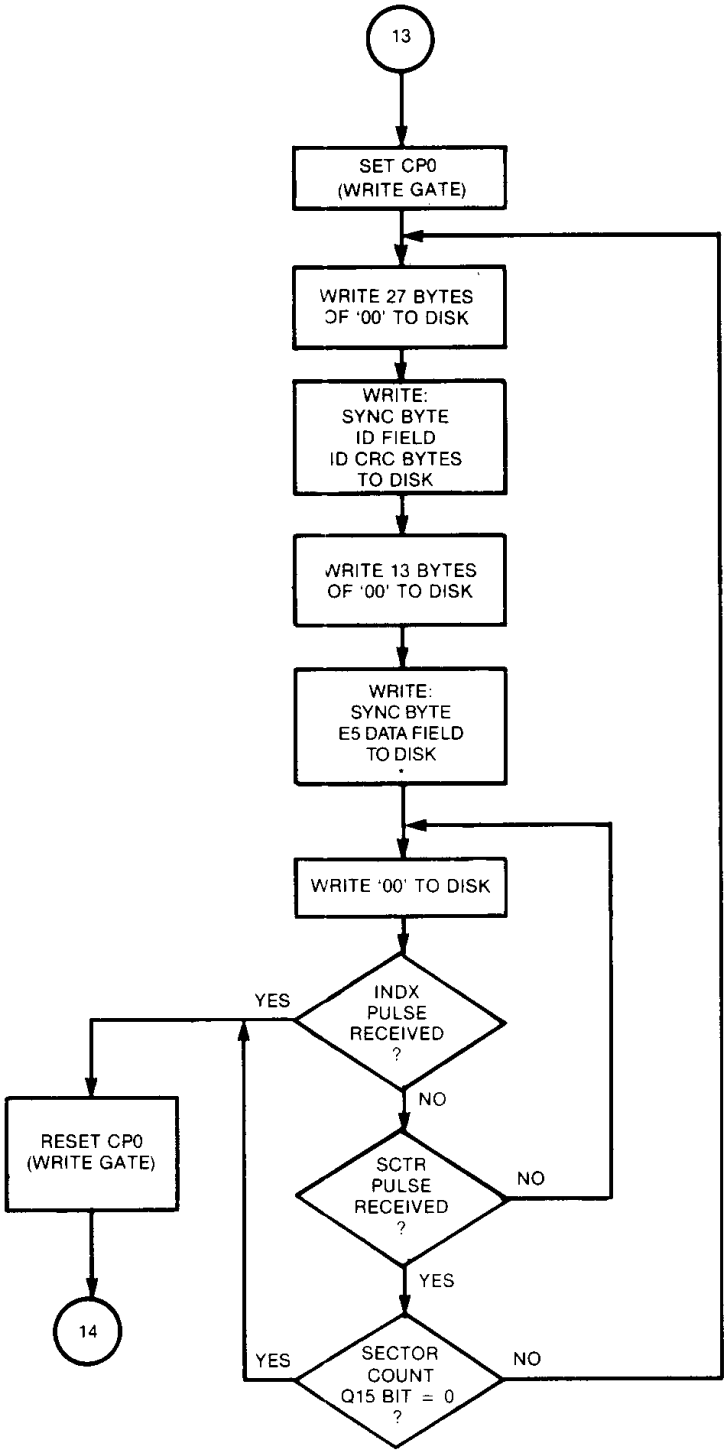


Note: If the R Flag is not set, 8 additional bytes are included in the Data Field for appended ECC.

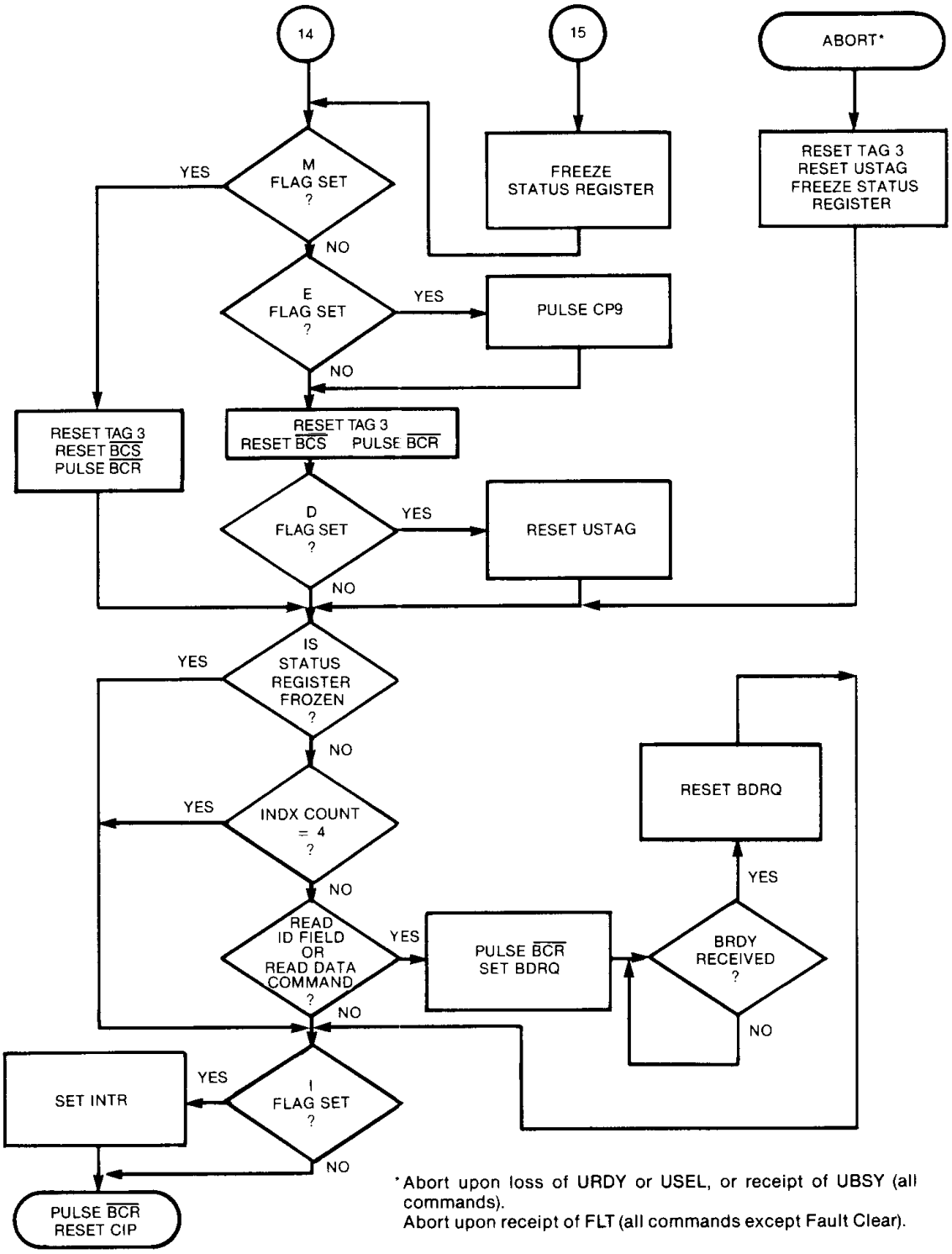

10
WRITE DATA COMMAND ?
YES
NO
SET CP1 (READ GATE)
SET CP0 (WRITE GATE)
COMPARE DATA FIELD SYNC BYTE
READ DATA FROM BUFFER
SET DFNF
YES
COMPARE ERROR ?
WRITE PAD, SYNC, DATA & CRC (IF ENABLED) TO DISK
NO
READ DATA FROM DISK
RESET CP0 (WRITE GATE)
TRANSFER DATA TO BUFFER
YES
READ DATA COMMAND ?
NO
READ CRC BYTES
YES
CRC ERROR ?
SET DFCRC RESET CP1 (READ GATE)
NO
RESET CP1 (READ GATE)
11
12



Note: if the R flag is not set, 8 additional E5 bytes are included in the Data Field for ECC extension.



* Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).



*Abort upon loss of URDY or USEL, or receipt of UBSY (all commands).
Abort upon receipt of FLT (all commands except Fault Clear).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... -0.5V to +7V
Operating Temperature ... 0°C(32°F) to 70°C(158°F)
Storage Temperature ..... -55°C(-67°F) 50 +125°C(257°F)

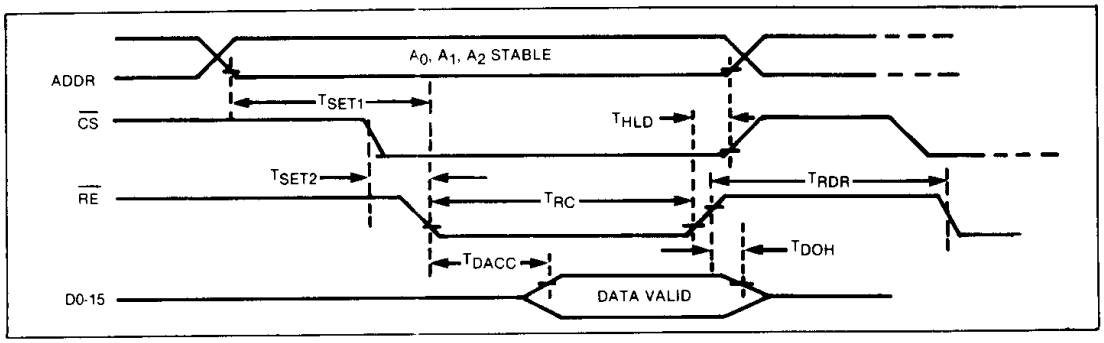
NOTE:

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC Operating Characteristics T_A = 0°C to 70°C; V_{SS} = OV, V_{CC} = +5V ±.25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = 100μA
V_{OL}	Output Low Voltage		0.4	V	IO = 1.6 mA
I_{CC}	Supply Current		200	mA	All Outputs Open
	FOR PINS 25, 26,27:				See Note 1
V_{IH}	Input High Voltage	V_{CC}		V	
V_{IL}	Input Low Voltage		V_{SS} + ≤0.4 V	V	

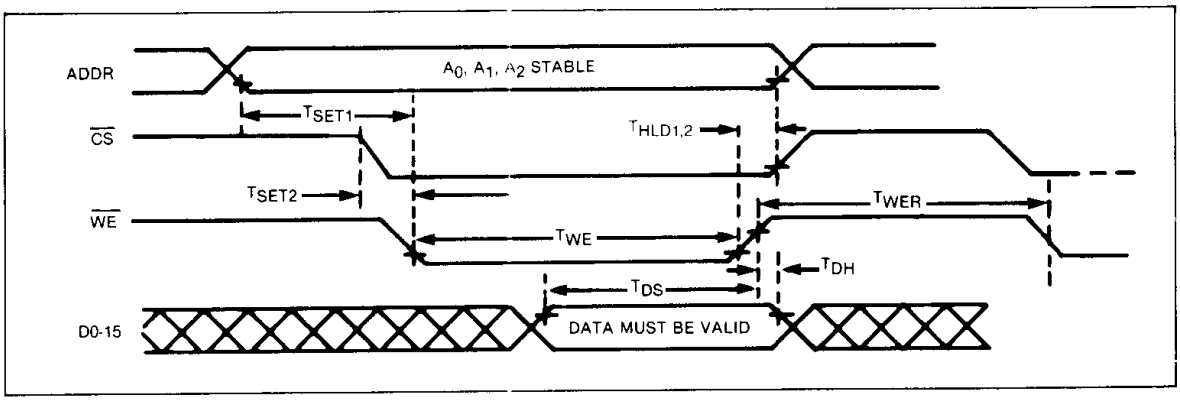
AC Timing Characteristics T_A = 0°C to 70°C; V_{SS} = OV, V_{CC} = +5V ±.25V



HOST READ TIMING

HOST READ TIMING

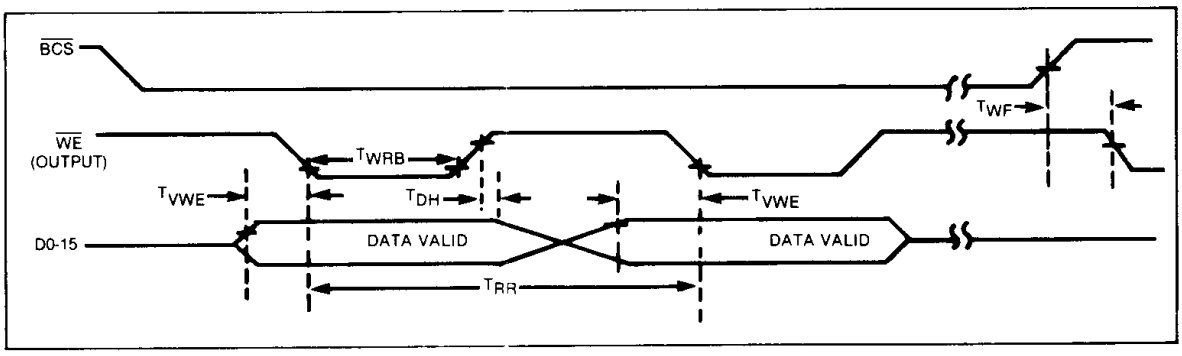
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$^tSET\ 1$	ADDR, Set up to $\overline{RE}$	80		nsec	
$^tSET\ 2$	$\overline{CS}$ Set up to $\overline{RE}$	0		nsec	
^tDACC	Data Valid from $\overline{RE}$		375	nsec	C_L = 100pF
^tRC	Read Enable Pulse Width	.375	5.0	μsec	
^tDOH	Data Hold from $\overline{RE}$		150	nsec	
^tHLD	ADDR. $\overline{CS}$, Hold from $\overline{RE}$	0		nsec	
^tRDR	Read Recovery Time	500		nsec	



HOST WRITE TIMING

HOST WRITE TIMING

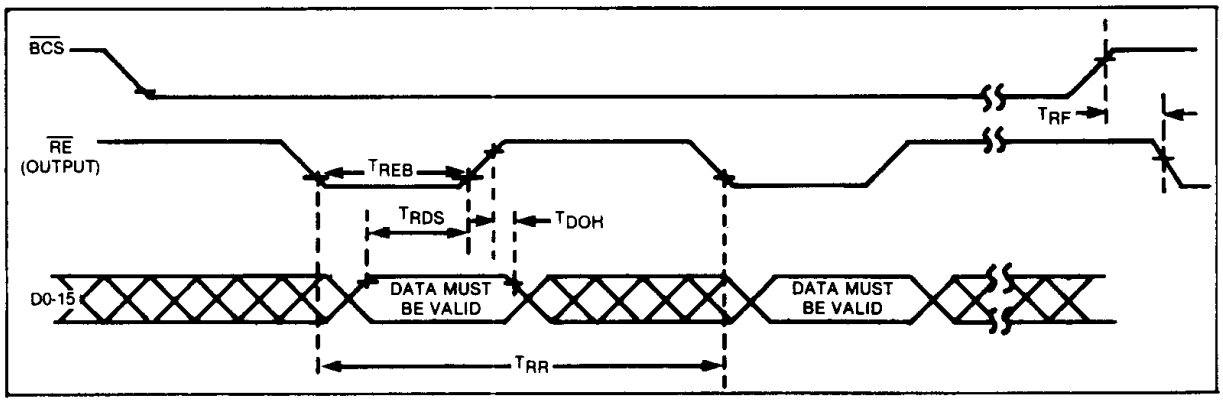
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
$^tSET_1$	ADDR, Set up to $\overline{WE}$	80		nsec	
$^tSET_2$	$\overline{CS}$ Set up to $\overline{WE}$	0		nsec	
^tDS	Data Bus Setup to $\overline{WE}$	100		nsec	
^tWE	Write Enable Pulse Width	200		nsec	
^tDH	Data Bus Hold from $\overline{We}$	80		nsec	
$^tHLD_1$	$\overline{CS}$ Hold from $\overline{WE}$	0		nsec	
$^tHLD_2$	ADDR Hold from $\overline{WE}$	30		nsec	
^tWER	Write Recovery Time	1.0		μsec	



BUFFER WRITE TIMING

BUFFER WRITE TIMING (READ SECTOR CMD)

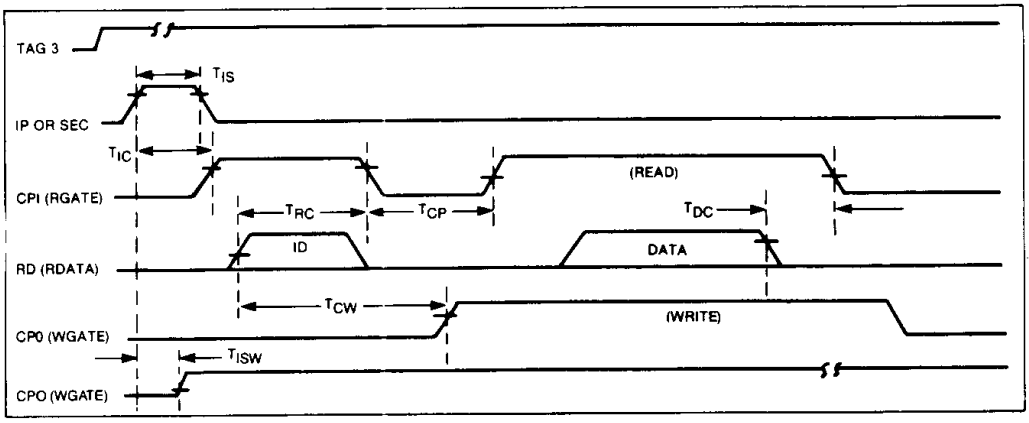
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
^tWRB	$\overline{WE}$ Output Pulse Width		4		SC	See Note 2
^tVWE	Data Set up to $\overline{WE}$		4		SC	See Note 2
^tDH	Data Hold from $\overline{WE}$		4		SC	See Note 2
^tRR	$\overline{WE}$ Repetition Rate		16		SC	See Note 2
^tWF	$\overline{WE}$ Float from $\overline{BCS}$			0	nsec	



BUFFER READ TIMING

BUFFER READ TIMING (WRITE SECTOR CMD)

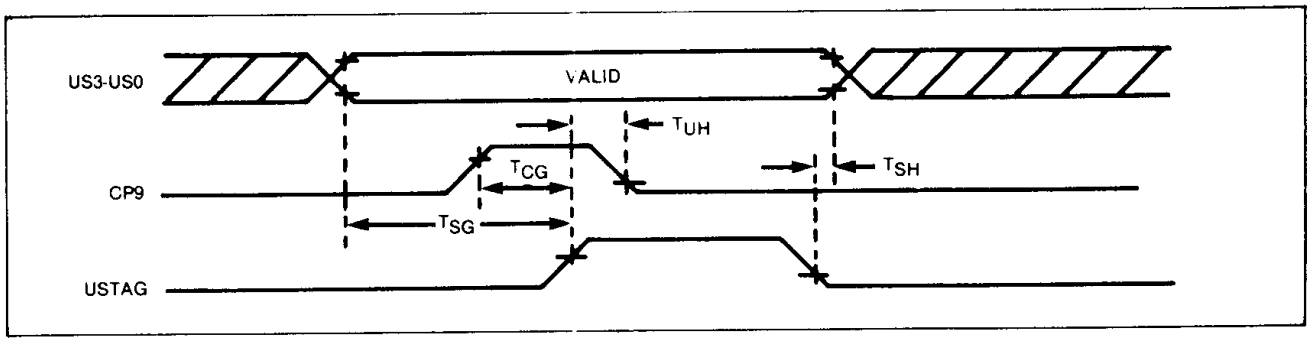
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tREB	$\overline{RE}$ output Pulse Width		4		SC	See Note 2
tRDS	Data Setup to $\overline{RE}$	140			nsec	
tRR	$\overline{RE}$ Repetition Rate		16		SC	See Note 2*
tDOH	Data Hold From $\overline{RE}$	80			nsec	
tRF	$\overline{RE}$ Float from $\overline{BCS}$			0	nsec	



DISK R/W CONTROL TIMING

DISK R/W CONTROL TIMING (SCLK = 9.677 MHZ)

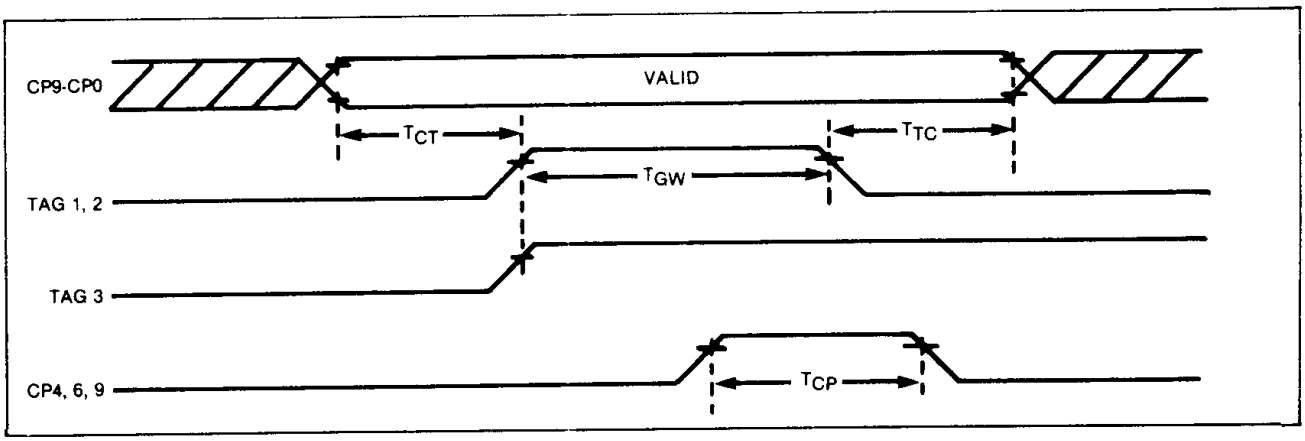
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tIS	Index/Sector Pulse Width	.2	1.25	3.0	μsec	
tIC	Index/Sector to CP1 High		60		SC	See Note 3
tRC	CP1 Low from Read Data		56		SC	See Note 3
tCP	CP1 Low to CP1 High		12		SC	See Note 3
tDC	Last Read Data to CP1 Low		16		SC	See Note 3
tCW	CP0 High from Read Data		60		SC	See Note 3
tSW	Index/Sector High to CP0 High on FORMAT			250	nsec	



UNIT SELECT TIMING

UNIT SELECT TIMING (SCLK = 9.677 MHZ)

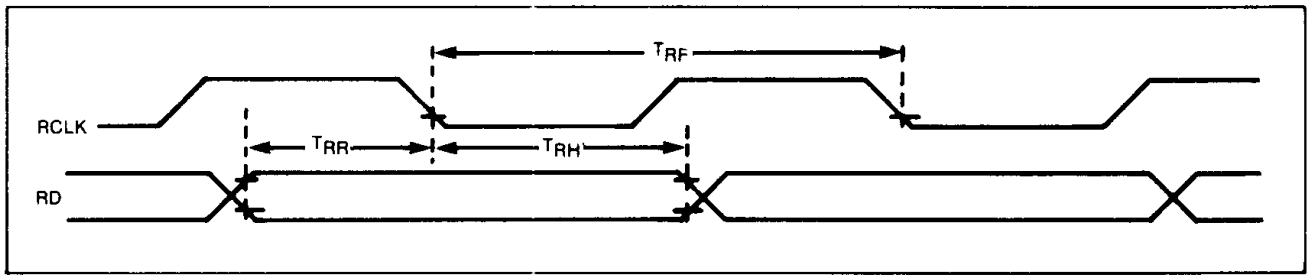
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
^tSG	US3-US0 Setup to USTAG	1.0			μsec	
^tCG	CP9 Setup to USTAG		4		CLK	See Note 4
^tUH	CP9 Hold Time from USTAG		4		CLK	See Note 4
^tSH	US3-US0 Hold Time from USTAG	1.0			μsec	



CP TAG TIMING

CP TAG TIMING 9SCLK = 9.677 MHZ)

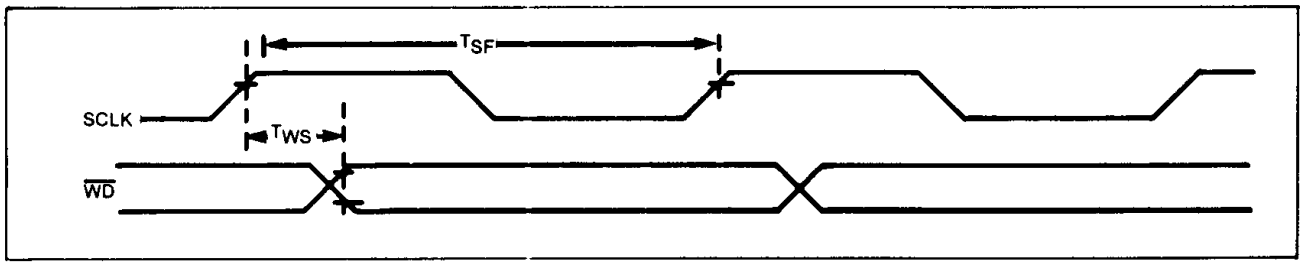
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
^tCT	CP9-CP0 Set up to TAGS 1, 2, or 3		5		CLK	See Note 4
^t6GW	TAGS 1 & 2 Pulse Width		4		CLK	See Note 4
^tTC	CP9-CP0 Hold Time from TAG 1, 2 Low		2		CLK	See Note 4
^tCP	CP4, 6, 9 Pulse Width During TAG 3 True		4		CLK	See Note 4



READ DATA TIMING

READ DATA TIMING

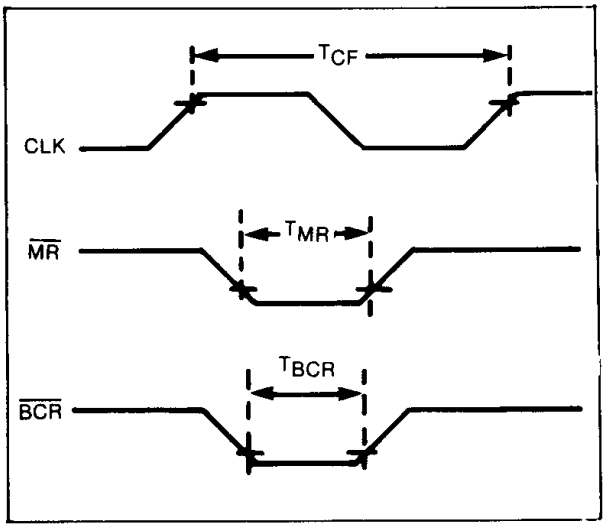
SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITIONS
tRF	RCLK Frequency	1.0	9.677	10.1	MHZ	
tRR	Read Data Setup to RCLK Low	35			nsec	
tRH	Read Data Hold Time from RCLK Low	0			nsec	



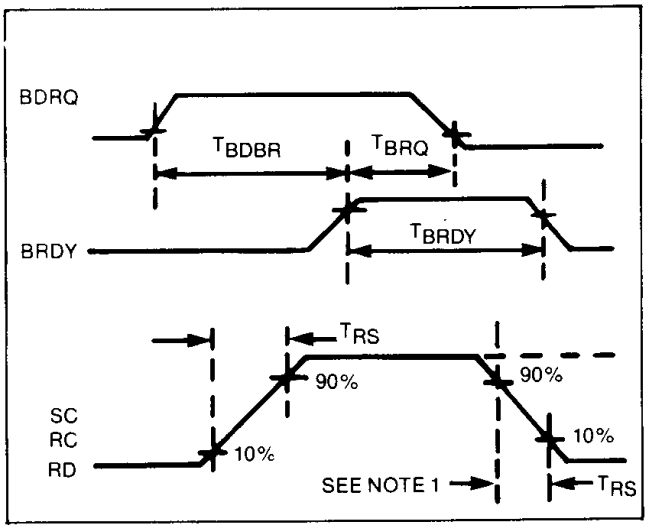
WRITE DATA TIMING

WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
tSF	Servo Clock Frequency	1.0	9.677	10.1	MHZ	
tWS	WD Valid from Servo Clock High			85	nsec	C_L = 15 pf. See Note 5



MISCELLANEOUS TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
$_tCF$	Master Clock Frequency		2.0	2.5	MHZ	50% Duty Cycle
$_tMR$	Master Reset Pulse Width	12			μsec	CLK Active
$_tBCR$	$\overline{BCR}$ Pulse Width		4		CLK	See Notes 4&7
$_tBRQ$	BDRQ Reset from BRDY	50		600	nsec	
$_tRS$	Rise of Fall Time			15	nsec	See Note 1
$_tBDBR$	BRDY High from BDRQ High	4				See Note 8
$_tBRDY$	BRDY Pulse Width	4				See Note 8

NOTES:

1. It is recommended to buffer the line receiver stage with a TTL or Schottky TTL stage on pins 27, 28 and 29. A current sink capability of 48 mA with a 100 ohm pull-up resistor will provide both the required rise and fall times and also the required voltage swing. It is recommended to locate these buffers physically near the WD 1050 to minimize inductive ringing.
2. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. SCLK periods is specified. (Disregard "TYP" in this case).
3. Timing is a function of the Servo Clock (SCLK) frequency. The number of negative SCLK transitions plus 400 nsec. max. is specified. (Disregard the "TYP" in this case).
4. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods is specified. (Disregard the "TYP" in this case).
5. WD is an open drain output and requires an external 1K ohm pull-up to V_{CC}. This pin is inverted relative to the SMD interface cable. It is recommended that this output go to the 'D' input of a 74S74 flip-flop that is clocked by the SCLK buffer described in Note 1. The 74S74 Q output may then connect to the interface line driver. It is recommended that the 74S74 be located physically near the Wd1050.
6. All AC timing is measured at V_{OL} = 0.8 V, V_{OH} = 2.0V.
7. Certain occurrences of BCR can have variable pulse widths. Deactivation of $\overline{BCR}$ is dependent upon the next occurance of INDX or SCTR for these instances.
8. Timing is a function of the Master Clock (CLK) frequency. The number of CLK periods, plus 100 nsec. min. is specified.

WD1050 SMD Controller/Formatter Application Notes

INTRODUCTION

Prior to the introduction of 5¼ and 8 inch Winchester disks drives in the late 1970's, minicomputers and mainframes were the only systems that utilized rigid disks. These drives were relatively expensive; sometimes as high as $200 per megabyte. They offered the minicomputer designer a fixed or removable drive with capacities from 10 to 300 megabytes. Initially, there was no need for interface standards. IBM Corporation was the predominant leader in the marketplace, and anyone else who decided to build drives were IBM compatible units. But as competition increased, more and more companies began producing lower cost units with increased capacity. Minicomputer companies were being formed, offering complete systems that were non-IBM compatible. The disk drive race was on.

In order to standardize a common interface and to prevent product obsolescence, Control Data Corporation developed an intelligent interface called the Storage Module Device or SMD. This interface allowed a variety of drives to use the same hardware signals, even though their capacities and physical sizes differed. Variations of the SMD were also introduced. Some of these are the CMD (Cartridge Module Drive) and the MMD (Memory Module Drive). The SMD interface began to gain acceptance in the marketplace as competitive manufacturers offered "SMD-compatible" drives as well. The SMD was well on its way to becoming a defacto standard in the industry. Its longevity has been proved by over 10 years worth of product based on this "intelligent" interface.

With today's smaller diameter low cost drives, where does SMD stand? Oddly enough, the higher capacity 5¼ and 8 inch Winchesters are reviving the SMD protocol. Because the SMD interface offers several advantages over the ST506 type interface in the high capacity arena (such as parallel seek instead of serial step pulses), several manufacturers are planning to offer the SMD on their traditional small system disk drives. The SMD, however, is not a trivial interface when it comes down to designing a controller.

A LOOK AT THE SMD

Figure 1 illustrates the electrical signals of the SMD. Two separate cables are used: one for control and one for data. The control cable (commonly referred to as the "A" cable) is responsible for all head movement, status reportings and issuing commands. The data cable (or "B" cable) is used for reading and writing NRZ data to a particular sector on the drive. Note that all lines on both cables are differential signals; they require a differential driver/receiver at both ends.

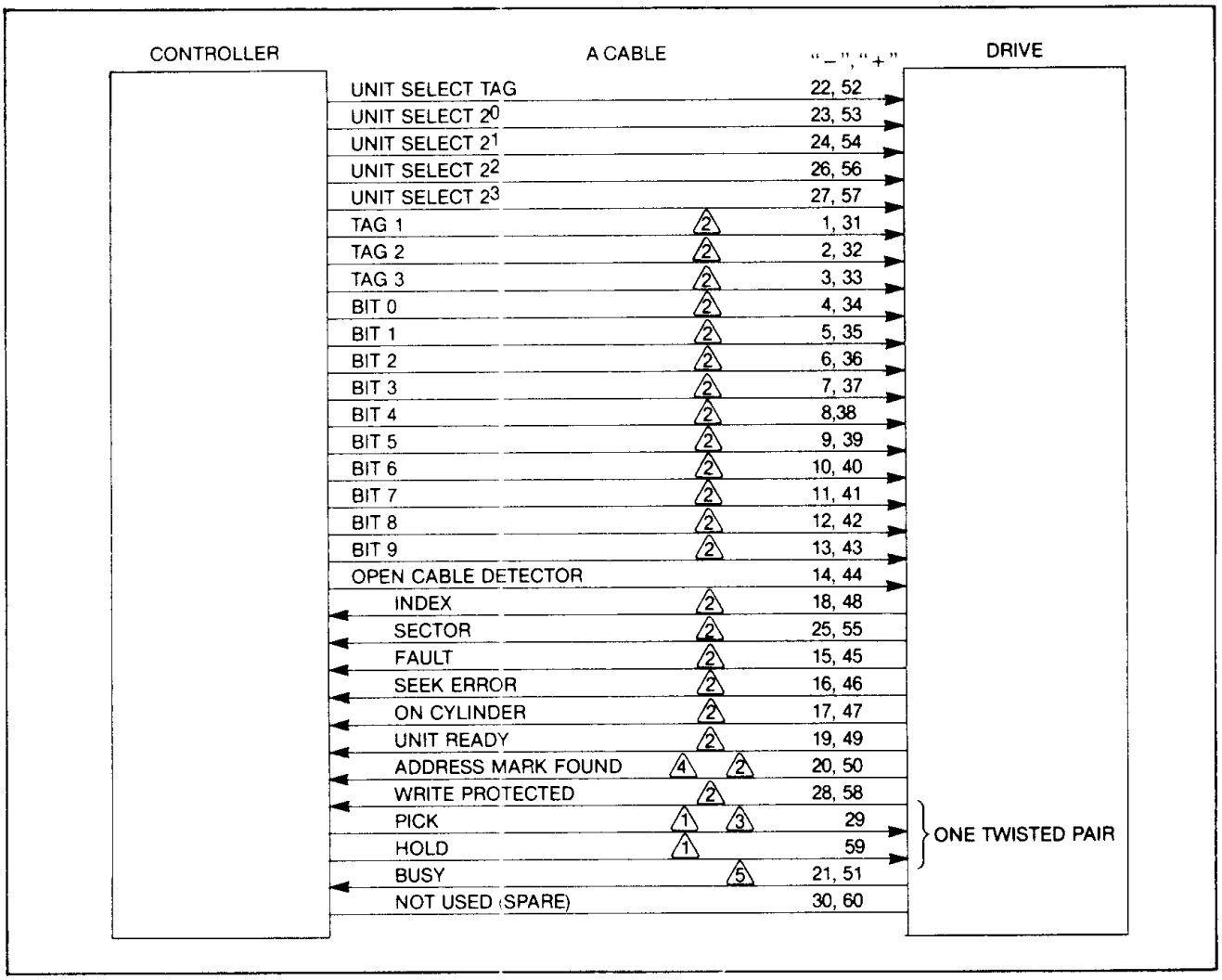
Primary control over the "A" cable is based upon a 10 bit bus called the Tag Bus. These 10 lines send particular information to the driver and initiate a command. Three Tag lines (Tag 1-3) are used to tell the drive what the bus contains during the strobing of the Tags. For example, Tag 1 tells the drive that the Tag bus contains a cylinder number that the head assemblies should be moved to for reading or writing. Tag 2 tells the drive the Head/Volume to select, while Tag 3 is used to initiate read or write commands and to perform special recovery routines.

Drives are selected by separate UNIT SELECT lines on the "A" cable, which have their own strobe line called Unit Select Tag. Other signals on the "A" cable serve status reporting type functions. SEEK ERROR and ON CYLINDER are examples of status lines.

The "B" cable is used to transmit serial, NRZ data to and from the drive. Associated with the R/W lines are clocks: Write Clock for write recovery and Read Clock for read recovery. Additional signals aid in determining the status of each drive on the bus.

In a multiple drive configuration, the two cables are connected as shown in Figure 2. The "A" cable is daisy-chained; each drive is tied together in parallel with termination resistors on the last drive. The "B" cable is radial-connected; a separate cable from each drive connects to the controller.

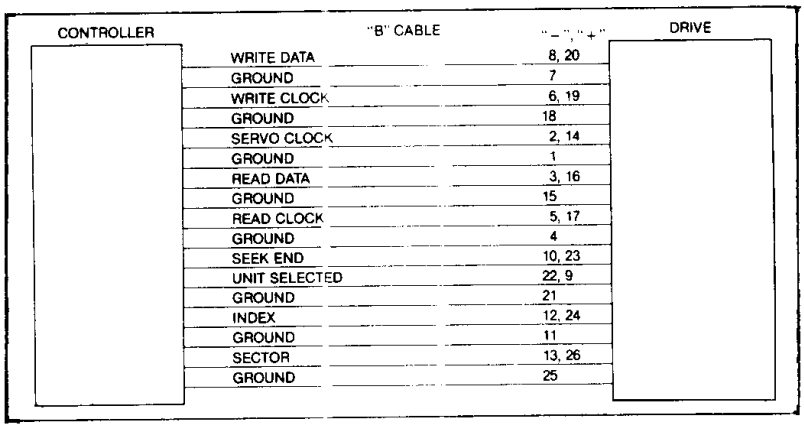
It is probably obvious by now that a great deal of control is necessary to perform even a simple Read or Write operation on the SMD Bus. The drive controller must perform simultaneous operations on both cables, as well as monitoring status signals to determine successful execution of operation. A typical SMD controller can consist of 150 SSI/MSI Integrated Circuits and a local microprocessor or bit-slice to perform the necessary functions. SMD controller designers of today can take advantage of a new LSI chip that will reduce the number of I.C.'s to well under 40.



NOTE: 60 Position
30 Twisted pair–straight flat cable
Maximum Length–100 ft. (30.48 meters)

1 Special signal, not a balanced transmission signal
2 Gated by unit selected
3 Not interpreted, is Daisy chained, no driver connection within the LMD
4 Not activated, is Daisy chained, always a logic zero output if unit is selected
5 Not generated, is Daisy chained, no driver connection within the LMD

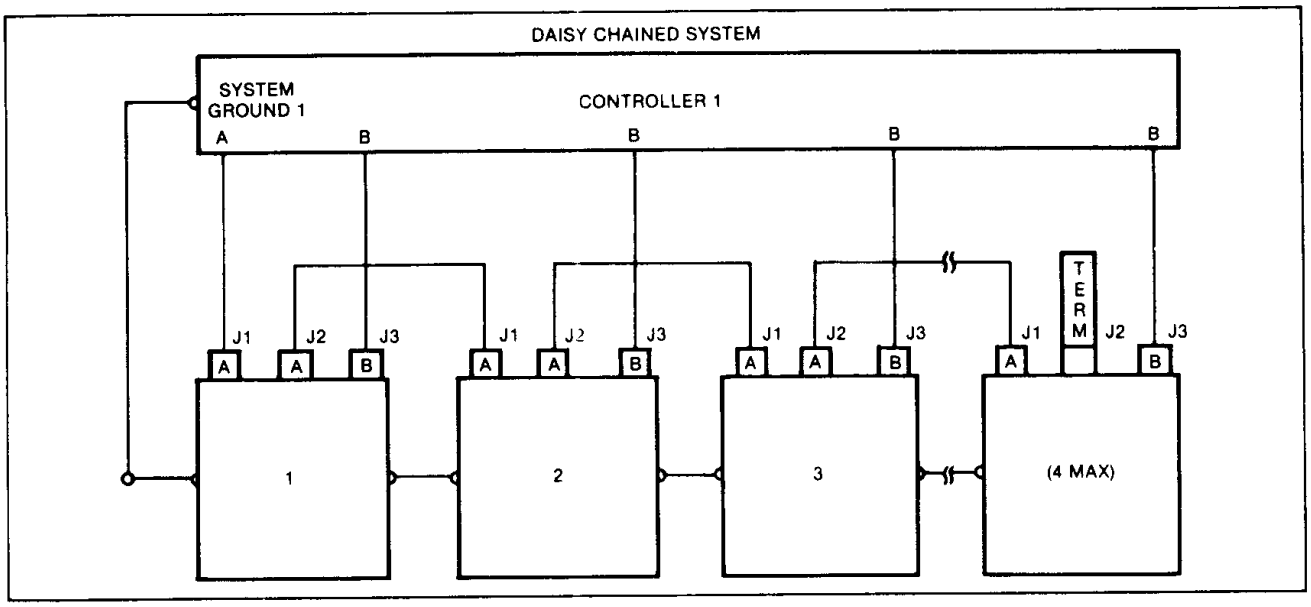
Figure 1(A). Tag Bus I / O Interface ("A" Cable)



NOTES:
1. 26 conductor flat cable.
   Maximum Length-50 ft. (15.24 meters)
2. No signals gated by "A" cable unit select

Figure 1 (B). "B" Cable Interface

NOTES:
1. Maximum individual A cable lenghts = 100 feet (30.48 meters)
2. Maximum individual B cable lenghts = 50 feet (15.24 meters)



NOTES:
1. Termination of "A" cable lines are required at controller and the last unit of the Daisy chain or each unit in a radial configuration.
2. Termination of "B" cable receiver lines are required at the controller and are on the unit receiver cards.
3. Maximum cumulative "A" cable length per controller = 100 feet (30.48 meters) maximum individual "B" cable lenght = 50 feet (15.24 meters).

Figure 2. Daisy Chained System

WD1050 SMD CONTROLLER CHIP

Western Digital Corporation offers an LSI controller chip for the SMD protocol. This device, called the WD1050, has been designed to interface an SMD rigid disk drive to a 16-bit Host processor. A set of macrocommands allows the Host to request a specific operation such as seek, read, etc., in which all Tag and control lines on the drive interface perform their appropriate signaling. By using this device, the designer is free to concentrate on operating system software intervention, rather than meeting electrical requirements of the drive protocol. Figure 3 shows the Block Diagram of the WD1050. Data or commands are entered in 16-bits through the Data I/O Buffers. This information is stored in the Task File and tells the device parameters about a specific command. This could be a cylinder address, a sector number to search for, a particular drive that should be selected, etc. After this information is loaded, a command is issued. The Control Unit instructs the various pins on the drive interface to generate their proper signals. Upon completion of a command, the WD1050 interrupts the Host and reports via the status register if any errors were encountered. The device is then ready for the next command.

Figure 4 illustrates the Task File and its contents. The Host processor generates the three address lines shown, then performs a read or write operation to the selected 16-bit register. All registers can be read or written to with the exception of the Command/Status Register. Since both of these registers share a common address location, a "write" will cause a command to execute, while a "read" will cause the status to be fetched from the device. This memory mapped architecture allows the Host to randomly access any location in the Task File without disrupting or reloading the data in other registers.

The Instruction Set of the WD1050 is shown in Figure 5. Return to Zero, and Seek Cylinder commands are used for head movement, while the remaining commands are responsible for reading or writing data. Each Read/Write command also contains an "Implied Seek" feature. This allows the Host processor to issue a read or a write function even though the heads are sitting over the wrong cylinder. The WD1050 will perform an automatic seek operation

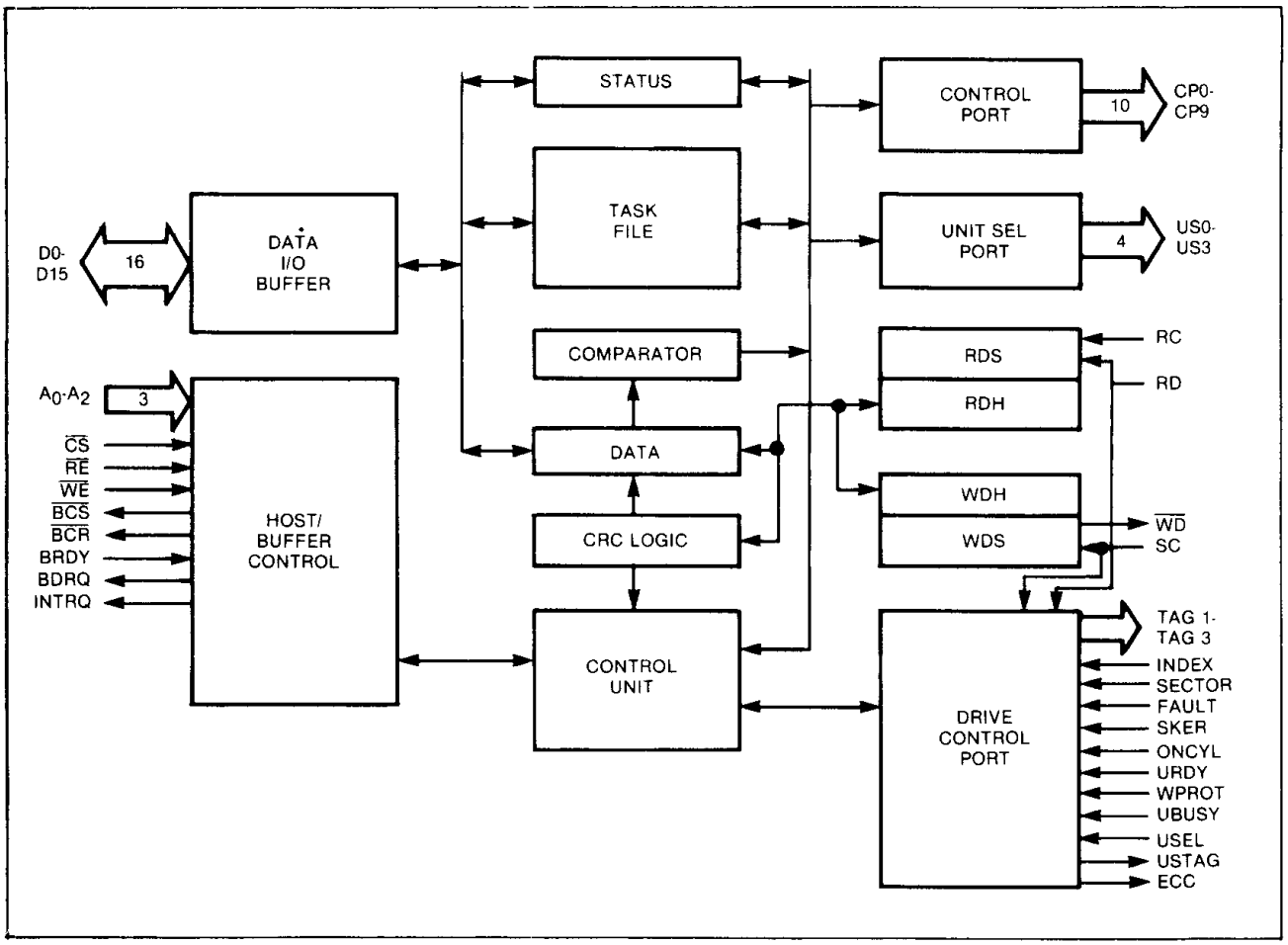


FIGURE 3. WD1050 BLOCK DIAGRAM

before the actual read or write. Because of this, the head movement commands (Return to Zero and Seek Cylinders) are usually restricted for use in overlap seeks. This is the ability to perform seek operations on several drives simultaneously.

After a command has finished execution, the WD1050 will report to the Host through its Status Register (shown in Figure 6) how successful a command execution was. Many commands will not execute if certain conditions are not met. For example, a FAULT condition, shown by status bit 6, will prevent all commands except Fault Clear from executing. Read / Write commands will not execute if the "On Cylinder" bit is false, either. In summary, the Host must examine the various bits to determine what action to take next.

HOST SECTOR BUFFER

Because of the high data rates used on the SMD protocol (9.677 Mbits / sec.), even a fast micro- processor will have trouble keeping up in a Programmed I / O environment. For this reason, the WD1050 has been designed to use a sector buffer.

Figure 7 shows a Host Interface to the device using a low cost Static RAM and a binary counter. Since the WD1050 will be transferring data directly to the RAM, a transceiver will be needed to isolate the Host from the RAM / WD1050 logic. This transceiver, as shown in Figure 7, is disabled by Buffer Chip Select (BCS). Whenever BCS is active, the WD1050 is reading or writing to the RAM. During this condition, the Host cannot read status or any other registers. When the data transfer is over, the device disables BCS and enables Buffer Data Request (BDRQ). This tells the Host that the buffer is now available for use. If a read command had been issued, the sector buffer would have filled the data requested.

During this process, the WD1050 takes control over Write Enable ($\overline{WE}$) by making it an output. It places its first data word on the bus and strobes $\overline{WE}$. This causes a write operation to the RAM and increments the binary counter that is tied to the RAM's address lines. Another $\overline{WE}$ strobe then occurs, increments the counter again, and the process continues until the sector is transferred. If a single sector operation was requested, the WD1050's use of the sector buffer is completed. However, multiple sectors may be transferred as an option within the command. In this case, the Buffer Ready (BRDY) input to the device is examined. If false, the WD1050 assumes there is more RAM available and transfers the next sector of data. The BRDY signal is normally generated by a "carry" or overflow out of the binary counter. If BRDY has gone active but the device still has more sectors to transfer, BDRQ will be made active to allow the Host to unload the data in the RAM, making room for the additional sectors. The WD1050 will then resume its operation of finding a sector and writing the data to the buffer. After all the data has been transferred, the command will terminate. To complete the scheme, a signal called Buffer Counter Reset (BCR) is used to zero the counters before the Host or device starts a transfer. A BCR pulse is generated whenever BCS makes a transition.

By using this buffer scheme, the designer has the ability with one command to transfer the maximum number of sectors specified by the Sector Counter in the SDH Register.

CONCLUSION

Using the WD1050 as the basis for an SMD controller design, can reduce the complexity of the design effort considerably. However, challenges still remain in interfacing the device to maximize the efficiency of the interface. The buffer control signals, for example, can be changed to accomodate a DMA controller for higher throughput. ECC can be appended to the buffer for data correction purposes. A local microprocessor dedicated on the SMD controller board could even be used to emulate existing SMD / Host software routines.

Regardless of the application, the WD1050 signifies a trend in the semiconductor industry to not only replace logic in a discrete design, but to offer complete functions in large scale integration. This device is certainly not the first to offer an LSI functional building block, and will not be the last.

A2	A1	A0	REGISTER SELECTED
0	0	0	Head Number/Sector Address
0	1	0	Sector Count/Length/Unit Address
1	0	0	16 Bit Cylinder Register
1	1	0	Command Register (Write Only)
1	1	1	Status Register (Read Only)

Figure 4. WD1050 Task File

COMMAND	LSB				COMMAND REGISTER BITS											MSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault Clear	1	0	0	0	0	0	0	I	0	0	0	0	U	S	E	L
Return to Zero	1	0	0	1	V	L	O	I	0	0	0	M	U	S	E	L
Seek Cylinder	1	0	1	0	V	L	O	I	Z	C	H	M	U	S	E	L
Read ID Field	1	0	1	1	R	L	O	I	Z	C	H	M	U	S	E	L
Read Sector	1	1	0	0	R	L	O	I	Z	C	H	M	U	S	E	L
Write Sector	1	1	0	1	R	L	O	I	Z	C	H	M	U	S	E	L
Format	1	1	1	0	R	P	O	I	Z	C	H	M	U	S	E	L
Verify	1	1	1	1	R	P	O	I	Z	C	H	M	U	S	E	L

FLAG SUMMARY	
V = Verify	I = Interrupt Enable
R = CRC Enable	Z = Volume/Head change
L = Logical Sectoring	C = Cylinder Address
P = Programmable Sectors	H = Head Selection
O = On Cylinder	M = Marginal Data Recovery
E = Priority Release/Early	U = Unit Sel/Servo Minus
L = Unit Deselect/Late	S = Priority Sel/Servo Plus

Figure 5. WD1050 Instruction Set

BIT	NAME	DESCRIPTION
0	ID Field Not Found (ID/NF)	Set if the sync character preceding the ID Field or ID Field contents read from the disk do not match the respective Task File contents.
1	ID CRC Error (IDCE)	Set if the CRC calculation on the ID Field read from the disk is in error.
2	Data Field Not Found (DFNF)	Set if the Data Field sync pattern following the ID Field does not match the sync character.
3	Data Field CRC Error (DFCE)	Set if the CRC Calculation on the Data Field read from the disk is in error.
4	Not Used	This bit is not used; it is forced to a zero.
5	Buffer Data Request (BDRQ)	Reflects the Buffer Data Request output.
6	Fault (FLT)	Reflects the status of the Fault (FLT) input.
7	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output.
8	Seek Error (SKER)	Reflects the status of the Seek Error (SKER) input.
9	On Cylinder (OCYL)	Reflects the status of the On Cylinder (OCYL) input.
10	Unit Ready (URDY)	Reflects the status of the Unit Ready (URDY) input.
11	Write Protect (WPRT)	Reflects the status of the Write Protect (WPRT).
12	Unit Selected (USEL)	Reflects the status of the Unit Selected (USEL) input.
13	Unit Busy (UBSY)	Reflects the status of the Unit Busy (UBSY) input.
14	CIP	Set when a command is in progress.
15	Buffer Chip Select (BCS)	This bit is an inverted copy of the Buffer Chip Select ($\overline{BCS}$) output. This bit also appears in STATUS Bit 7.

Figure 6. WD1050 Status Register

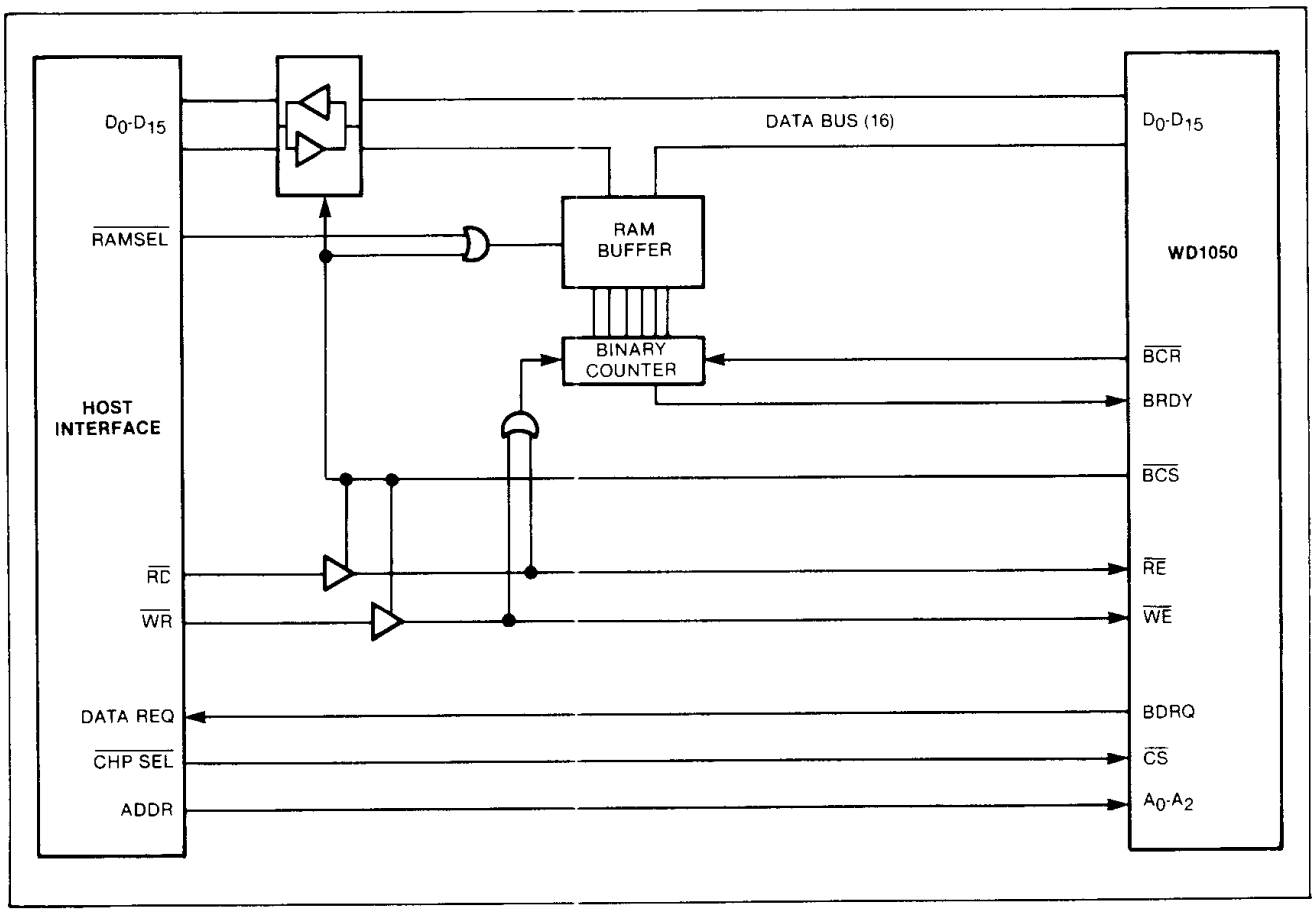


Figure 7. WD1050 Host Interface