WD10C27

Data

Separator

WESTERN DIGITAL

13

TABLE OF CONTENTS

T-52-38

T-52-38

TABLE OF CONTENTS (Continued)

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

T-52-38

1.0 INTRODUCTION

T-52-38

1.1 GENERAL DESCRIPTION

The WD10C27 Read/Write Channel is a fully integrated LSI device intended for variable frequency applications in conjunction with the WD61C22 Hard Disk Controller/Buffer Manager.

In a typical application, the WD10C27 performs all of the handling of the sensitive read/write signals between a disk controller and data drivers and receivers. Raw read data corresponds to previous write data, with added phase, frequency, and write splice noise. The fundamental purpose of the WD10C27 is to remove these noise components and present a clean digital recovered data and reference clock to the controller.

1.2 Features

- General
  - Specifically designed for the WD61C22 Hard Disk Controller/Buffer Manager
  - Supports Zone Bit Recording from 7.5-27MBps with no component changes
  - 1.25 micron +5 volt only CMOS technology
  - Available in 52-pin EIAJ package
- Frequency Synthesizer
  - Programmable input reference frequency to 40 MHz
  - Multiple dividers for extremely high resolution
- Micro-Processor Interface
  - Eight bit Intel compatible multiplexed address/data port
  - Programmable test and low power modes
- Write Data Conditioner
  - Crystal controlled processing of the write data to eliminate pulse pairing
  - Programmable pattern dependent Skew Symmetric Precompensation matrix for precomp. of up to ±25% with 2^{-6} resolution
- Encoder/Decoder
  - IBM Compatible 1,7 RLL
  - Hard/soft sector support and Address Mark Detection
- Data Synchronizer
  - Precision internal self adjusting VCO compensates for component, temperature, voltage, and aging variations
  - Internal gain/bandwidth modulation linearizes loop gain and increases phase margin across zones
  - Dual gain charge pump for faster acquisition and better jitter rejection while tracking
  - Dual mode phase/phase-frequency detector eliminating quadrature and harmonic lock
  - mP controlled Window Shift Synthesis for window shifting up to ±50% of the window
  - Window monitoring capability
- Channel Control
  - 5-bit DACs specifically designed for use with the SSI8011 and SSI3040 read channel devices
  - Bandwidth, Boost and Hysteresis Control for ZBR
  - Two Programmable Micro Processor Ports

T-52-38

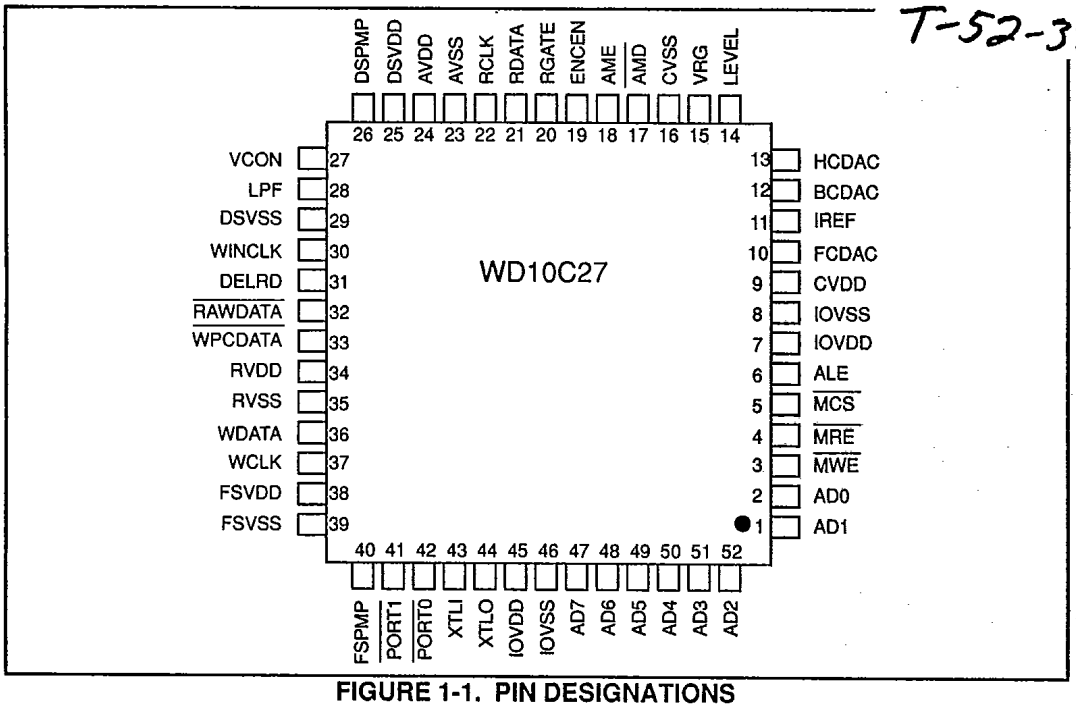


FIGURE 1-1. PIN DESIGNATIONS

T-52-38

PIN NUMBER (IO MAP)	MNEUMONIC	SIGNAL NAME	I/O A/S	FUNCTIONAL DESCRIPTION
47-52, 1-2	AD7-0	Address/Data Bus	I/O	ADDRESS inputs used in conjunction with ALE to select the internal register to be transmitted or received on the DATA input/outputs.
3	$\overline{MWE}$	Write Enable	I	When asserted will transmit data from the AD bus into internal registers.
4	$\overline{MRE}$	Read Enable	I	When asserted will transmit data from internal registers onto the AD bus.
5	$\overline{MCS}$	Chip Select	I	When asserted allows information to be read from or written to the AD bus.
6	ALE	Address Latch Enable	I	Address information is latched on the falling edge.
7,45	IOVDD	I/O Supply	S	+5 volt supply to all I/O except $\overline{WPCDATA}$, $\overline{RAWDATA}$, and analog pins.
8,46	IOVSS	I/O Ground	S	Dedicated ground to all I/O except $\overline{WPCDATA}$, $\overline{RAWDATA}$, and analog pins (designated "A").
9	CVDD	Analog Supply	S	Dedicated +5v for the Channel Control DAC circuitry.
10 (14)	FCDAC	Freq. Ctl. DAC	A	Frequency Control current DAC output.
11 (13)	IREF	Current Reference	A	External current reference used to set the compliance of IDAC. When not used, IREF should be connected to CVSS.
12 (15)	BCDAC	Boost Ctl. DAC	A	Boost Control voltage DAC output.
13 (11)	HCDAC	Hyst. Ctl. DAC	A	Hysteresis Control voltage DAC output.
14 (10)	LEVEL	Level	A	External voltage used to adjust the Hysteresis DAC offset. Should be tied to CVSS when not used.
15 (12)	VRG	Voltage Reference	A	External voltage reference used by the DAC circuits. Should be tied to CVSS when the Boost Control, Frequency Control, and Hysteresis Control DACs are not used.
16	CVSS	Analog Ground	S	Dedicated ground for the Channel Control DAC circuitry.
17 (19)	$\overline{AMD}$	Address Mark Detect	O	In soft sector, this signal indicates to the controller that after requesting an address mark search (AME), an address mark has been detected.
18 (21)	AME	Address Mark Enable	I	In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
19 (17)	ENCEN	Encode Enable	I	Asserted during write commands to enable the Encoder and associated write circuits.

TABLE 1-1. PIN DESCRIPTIONS

T-52-38

PIN NUMBER (IO MAP)	MNEUMONIC	SIGNAL NAME	I/O A/S	FUNCTIONAL DESCRIPTION
20 (22)	RGATE	Read Gate	I	In soft sector, RGATE responds to $\overline{AMD}$ to validate the acquisition sequence during reads. In hard sector, RGATE initiates the acquisition sequence w/o $\overline{AMD}$ qualification.
21 (18)	RDATA	Recovered Data	O	Recovered NRZ read data represents the decoded RLL raw read data with all phase and frequency noise removed.
22 (20)	RCLK	Regenerated Clock	O	Nominally at the NRZ data frequency, RCLK tracks the low frequency variations on $\overline{RAW-DATA}$ during reads, otherwise tracks the crystal reference.
23	AVSS	Main Analog Ground	S	Main ground dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase Detectors, etc.). This supply also supports the sensitive $\overline{WPCDATA}$ and $\overline{RAWDATA}$ I/O to prevent intermodulation with IOVDD /IOVSS.
24	AVDD	Main Analog Supply	S	Main +5v supply dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase detectors, etc.). This supply also supports the sensitive $\overline{WPCDATA}$ and $\overline{RAWDATA}$ I/O to prevent intermodulation with IOVDD /IOVSS.
25	DSVDD	Analog Supply	S	Dedicated +5v for the Data Synchronizer circuitry.
26 (28)	DSPMV	Data Synchronizer Pump	A	Charge pump to the data synchronizer PLL filter.
27 (30)	VCON	N-Channel Voltage Control	A	N-channel control voltage for the internal VCO and charge pump. This voltage is the filtered output of the charge pump.
28 (26)	LPF	Low Pass Filter	A	Controls low pass filter characteristics under zone control via the AD bus.
29	DSVSS	Analog Ground	S	Ground dedicated to the Data Synchronizer PLL.
30 (27)	WINCLK	Window Clock	O	This output, when enabled, represents the window clock at the Data Detector and may be used for window monitoring. Phase detector pump down output in test mode.
31 (33)	DELRD	Delayed Read Data	O	This output, when enabled, represents the latched RAWDATA at the Data Detector and may be used for window monitoring. Phase detector pump up output in test mode.

TABLE 1-1. PIN DESCRIPTIONS (Continued)

T-52-38

PIN NUMBER (IO MAP)	MNEUMONIC	SIGNAL NAME	I/O A/S	FUNCTIONAL DESCRIPTION
32 (37)	$\overline{\text{RAWDATA}}$	Raw Data	I	Disk drive raw read data from the read channel circuits. Leading edge timing, programmable polarity.
33 (31)	$\overline{\text{WPCDATA}}$	Write Precomp Data	O	Precompensated/Conditioned encoded write data sent to the write channel drivers. Leading edge timing, programmable polarity.
34	RVDD	Analog Supply	S	Dedicated +5v supply to Ramp Locked Loop circuits.
35	RVSS	Analog Ground	S	Dedicated ground to Ramp Locked Loop circuits.
36 (41)	WDATA	Write Data	I	NRZ write data from the controller. This data is conditioned and precompensated and sent out on $\overline{\text{WPCDATA}}$.
37 (32)	WCLK	Write Clock	I	Running at the NRZ data frequency. WCLK is provided from the the hard disk controller and serves as a reference clock for sampling the incoming WDATA.
38	FSVDD	Analog Supply	S	Dedicated +5v for the Frequency Synthesizer circuitry.
39	FSVSS	Analog Ground	S	Dedicated ground for the Frequency Synthesizer circuitry.
40 (42)	FSPMP	Frequency Synthesizer Pump	A	Charge pump for the frequency synthesizer PLL.
41 (36)	$\overline{\text{PORT1}}$	Port One	O	Open drain TTL output. This output is directly programmable via the micro-processor interface.
42 (40)	$\overline{\text{PORT0}}$	Port Zero	O	Open drain TTL output. This output is directly programmable via the micro-processor interface
43 (44*)	XTLI	Crystal Input	I	Input to active stage of integrated oscillator circuit, this frequency establishes the frequency synthesizer reference. The reference frequency is programmable via the AD bus.
44 (43*)	XTLO	Crystal Output	O	Output from active state of integrated oscillator circuit. This output is left open if an external source is desired.

* XTLO is an inversion of XTLI through the active stage. XTLO may not be driven and sensed on XTLI.

TABLE 1-1. PIN DESCRIPTIONS (Continued)

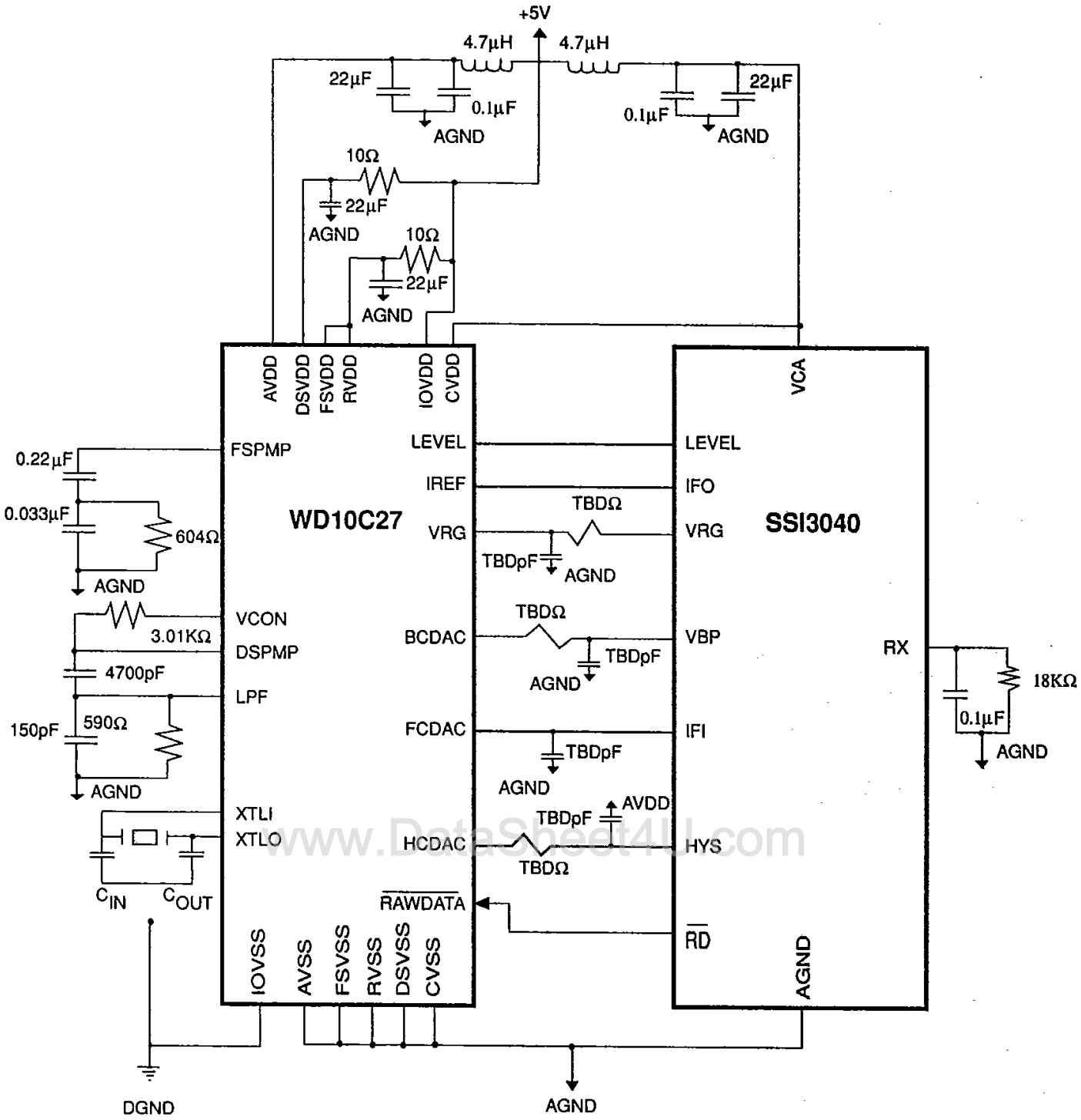


FIGURE 1-2. VARIABLE FREQUENCY CHANNEL SCHEMATIC

T-52-38

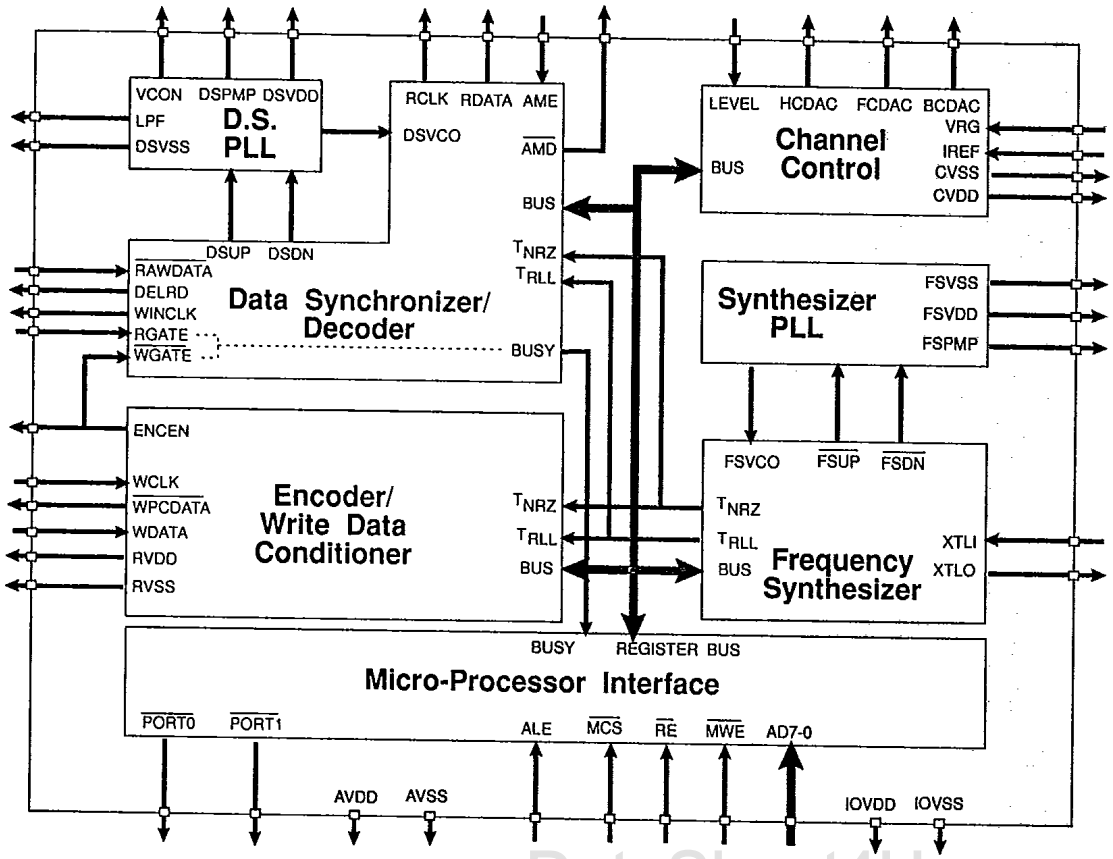


FIGURE 1-3. WD10C27 BLOCK DIAGRAM

13

T-52-38

2.0 MICROPROCESSOR INTERFACE

The WD10C27 provides an 8- bit interface to the microprocessor for programmability. The interface is compatible with the Intel multiplexed address/data bus architecture. Virtually all of the sub-systems within the WD10C27 are accessible via this interface. The processor interface is decoupled from the input pads during disk reads/writes to reduce the possibility of unwanted disturbances to sensitive signal processing. Ensuring that de-coupling is performed is accomplished by deactivating the $\overline{\text{BZOVR}}$ (busy override) bit in the Configuration register. In either configuration, registers should never be modified unless the Hard Disk Controller is not indicating a busy status.

2.1 REGISTER DESCRIPTION

Registers are accessed by placing the correct address word on the AD bus and latching this address on the falling edge of ALE. Subsequent reads/writes will access the addressed registers. Read/writes are performed when $\overline{\text{MCS}}$ is low and the $\overline{\text{MRE}}$/$\overline{\text{MWE}}$ lines are strobed.

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
11000000	TEST0	Test Modes Zero
11000001	TEST1	Test Modes One
11000010	TEST2	Test Modes Two
11000011	-	Unused
11000100	-	Unused
11000101	WSCOD	Window Synthesizer Clock Oscillator Divider
11000110	WSVCOD	Window Synthesizer VCO Divider
11000111	SAM	Window Synthesizer Amplifier
11001000	FCDAC	Frequency Control DAC
11001001	BCDAC	Boost Control DAC
11001010	HCDAC	Hysteresis Control DAC
11001011	TSTADD1	Test Address 1
11001100	TSTADD2	Test Address 2
11001101	-	Unused
11001110	FSCOD	Frequency Synthesizer Clock Oscillator Divider
11001111	FSVCOD	Frequency Synthesizer VCO Divider
11010000	WPC10	Write Precompensation One/Zero
11010001	WPC32	Write Precompensation Three/Two
11010010	WPC54	Write Precompensation Five/Four
11010011	WPC76	Write Precompensation Seven/Six
11010100	WPC98	Write Precompensation Nine/Eight
11010101	WPC1110	Write Precompensation Eleven/Ten
11010110	WPC1312	Write Precompensation Thirteen/Twelve
11010111	WPC1514	Write Precompensation Fifteen/Fourteen
11011000	WPC1716	Write Precompensation Seventeen/Sixteen
11011001	WPC1918	Write Precompensation Nineteen/Eighteen

TABLE 2-1. REGISTER ADDRESS MAP

T-52-38

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
11011010	WFC2021	Write Precompensation Twenty/Twenty-One
11011011	-	Unused
11011100	CFG0	Configuration Zero
11011101	CFG1	Configuration One
11011110	CFG2	Configuration Two
11011111	CFG3	Configuration Three

TABLE 2-1. REGISTER ADDRESS MAP (Continued)

All registers in the WD10C27 are read/write registers, with the exception of the Version ID Register. As previously stated, register access is limited to times when read and write operations are inactive. Register bits correspond to bits 7-0 of the AD bus such that the most significant maps to AD7, the least significant to AD0.

The internal read data bus utilizes a repeater which will latch this bus to the value of the register which was last read and for which the address is not "unused." All registers load asynchronously, thereby requiring no clocks to the device. Exceptions are the Frequency Synthesizer and the Window Shift Synthesizer Registers.

For the Frequency Synthesizer, reads/writes are performed to a master stage. The slave will not be updated however until synchronization circuitry has deemed it appropriate. This requires XTLI and Frequency Synthesizer VCO clocks.

The WSS will not allow loads to its registers when WSSEN is active.

At power up, the ARSTPDN bit in the Configuration register will be set (see section 6.0, "Power On Reset") and all other register bits placed in their specified initial state (see ARSTPDN and RSTPDN bits in section 2.1.1).

Following a soft reset/power down mode, a reset must be issued and all registers re-loaded.

There are eight main registers banks in the WD10C27:

- Configuration
- Frequency Synthesizer Dividers
- Window Synthesizer Control
- Skew Symmetric Precompensation
- Channel Control
- Test

2.1.1 Configuration Registers

The configuration (CFG) registers control the basic functions of the sub-circuits. These registers are eight bits wide.

CFG0 Register:

7:RLLEN	6:WPCEN	5:WSSEN	4:PWSEN	3:PWSI	2:PWS0	1:FBS1	0:FBS0

Bit 0: Frequency Band Select Zero. In conjunction with FBS1, FBS0 controls the Data Synchronizer, Frequency Synthesizer, and Ramp Lock Loop characteristics. See "Table 4-3 - Frequency Band Selection" for band selection.

Bit 1: Frequency Band Select One. See Bit 0 above.

Bit 2: Percentage Window Shift Zero. Used in conjunction with PWS1, PWS0 controls the direction of window shift when PWSEN is

T-52-38

active. (See "Table 4-3 - PWS Direction and Magnitude Selection").

Bit 3: Percentage Window Shift One. Used in conjunction with PWS0, PWS1 controls the magnitude of window shift when PWSEN is active. (See "Table 4-3 - PWS Direction and Magnitude Selection").

Bit 4: Percentage Window Shift Enable. When active, this bit enables the PWS system.

Bit 5: Window Shift Synthesis Enable. When active, this bit enables the WSS system. Must be inactive during loads to the WSS registers. (See section 4.3.4, "Window Shifting").

Bit 6: Write Precompensation Enable. When active, this bit enables the Pattern Dependent Precompensation system (RLLEN must be set to utilize fine resolution capabilities). (See section 5.2, "Pattern Dependent Precompensation").

Bit 7: Ramp Locked Loop Enable. This bit, when set in conjunction with WPCEN, activates the fine resolution capabilities of the write precompensation sub-circuit. (See section 5.2, "Pattern Dependent Precompensation").

CFG1 Register:

7:TSTEN	6:PORT1	5:PORT0	4:ARSTPDN	3:RSTPDN	2:$\overline{\text{BZOVR}}$	1:IOMAP	0:HIZEN

Bit 0: High Impedance Enable Test. When active, this bit will cause all output drivers and analog pins to be placed in a high impedance state. Exceptions include the micro-processor pins and XTLO. The micro-processor outputs may be tri-stated by asserting either RGATE or ENCEN with $\overline{\text{BZORV}}$ inactive.

Bit 1: Input/Output Mapping. When set, this bit will configure the WD10C27 input/output in accordance with the I/O map. IOMAP will be logically or'd with HIZEN to ensure all outputs and analog pins are tri-stated during I/O mapping. (See "Table 1-1- Pin Description").

Bit 2: $\overline{\text{Busy Override}}$. When active, this bit defeats the decoupling of the AD7-0 pads from the Micro-Processor Interface during disk read/write operations. Override mode is not recommended. Busy should be defeated during certain test modes. (See section 2.1.6, "Test Registers".)

Bit 3: Reset/Power Down. When active, this bit will reset/power down all functions and set all register bits to a logic zero for initialization and/or reduced power. All outputs will be held in their inactive states, and the crystal oscillator stopped. Exceptions include: FCDAC, HCDAC, and BCDAC registers and related functions, all of which are not effected by this bit; the COD and VCOD registers in both the Frequency and Window Shift Synthesizers, which are set to logic ones; and PORT0/1, which are not effected. The micro-processor interface is operable during rest/power down, and reset/power down remains active until the RSTPDN bit is written off.

Bit 4: All Reset/Power Down. This bit, when active, performs the same functions as the RSTPDN bit, with the addition that it will reset/power down the FCDAC, HCDAC and BCDAC registers and circuitry, as well as the RSTPDN bit itself. This bit will be set on power up. (See section 6.0, "Power On Reset").

Bit 5: Port Zero. This bit is used to set or reset the $\overline{\text{PORT0}}$ open drain output. Note that setting this bit forces $\overline{\text{PORT0}}$ low.

Bit 6: Port One. This bit is used to set or reset the $\overline{\text{PORT1}}$ open drain output. Note that setting this bit forces $\overline{\text{PORT1}}$ low.

Bit 7: Test Enable. When active, this bit enables the activation of test modes based on the

T-52-38

contents of TEST0-3 registers. When not active, this bit serves to lockout all test modes. (See section 2.1.6, "Test Registers").

CFG2 Register:

7:$\overline{\text{HFCEN}}$	6:VLOCK1	5:VLOCK0	4:WPCPOL	3:RAWPOL	2:WMEN	1:ERRPAT	0:DECERR

Bit 0: Decoder Error. When set, this bit represents an error detected in the $\overline{\text{RAWDATA}}$ bit stream into the Decoder. This bit should be cleared via a soft reset or an explicit write to this bit. (See section 4.4, "Decoder").

Bit 1: Error Pattern. When high, forces the Decoder to output NRZ ones when illegal 1,7 codes sequences are encountered on the $\overline{\text{RAWDATA}}$ input When low, NRZ zeros will be output for illegal sequences.

Bit 2: Window Monitor Enable. When set, this bit enables the DELRD and WINCLK outputs for window monitoring capabilities. (See section 4.3.3, "Window Monitoring").

Bit 3: Raw Data Polarity. When set, this bit selects active high leading edge polarity on the $\overline{\text{RAWDATA}}$ output. When not set, active low leading edge polarity is selected.

Bit 4: Write Precomp. Data Polarity. When set, this bit selects active high leading edge polarity on the $\overline{\text{WPCDATA}}$ output. When not set, active low leading edge polarity is selected.

Bit 5: Velocity Lock Zero. In conjunction with VCLOCK1, this bit set the velocity lock time for the acquisition sequence. (See section 4.2, "Acquisition Sequencer").

Bit 6: Velocity Lock One. See Velocity Lock Zero above.

Bit 7: $\overline{\text{High Frequency Clock Enable}}$. When active, this bit will divide the XTLI frequency by two at the HFCOD prior to the division which occurs at the FSCOD. (See section 3.0, "Frequency Synthesizer").

CFG3 Register:

7:VID3	6:VID2	5:VID1	4:VID0	3:Unused	2:Unused	1:$\overline{\text{ENODD}}$	0:$\overline{\text{AMODD}}$

The upper four bits of this register are read only.

Bit 0: $\overline{\text{AME Odd}}$. This bit controls relationship between the AME input and the NRZ code word boundary. With $\overline{\text{AMODD}}$ active, the code word is assumed to start on an odd bit in the NRZ synchronization byte (i.e. the first non-zero bit is bit 1,3,5,7); when inactive, the code word starts on an even bit (i.e., 0,2,4,6).

Bit 1: $\overline{\text{ENCEN Odd}}$. This bit controls relationship between the ENCEN input and the NRZ code word boundary. With $\overline{\text{ENODD}}$ active, the code word is assumed to start on an odd bit in the NRZ synchronization byte (i.e., the first non-zero bit is bit 1,3,5,7); when inactive, the code word starts on an even bit (i.e., 0,2,4,6).Unused. May be read/written. This bit reflects the code word boundary for GAP prior to address mark in ID fields, as well as the sync. byte following the synchronization field in DATA fields. this implies that the GAP data and synchronization byte must have the same code word odd/even boundary.

Bit 2: Unused. May be read/written.

Bit 3: Unused. May be read/written.

Bit 4: Version Identification Zero. VID3-0 are used to store a binary number which represents the version number of the device. The version number may be used to verify the cor-

rect iteration by the system. This bit is read only.

Bit 5: Version Identification One. See VID0 above.

Bit 6: Version Identification Two. See VID0 above.

Bit 7: Version Identification Three. See VID0 above.

2.1.2 Frequency Synthesizer Registers

The Frequency Synthesizer is controlled by the Clock Oscillator Divider (FSCOD) and the VCO Divider (FSVCOD) which are programmed via the contents of the FSCOD and FSVCOD registers. These registers hold eight bit unsigned integers. Programming is performed using the information given in section 3.3, "Programming the FS Dividers". Pre-scaling of the input to the FSCOD is performed based on the state of the $\overline{\text{HFCEN}}$ bit in the Configuration registers.

FSCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

FSVCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

2.1.3 Window Synthesizer Registers

The Window Synthesizer Clock Oscillator Divider (WS-COD), VCO Divider (WSVCOD), and Shift Amplifier are controlled by the WSCOD, WSVCOD, and SAM registers respectively. The WSCOD, WSVCOD, and SAM registers hold four and five bit unsigned integers. These registers should be programmed using the information given in section 4.3.4, "Window Shift Synthesis."

WSCOD Register: T-52-38

3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

WSVCOD Register:

4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

SAM Register:

3:SAM 8	2:SAM 4	1:SAM 2	0:SAM 1

2.1.4 Skew-Symmetric Precomp. Registers

There are twenty-two 4 bit wide nibbles which control the magnitude of precompensation for the Skew-Symmetric Precompensation system. Each nibble corresponds to a phase shift value in percent of the code bit window, T, for a given three bit sequence. The upper two bits are programmed to generate a coarse setting, while the lower two bits generate a fine setting. Eleven registers are used to hold the complete precompensation matrix, each register holding two consecutive nibbles. Note that WPC2021 has the nibbles reversed. See section 5.2, "Pattern Dependent Precompensation."

WPC0-10 Registers:

7:HiCoarse 1	6:HiCoarse 0	5:HiFine 1	4:HiFine 0	3:LoCoarse 1	2:LoCoarse 0	1:LoFine 1	0:LoFine 0

2.1.5 Channel Control Registers

The Channel Control registers consist of registers for controlling the three on board DACs. These registers and their associated functions will remain unaffected by the RSTPDN bit. Resetting and power reduction are accomplished by the ARSTPDN bit.

The DAC registers hold five bit unsigned integers representing the DAC conversion values for each of the three DACs. In addition, each register has a bit which can be used to disable the DAC for reduced power. The HCDAC has one additional bit for function control. See section 6.0, "Power On Reset" for details.

FCDAC & BCDAC Registers:

5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

HCDAC Registers:

$\overline{6:HCTL}$	5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

2.1.6 Test Registers

There are three registers which control test functions on the WD10C27 called TEST0-2. TSTEN must be active in the Configuration register before the test modes will be invoked. T-52-38

Each bit in the TEST registers represents a unique mode which has been created to ensure the quality of the product through design for testability. Some of the test modes provide synchronization of otherwise asynchronous circuits, while others provide visibility of internal logic structures to ensure high fault coverage.

See "Appendix B - Using the Test Modes" for a detailed explanation of these test features.

TEST0 Register:

7:PATREC	6:WPCDC	5:PORTST	4:CNTRS	3:FSSYNC	2:FSFDN	1:FSFUP	0:PDIO

Bit 0: Frequency and Window Shift Synthesizer Phase Detector I/O Test. This test takes the Frequency Synthesizer's phase detector pump up and pump down outputs to AD0-1 respectively, the Frequency Synthesizer's phase detector inputs (the FSVCOD and FSCOD outputs) to AD2-3 respectively, the Window Synthesizer's phase detector pump up and pump down outputs to AD4-5 respectively, and the Window Synthesizer's phase detector inputs (the WSVCOD and WSCOD outputs) to AD6-7 respectively during reads of the special address, TSTADD1. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 1: Frequency Synthesizer Frequency Up Test. This test forces a DC pump up error in the Frequency Synthesizer by gating off the FSCOD input to the phase detector. When both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 2: Frequency Synthesizer Frequency Down Test. This test forces a DC pump down error in the Frequency Synthesizer by gating off the FSVCOD input to the phase detector. When both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 3: Frequency Synthesizer Synchronization Test. This test takes the output of the HFCOD to the input of the FSVCOD as well as to the Frequency Synthesizer output for synchronous open loop testing. The ring oscillator is halted.

Bit 4: Frequency Synthesizer and Window Shift Synthesizer COD/VCOD Counts. This test takes each of the eight counts out of the Frequency Synthesizer's FS-COD to the AD bus during reads of the FSCOD, each of the eight counts out of the Frequency Synthesizer's FSVCOD to the AD bus during reads of the FSV-COD, each of the four counts of the Window Shift Synthesizer's WSCOD to AD0-3 during reads of the WSCOD, and each of the five counts of the Window Shift Synthesizer's WSVCOD to AD0-4 during reads of the WSVCOD. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 5: Power On Reset Test. When active, this bit will force the POR RC circuit to discharge, thereby activating POR and latching the ARSTPDN bit in the Configuration register (see ARSTPDN in section 2.1.1, "Configuration Registers"). This is the only way to reset the PORT0/1 bits in the Configuration register, excluding a normal POR issued upon power up. Note that PORTST will reset (via the ARSTPDN bit) both TSTEN and PORTST itself, leaving the WD10C27 in a post-POR state identical to that of a normal power up generated POR.

Bit 6: $\overline{\text{WPCDATA}}$ DC Test. When active, this bit causes the output on $\overline{\text{WPCDATA}}$ to remain inactive during disk write operations, resulting in DC erasure of the media. This bit will not affect the internal $\overline{\text{WPCDATA}}$ signal used during loopback testing.

T-52-38

Bit 7: Pattern Recognizer Test. When active, this bit allows special control of the precompensation circuits. Used in conjunction with a read from any of the WPC registers, the Pattern Recognizer's register selection will be dynamically directed to the AD4-0, with AD4 reflecting precompensation direction (high is late, low is early). Used in conjunction with writes to any of the WPC registers, the value written on AD4-0 will subsequently be used as a constant precompensation value, thus bypassing the Pattern Recognizer. Writes must be at least two T long, and must not be followed by a read unless XTLI is temporarily stopped.

TEST1 Register:

7:NLBTST	6:RLBTST	5:DLLTST	4:WSUSDTST	3:WSLSDTST	2:WSSYNCTST	1:WSFDNTST	0:WSFUPTST

Bit 0: Window Shift Synthesizer Frequency Up Test. This test forces a DC pump up error in the Window Shift Synthesizer by gating off the WSCOD input to the phase detector. When both WSFUPTST and WSFDNTST are set, neither test is activated.

Bit 1: Window Shift Synthesizer Frequency Down Test. This test forces a DC pump down error in the Window Shift Synthesizer by gating off the WSVCOD input to the phase detector. When both WSFUPTST and WSFDNTST are set, neither test is activated.

Bit 2: Window Shift Synthesizer Synchronization Test. This test takes the input of the WSCOD to the input of the WSVCOD for synchronous open loop testing.

Bit 3: Window Shift Synthesizer Lower SAM Decode Test. This test takes the Window Shift Synthesizer's lower eight of sixteen SAM decode values to the AD bus during reads of the SAM register. The decode is active low. Note that if both Upper and Lower SAM Decode tests are selected, neither will be excepted. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 4: Window Shift Synthesizer Upper SAM Decode Test. This test takes the Window Shift Synthesizer's upper eight of sixteen SAM decode values to AD bus during reads of the SAM register. The decode is active low. Note that if both Upper and Lower SAM Decode tests are selected, neither will be excepted. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 5: Delay Locked Loop Test. When set, this bit forces the DLL control voltages to the rails and bypasses the RLL, allowing low frequency functional testing without concern for DLL/RLL frequency limitations. $\overline{\text{RAWDATA}}$ and $\overline{\text{WPCDATA}}$ pulse forming are disabled.

Bit 6: RLL Loop Back Test. When set, this bit will internally connect the RDATA/RCLK outputs to the WDATA/WCLK inputs for simultaneous testing of the Data Synchronizer, Decoder, Encoder, and Write Data Conditioner functions by driving RLL $\overline{\text{RAWDATA}}$ and inspecting RLL $\overline{\text{WPCDATA}}$. When both NLBTST and RLBTST are set, neither test is activated and FSFUP/FSFDN and DSFUPTST /DSFDNTST drive the charge pump circuits directly, requiring no digital stimulation to test pump currents. Note that loopback tests do not use the polarity bit in the configuration register.

Bit 7: NRZ Loop Back Test. When set, this bit will internally connect the $\overline{\text{WPCDATA}}$ output to the $\overline{\text{RAWDATA}}$ input for simultaneous testing of the Encoder, Write Data Conditioner, Data Synchronizer, and Decoder functions by driving NRZ WDATA/WCLK and inspecting NRZ RDATA/RCLK. When both NLBTST and RLBTST are set, neither test is activated and FSFUP /FSFDN and DSFUPTST /DSFDNTST drive the charge pump circuits directly, requiring no digital stimulation to test pump currents. Note that loopback tests do not use the polarity bit in the configuration register.

T-52-38

TEST2 Register:

7:PDMXTST	6:DSPLKTST	5:DSVLKTST	4:XVCOTST	3:OLPTST	2:DSFDNTST	1:DSFUPTST	0:ACQTST

Bit 0: Acquisition Sequencer Test. This test takes the Acquisition Sequencer outputs DET6, DET9, HFDET, TIMEOUT, PLOCK, FRAMED, FIFORST, and DECERR to AD0-7 respectively during reads of the special address, TSTADD2. If the PWSD test has also been selected, neither test mode will be activated Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 1: Data Synchronizer Frequency Down Test. This test force a DC pump up error in the Data Synchronizer by gating off the data input to the phase detector. When both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 2: Data Synchronizer Frequency Up Test. This test force a DC pump down error in the Data Synchronizer by gating off the VCO input to the phase detector. When both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 3: Open Loop Test. This test disconnects the Data Synchronizer's charge pump output, DSPMP, from the VCON pin to allow for testing of the charge pump and VCO characteristics. It also disables the voltage clamps on both the Data Synchronizer's

and Frequency Synthesizer's VCOs. The ring oscillators are not affected.

Bit 4: External VCO Enable Test. When active, this bit allows for an external VCO signal to be applied on the LPF pin. The VCO signal should be at TTL levels and at a frequency which equals three times the NRZ data rate. The ring oscillator is halted.

Bit 5: Data Synchronizer Velocity Lock Test. This test will force the Data Synchronizer to remain in Velocity Lock mode by stalling the Acquisition Sequencer prior to entering Phase Lock.

Bit 6: Data Synchronizer Phase Lock Test. This test will force the Acquisition Sequencer and Data Synchronizer charge pump and filter into phase lock configuration to allow for testing of the PLL tracking characteristics without the need to stimulate the Acquisition Sequencer or Address Mark Detector. VCO clocks will still be required to synchronize phase lock to the digital circuits.

T-52-38

Bit 7: Phase Detection Multiplex Enable Test. When active, this bit directs the phase detector frequency up/down error signals to the DELRD/WINCLK outputs respectively. The WMEN bit must be set in the configuration register. (See section 2.1.1, "Configuration Registers").

3.0 FREQUENCY SYNTHESIZER

The frequency synthesizer output serves as the "crystal" reference for several sub-circuits: the Delay Locked Loop and Ramp Locked Loop circuits for scaling with data rate; the Data Synchronizer for reference when the PLL is not locked to RAWDATA; the Address Mark Detector and Acquisition Sequencer; and the Write Data Conditioner/Encoder for processing of sensitive write signals.

The WD10C27 utilizes a dual divider frequency synthesizer architecture to generate frequencies at an extremely high resolution. Given this, and the flexibility of the programmable crystal input frequency, highly efficient use of zones may be accomplished.

3.1 PROGRAMMABLE FS CRYSTAL REFERENCE (XTLI)

The crystal input is designed to accept input frequencies up to 16 MHz when using the active stage, or up to 40 MHz when an external source is provided. If an external source is used, XTLO is left open. The crystal input frequency should never exceed 20 MHz unless $\overline{\text{HFCEN}}$ is active in the Configuration register.

T-52-38

3.2 FS DIVIDER OPERATION

The digital portion of the synthesizer consists of a High Frequency Clock Oscillator Divider, a Clock Oscillator Divider to divide the input reference (XTLI), and a VCO Divider to divide the VCO output. The crystal input frequency is divided down based on the contents of the $\overline{\text{HFCEN}}$ bit in the Configuration registers, and the contents of the FSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the FSVCOD register, to match the frequency output of the FSCOD output.

The PLL architecture is almost identical to that of the Data Synchronizer. Phase-frequency locked

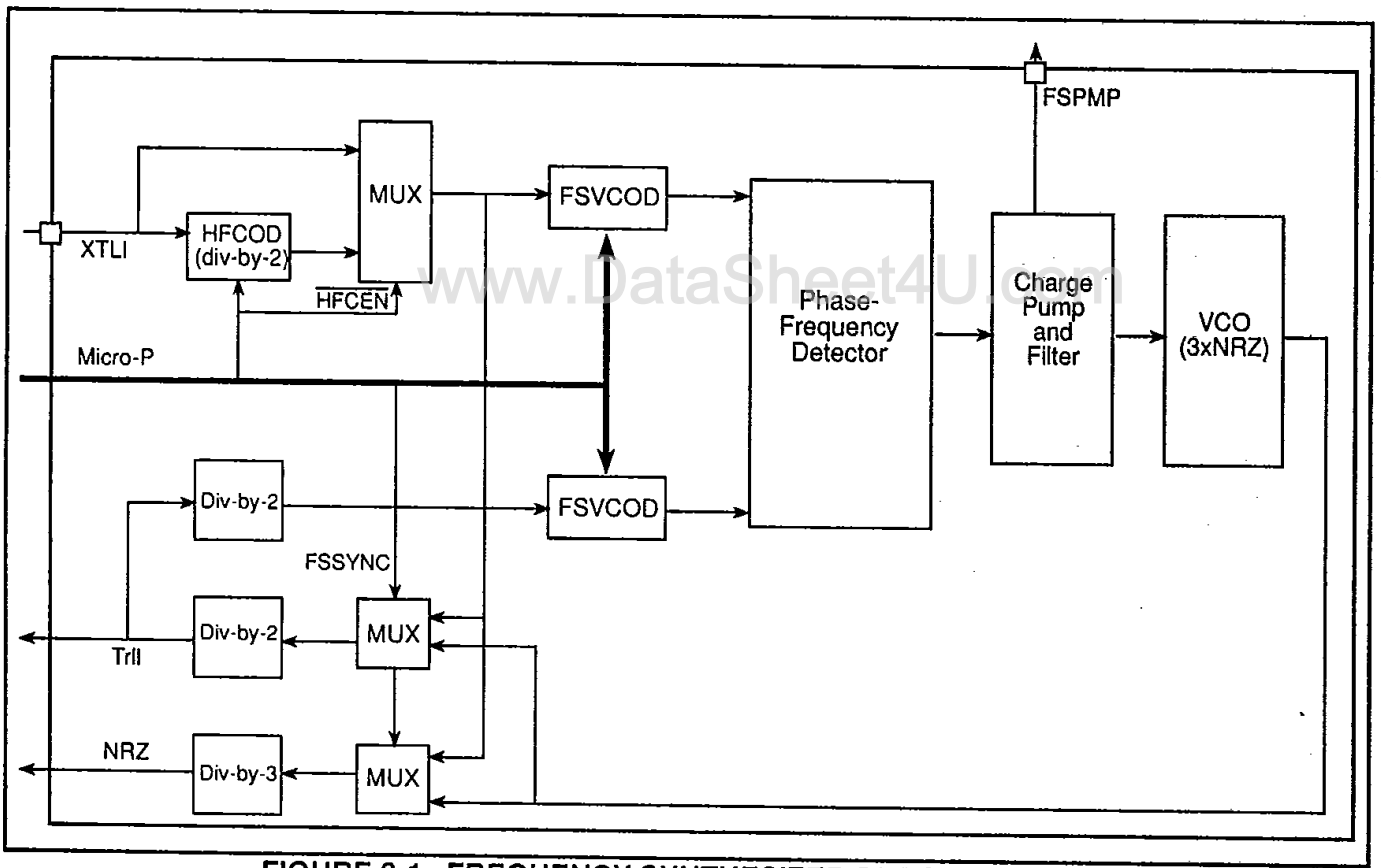


FIGURE 3-1. FREQUENCY SYNTHESIZER BLOCK DIAGRAM

loop synchronization is performed on the output of the FSCOD. The Charge Pump drives a VCO which utilizes a ring oscillator architecture at three times the NRZ data rate. The output of the charge pump is filtered at a very low bandwidth for high jitter rejection, while the VCO gain is modified based on the current zonal frequency to establish loop gain constancy.At the output of the Frequency Synthesizer, the VCO is operating at three times the NRZ data frequency. The NRZ and channel rate frequencies are ultimately steered to the other sub-circuits as their "crystal references". The coded rate, channel rate, or window clock, is herein referred to as T_{RLL}. The period, T, of the window clock defines the width of the phase and data detection windows. The frequency of T_{RLL} defined with respect to the NRZ data rate (F_{NRZ}), is therefore given by

EQ. 1.0

$$Frll = \frac{3 \times Fnrz}{2}$$

where

EQ. 2.0

$$Trll = \frac{1}{Frll}$$

and

EQ. 3.0

$$7.5\ MHz \leq Fnrz \leq 27\ MHz$$

Finally, the 3X NRZ VCO output is divided by two and used as the input to the FSVCOD.

3.3 PROGRAMMING THE FS DIVIDERS

Programming the Frequency Synthesizer is accomplished by programming the FSCOD and FSVCOD registers such that the equality

EQ 4.0

$$\frac{3/4 \times Fnrz}{FSVCOD + 1} = \frac{Fhfcod}{FSCOD + 1} = Fspll$$

is satisfied, where Ffspll is the Frequency Synthesizer PLL operating frequency range and is given by

T-52-38

EQ. 5.0

$$95\ KHz \leq Ffspll \leq 105\ KHz$$

Rearranging EQ. 4.0,

EQ. 6.0

$$Fnrz = \frac{(4)}{(3)} \times Fhfcod \times \frac{(FSVCOD + 1)}{(FSCOD + 1)}$$

it can easily be seen that the NRZ frequency is simply a ratio of the crystal reference frequency which may be pre-scaled in the HFCOD.

Because each side of EQ. 4.0 must not only satisfy the equality, but satisfy EQ. 5.0, selection of VCOD value can now be determined based on the NRZ data rate and the preferred crystal frequency. Note that to program a value of N, the registers must be loaded with a value of N-1.

The FSCOD and FSVCOD registers are eight bits, allowing for division up to 256 in both dividers. In addition, if the $\overline{HFCEN}$ (high frequency clock enable) bit in the Configuration registers is active, the XTLI frequency is divided by two in the HFCOD prior to entering the FSCOD. This results in the FSCOD values effectively being doubled, allowing for division of the input from 2 up to 512 in multiples of 2. $\overline{HFCEN}$ will be active on power up.

Minimum and maximum divider values are determined from EQ. 3.0 through EQ. 5.0 as follows. For the legal range of FSVCOD values, given the NRZ frequency range and the FS PLL range, we have

EQ. 7.0

$$\frac{3/4 \times Fnrz\ (min)}{Fpll\ (max)} \leq FSVCOD + 1 \leq \frac{3/4 \times Fnrz\ (max)}{Fpll\ (min)}$$

EQ. 7.1

$$\frac{5.625\ MHz}{105\ KHz} \leq FSVCOD + 1 \leq \frac{20.25\ MHz}{95\ KHz}$$

EQ. 7.2

$$53 \leq FSVCOD \leq 212$$

For the FSCOD values, the legal maximum is constrained by the maximum frequency of the crystal reference. This reference may never exceed 40 MHz Since the $\overline{HFCEN}$ bit must be set for crystal reference frequencies greater than 20 MHz, the output of the HFCOD will never exceed 20 MHz.

T-52-38

Therefore, we have

EQ. 8.0

$$\frac{Fhfcod\ (min)}{Fpll\ (max)} \leq FSCOD + 1 \leq \frac{Fhfcod\ (max)}{Fpll\ (min)}$$

EQ. 8.1

$$\frac{0\ MHz}{105\ KHz} \leq FSCOD + 1 \leq \frac{20\ MHz}{95\ KHz}$$

EQ. 9.0

$$0 \leq FSCOD \leq 209$$

T-52-38

4.1 ADDRESS MARK DETECTOR

The Acquisition Sequencer is initiated off of $\overline{AMD}$ in soft sector formats. When AME is asserted and ENCEN is not active, pulse formed raw read data is synchronized to T_{RLL} and sent to the Address Mark Detection circuitry. The previously written address mark (AM) is matched, $\overline{AMD}$ is asserted and the AM search is complete. At this time, the hard disk controller should respond by asserting RGATE and de-asserting AME.

4.1.1 Address Mark Detection Rules

Address mark detection is assumed to be successful only when specific pattern sequences have been detected on the synchronized raw read data. The patterns must be found in sequence according to the following rules, and only following assertion of AME. (See "Table 4-1, Address Mark Detect Sequences"):

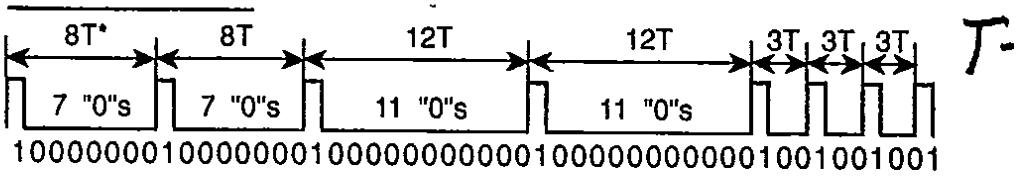
1. Detect a "1" followed by at least six consecutive "0"s (i.e., 1...00000...)
2. Detect a "1" followed by at least nine consecutive "0"s (i.e., 1...000000000...) no more than 3 NRZ byte times following detection of sequence 1.
3. Detect a "1" followed by at least three consecutive high frequency (HF) intervals (i.e., ...1001001001) no more than 3NRZ byte times following detection of sequence 2.

Address marks are formatted with several unique qualities which are important in ensuring high probability of correct detection. The AM used by the WD10C27 is formatted as 8T8T12T12T3T3T3T. The leading "1" in the AM is always formatted preceding the first 8T interval in order to guarantee the interval width.

The 8T8T part of the AM is a sequence that, although not in violation of the d,k code constraints, is not possible by virtue of the encode rules (see section 5.1, "Encoder"). Detection of at least six "0"s allows for asynchronisms between the raw read data and T_{RLL}. As six "0"s may be detected in either 8T interval, redundancy is ensured.

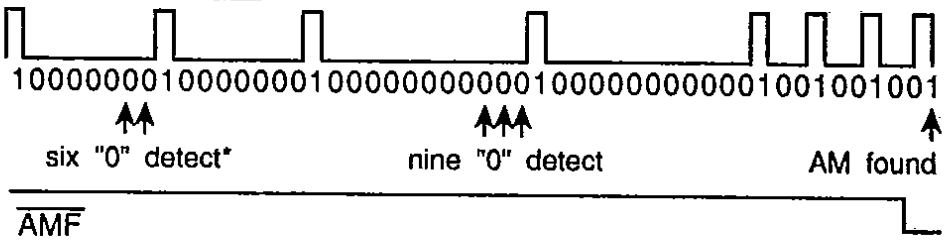
The selection of the 12T12T portion of the AM is an illegal run length and in violation of the k constraint in the 1,7 code. Once again two intervals ensure redundancy. In addition, the second 12T interval will significantly reduce the effects of intersymbol interference which, given only on 12T interval, would tend to shorten the interval.

Address Mark

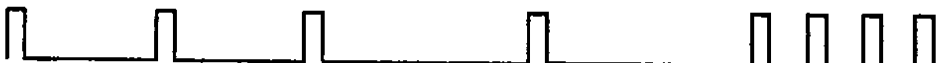


T-

Detect Case 1



Detect Case 2



4.1.2 Formatting to Reduce False AM Detection

When AME is asserted during disk write operations, the AM is "jammed" into the serial encoded bit stream. This is necessary to ensure that the AM placement is exact and does not depend upon synchronization to a previous interval. Jamming of the AM therefore will create an arbitrary run length between the user programmed gap and the AM. This may result in a violation of the d constraints of the 1,7 code, such that a 1T interval is created.

In the event that a 1T interval is created at the leading edge of the AM, the second of the two "1"s will be suppressed, and the AM sent to the write electronics will be

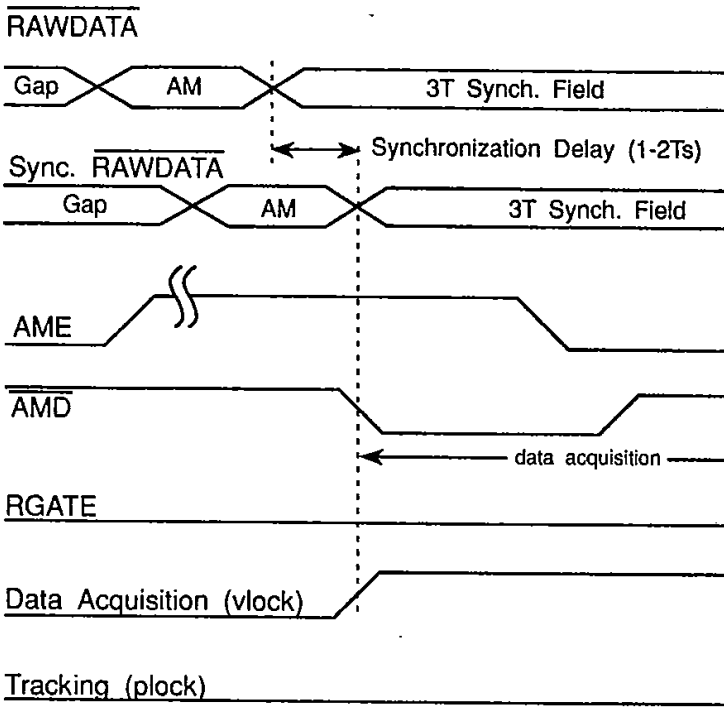
9T8T12T12T3T3T3T.

long enough that
occur within the re
accomplished by
less than 3 NRZ b

In summary, form
bytes of 5T gap pr
the susceptibility t
be done with a re
tern.

4.2 ACQUISITI

The WD10C27 su
formats. The acc
when either RGAT
than the Address
acquisition off of
tinctions between



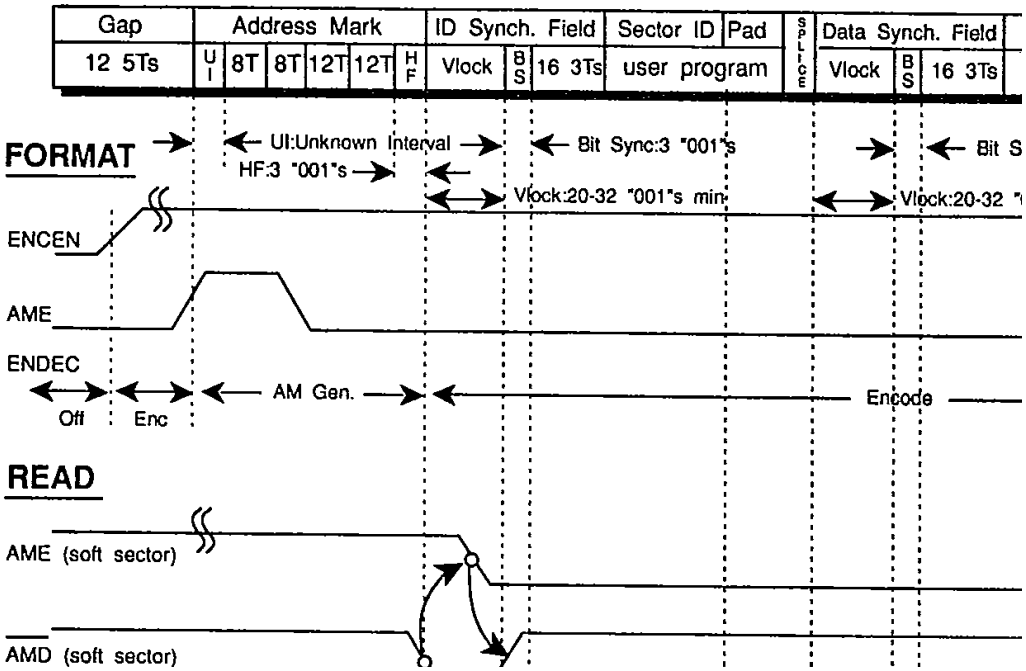
VLOCK1	VLOCK0	Vlock Time Tvlk
0	0	60 T (4 NRZ Bytes)
0	1	72T (5 NRZ Bytes)
1	0	84T (6 NRZ Bytes)
1	1	96T (7 NRZ Bytes)

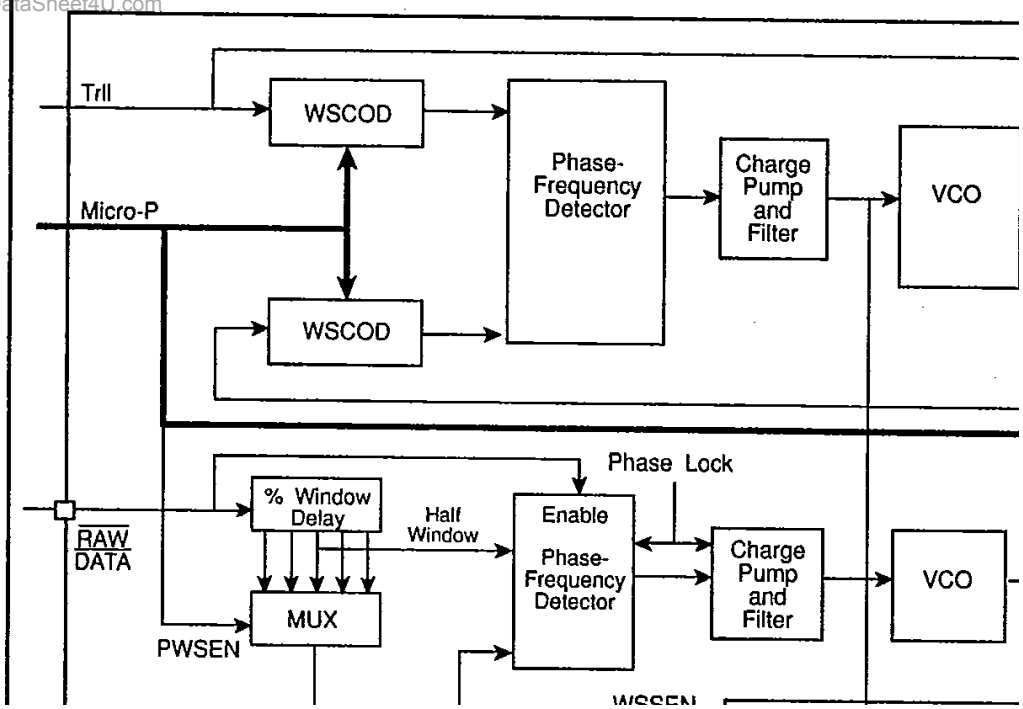
TABLE 4-2. VELOCITY LOCK TIME SELECTION

4.2.3 RCLK Source

In the WD10C27 architecture, it is assumed that the hard disk controller will be using RCLK during write commands as its NRZ reference clock,

WCLK. To accom
write times (i.e., F
assertion), RCLK
reference without
sociated with a
Synchronizer's ref
onset and termina
cy Synthesizer
divided down to th
the RCLK output
tion, RCLK will b
clock cycles to pe
vide a glitch-free F





The VCO ring oscillator architecture is fully integrated, allowing for precise compensation of temperature, voltage, processing, and aging effects. The VCO operates at three times the NRZ data rate (two times the channel rate) and is divided down to the NRZ data rate at the RCLK output.

The WD10C27 optimizes loop gain and bandwidth using fre-quency information obtained via the processor interface. PLL characteristics are modified at pre-determined frequency bands, selectable via the frequency band selection bits FBS0 and FBS1 in the CFG register.

4.3.2 Window Generation

The Data Synchronizer utilizes Western Digitals proven DLL technology to generate precision

4.3.3 Window Mo

Window monitoring
spection of the DE
Window centering
rising edges are ce
of WINCLK. With th
multiplex test) bit ac
outputs will reflect t
out of the phase de
frequency up errors,
frequency down err
signals may be us
amplifier envelope d
ing.

Window monitoring
WMEN bit in the c
WMEN is not set, t
puts will be held low

data rate. Both methods may be used simultaneously.

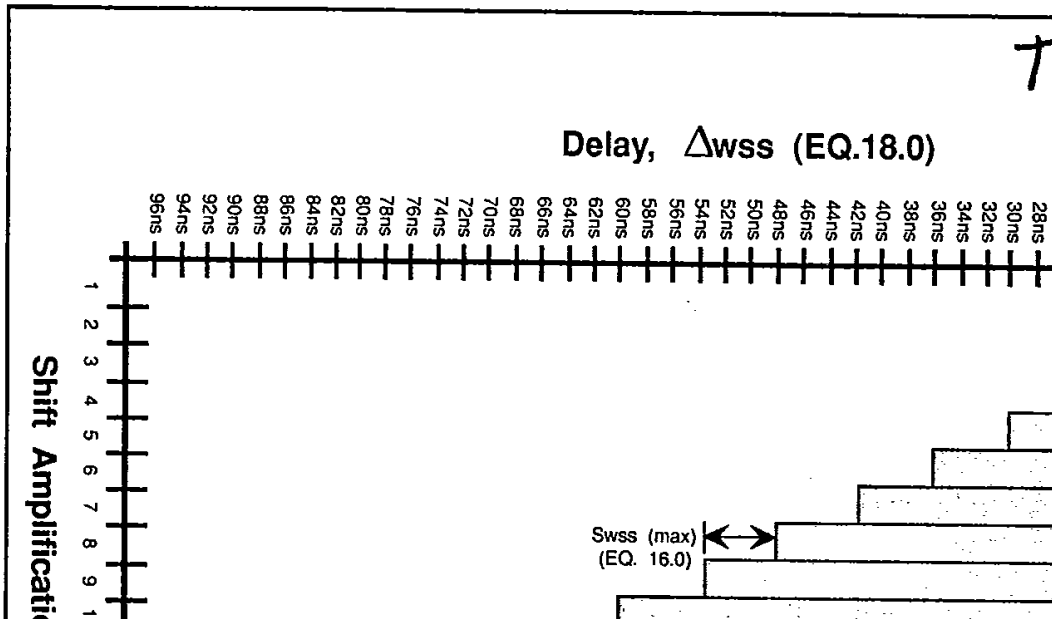
Window Shift Synthesizer

The Window Shift Synthesis (WSS) system employed on the WD10C27 uses information programmed through the micro-processor interface to synthesize virtually any value of window shift which may be desired. Synthesis is achieved in a manner similar to the Frequency Synthesizer.

The WSS, using T_{RLL} as its reference, synthesizes the user selected delay value in a servo controlled delay element. Delay elements may be

programmed esser
range of 2ns to 6ns
are chained back
delay line which se
mable amplification
the servo delay ele
of 2ns to 96ns is
delayed raw data
leading edge of the

WSS is enabled by
the CFG register.



WSS Divider/Shift Amp. Operation

The digital portion of the synthesizer consists of a Clock Oscillator Divider to divide the input reference (T_{RLL}), and a VCO Divider to divide the VCO output. The T_{RLL} input frequency is divided down based on the contents of the WSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the WSVCOD register, to match the frequency output of the WSCOD.

The VCO design utilizes 4.5 double inverting stages in a ring oscillator architecture. When phase-frequency lock is achieved on the output of the WSCOD, the delay through each VCO stage will be precisely controlled. These stages are duplicated in the Shift Amplifier to generate a precision delay line. The delay may be amplified

EQ. 12.0

18.52 MHz

Note that to prog
a value of N-1 mu

The WSCOD and
bits respectively.
values are deterr
12.0 as follows.

For the legal rang
WSS VCO range
have

EQ 13.0

$$\frac{Fwsvco\ (min)}{Fwspll\ (max)} \leq W$$

EQ. 15.0

$$Fwsvco = \frac{1000}{9 \times \delta wss}$$

Combining EQ. 2.0, EQ. 4.0, and EQ. 15.0, we derive the relationship

EQ. 16.0

$$\delta wss = \left(\frac{Trll}{9}\right)\left(\frac{WSCOD + 1}{WSVCOD + 1}\right)$$

Since the SAM may amplify δwss from one to sixteen times, the legal SAM values are bounded by

EQ. 17.0

$$1 \leq SAM + 1 \leq 16$$

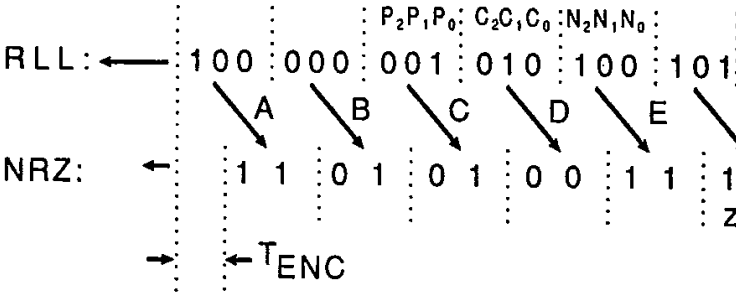
Percentage Windo

The Percentage W
allows for window s
window, T. This s
simple to use and
Window shifting car
12.5% of T using thi

PWS is enabled by
the CFG register, v
are selected by p
PWS1 bits in the CF

PWS1	PWS0
0	0
0	1

Code Word Relationship



Decode Table Entry

	$P_1 P_0 C_2 C_1 C_0 N_2 N_1 \rightarrow Z_1 Z_0$
A) Case 9	XX10000 → 11
B) Case 1	0000000 → 01
C) Case 2	0000101 → 01

Case No.	1,7 RLL Code Word			NRZ Data Word
	Previous $P_1 P_0$	Current $C_2C_1C_0$	Next $N_2 N_1$	NRZ $Z_1 Z_0$
1	00	000	00	01
2	00	000	01	01
3	00	000	10	01
4	00	001	00	01
5	00	001	01	01
6	00	010	00	11
7	00	010	01	10
8	00	010	10	10
9	00	100	00	11
10	00	100	01	11
11	00	100	10	11

If the Decoder se
decode word, the N
either a "00" or "11
ERRPAT bit in the (
DECERR bit will be
error has occurred.
legal RLL seque
8T8T...8T, 8T7T, 3T
these sequences ar
encode rules. Since
the decode, these
states in the decode

The NRZ data word
the channel rate
Synchronizer. The I
the Data Synchroniz
at the RDATA outp
edges on RCLK.

appropriate DAC registers and activating the DACEN bit.

4.5.1 Frequency Control (FCDAC)

The Frequency Control DAC, FCDAC, has been specifically designed to allow for bandwidth optimization of the read channel. In a typical variable frequency application, selection of the channel bandwidth is made based on signal-to-noise ratio and recording frequency considerations.

FCDAC is a current DAC whose compliance is set by an external current reference applied at the IREF input. FCDAC is enabled and programmed via the FCDAC register described in section 2.1.5, "Channel Control Registers."

progression. When
SSI3040, this state
will assume a nomi

Note that after ARS
zero count but will
without modifying
boost configuration

4.5.3 Hysteresis

Hysteresis Contro
specifically designe
controlled threshol
DAC whose compli
ratio of the voltage
LEVEL voltage and
tional to the VRG

5.0 WRITE CHANNEL

The Write Data Conditioner processes the NRZ write data (WDATA) from the hard disk controller. Encoded data is resynchronized from the encoder off of the crystal reference from the Frequency Synthesizer (T_{RLL}) to remove any sources of timing jitter. The re-conditioned write data is sent out to the write channel electronics on the $\overline{WPCDATA}$ pin, where high-to-low transitions represent the accurate crystal controlled timing edges. When $\overline{WGATE}$ is inactive, the Write Data Conditioner sleeps to conserve power. $\overline{WPCDATA}$ is held high during this time.

5.1 ENCODER

Upon assertion of ENCEN and after some synchronization delay, WDATA is shifted into a FIFO on the rising edges of WCLK. The output of

$\overline{ENODD}$ is inactive (such that the NRZ da N_0N_7, etc., are enco transition on WDATA 0.

Case No.	NRZ Data Wor	
	Current C_1C_0	
1	00	
2	00	
3	00	
4	00	
5	00	

Since ENCEN is asserted prior to gap during formats, and prior to data fields during writes, the odd/even framing requirement must be consistent. This implies that the synchronization byte usually written just after the synchronization field and the gap data must both have either odd or even framing.

5.1.2 Framing in Soft Sector Formats

Framing must be re-established following the insertion of address marks via AME. While $\overline{\text{ENODD}}$ is used to establish framing following assertion of ENCEN, $\overline{\text{AMODD}}$ is similarly used following assertion of AME.

Following the address mark generation, WDATA is once again encoded and shifted out to $\overline{\text{WRCDATA}}$. Because WDATA must be ODD follow

Framing following
have to be the
synchronization by
data fields, framin
This is due to the
sistent between
synchronization by
consistent followin
fields) or ENCEN (

5.2 PATTERN D
PRECOMPI

Write precompens
plementation of a
metric precompens
matrix is defined
diagonal while b

One exception to the skew-symmetric rule is the inclusion of the 2T/2T pulse period pair. This pair has a matrix entry to account for write induced peak shift on 2T runs. Also note that although entries exist for 7T8T and 8T7T pulse period pairs, these are pairs which cannot be realized by virtue of the encode rules (8T8T is another such pair, although it has no entry due to its position along the diagonal). These entries may however be utilized at the gap-to-Address Mark transition.

The Pattern Recognizer has been designed to recognize two special cases of run length violations which can occur in soft sector applications during formats: pulse periods greater than 8T (i.e. 12T) generated in the Address Mark; pulse periods less than 2T or greater than 8T (i.e. 1T or 9T) generated at the gap-to-Address Mark transit well as $\overline{\text{WPCDATA}}$

Coarse 1	**Coarse 0**
0	0
0	0
0	0
0	0
0	1
0	1
0	1
0	1
1	0

Write precompensation is enabled through the micro-processor interface by activating the WPCEN bit in the CFG register. Precompensation takes place by means of a pattern detector which determines the distance of the previous and next bits to the current bit. The pulse period pair which has been detected addresses the WPC registers, keeping track of the order of the pulse periods, or sign. This information is passed to the Write Precompensation circuits for appropriate phase shifting of the $\overline{\text{WPCDATA}}$ output.

The WPC registers have two bits for coarse precompensation selection and two bits for fine resolution, both based on a percentage of the code bit window, T. The value of the coarse setting will be summed with the value of the fine

setting to produce
value, as depicted i
Selection".

RLLEN must be se
to utilize the fine re
is disabled, the Ra
performs fine resol
powered down and
the WPC registers
needs time to acqui
ence, this bit shoul
of a write operatio
specifications of the

6.0 POWER ON RESET

The Power On Reset (POR) circuit in the WD10C27 has been designed to guarantee configuration upon activation of the system +5 volt power supply. POR provides a reset pulse derived from a time-lag circuit which slaves off of the power supply ramp.

POR is used to set the ARSTPDN bit in the Configuration register. (See section 2.1.1, "Configuration Registers"). In this way, the WD10C27 will be guaranteed to po
with all registers
the PORT0/1 bit
which are otherwi

ARSTPDN must
configured befor
mence.

7.0 PERFORMANCE SPECIFICATIONS

7.1 MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Contir
is not intended and should be limited to those conditions specified in the

PARAMETER	RATING	UNIT
V_{DD} with respect to V_{SS}	+7	V
Voltage on any pin with respect to V_{SS} (ground)	-0.5 to +7	V
Ambient Operating Temperature (T_A)	0 to 70	°C

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): $\overline{AMD}$, RDATA, RCLK					
V_{OH}	Output High Voltage	2.4			V
V_{OL}	Output Low Voltage			0.4	V
I_{OLK}	Output Leakage Current	-10		+10	µA
T_{RF}	Output Rise Time			2.5	nS
T_{FL}	Output Fall Time			2.1	nS
PIN(S): WINCLK, DELRD, $\overline{WPCDATA}$					
V_{OH}	Output High Voltage	2.4			V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): AD7-0, $\overline{MWE}$, $\overline{MRE}$, $\overline{MCS}$, ALE, AME, ENCEN, RGATE, LPF (te WCLK					
V_{IH}	Input High Voltage	2.0	1.4		V
V_{IL}	Input Low Voltage		1.4	0.8	V
I_{ILK}	Input Leakage Current	-10		+10	µA

TABLE 7-4. INPUT RECEIVERS DC SPECIFICA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): DSPMP, VCON					
V_{HFCA}	VCO High Freq. Clamp Act. Voltage †	TBD		TBD	V
V_{HFCD}	VCO High Freq. Clamp De-act. Voltage †	TBD		TBD	V
V_{LFC}	VCO Low Frequency Clamp Voltage ‡	TBD		TBD	V
I_{HFC}	VCO High Frequency Clamp Current †	TBD		TBD	mA
I_{LFC}	VCO Low Frequency Clamp Current ‡	TBD		TBD	mA

TABLE 7-6. DATA SYNCHRONIZER INTERNAL VCO DC S

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): VRG, LEVEL, HCDAC					
V_{RG}	External Voltage Reference	2.2			V
V_{RC}†	Internal Level Shift Accuracy				mV
V_{LEV}	LEVEL Input Voltage - V_{RC}	0	+0.7		V
V_{OFFSET}	Output Offset Voltage (code zero)		15		mV mV
LSB	Resolution (5-bit)		V_{LEV} /31		V
GAIN	Gain Accuracy				%
INL	Integral Non-Linearity				LSB
DNL	Differential Non-Linearity				LSB

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): IREF, VRG, FCDAC					
V_{RG}	External Voltage Reference	2.2		2.45	V
I_{REF}	External Current Reference	45	60	96	µA
V_{IREF}	IREF Voltage Accuracy			±30	mV
LSB	Resolution (5-bit)		IREF /93		µA
$I_{INITIAL}$	Zero Code Current	7.5	8	8.5	LSB
GAIN	Gain Accuracy			3.5	%
INL	Integral Non-Linearity			±0.5	LSB
DNL	Differential Non-Linearity			±0.5	LSB
C_{EXT}†	FCDAC Filter Capacitance			TBD	pF

7.3 AC ELECTRICAL AND TIMING CHARACTERISTICS

The following specifications are over T_A = 0°C to 70°C, T_J = 0°C to 90°C, V (max of 100mV p-p ripple), V_{OH} = 2.0V, V_{OL} = 0.8V, V_{IL} = 0.4V, V_{IH} = 2.4 otherwise specified. When indicated (*), limits represent characterized valu

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
I_{DDA}	Active Power Supply Current		20 50	30 75	mA mA
I_{DDLP1}	Power Down Supply Current		15	TBD	mA
I_{DDLP2}	All Power Down Supply Current		13	TBD	mA
T_{RDY}*	Time from valid configuration to full operating capability (e.g. lockup of PLLs)			3	ms

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$					
t_{SWC}	Setup of ENCEN and WDATA to WCLK Rising	5			ns
t_{HWC}	Hold of ENCEN and WDATA from WCLK Rising	5			ns
f_{NRZ}	WCLK Frequency ($1/T_{NRZ}$)	7.5		27	MHz
t_{ENCON1}	ENCEN Rising to Encode On	t_{SWC}		t_{SWC} +1	T_{NRZ}
t_{ENCOFF}	ENCEN Falling to $\overline{\text{WPCDATA}}$ Off	t_{SWC}		tSWC +2	TNRZ
t_{ENC}	WDATA to $\overline{\text{WPCDATA}}$ Encode Delay	15		22	T_{NRZ}

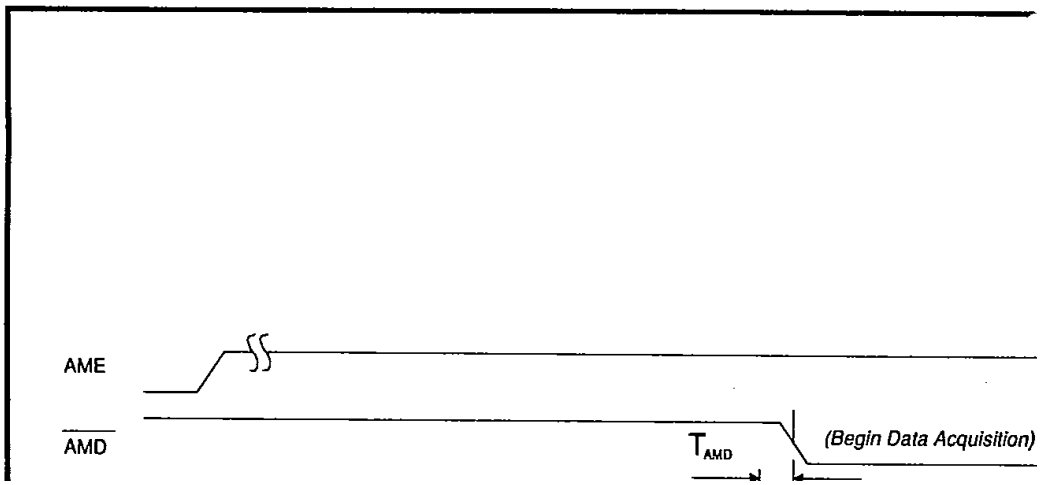
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$					
t_{SWC}	Setup of AME to WCLK Rising	5			ns
t_{HWC}	Hold of AME from WCLK Rising	5			ns
t_{AME}	AME Pulse Width	1			T_{NRZ}
t_{ENCON2}	AME Rising to Encode On			36	T_{NRZ}
t_{DAM}	AME to AM on $\overline{\text{WPCDATA}}$ Delay	10		13	T_{NRZ}
t_{SAMG}	Setup of AME to End of Gap on WDATA	0			ns
t_{AM}	Address Mark Length			50	T_{NRZ}

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	
PIN(S): $\overline{\text{WPCDATA}}$						
LSB	Resolution		T_{RLL} /64			for
INL	Integral Non-Linearity			±0.5	LSB	
DNL	Differential Non-Linearity			±0.5	LSB	
t_{WPC}	$\overline{\text{WPCDATA}}$ Pulse Width	11/16		17/16+x	T_{RLL}	x is T_{RL}
t_{WTJ}‡	$\overline{\text{WPCDATA}}$ Timing Jitter			100	ps	one
t_{WTJ}‡	$\overline{\text{WPCDATA}}$ Timing Jitter		TBD		ps	one 10(ripp
			TBD		ps	one

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UN
PIN(S): $\overline{\text{RAWDATA}}$, RDATA, RCLK					
t_{DWL}	Data Detection Window Loss			+250	p
t_{DWC}	Data Detection Window Centering Error			± 1	%
t_{PWC}	Phase Detection Window Centering Error			± 2	%

TABLE 7-15. PHASE & DATA DETECTION WINDOW TI

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UN
PIN(S): AMF, $\overline{\text{AMD}}$, $\overline{\text{RAWDATA}}$, RDATA, RCLK					

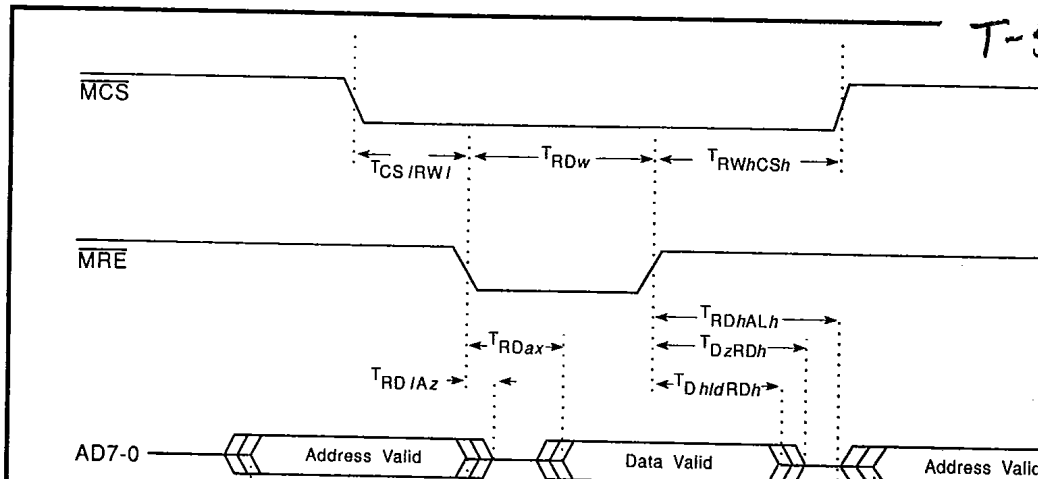


T-3

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CO
PIN(S): DSPMP, LPF, VCON						
K_{DO}†	Phase Detector Gain, BAND0	TBD	TBD	TBD	µA/rad	Phase Lo
K_{D1}†	Phase Detector Gain, BAND1	TBD		TBD	µA/rad	Phase Lo
K_{D2}†	Phase Detector Gain, BAND2	TBD		TBD	µA/rad	Phase Lo
K_{D3}†	Phase Detector Gain, BAND3	TBD		TBD	µA/rad	Phase Lo
K_{OO}†	VCO Gain, BAND0	TBD		TBD		
K_{O1}†	VCO Gain, BAND1	TBD		TBD		
K_{O2}†	VCO Gain, BAND2	TBD		TBD		

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	
PIN(S): FSPMP						
K_{DO} †	Phase Detector Gain. BAND0	TBD		TBD	µA/rad	F
K_{D1} †	Phase Detector Gain. BAND1	TBD		TBD	µA/rad	P
K_{D2} †	Phase Detector Gain. BAND2	TBD		TBD	µA/rad	P
K_{D3} †	Phase Detector Gain. BAND3	TBD		TBD	µA/rad	P
K_{O0} †	VCO Gain, BAND0	TBD		TBD	rad/s-V	

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS
PIN(S): ALE, $\overline{MCS}$ (Chip Select), $\overline{MRE}$ (Read), $\overline{MWE}$ (Write), AD7-0 (Add					
T_{ALw}	ALE pulse width high	15			ns
T_{ASALl}	Address setup to ALE low	10			ns
$T_{AhldALl}$	Address hold after ALE low	5			ns
T_{AzRDl}	Read low to Address tri-state			15	ns
T_{RDw}	Read pulse width	110			ns
T_{RDhALh}	Read high to next ALE high	15			ns
T_{RDax}	Read (data) access time	18		90	ns
$T_{DhldRDh}$	Data hold after Read high	5			ns



APPENDIX

T-52-

A.0 APPLICATION NOTES

A-1 FREQUENCY SYNTHESIZER

As discussed in section 3.0, "Frequency Synthesizer", the Frequency Synthesizer utilizes one divider to divide the crystal reference (COD) and one for the VCO (VCOD). This leads to some confusion as to the resolution which can be expected in generating the NRZ data rate.

As can be seen from EQ. 6.0, the output of the Synthesizer is simply a ratio of the crystal input frequency pre-scaled by the HFCOD. That is, for any given crystal frequency, there is a set of ratios

is 1/90. This phenomena repeat
ratios. In fact, it can be show tha
similarly degrades around multiple
a much lesser degree. This proc
with the resolution around multipl
better an 1/2, but worse than 1/4, e

Following this same pattern, the I
thesizer will have resolutions whic
and around integer ratios of the V
it can be said that the worst pos
will be equal to 1/COD, in the sam

```
#include <stdio.h, math.h. string.h>
main(argc, argv)
int argc;
char *argv[ ];
{
        float fxtli = 0.0;
        float fxtlicod       = 0.0;
        float fvco           = 0.0;
        float fnrz           = 0.0;
        float cod            = 1.0;
        float vcod           = 1.0;
        char *fxtliptr;
```

T-52

A-2 WINDOW SHIFT SYNTHESIZER

For discussion of the resolution, refer to "A-1 Frequency Synthesizer". The following C program is provided to assist in programming the Synthesizer. The program requires as its input the expected data rate. The output will be the exhaustive set of all possible data rates along with the necessary COD and VCOD values. Taking the output of this program and sorting based on the first column (NRZ data rate) produces a convenient look up table of data rates for the given crystal frequency.

```
#include <stdio.h, math.h, string.h
main(argc, argv)
int argc;
```

T-5

```
fvco = ftclkcod*vcod;
 delta = (1000.0/fvco)/9.0;
 if ((delta <= 6) && (delta >= 2))
 {
          while (SAM  16)
          {
                   delay = (SAM*delta);
                   wsi = (int) (delay/tclk);
                   wsf = (float) wsi;
                   ws = 100*((((tclk/2) * ((2*wsf
                   printf("%02f percent (delay =
                      cod =%02f vcod =%02f
                      SAM =  %02f/n".ws, delay
                      (vcod-1), ( SAM-1)):
         SAM=SAM+1.0;
         }
```