WD1510-00, 01 LIFO/FIFO BUFFER REGISTER

FEATURES

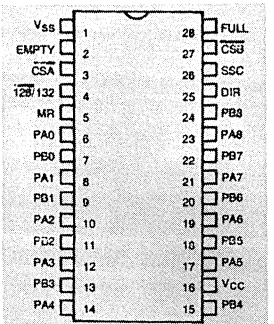
- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (-00), 1 MHz (-01)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- MASTER RESET

APPLICATIONS

- POINT OF SALE TERMINALS
- COMPUTER-TO-PERIPHERAL BUFFER
- CRT BUFFER MEMORY
- LINE PRINTER BUFFER
- INTERRUPT STACK (LIFO MODE)

GENERAL DESCRIPTION

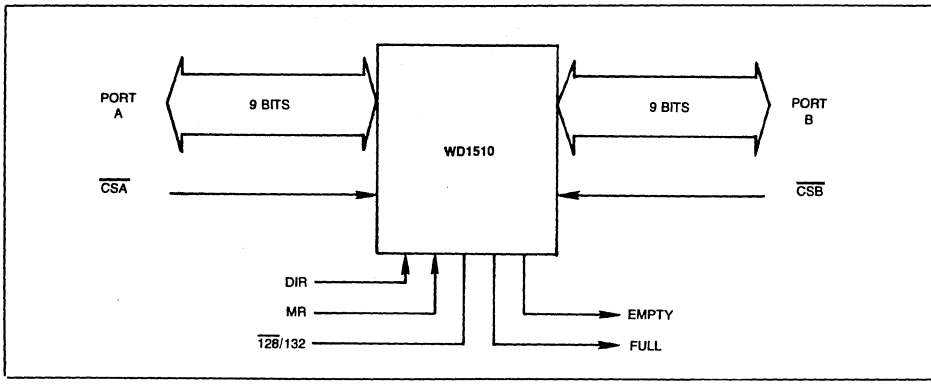
The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.



PIN CONNECTIONS

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{CSA}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{128}$/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14, 17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing data
7,9,11,13,15 18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing data
16	V_{CC}	V_{CC}	+5 volts ±.25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from
26	SYSTEM SENTINEL™ CHECKOUT	SSC	No connection (For future use)
27	CHIP SELECT PORT B	$\overline{CSB}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data



OPERATION

The WD1510 contains a 132 × 9 buffer which may be programmed for 128 × 9 operation. Setting the 128/132 pin to a Logic 0 enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the 128/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately 5KΩ.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a Logic 1, then data is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate $\overline{CS}$ (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of $\overline{CSA}$ or $\overline{CSB}$. In a Read mode, data is valid as long as $\overline{CS}$ remains active. Both Ports return to the high impedance state when $\overline{CS}$ is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes (128/132 = 0) or 1 thru 131 bytes (128/132) = 1.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

V_{CC} with respect to V_{SS} (Ground) = +7V
Max Voltage on any Pin with respect to V_{SS} = −0.5V to +7V
Operating Temperature = 0°C to 70°C
Storage Temperature = −55°C to +125°C

Operating Characteristics (DC)

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}, V_{SS}$
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			.7	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -40\mu A$
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA
I_{CC}	Power Supply Current		125	200	mA	All outputs open

A.C. TIMING CHARACTERISTICS

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V, V_{OH} = 2.0V, V_{OL} = 0.8V

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SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
T_{MR}	Master Reset Time	400			NS.	
T_{DV}	Data Valid from CS			550	NS.	
T_{DH}	Data Hold from CS	150			NS.	
T_{DIR}	DIR Setup Time	1500			NS.	
T_{EV}	EMPTY Valid from CS			550	NS.	
T_{FV}	FULL Valid from CS			550	NS.	
T_{CSL}	CS Pulse Width Low	600			NS.	
T_{CSH}	CS Pulse Width High	600			NS.	
T_{CY}	CS Cycle Time	1540			NS.	
T_{DS}	Data Setup Time	80			NS.	
FMAX	Data Transfer Rate			650	KHZ	

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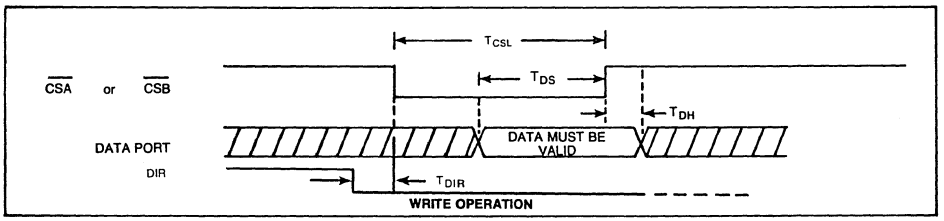
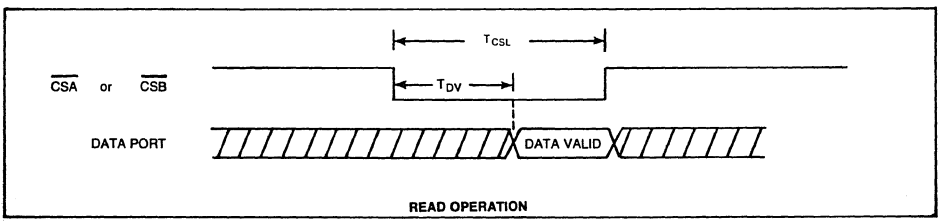
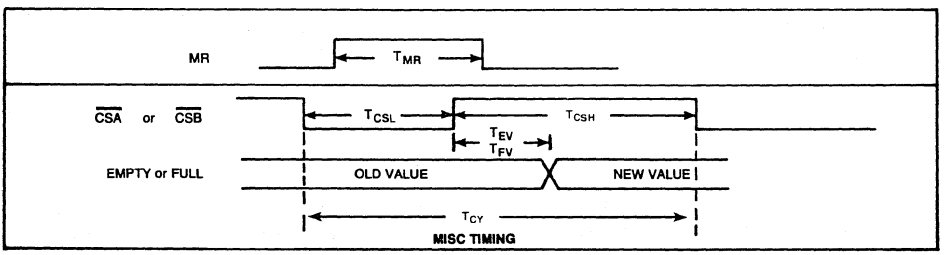
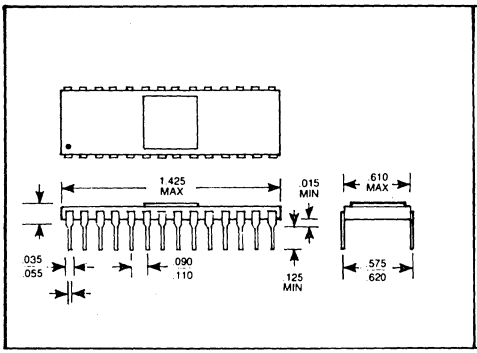
T_{MR}	Master Reset Time	250			NS.	
T_{DV}	Data Valid from CS			350	NS.	
T_{DH}	Data Hold from CS	100			NS.	
T_{DIR}	DIR Setup Time	1000			NS.	
T_{EV}	EMPTY Valid from CS			350	NS.	
T_{FV}	FULL Valid from CS			350	NS.	
T_{CSL}	CS Pulse Width Low	500			NS.	
T_{CSH}	CS Pulse Width High	500			NS.	
T_{CY}	CS Cycle Time	1000			NS.	
T_{DS}	Data Setup Time	50			NS.	
FMAX	Data Transfer Rate			1	MHZ	



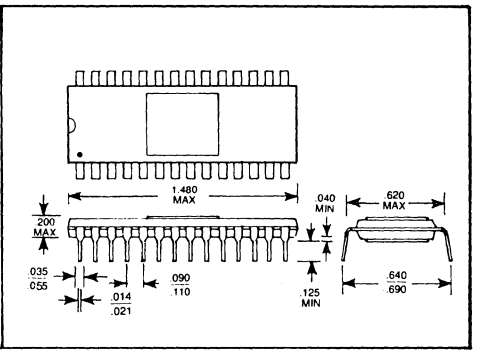




SECTION 2



WD1510E-XX CERAMIC PACKAGE



WD1510F-XX PLASTIC PACKAGE

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00 650kHz, version

01 1.0 MHz version

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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