WD1772 Floppy Disk Formatter/Controller

WESTERN DIGITAL CORPORATION

Edited By Jean Louis-Guérin

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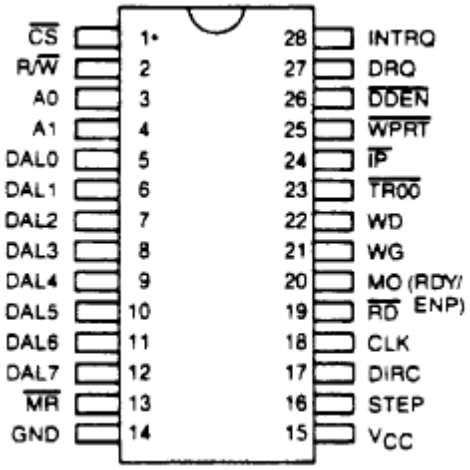
Preface

This datasheet describes the **WD1772** used in Atari Computers. It is based on the original WD177X-00 Western Digital datasheet. However I have kept only the information relevant to the WD1772 (i.e. I have removed information specific to WD1770 and WD1773). I have also corrected several **errors** (especially on diagrams and tables) from the original specification and added extra information. The original information is displayed in black and the added and/or modified information is displayed in blue.

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- BUILT-IN DIGITAL DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- MOTOR CONTROL
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8-BIT BI-DIRECTIONAL DATA BUS

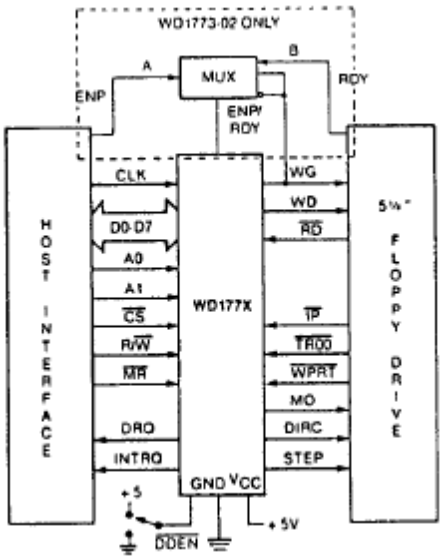


GENERAL DESCRIPTION

The WD1772 is a MOS/LSI device which performs the functions of a Floppy Disk Formatter/Controller. It is similar to its predecessor, the FD179X, but also contains a ***digital data separator*** and *write pre-compensation circuitry*. The drive side of the interface needs no additional logic except for buffers/receivers. It is designed for single (**FM**) or double (**MFM**) density operation.

The WD1772 is implemented in NMOS silicon gate technology and is available in a 28-pin dual-in-line as well as in quad pack

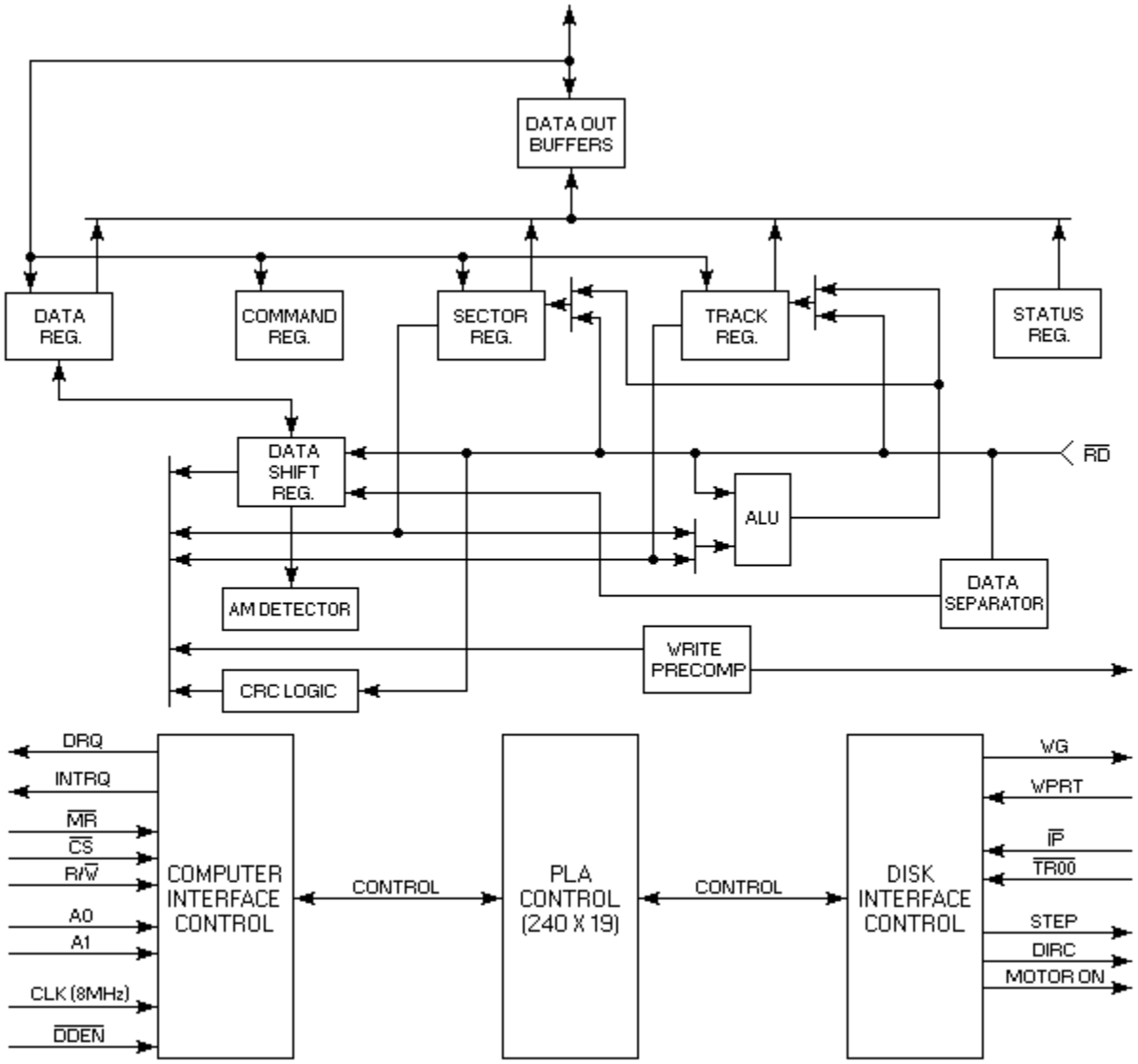
The WD1772 device contains a built-in **digital data separator** which virtually eliminates all external components and adjustments associated with data recovery in previous designs. A single read line (RD, Pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device is designed for control of floppy disk drives with data rates of 125 Kbits/Sec (single density) and 250 Kbits/Sec (double density). In addition, write pre-compensation of 125 nanoseconds from nominal is enabled at any point through simple software commands. Another programmable feature on the WD1772 is Motor On, which enables the spindle motor automatically prior to operating a selected drive.



The processor interface consists of an 8-bit bidirectional bus for transfer of status, data, and commands. All Host communication with the drive occurs through these lines. They are capable of driving one standard TTL load or three LS loads.

Pin	Mnemonic	Signal Name	i/o	Function
1	CS*	Chip Select*	I	A logic low on this input selects the chip and enables Host communication with the device.
2	R/W*	Read/Write*	I	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register
3,4	A0,A1	Address 0,1	I	These two inputs select a register to Read/Write data **CS A1 A0 R/W*=1 R/W*=0** 0 0 0 status reg command reg 0 0 1 track reg track reg 0 1 0 sector reg sector reg 0 1 1 data reg data reg
5-12	DAL0-DAL7	Data access lines 0 through 7	I/O	Eight-bit bi-directional bus used for transfer of data control, or status. This bus is enabled by CS* and R/W*. Each line will drive one TTL load
13	MR*	Master reset*	I	A logic low pulse on this line resets the device and initializes the Status Register (internal pull-up).
14	GND	Ground		Ground
15	VCC	Power supply		+ 5V ± 5% power supply input.
16	STEP	Step	O	The Step input contains a pulse for each step of the drive's R/W head
17	DIRC	Direction	O	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLK	Clock	I	This input requires a free-running 50% duty cycle clock (for Internal timing) at 8 MHz +/- 0.1%.
19	RD*	Read data*	I	This active low Input is the raw data line containing both clock and data pulses from the drive
20	MO	Motor on	O	Active high output used to enable the spindle motor prior to read, write or stepping operations.
21	WG	Write gate	O	This output is made valid prior to writing on the diskette.
22	WD	Write data	O	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TR00*	TRACK00*	I	This active low input informs the WD1772 that the drive's R/W heads are positioned over Track zero.
24	IP*	Index pulse*	I	This active low input informs the WD1772 when the physical Index hole has been encountered on the diskette
25	WPRT*	Write protect*	I	This Input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).
26	DDEN*	Double density enable*	I	This input pin selects either single (FM) or double (MFM) density. When DDEN = 0, double density is selected (internal pull-up).
27	DRQ	Data request	O	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTRQ	Interrupt request	O	This active high output is set at the completion of any command, is reset by a read of the Status Register.

ARCHITECTURE



The primary sections of the Floppy Disk Formatter are the Parallel Processor Interface and the Floppy Disk Interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (RD) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register - This 8-bit register is used as a holding register during disk Read and Write operations. In disk **read** operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk **write** operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek Command, the Data Register holds the address of the desired Track position. This register is loaded from the DAL (Data Access Line) and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The

Track Register can be loaded from or transferred to the DAL. This Register is not loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register is not loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register is not loaded when the device is busy unless the new command is a force interrupt. The Command Register is loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register is read onto the DAL, but not loaded from the DAL.

CRC Logic - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:

- $G(x) = x16 + x12 + x5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC Register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control - All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The WDI772 has two different modes of operation according to the state of DDEN*

- When DDEN* = 0, double density (MFM) is enabled.
- When DDEN* = 1, single density (FM) is enabled.

AM Detector - The address mark detector detects ID, Data and index address marks during read and write operations.

Data Separator - A **digital data separator** consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The Interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1772. The DAL are three state buffers that are enabled as output drivers when CS* and R/W* = 1 are active or act as input receivers when CS* and R/W* = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the Host processor, the device address is decoded and CS* is made low. The address bits Al and A0, combined with the signal R/W* during a Read operation or Write operation are interpreted as selecting the following registers:

Floppy Disk Controller Devices

Al	**A0**	**READ (R/W* = 1)**	**WRITE (R/W* = 0)**
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

After any register is written to, the same register can not be read from until 16 µsec In MFM or 32 µsec in FM have elapsed.

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1772 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request bit is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the *Lost Data* bit is set in the Status Register. The Read operations continue until the end of sector is reached.

On Disk Write operations the Data Request bit is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the *Lost Data* bit is set In the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt Command condition is met.

The WD1772 has two mode of operation according to the state of DDEN*, When DDEN* = 1, single density is selected. In either case, the CLK input is at 8 MHz

GENERAL DISK READ OPERATIONS

Sector lengths of 1281 256, 512 or 1024 are obtainable in either FM or MFM formats. For **FM**, DDEN* is placed to logical 1. For **MFM** formats, DDEN* is placed to a logical 0. Sector lengths are determined at format time by the fourth byte in the ID field.

SECTOR LENGTH TABLE	
Sector Length Field (Hex)	**Number Of Bytes In Sector (Dec)**
00	128
01	256
02	512
03	1024

Only the last two bits of the byte are used to compute the number of bytes. Therefore the remaining 6 bits can take any value. For example $03 is equivalent to $FF

The number of sectors per track for the WD1772 range from 1 to 240. The number of tracks for the WD1772 range 0 to 240.

GENERAL DISK WRITE OPERATION

When writing on the diskette the WG output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte is loaded into the Data Register in response to a Data Request from the device before the WG is activated.

Writing is inhibited when the WPRT* input is asserted, in which case any Write Command is immediately terminated, an interrupt is generated and the Write Protect Status bit is set.

For Write operations, the WD1772 provides WG to enable a Write condition, and WD which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. WD provides the unique missing clock patterns for recording Address Marks.

On the WD1772, the Precomp Enable bit in Write Commands allows automatic Write pre-compensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nsec according to the following table:

PATTERN				**MFM**	**FM**
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A
previous Bits sent		current Bit sending	next Bit to be sent		

Precompensation is typically enabled on the inner most tracks where bit shifts usually occur and bit density is at its maximum. READY is true for read/write operations (all Type II and III Command executions).

COMMAND DESCRIPTION

The WD1772 accepts 11 commands. Command words are only loaded in the Command Register when the Busy Status bit is off (Status bit 0). The one exception is the Force Interrupt Command. Whenever a command is being executed, the Busy Status bit is set. When a command is completed, an interrupt is generated and the Busy Status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. Commands are divided into four types and are summarized in the following table.

COMMAND SUMMARY

		BITS							
TYPE	**COMMAND**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I	Restore	0	0	0	0	h	v	r1	r0
I	Seek	0	0	0	1	h	v	r1	r0
I	Step	0	0	1	u	h	v	r1	r0
I	Step-in	0	1	0	u	h	v	r1	r0
I	Step-out	0	1	1	u	h	v	r1	r0
II	Read Sector	1	0	0	m	h	e	0	0
II	Write Sector	1	0	1	m	h	e	p	a0
III	Read Address	1	1	0	0	h	e	0	0
III	Read Track	1	1	0	1	h	e	0	0
III	Write Track	1	1	1	1	h	e	p	0
IV	Force Interrupt	1	1	0	1	i3	i2	i1	i0

Flag Summary

u = Update Flag (Bit 4)		**m = Multiple Sector Flag (Bit 4)**	
0	No Update	0	Single Sector
1	Update Track Register	1	Multiple Sector
h = Motor On Flag (Bit 3)		**e = 15ms Settling Delay (Bit 2)**	
0	Enable Spin-up Sequence	0	No Delay
1	Disable Spin-up Sequence	1	Add 15ms Delay
v = Verify Flag (Bit 2)		**p = Write Precompensation (Bit 1)**	
0	No Verify	0	Unable Write Pre-comp
1	Verify on Destination Track	1	Disable Write Pre-comp
r1,r0 = Stepping Rate (Bits 1,0)		**a0 = Data Address Mark (Bit 0)**	
0,0	6 ms	0	Write Normal Data Mark
0,1	12 ms	1	Write Deleted Data Mark
1,0	2 ms	**i3,i2,i1,i0 Interrupt condition (Bits 3-0)**	
1,1	3 ms	1,0,0,0	Immediate Interrupt
		0,1,0,0	Interrupt on Index Pulse
		0,0,0,0	Terminate without interrupt

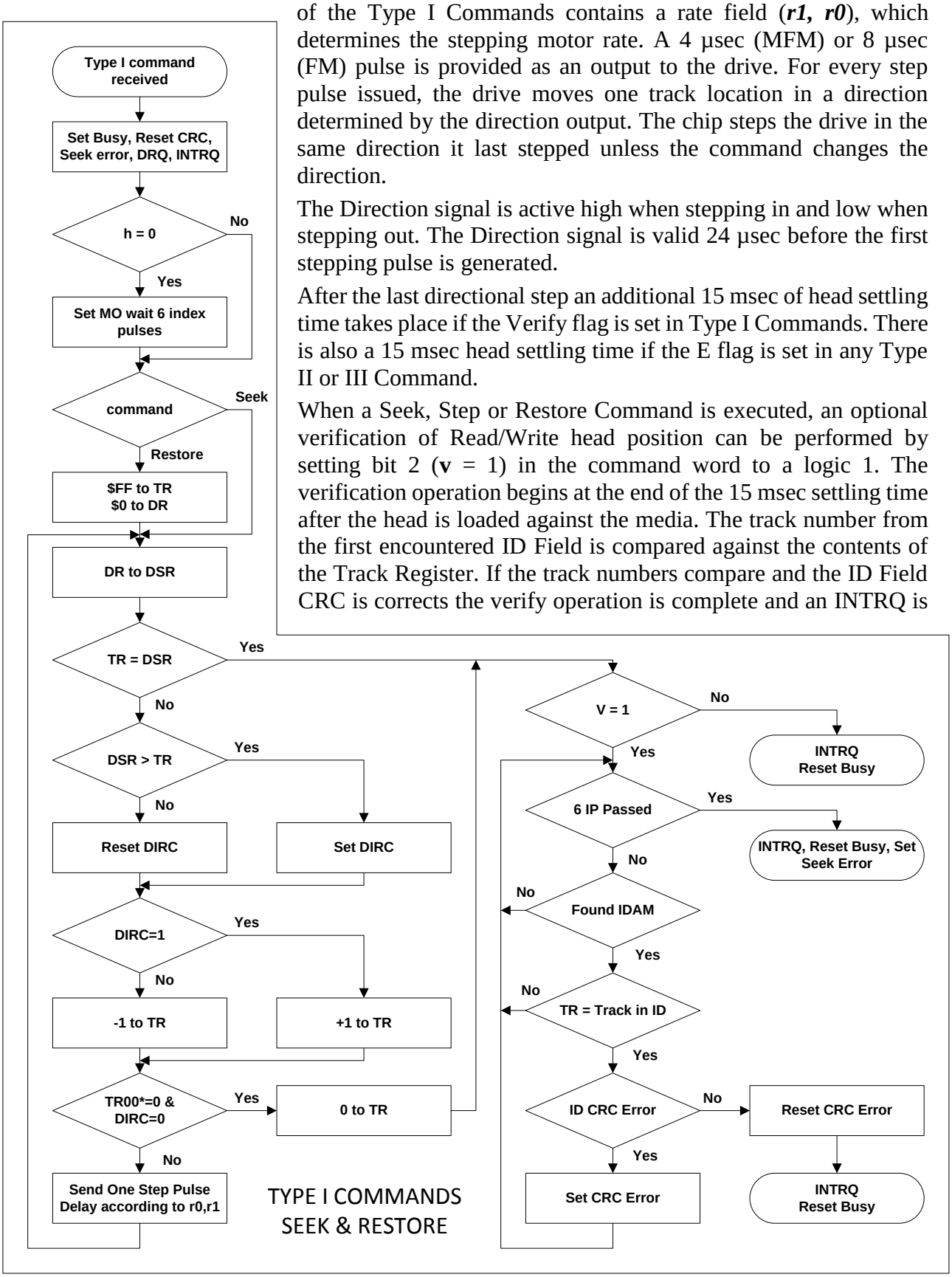
TYPE I COMMANDS

The Type I Commands Include the *Restore*, *Seek*, *Step*, *Step-in* and *Step-Out* Commands. Each of the Type I Commands contains a rate field (***r1, r0***), which determines the stepping motor rate. A 4 µsec (MFM) or 8 µsec (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip steps the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 µsec before the first stepping pulse is generated.

After the last directional step an additional 15 msec of head settling time takes place if the Verify flag is set in Type I Commands. There is also a 15 msec head settling time if the E flag is set in any Type II or III Command.

When a Seek, Step or Restore Command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (**v** = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 msec settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field CRC is corrects the verify operation is complete and an INTRQ is



generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation.

If ***v*** = 1 the WDI772 must find an ID Field with correct track number and correct CRC within 5 revolutions of the media, or the Seek Error is set and an INTRQ is generated. It ***v*** = 0, no verification is performed.

On the WD1772 all commands, except the Force Interrupt Command, are programmed via the ***h*** Flag to delay for spindle motor start up time. If the ***h*** Flag is not set and the MO signal is low when a command is received, the WD1772 forces MO to a logic 1 and waits 6 revolutions before executing the command. At 300 RPM, this guarantees a one second spindle start up time. If after finishing the command, the device remains idle for 9 revolutions, the MO signal goes back to a logic 0. If a command is issued while MO is high, the command executes immediately, defeating the 6 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1772 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 (TR00*) input is sampled. If TR00* is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00* is not active low, stepping pulses at a rate specified by the rate field (***r1, r0***) are issued until the TR00* input is activated.

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the TR00* input does not go active low after 255 stepping pulses, the WD1772 terminates operation, interrupts, and sets the Seek Error status bit, providing the ***v*** flag is set.

A verification operation also takes place if the ***v*** flag is set. The ***h*** bit allows the Motor On option at the start of a command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD1772 updates the Track Register and issues stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the ***v*** flag is on. The ***h*** bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the Track Register is updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD1772 Issues one Stepping Pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the rate fields ***(r1, r0)***, a verification takes place if the ***v*** flag is on. If the ***u*** flag is on, the Track Register is updated. The ***h*** bit allows the Motor On option at the start of the command. An Interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD1772 issues one Stepping Pulse In the direction towards track 76. If the ***u*** flag is on, the Track Register is incremented by one. After a delay determined by the rate (***r1, r0***) fields a verification takes place If the ***v*** flag is on, The ***h*** bit allows the Motor

On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the WD1772 issues one stepping pulse in the direction towards track 0. If the ***u*** flag is on, the Track Register is decremented by one. After delay determine by the rate (***r1, r0***) field, verification takes place if the ***v*** flag is on. The ***h*** bit allows the Motor On option at the start of the command, An Interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the ***Read Sector*** and ***Write Sector*** commands. Prior to loading the Type II command into the Command Register, the computer loads the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy Status bit is set. If the flag ***e*** = 1 the command executes after a 15 msec delay.

When an ID field is located on the disk, the WD1772 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is no Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the Data field is located and is either written into, or read from, depending upon the command.

The WD1772 must find an ID field with the correct Track number, Sector number, and CRC within four revolutions of the disk, or, the Record Not Found Status bit is set (Status Bit 4) and the command is terminated with an INTRQ.

An ID field is located when exactly 3 consecutive sync bytes (not more not less) are found followed by an IDAM (ID Address Mark). The standard IDAM value as described in the datasheet is $FE, however the IDAM can be any value between $FC and $FF.

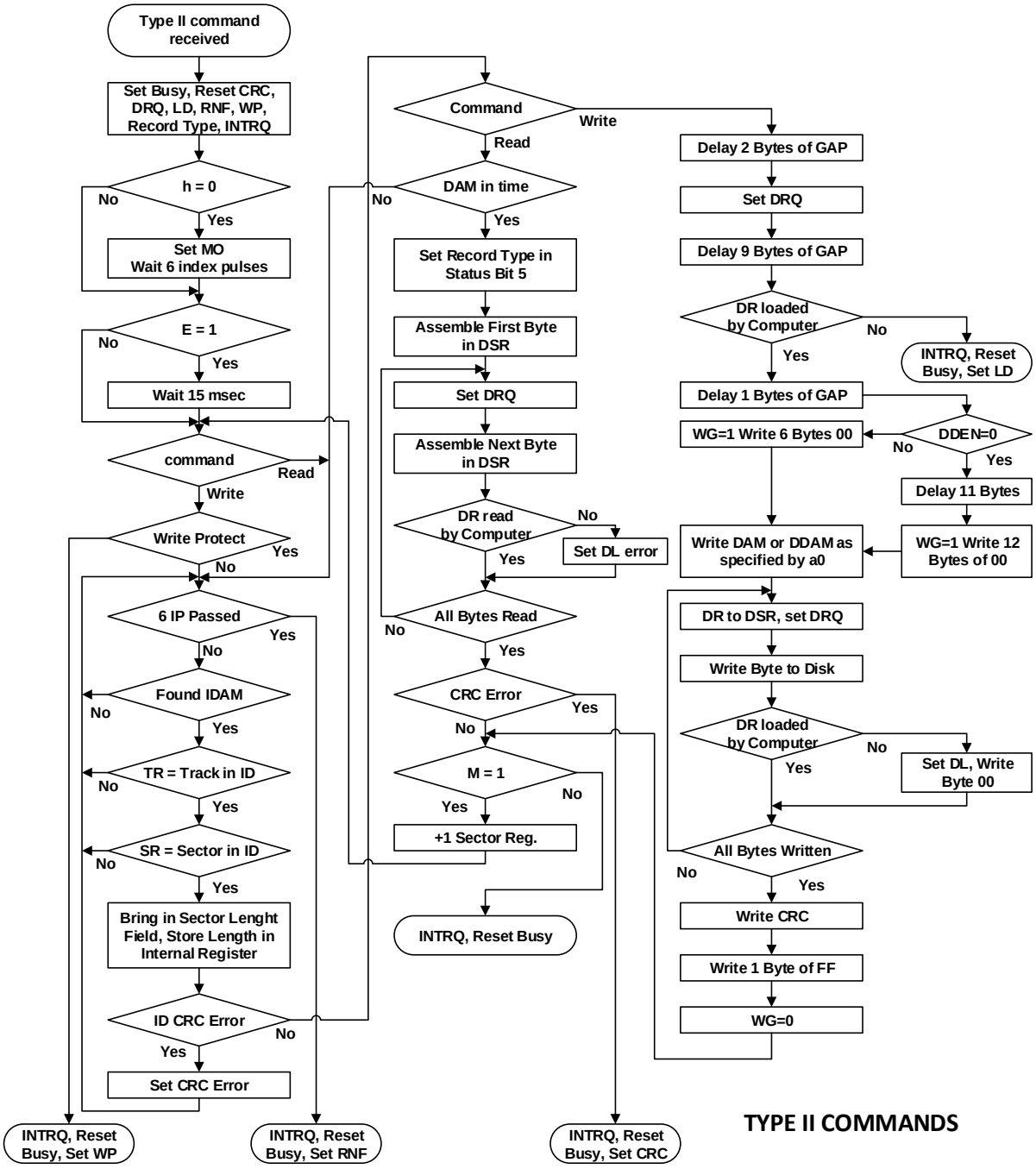
A Data field is located when 3 consecutive sync bytes or more are found followed by a DAM (Data Address Mark) or DDAM (Deleted Address Mark). The DAM value is normally $FB, however the value $FA can be used. The DDAM value is normally $F8, however the value $F9 can be used.

Each of the Type II Commands contains an ***m*** flag which determines II multiple records (sectors) are read or written, depending upon the command. If ***m*** = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If ***m*** = 1, multiple records are read or written with the Sector Register internally updated so that an address verification occurs on the next record. The WD1772 continues to read or write multiple records and updates the Sector Register in numerical ascending sequence until the Sector Register exceeds the number of sectors on the track or until the Force interrupt Command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: if the WD1772 is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The WD1772 searches for 5 disk revolutions, interrupts out, resets Busy, and sets the Record Not Found (RNF) Status Bit.

READ SECTOR

Upon receipt of the Read Sector Command, the Busy Status Bit is set, then when an ID field is encountered that has the correct Track number, correct Sector number, and correct CRC, the Data field is searched. The Data Address Mark of the data field is to be found within 30 bytes in Single Density and 43 bytes in Double Density from the last ID field CRC byte. If not, the ID field is searched for and verified again followed by the Data Address Mark search. If, after five revolutions the DAM is not found, the Record Not Found Status Bit is set and the operation is terminated. When the first character or byte of the data field is shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents or the DR before a new character is transferred that character is lost and the Lost Data Status Bit Is set. This sequence continues until the complete data field is transferred to the computer. If there is a CRC error at the end of the data field, the CRC Error Status bit is set, and the command is terminated (even if it is a multiple record command).



At the end of the Read operation, the type of Address Mark encountered in the Data field is recorded In the Status Register (Bit S5) as shown:

Status Bit S5	Data Address Mark	AM Byte
1	Deleted Data Mark	$F8 $F9
0	Data Mark	$FB $FC

WRITE SECTOR

Upon receipt of the Write Sector-Command, the Busy Status Bit is set. When an ID field is encountered that has the correct Track number, correct Sector number, and correct CRC, a DRQ is generated. The WD1772 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the WG output is made active if the DRQ is serviced (i.e. the DR is loaded by the computer). If DRQ is not serviced, the command is terminated and the Lost Data Status Bit is set. If the DRQ is serviced, the WG is made active and six bytes of zeroes in single density or 12 bytes of zeroes in double density are written on the disk. The Data Address Mark is then written on the disk as determined by the ***a0*** field of the command as shown:

a0 Bit 0	**Data Address Mark**	**DAM Byte**
1	Deleted Data Mark	$F8
0	Data Mark	$FB

The WD1772 writes the Data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte is written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ sets 24 µsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address

Upon receipt of the Read Address Command, the Busy Status Bit is set. The ***next*** encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown:

Track Addr	Side Number	Sector Addr	Sector Length	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD1772 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the *Sector register* so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

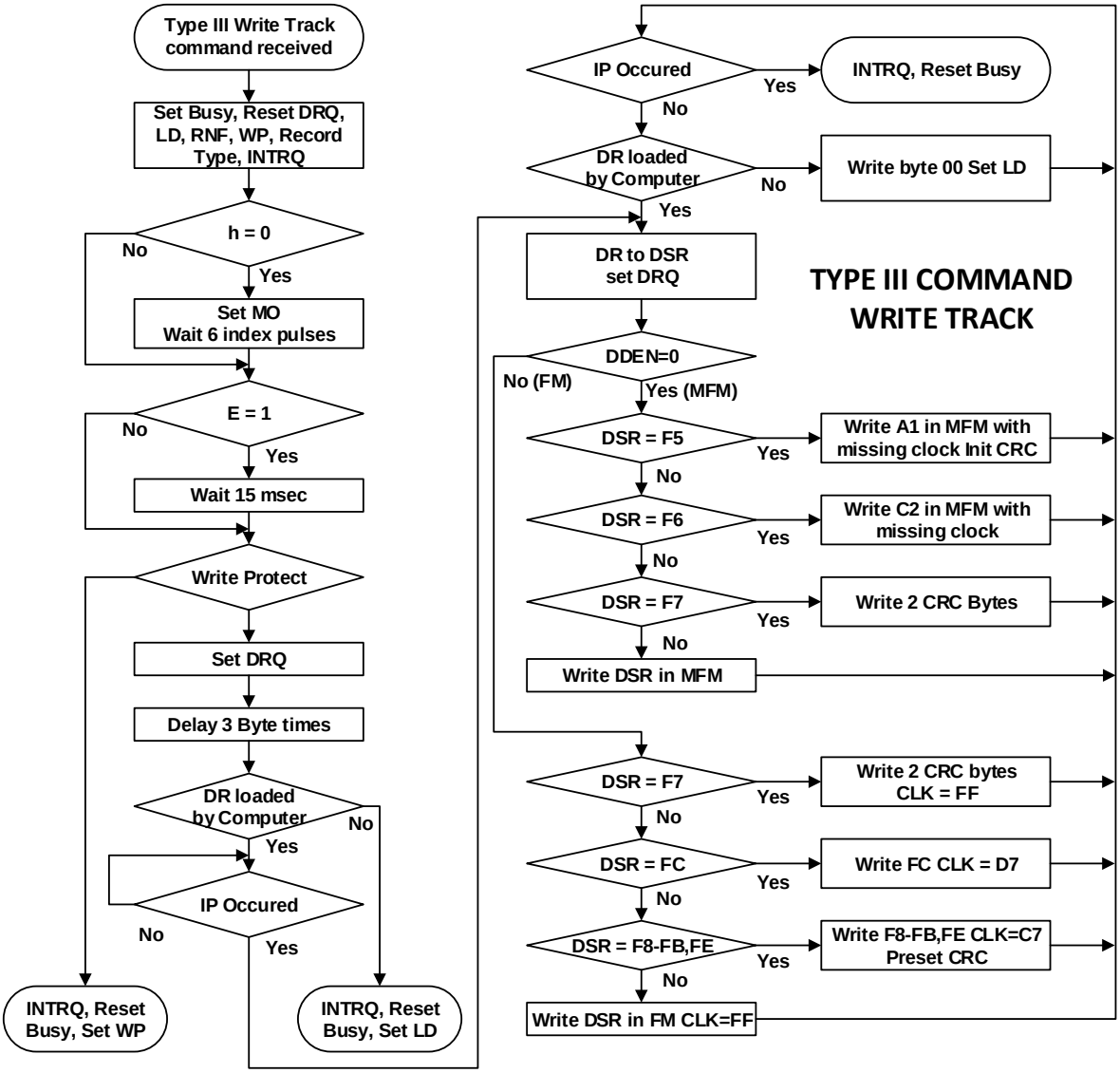
Read Track

Upon receipt of the Read Track Command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each **Address Mark** encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the Address Mark Detector is on for the duration of the command. Because the AM detector is always on, write-splices or noise may cause the chip to look for an AM.

The ID AM, ~~ID field, ID CRC~~ bytes, DAM, ~~Data, and Data CRC~~ Bytes for each sector are correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

The ID field (including CRC bytes), Data field (including CRC bytes) and Gap fields for each sector may be read incorrectly because of false synchronization on C2 Address mark.


Type III Write Track command received
Set Busy, Reset DRQ, LD, RNF, WP, Record Type, INTRQ
h = 0
No
Yes
Set MO
Wait 6 index pulses
E = 1
No
Yes
Wait 15 msec
Write Protect
Set DRQ
Delay 3 Byte times
DR loaded by Computer
No
Yes
IP Occured
No
Yes
INTRQ, Reset Busy, Set WP
INTRQ, Reset Busy, Set LD
IP Occured
Yes
INTRQ, Reset Busy
No
DR loaded by Computer
No
Write byte 00 Set LD
Yes
DR to DSR set DRQ
TYPE III COMMAND
WRITE TRACK
DDEN=0
No (FM)
Yes (MFM)
DSR = F5
Yes
Write A1 in MFM with missing clock Init CRC
No
DSR = F6
Yes
Write C2 in MFM with missing clock
No
DSR = F7
Yes
Write 2 CRC Bytes
No
Write DSR in MFM
DSR = F7
Yes
Write 2 CRC bytes CLK = FF
No
DSR = FC
Yes
Write FC CLK = D7
No
DSR = F8-FB,FE
Yes
Write F8-FB,FE CLK=C7 Preset CRC
No
Write DSR in FM CLK=FF

WRITE TRACK FORMATTING THE DISK

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired Track number and issuing the Write Track Command. Upon receipt of the Write Track Command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered Index Pulse and continues until the next index Pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing does not start until after the first byte is loaded into the Data Register. If the DR is not loaded within three byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one Index Pulse to the next. Normally whatever data pattern appears in the Data Register is written on the disk with a normal clock pattern. However, if the WD1772 detects a data pattern of **F5** through **FE** in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from **F8** to **FE** is transferred from the DR to the DSR in **FM** or by receipt of **F5** in **MFM**. An **F7** pattern generates two CRC characters in **FM** or **MFM**. As a consequence, the patterns **F5** through **FE** do not appear in the gaps, data field, or ID fields. Also, CRC's are generated by an **F7** pattern.

Disks are usually formatted using the IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

Data Pattern In DR (HEX)	In FM (DDEN* = 1)	In MFM (DDEN* = 0)
00 - F4	Write 00 - F4 with CLK = FF	Write 00 - F4, in MFM
F5	Not Allowed	Write Al[1] in MFM, Preset CRC
F6	Not Allowed	Write C2[2] in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 - FB	Write F8 - FB, CLK = C7 Preset CRC	Write F8 through FF, in MFM
FC	Write FC with CLK = D7	
FD	Write FD with CLK = FF	
FE	Write FE, CLK = C7, Preset CRC	
FF	Write FF with CLK = FF	

CRC computation / verification in MFM

A normal sync sequence is composed of 3 Sync characters followed by an Address Mark.

During a write track command, when exactly three **F5** are used in front of the AM, you can consider that the CRC is preset to **FFFF** on the first **F5** and computation continues until the **F7** is transmitted. However in practice the internal CRC logic is preset to **CDB4** (the CRC value for three A1) each time an **F5** is received. It is useful to know this information when more or less than 3 sync are used and you want to check the written CRC value.

[1] Missing clock transition between bits 4 and 5.

[2] Missing clock transition between bits 3 and 4.

TYPE IV COMMANDS

The Forced Interrupt Command is used to terminate a multiple sector read or write command or to insure Type I status in the Status Register. This command is loaded into the Command Register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset. The lower four bits of the command determine the conditional interrupt as follows:

- i0,i1 = Not used with the WD1772 (set to zero)
- i2 = Every Index Pulse
- i3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (i3-i0) are set to a 1. When the condition for interrupt is met the INTRQ line goes high signifying that the condition specified has occurred. If i3-i0 are all set to zero (Hex D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (i3 = 1) an interrupt is immediately generated and the current command terminated. Reading the status or writing to the Command Register does not automatically clear the interrupt. The Hex D0 is the only command that enables the immediate interrupt (Hex D8) to clear on a subsequent load Command Register or Read Status Register operation. Follow a Hex D8 with D0 command.

Wait 16 µsec (double density) or 32 µsec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt Command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy Status Bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy Status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

BITS							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal sync cycles, certain time delays are observed when operating under programmed I/O, as shown.

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48µsec	24µsec
Write to Command Reg.	Read Status Bits 1-7	64µsec	32µsec
Write Register	Read Same Register	32µsec	16µsec

Status Register Description

BIT NAME	MEANING
S7 Motor On	This bit reflects the status of the Motor On output
S6 Write Protect	On Read: Not Used. On Write: It indicates a Write Protect. This bit is reset when updated
S5 Record Type / Spin-up	• On Type I commands: When set, this bit indicates that the Motor Spin-Up sequence has completed (6 revolutions). • On Type II & III commands: this bit indicates record Type. 0 =Data Mark. 1 = Deleted Data Mark.
S4 Record Not Found (RNF) / Seek Error	• On Type I commands: When set the desired track was not verified • On Type II & III commands: When sets it indicates that the desired track, sector, or side were not fount. This bit is reset when updated.
S3 CRC Error	If S4 is set, an error is found in one of more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 Lost Data Byte / TR00	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 Data Request / Index Pulse	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type I commands, this bit indicates the status of the IP signal
S0 Busy	When set, command is under execution. When reset, no command is under execution

Status Register Summary

Type	Command	S7	S6	S5	S4	S3	S2	S1	S0
I	All Type I	MO	X	SU	SE	CRC	T0	IP	BSY
II	Read Sector	MO	X	RT	RNF	CRC	LD	DRQ	BSY
II	Write Sector	MO	WP	RT	RNF	CRC	LD	DRQ	BSY
III	Read Address	MO	X	X	RNF[3]	CRC	LD	DRQ	BSY
III	Read Track	MO	X	X	X	X	LD	DRQ	BSY
III	Write Track	MO	WP	X	X	X	LD	DRQ	BSY
IV	Interrupt while busy	-	-	-	-	-	-	-	0
IV	Interrupt while idle	MO	X	X	X	X	T0	IP	0
	Idle	MO	WP[4]	X	X	X	T0	IP	0

Where:

- 0 = always 0
- X = undefined
- - = retains previous value
- MO = motor on (1 = motor on)
- WP = write protect (1 = write protected)
- SU = spin up (1 = spin-up completed)
- SE = Seek Error (1 = desired track not verified)
- RT = record type (1 = deleted data)
- RNF = record not found (1 = record not found / seek error)
- CRC = CRC (1 = error ➔ if RNF=1 error in ID field, if RNF=0 error in data field)
- T0 = TRK00* (1 = head at track 0)
- LD = lost data (1 = lost data)
- IP = index pulse (1 = disk at index pulse)
- DRQ = data request (1 = data register requires service)
- BSY = busy (1 = controller busy)

[3] Not documented but when performing a ***read address*** to a track without addresses the RNF bit is set.

[4] Not documented but after execution of a Type I command the WP status bit is continuously updated and can be polled like MO and T0, but this is **not true** after a Type II or III command

Single Density - 128 Bytes/Sector

The recommended single-density format with 128 bytes/sector is shown. In order to format a diskette, the user issues the Write Track Command, and loads the Data Register with the following values. For every byte to be written there is one Data Request.

	Number Of Bytes	Hex Value Of Byte Written
	40 (GAP 1)	FF (or 00)
+--	6 (GAP 2)	00
|	1 (ID REC)	FE (ID Address Mark)
|	1 (ID REC)	Track Number
|	1 (ID REC)	Side Number (00 or 01)
|	1 (ID REC)	Sector Number (1 thru 10)
|	1 (ID REC)	00 (Sector Length)
|	1 (ID REC)	F7 (2 CRC's written)
|	11 (GAP 3)	FF (or 00)
|	6 (GAP 3)	00
|	1 (DATA REC)	FB (Data Address Mark)
|	128 (DATA REC)	Data (IBM uses E5)
|	1 (DATA REC)	F7 (2 CRC's written)
+--	10 (GAP 4)	FF (or 00)
	369[5] (GAP 5)	FF (or 00)

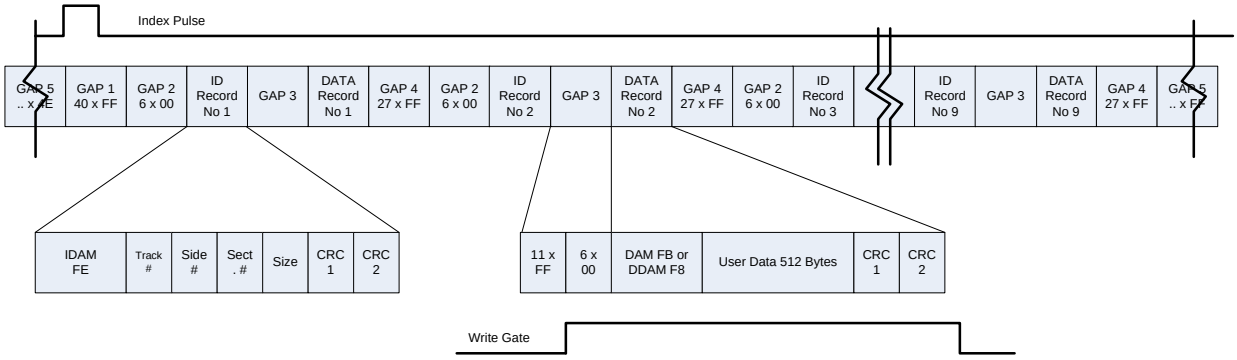
Double Density - 512 Bytes/Sector

Shown below is the recommended dual-density format with 512 bytes/sector. In order to format a diskette the user issues the Write Track Command and loads the Data Register with the following values. For every byte to be written there is one data request.

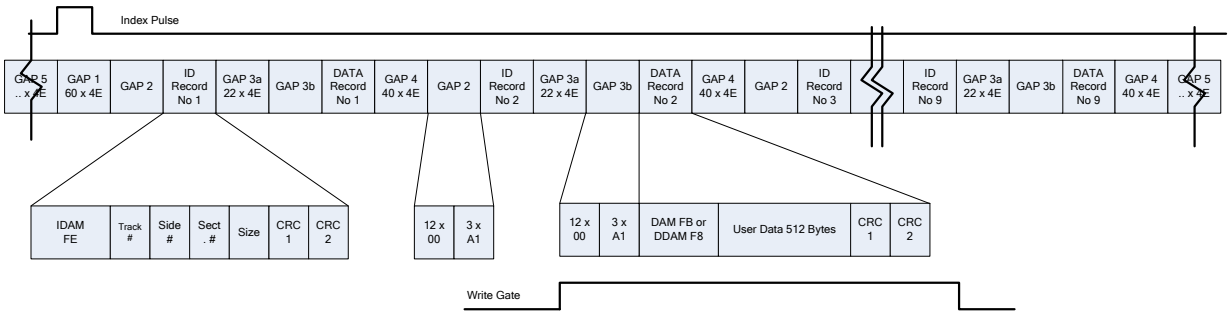
	Num. Bytes	Hex Value Byte Written	
	60	4E	GAP 1 – Post Index Gap
+--	12	00	GAP 2 – PLL Lockup time
|	3	F5 (Writes A1)	GAP 2 – Sync Bytes
|	1	FE (ID Address Mark)	ID Record - IAM
|	1	Track Number (0-4C)	ID Record - Track
|	1	Side Number (0 or 1)	ID Record - Side
|	1	Sector Number (1 thru 10)	ID Record - Sector
|	1	01 (Sector Length)	ID Record - length
|	1	F7 (2 CRC's written)	ID Record – 2 CRC bytes
|	22	4E	GAP 3a – Post ID Gap
|	12	00	GAP 3b – Write splice time / PLL Lockup time
|	3	F5 (Writes A1)	GAP 3b – Synch Bytes
|	1	FB (Data Address Mark)	DATA Record - DAM
|	512	Data (IBM uses E5)	DATA Record - Data
|	1	F7 (2 CRC's written)	DATA Record – 2 CRC bytes
+--	40	4E	GAP 4 – Post Data Gap
	668[6]	4E	GAP 5 – Pre Index (run out) Gap

[5] Continue writing until WD177X-00 interrupts out at index pulse: Approximately 369 bytes.

[6] Continue writing until WD177X-00 interrupts out at index pulse: Approximately 668 bytes.



FM Single Density Format



MFM Double Density Format

Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

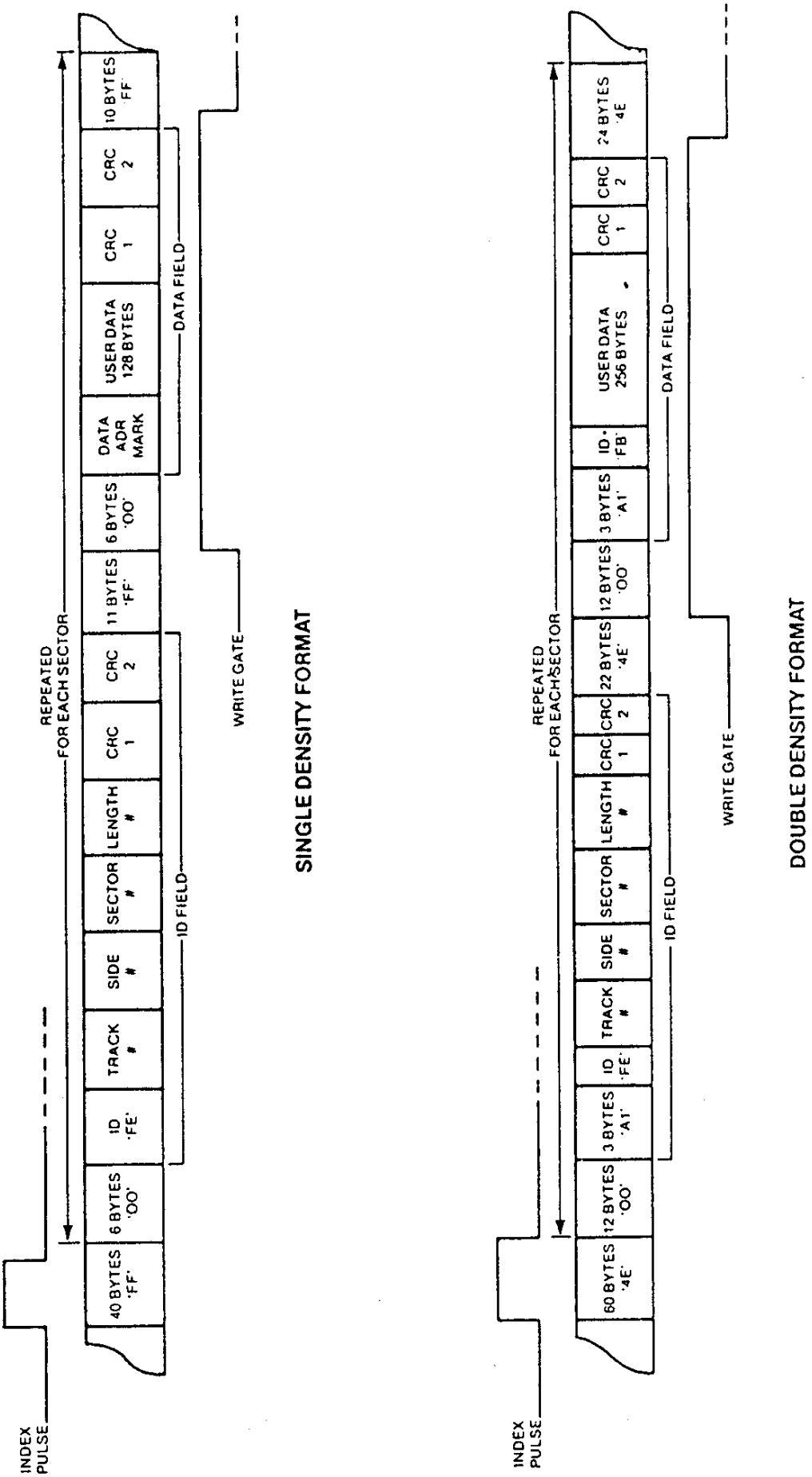
1) Sector size must be 128, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of Al must be used in MFM.

In addition, the Index Address Mark (IAM) is not required for operation by the WD1772. Gap 1, 3 and 4 lengths are as short as 2 bytes for WD1772 operation, however PLL lock up time, motor speed variation, write-splice area, etc. adds more bytes to each gap to achieve proper operation. For highest system reliability use the recommended format.

	FM	**MFM**
Gap 1	16 bytes FF	32 bytes 4E
Gap 2	6 bytes 00[7]	12 bytes 00[7] 3 bytes Al[7]
Gap 3	10 bytes FF[8] 4 bytes 00[8]	24 bytes 4E[8] 8 bytes 00[8] 3 bytes Al[7]
Gap 4	27 bytes FF	38 bytes 4E

[7] Byte counts must be exact.

[8] Byte counts are minimum


INDEX PULSE
40 BYTES 'FF'
6 BYTES '00'
ID 'FE'
TRACK #
SIDE #
SECTOR #
LENGTH #
CRC 1
CRC 2
11 BYTES 'FF'
6 BYTES '00'
DATA ADR MARK
USER DATA 128 BYTES
CRC 1
CRC 2
10 BYTES 'FF'
REPEATED FOR EACH SECTOR
ID FIELD
DATA FIELD
WRITE GATE
SINGLE DENSITY FORMAT
INDEX PULSE
60 BYTES '4E'
12 BYTES '00'
3 BYTES 'A1'
ID 'FE'
TRACK #
SIDE #
SECTOR #
LENGTH #
CRC 1
CRC 2
22 BYTES '4E'
12 BYTES '00'
3 BYTES 'A1'
ID 'FB'
USER DATA 256 BYTES
CRC 1
CRC 2
24 BYTES '4E'
REPEATED FOR EACH SECTOR
ID FIELD
DATA FIELD
WRITE GATE
DOUBLE DENSITY FORMAT

Electrical and Timing Characteristics

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature . . . . . 55°C (67°F) to + 125°C (257°F)

Operating Temperature. . . . . 0°C (32°F) to 70°C (158°F) Ambient

Maximum Voltage to Any Input with Respect to V_{SS} . . . . . + 7V to -0.5V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

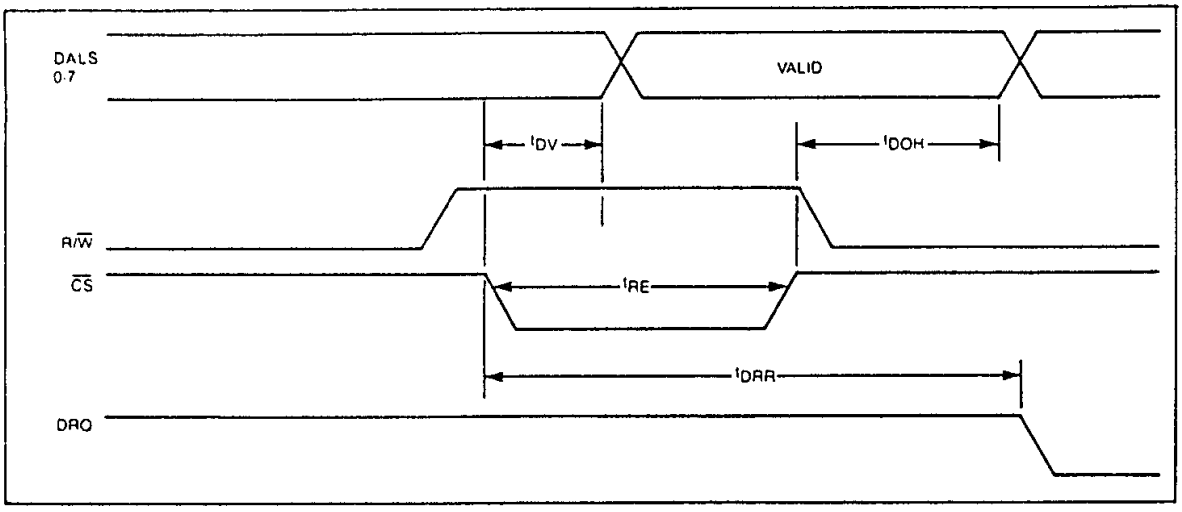
DC OPERATING CHARACTERISTICS

TA = 0°C(32°F) to 70°C (158°F), V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	µA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	µA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IH}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_0 = -100 µA
V_{OL}	Output Low Voltage		0.40	V	I_0 = 1.6 mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	µA	V_{IN} = 0V
I_{CC}	Supply Current	75(Typ)	150	mA	

AC TIMING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F), V_{SS} = 0V, V_{CC} = +5V ± .25V

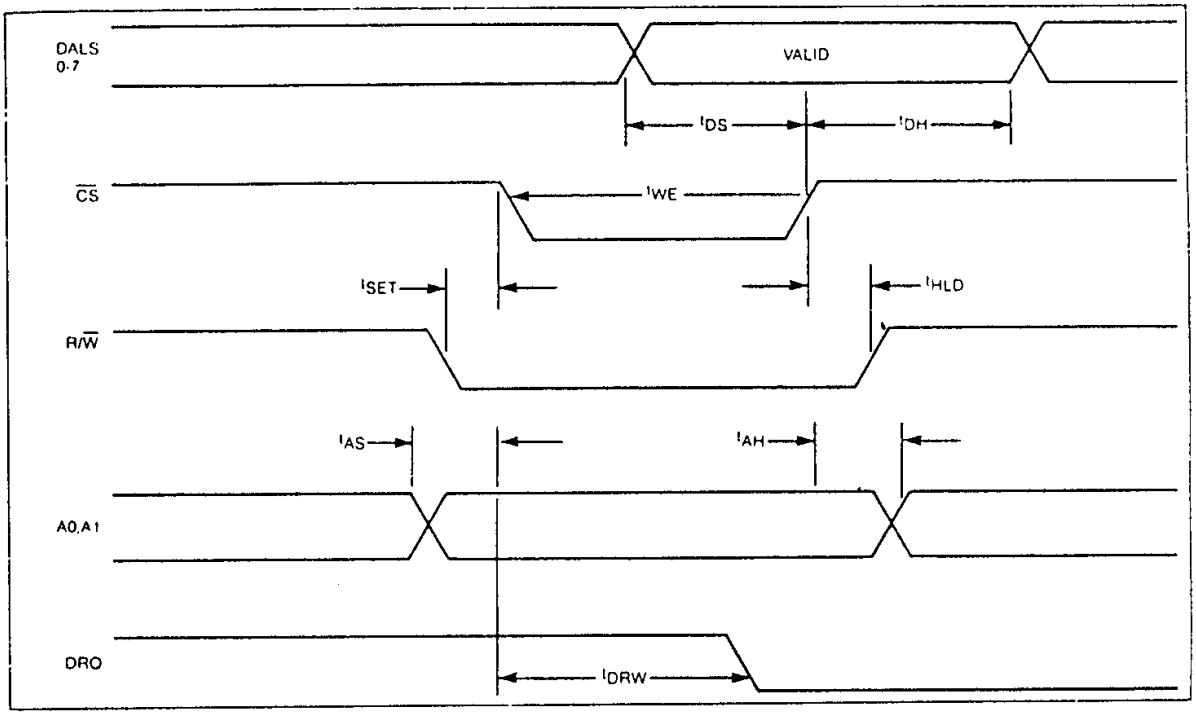


READ ENABLE TIMING

READ ENABLE TIMING - $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
t_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50 pf
	INTRQ Reset from $\overline{RE}$			8	µsec	

Note: DRQ and INTRQ reset are from rising edge (lagging) of $\overline{RE}$, whereas resets are from falling edge (leading) of $\overline{WE}$. Worst case service time for DRQ is 23.5 µsec for MFM and 47.5 µsec for FM.



WRITE ENABLE TIMING

WRITE ENABLE TIMING – $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

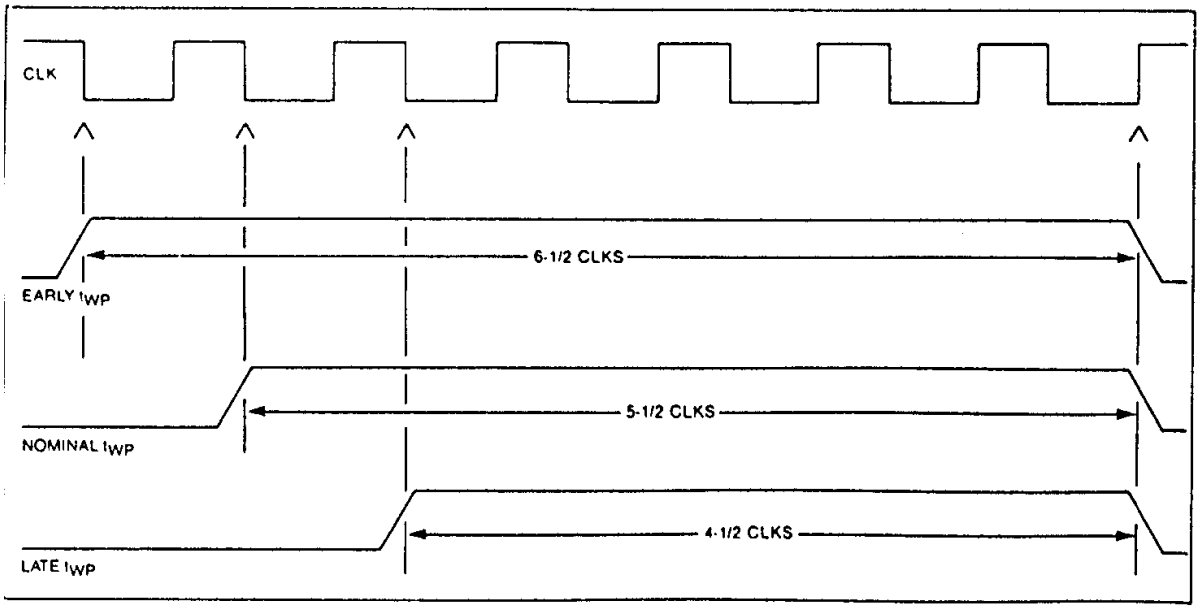
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	µsec	

READ DATA TIMING:

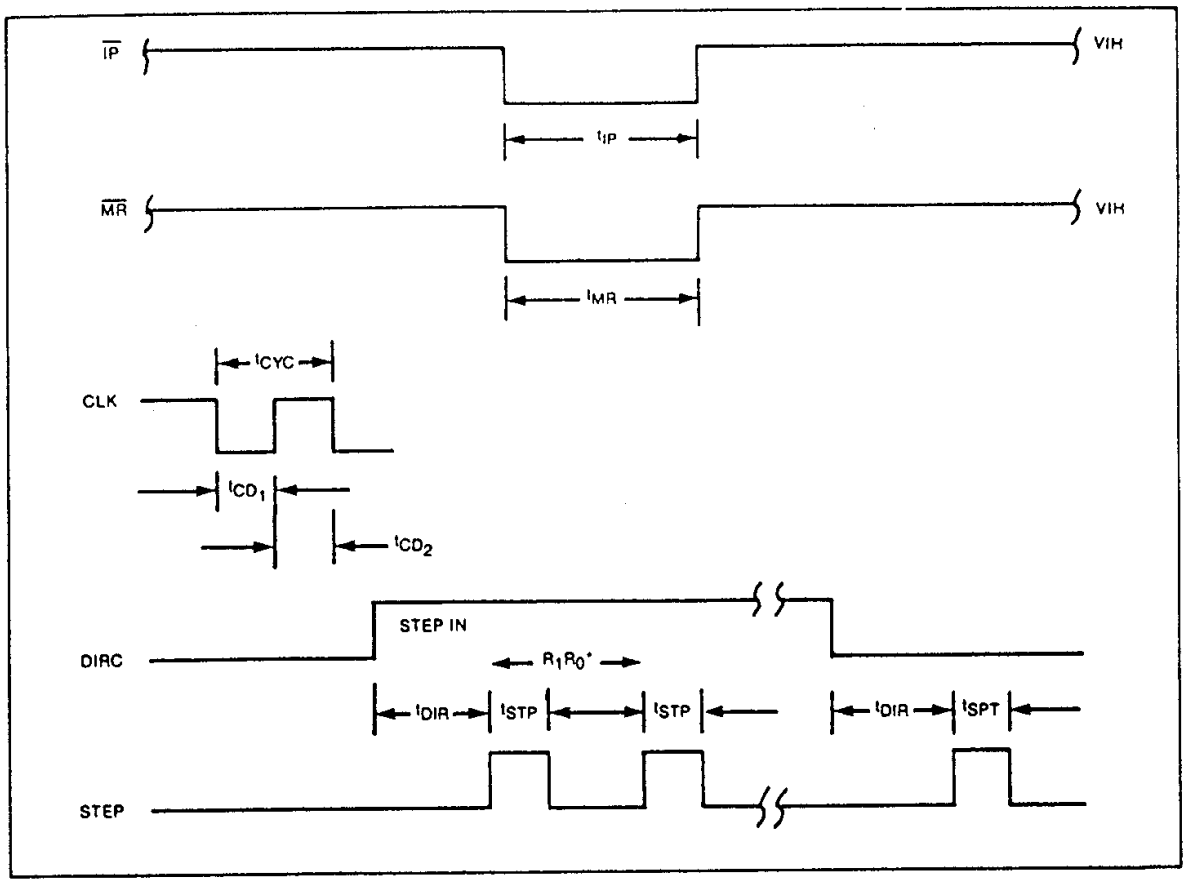
CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	µsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			µsec	

WRITE DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		µsec	FM
			2		µsec	MFM
	Write Data Cycle Time		4,6,8		µsec	
	Write Gate off from WD		4		µsec	FM
			2		µsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		µsec	FM



WRITE DATA TIMING



MISCELLANEOUS TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		µsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		µsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	20			µsec	