WESTERN DIGITAL
CORPORATION

WD1931 Asynchronous/Synchronous Receiver/Transmitter

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5- to 8-Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Detection and Stripping
- Programmable SYN and DLE-SYN Fill
- Transparent BI-SYNC Operation

ASYNCHRONOUS MODE
- Selectable 5- to 8-Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection
- Automatic Serial Echo Mode
- Overrun and Framing Error Detection

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Chip Select, RE, WE, A0, A1 Interface to CPU
- On-Line Diagnostic Capability
- Data Set, Carrier Detect, and Ring Interrupts

BAUD RATE — DC TO 1M BAUD/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock ad Up to Four Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

PINOUT COMPATIBLE TO SD1933 FOR MULTIPROTOCOL BOARD APPLICATIONS

APPLICATIONS

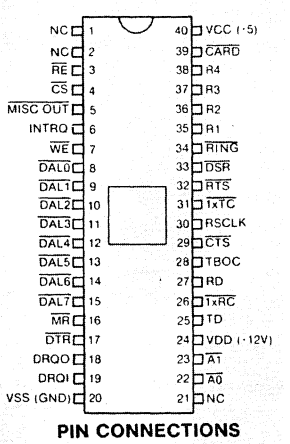
SYNCHRONOUS COMMUNICATIONS

ASYNCHRONOUS COMMUNICATIONS

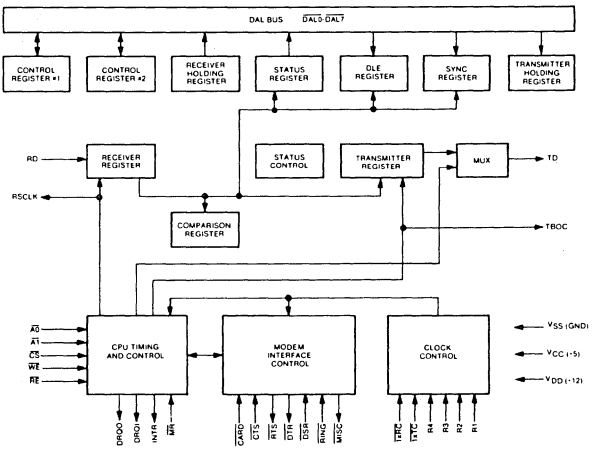
SERIAL/PARALLEL COMMUNICATIONS

GENERAL DESCRIPTIONS

The WD1931 is a MOS/LSI device which performs the functions of interfacing a serial data communications channel to a parallel digital system. This device is capable of full duplex communications with asynchronous and/or synchronous systems. Western Digital has made device pin assignments for the WD1931 to make it compatible with the WD1933 (Synchronous Data Link Controller). This pin out allows the user to implement a one-board multiprotocol design. For character-oriented asynchronous and/or synchronous (bi-sync) protocols, the WD1931 is used, and for bit-oriented SDLC, HDLC and ADCCP protocols the WD1933 is used (see WD1933 data sheet).



PIN CONNECTIONS



WD1931 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	—	NC	No connection; see Note 4.
2	—	NC	No internal connection.
3	READ ENABLE	$\overline{RE}$	When this line is low the device, if selected, gates the contents of the addressed register on the DAL.
4	CHIP SELECT	$\overline{CS}$	The chip is selected when this signal is low.
5	MISCELLANEOUS OUT	$\overline{MISC\ OUT}$	This output is controlled by Bit 5 of Control Register 1 when in the Asynchronous mode and by Bit 4 when in the Synchronous mode. (See Note 1.)
6	INTERRUPT	INTRQ*	This output is made high when one of the interrupt conditions occurs. Reading the Status Register resets this signal.
7	WRITE ENABLE	$\overline{WE}$	When this line is low the device, if selected, accepts the data on the DAL and gates it into the addressed register.
8-15	DATA ADDRESS LINES	$\overline{DAL0\text{-}DAL7}$	Eight-bit Bi-directional bus for transfer of data, control and status information. Active low.
16	MASTER RESET	$\overline{MR}$	The Control and Status Registers and other controls are cleared when this input is low.
17	DATA TERMINAL READY	$\overline{DTR}$	This output is controlled by Bit 0 of Control Register 1 and is intended to control Circuit CD of the data set.
18	DATA REQUEST OUT	DRQO*	This output is made high when the THR is empty while the transmitter is enabled. Loading the THR resets this signal.
19	DATA REQUEST IN	DRQI*	This output is made high when the RHR is full while the receiver is enabled. Reading the RHR resets this signal.
20	POWER SUPPLY	V_{SS}	Ground
21	—	NC	No internal connection.
22	ADDRESS 0	$\overline{A0}$	This input is the low-order address bit for register selection.
23	ADDRESS 1	$\overline{A1}$	This input is the high-order address bit for register selection.
24	POWER SUPPLY	V_{DD}	+12V
25	TRANSMITTED DATA	TD	This output is the transmit serial data. This output is held in a MARKING condition when the transmitter is not enabled. It is intended to control Circuit BA of the data set.
26	RECEIVER TIMING	$\overline{1XRC}$	This input is the receiver 1X clock, when used. It is intended to be derived from Circuit DC of the data set. The Received Data is sampled on the positive transition of this signal.
27	RECEIVED DATA	RD	This input is the receive serial data and is intended to be derived from Circuit BB of the data set.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
28	TRANSMITTER BYTE OUTPUT COMPLETE	TBOC	This output goes high after the last bit of a byte is transmitted including parity if enabled, and is valid for one bit period. See Note 2.
29	$\overline{\text{CLEAR TO SEND}}$	$\overline{\text{CTS}}$	This input enables the transmitter when low and is intended to be derived from Circuit CB of the data set.
30	RECEIVER CLOCK	RSCLK	This output goes high when the receiver data is sampled, and is valid for one clock period. See Note 2.
31	$\overline{\text{TRANSMITTER TIMING}}$	$\overline{\text{1XTC}}$	This input is the transmitter 1X clock when used. It is intended to be derived from Circuit DB of the data set. The Transmitter changes on the negative transition of this signal.
32	$\overline{\text{REQUEST TO SEND}}$	$\overline{\text{RTS}}$	This output is controlled by Bit 1 of Control Register 1 and is intended to control Circuit CA of the data set. If Bit 1 of Control Register 1 is reset during a transmission then $\overline{\text{RTS}}$ will go high on the falling edge of the transmitter clock that follows the last bit of the current transmission character.
33	$\overline{\text{DATA SET READY}}$	$\overline{\text{DSR}}$	This input appears as Status Bit 6 and generates interrupts when going on or off if DTR is on. It is intended to be derived from Circuit CC of the data set.
34	$\overline{\text{RING INDICATOR}}$	$\overline{\text{RING}}$	This input generates an interrupt when made low with DTR off. It is intended to be derived from Circuit CE of the data set.
35-38	RATES	R1-R4	These four rate inputs are used for 32X-256X Local Transmit and Receive clocks. The rate is selected by the Control Register. (See Note 3.)
39	$\overline{\text{CARRIER DETECTOR}}$	$\overline{\text{CARD}}$	This input appears as Status Bit 5 and generates interrupts when going on or off if DTR is on. It is intended to be derived from Circuit CF of the daa set.
40	POWER SUPPLY	V_{CC}	+5V

* THE WD1931 OUTPUTS, INTRQ, DRQI, and DRQO ARE TRUE HIGH (TRUE= V_{OH}) OUTPUTS. ON THE UC1671, THESE OUTPUTS ARE TRUE LOW (TRUE= V_{OL}) AND OPEN DRAIN.

NOTE 1: If the system design does not make use of $\overline{\text{MISC IN}}$ on the WD1933, the user may tie this to +12V without harm or degradation to the WD1933. This has the same effect as a logic high input. If the system design does make use of $\overline{\text{MISC IN}}$, then provisions must be made to select +12V when the WD1931 is in the socket or $\overline{\text{MISC IN}}$ when the WD1933 is in the socket. This may be accomplished by a small switch or by jumpers.

NOTE 2: The outputs TB0C and RSCLK on the WD1931 may be tied to ground or to +5 volts through a 10K pull-up without harm or degradation to the WD1931.

NOTE 3: If R1-R4 are not selected by the command word in the WD1931, then anything may be on these inputs. If $\overline{\text{RI}}$ and $\overline{\text{CD}}$ are tied high on the WD1933, then the inputs (pins 35-38) may have anything on them. When both the rate fields in the WD1931 and RI and CD on the WD1933 are used, the system designer must make provisions by an external switch or jumpers.

NOTE 4: Pin 1 of the device must **not** be connected in any way to any signal, power or ground line. This pin is the output of an internal Back Bias Generator, and is used for testing only.

ORGANIZATION

The WD1931 block diagram is illustrated on page 1. The primary sections include the control, buffer, status, receiver, transmitter, comparison and sync registers.

Control Registers.

There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the $\overline{DAL}$ lines by a Write operation or read onto the $\overline{DAL}$ lines by a Read operation. The registers are cleared by a Master Reset.

Receiver Holding Register.

This 8-bit parallel buffer register presents assembled receiver characters to the $\overline{DAL}$ bus lines when requested through a Read operation.

Status Register.

This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the $\overline{DAL}$ lines by a Read operation.

DLE Register.

This 8-bit register is loaded from the $\overline{DAL}$ lines by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the WD1931 may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode. This register cannot be read onto the $\overline{DAL}$ lines. It must be loaded with logic zeroes in all unused high-order bits.

SYN Register.

This 8-bit register is loaded from the $\overline{DAL}$ lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding register during transmission. This register cannot be read onto the $\overline{DAL}$ lines. It must be loaded with logic zeroes in all unused high-order bits.

Transmitter Holding Register.

This 8-bit parallel buffer register holds parallel transmitted data transferred from the $\overline{DAL}$ lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Receiver Register.

This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. This incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

Transmitter Register.

This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

Comparator.

The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

Data Access Lines.

The $\overline{DAL}$ is an 8-bit bi-directional bus port over which all data, control, and status transfers occur.

WD1931 OPERATION

Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic zero) at the beginning of a character and a Stop bit (logic one) at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character. If enabled, the parity bit is checked and then stripped off.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is a logic one the character is determined to have correct framing and the WD1931 is prepared to receive the next character. If the Stop bit is a logic zero the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic zero when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic one is determined as

a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (least significant bit first) with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic one) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit may be shortened a maximum of 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-*, or 2-Stop bit selection. To shorten the Stop bit the user must load the Transmitter Holding Register exactly (X+2) 16ths of a bit period before the end of a stop bit transmission, where X= the number of 16ths the user wishes to strip. If X+2 exceeds the maximum then no shortening occurs. This feature does not work in 1X clocking mode.

*NOTE: As a special case, the 1.5 stop bit mode can be shortened from 1/24 to 11/24 of the whole period if the Transmitter Holding Register is loaded (X + 2) 24ths (of the whole period) before the end of the stop bit transmission.

Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, -3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding register. The unused higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Syc Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered, if the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost. New data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE registers are not loaded into the Receiver Holding Register and the DR interrupt is not generated if Bit 3 of Control Register 2 (CR23= SYN Strip) or Bit 4 of Control Register 1 (CR14=DLE Strip) are set respectively. The SYN-DET and DLE-DET status bits are set with the next non-SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter

Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the $\overline{\text{Clear To Send}}$ input is a logic zero. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bits 5=Force DLE and 6=TX Transparent of Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to ensure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic one will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16=0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1=Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the WD1931 is disabled. As soon as the $\overline{\text{CTS}}$ goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

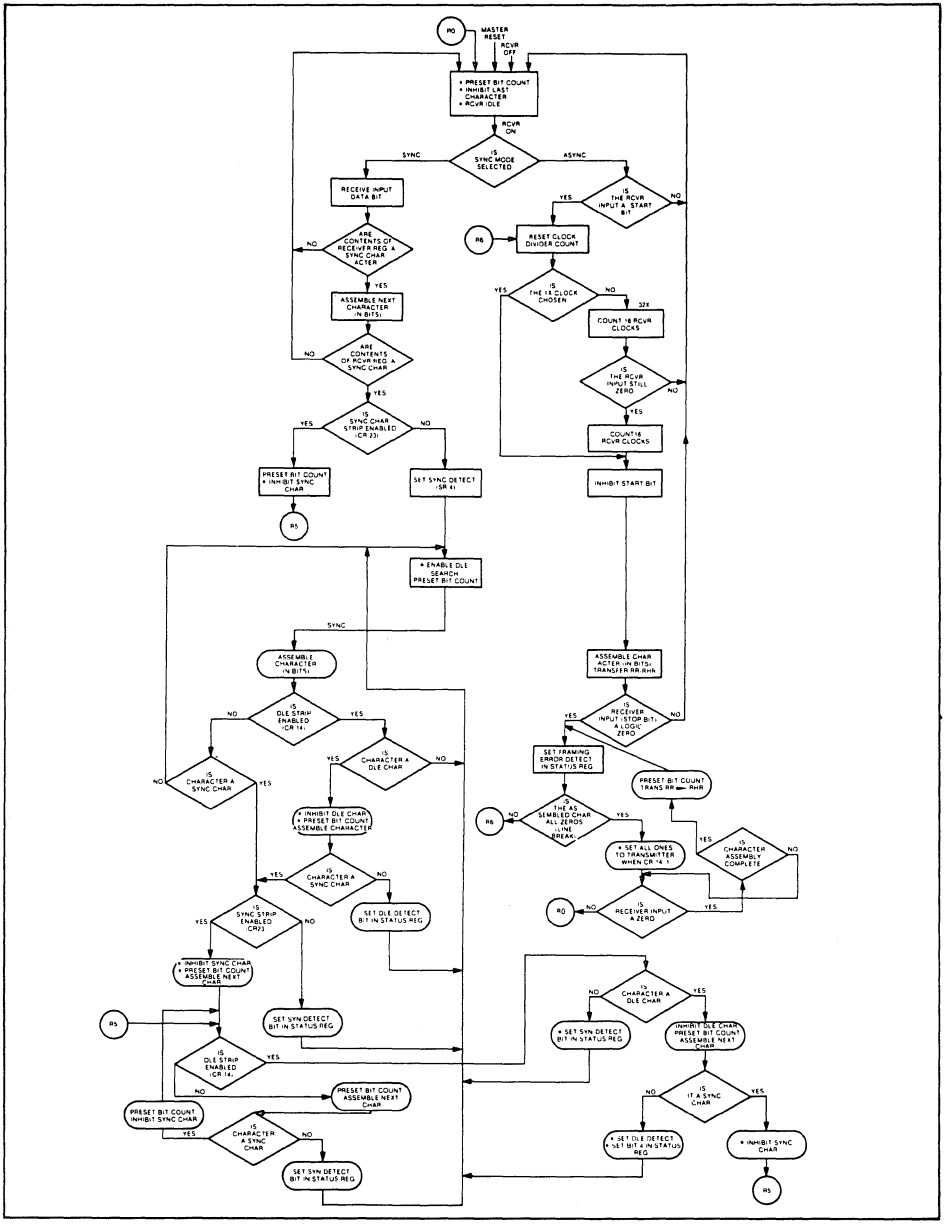
CLOCKING

Two clocking schemes are used. In one case a 1X Receiver Timing and Transmitter Timing are input from a Data Set and are used to clock their respective data. In the second case a local 32X clock is phased to the data and used to clock the data. The device is capable of selecting from four externally supplied rates.

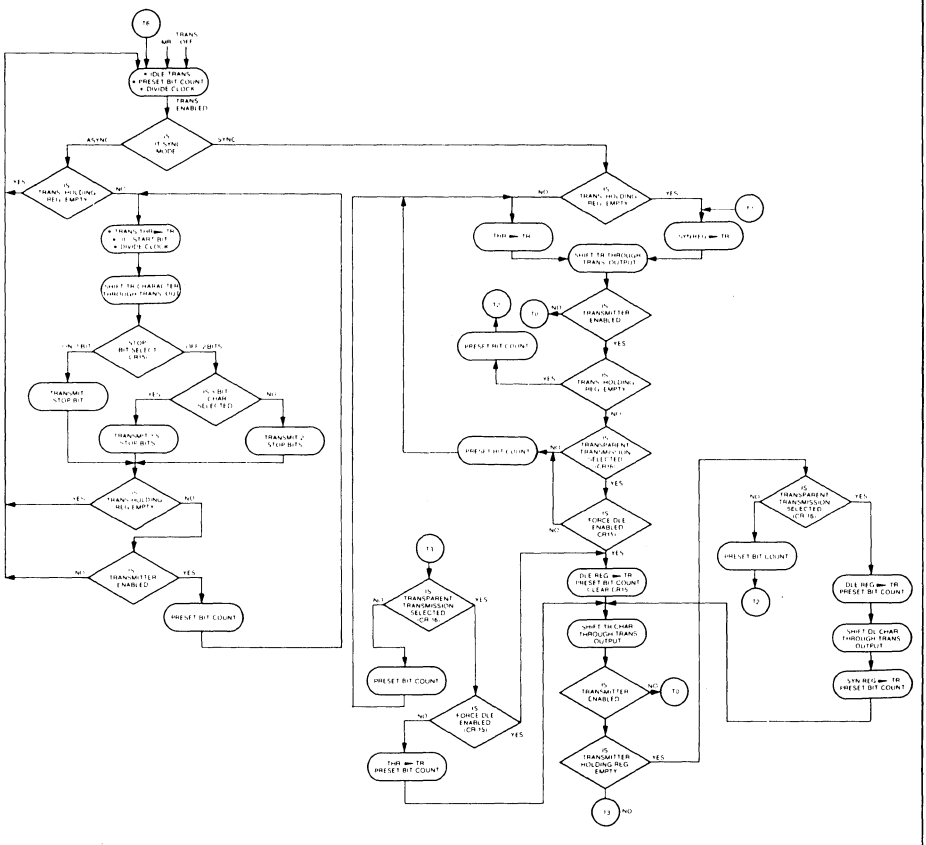
The use of the 1X clock is the same for the receiver and the transmmitter in both the Synchronous and Asynchronous Character modes.

The use of the 32X clock in the receiver differs depending on mode. In the Asynchronous Character mode the receive sampling clock is phased to the mark-space transition of Received Data input at the beginning of the Start bit, causing the Sampling clock to be approximately in the middle of the bit. The accuracy of sampling is +0%, -3%. In the Synchronous Character mode the Receive Sampling clock is phased to all the mark-space transitions on the Received Data input. Each such transition of the data causes an incremental correction of the Sampling clock of 1/32 of the bit period. The Sampling clock can be immediately phased with the data transitions by setting Bit 4 of Control Register 1 to a 1 bit with the receiver disabled. As long as this bit is a one the Sampling clock is locked to every mark-space data transition.

The transmitter divides the selected rate input down to the baud rate. This clock is phased to the THRE flag so that character transmission starts within two clocks of the THR loading when the transmitter is idling.



RECEIVER FLOW CHART



TRANSMITTER SECTION (ASYNCHRONOUS)

TRANSMITTER SECTION (SYNCHRONOUS)

TRANSMITTER FLOW CHART

AUTO ECHO FEATURE

The device is capable of serially echoing the received data with a one bit delay when in the Asynchronous mode and the Receiver on. This causes the clocked regenerated received data to be presented to the Transmit Data output rather than the output of the Transmitter Register or a steady marking. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Breaks are not echoed back. When the device detects a Zero Stop bit and a character of all zeroes, the echoing stops and a steady marking is transmitted until such time as normal character reception resumes. Because echoing is taking place during determination of a break condition, a single character of all zeroes (Null character) is echoed when a break is initiated at the terminal. The Echoing is enabled by setting Bit 4 of Control Register 1 to a 1 bit. Echoing does not start until the start of a receive character at a time when the transmitter is idle and $\overline{CTS}$ is zero. If the Transmitter is forced out of the idle mode while a character is being echoed transmission of that character is halted. The Transmitter is idle when CR11 is a zero or the Transmitter is waiting for the THR to be loaded in the Asynchronous mode.

LOOP FEATURE

The device has on-line diagnostic capability. When the Loop Control bit is a zero the data and data set controls are appropriately looped as follows:

- Transmit Data is connected to Receive Data, with the TD output pin held in a MARK condition and the RD input pin disregarded.
- When a 1X clock is selected the TD clock becomes the Receive clock.
- The Data Terminal Ready Control bit is connected to the Data Set Ready input with the $\overline{DTR}$ output pin held in an OFF condition and the $\overline{DSR}$ input pin disregarded.
- The Request To Send Control bit is connected to the Clear To Send and Carrier inputs, with the $\overline{CTS}$ output pin held in an OFF condition and the $\overline{CTS}$ and $\overline{CARD}$ input pins disregarded.
- $\overline{MISCELLANEOUS}$ Pin is held in an OFF condition.

INPUT/OUTPUT OPERATIONS

All data, control, and status information is transferred to DAL pins. Control and address lines provide for controlling the addressing, input and output operations. In addition other lines provide interrupt capability for alerting a controller that input/output is required. Input/output terminology is referenced to the controller; therefore, a Read or Input takes data from the device and places it on the DAL, while a Write or Output places data from the DAL into the device.

READ

A read operation is initiated when $\overline{CS}$ and $\overline{RE}$ go low. When the Read Enable ($\overline{RE}$) line goes low, the device gates the contents of the addressed register onto the DAL. The device becomes unselected when the $\overline{CS}$ and $\overline{RE}$ are both high. When the Receiver Holding Register is read, the DR Status bit is cleared to zero.

WRITE

A Write operation is initiated when $\overline{CS}$ and $\overline{WE}$ go low. When the Write Enable ($\overline{WE}$) line goes low, the device gates the data from the DAL into the addressed register. When the $\overline{CS}$ and $\overline{WE}$ go high the device becomes unselected. If the Transmitter Holding Register is written into, the THRE Status bit is cleared to zero.

The 10 address is used to load both the SYN and DLE Registers. After writing into SYN the device is conditioned to write into DLE if followed by another Write to that address. Any intervening Read or Write to other addresses reset this condition so that SYN will be addressed with 10.

$\overline{A0}$ and $\overline{A1}$ address device registers for Read/Write operations are shown:

REGISTER ADDRESS FOR READ/WRITE OPERATIONS

A1	A0	Read	Write
F	F	Control Register 1	Control Register 1
F	T	Control Register 2	Control Register 2
T	F	Status Register	SYN & DLE Register
T	T	Receiver Holding Register	Transmitter Holding Register

T = V_{IL} at pin
F = V_{IH} at pin

DEVICE PROGRAMMING

Programming of the WD1931 is done via two Control Registers, one Status Register, a SYN/DLE Register, and the Transmit and Receive Holding Registers. The two Control Registers are referred to as CR1 and CR2. The bits within CR1 are referred to as CR10 through CR17, and the bits within CR2 are referred to as CR20 through CR27. For any register bit 0 is the LSB.

Two general modes of operation exist for the WD1931, Asynchronous and Synchronous. Both modes of operation are discussed separately. BI-SYNC is a special case of Synchronous mode and is not treated separately.

Figures 4 through 6 show CR1, CR2, and the Status Register bit definitions. The meaning of each bit in each register is described twice: once for Asynchronous mode and again for Synchronous mode. The figures combine and summarize both modes.

ASYNCHRONOUS MODE

Control Register 1

Bit	Name	Function
0	DATA TERMINAL READY	Controls $\overline{\text{DATA TERMINAL READY}}$ output on Pin 17 for control of data set circuit CD. When set to a 1 bit, it enables Carrier and Data Set Ready interrupts. When set to a 0 bit, only the Ring interrupt is enabled.
1	REQUEST TO SEND	Controls $\overline{\text{REQUEST TO SEND}}$ output on Pin 32 for control of data set circuit CA. This bit must be a 1 bit and the $\overline{\text{CLEAR TO SEND}}$ input must be low for the transmitter to be enabled and for THRE interrupts to be generated. When this bit is set to a 0 bit the Transmitter is disabled and the $\overline{\text{RTS}}$ output turned off, but not till the end of any current character being transmitted. The $\overline{\text{RTS}}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	RECEIVER ENABLE	When set to a 1 bit, it enables the receiver allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3 and 4 to be updated, and Data Received interrupt to be generated. When set to a 0 bit, the above status bits are cleared. After this bit is set, character reception starts with the first bit after a valid start bit.
3	PARITY ENABLE	When set to a 1 bit, it enables check of parity on received characters and generation of parity for transmitted characters.
4	ECHO MODE	When set to a 1 bit and the RECEIVER is enabled, the clocked regenerated data is presented to the Transmitted Data output. The transmitter does not have to be enabled.
5	STOP BIT SELECTION/MISCELLANEOUS	When set to a 1 bit with the transmitter enabled it causes a single stop bit to be transmitted. When set to a 0 bit, it causes two stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1.5 stop bits for a character length of 5 bits. When the transmitter is not enabled this bit controls the $\overline{\text{MISCELLANEOUS}}$ output on Pin 5 to be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.
6	BREAK	When set to a 1 bit and the transmitter is enabled the Transmitted Data is held in a spacing condition starting with the end of any current character. Normal transmitter timing continues so that the break can be timed out by loading characters into the THR, i.e., interrupts are generated and the transmitter operates normally except for the output which remains low while this bit is a one.
7	LOOP/NORMAL	When this bit is set to a 0 bit, the device is configured to provide an internal data and control loop and the Ring interrupt is disabled. When this bit is set to a 1 bit the device is in normal full duplex configuration and the Ring interrupt is enabled.

Control Register 2

Bit	Name	Function
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — Transmit and Receive clock input (1X) 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 ÷ 2 (32X) (64X) 6 — Rate 4 ÷ 4 (32X) (128X) 7 — Rate 4 ÷ 8 (32X) (256X)
3	ALTERNATE RX CLOCK	A 0 bit selects Rate 1 as the Receiver clock rate and a 1 bit provides the same rate as Transmit. This bit must be a 1 bit if 1X clocking is selected in bits 2-0.
4	PARITY ODD/EVEN	A 1 bit selects Odd Parity and a 0 bit selects Even Parity, when Parity is enabled.
5	CHARACTER MODE	A 0 bit selects Asynchronous Character Mode. A 1 bit selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows: 0-8 bits 1-7 bits 2-6 bits 3-5 bits

SYNCHRONOUS MODE

Control Register 1

Bit	Name	Function
0	DATA TERMINAL READY	Controls $\overline{\text{DATA TERMINAL READY}}$ output on Pin 17 for control of data set circuit CD. When set to a 1 bit, it enables Carrier and Data Set Ready interrupts. When set to a 0 bit only the Ring interrupt is enabled.
1	REQUEST TO SEND	Controls $\overline{\text{REQUEST TO SEND}}$ output on Pin 32 for control of data set circuit CA. This bit must be a 1 bit and the $\overline{\text{CLEAR TO SEND}}$ input must be low for the transmitter to be enabled and for THRE interrupts to be generated. When this bit is set to a 0 bit the Transmitter is disabled and the $\overline{\text{RTS}}$ output turned off, but not till the end of any current character being transmitted. The $\overline{\text{RTS}}$ output may be used for other functions such as "Make Busy" on 103 data sets.
2	RECEIVER ENABLE	When set to a 1 bit, it enables the receiver allowing received characters to be placed in the Receiver Holding Register, Status Bits 1, 2, 3, and 4 to be updated, and the Data Received interrupt to be generated. When set to a 0 bit, the above status bits are cleared. After this bit is set, character reception starts with a Start bit when in the asynchronous mode, or with two matches to the contents of SYN Register when in the synchronous mode.

Control Register 1 (Sync Mode continued)

Bit	Name	Function
3	PARITY ENABLE	When set to a 1 bit, it enables check of parity on received characters only.
4	DLE STRIP/MISCELLANEOUS	When set to a 1 bit and the receiver is enabled, received characters which match the contents of the DLE Register are stripped out. Also parity checking is disabled. When the receiver is not enabled this bit controls the MISCELLANEOUS output on Pin 5 to be used for New Sync on a 201 Data Set. When operating with a 32X clock for 1 bit with the receiver not enabled causes the receiver bit timing to synchronize on mark-space transitions.
5	TX PARITY ENABLE/FORCE DLE	When set to a 1 bit with Bit 6 of Control Register 1 a 0 bit Transmit Parity is enabled, otherwise no parity is generated. When set to a 1 bit with Bit 6 a 1 bit, it causes the contents of the DLE Register to be transmitted prior to the next character loaded in the Transmitter Holding Register. (See description of Transparency below.)
6	TX TRANSPARENT	When a 1 bit of the transmitter is conditioned for transparent transmission which implies that idle fill will be DLE-SYN and a DLE can be forced ahead of any character in the THR by use of Bit 5. (See description of Transparency.)
7	LOOP/NORMAL	When this bit is set to a 0 bit, the device is configured to provide an internal data and control loop (see Loop feature) and the Ring interrupt is disabled. When this bit is set to a 1 bit the device is in normal full duplex configuration and the Ring interrupt is enabled.

Control Register 2

Bit	Name	Function
2-0	CLOCK SELECT	Selects Transmit and Receive clock as follows: 0 — Transmit and Receive clock input (1X) 1 — Rate 1 (32X) 2 — Rate 2 (32X) 3 — Rate 3 (32X) 4 — Rate 4 (32X) 5 — Rate 4 ÷ 2 (32X) (64X) 6 — Rate 4 ÷ 4 (32X) (128X) 7 — Rate 4 ÷ 8 (32X) (256X)
3	STRIP SYN	When set to a 1 bit and the receiver is enabled, received characters which match the contents of the SYN Register are stripped out. Also the SYN status bit is set with the next character. No SYN stripping occurs with a 0 bit.
4	PARITY ODD/EVEN	A 1 bit selects Odd Parity and a 0 bit selects Even Parity, when parity is enabled.
5	CHARACTER MODE	A 0 bit selects Asynchronous Character Mode. A 1 bit selects Synchronous Character Mode.
7-6	CHARACTER LENGTH	Selects number of bits per character as follows: 0-8 bits 1-7 bits 2-6 bits 3-5 bits

TRANSPARENCY

The Transmit Transparency mode causes Idle Fill to be the pair of characters DLE-SYN rather than a single SYN, and provides for preceding a character loaded into the THR with a DLE without the possibility of an intervening DLE-SYN fill. Transparency is enabled by Bit 6 of Control Register 1, which allows force DLE to be controlled by Control Register 1, Bit 5, but the DLE-SYN fill is not activated until after the first forced DLE. All aspects of Transparency are disabled when Bit 6 is set to a 0 bit. When forcing transmission of a DLE, Bit 5 should be set to a 1 bit prior to loading the Transmitter Holding Register, otherwise the character in the Transmitter Holding Register may be transferred to the Transmitter Register prior to the setting of the Control Bit.

STATUS

The Status Register contains the following status information:

Bit	Name	Function
0	TRANSMITTER HOLDING REGISTER EMPTY (THRE)	This bit is a 1 bit when the Transmitter Holding Register does not contain a character and the transmitter is enabled. It is set to a 1 bit when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the transmitter is disabled.
1	DATA RECEIVED (DR)	This bit is set to a 1 bit when the Receiver Holding Register is loaded from the Receiver if the Receiver is enabled. It is cleared to a 0 bit when the Receiver Holding Register is read onto the DAL, or when the receiver is disabled.
2	OVERRUN ERROR (OE)	This bit is set to a 1 bit when the previous character in the Receiver Holding Register has *not* been read, causing DR to not be reset, at the time a new character is ready to be transferred to the Receiver Holding Register; otherwise the bit is cleared when a character is transferred to the Receiver Holding Register. It is cleared when the receiver is disabled.
3	PARITY ERROR/DLE DETECT	This bit is set to a 1 bit when the receiver and Receive parity are enabled and the last received character has a parity error, and is set to a 0 bit if the character has correct parity. When the DLE strip is enabled the Receive parity check is disabled and this bit is set to a 1 bit if the *previous character* matched the contents of the DLE Register and was stripped, otherwise it is set to a 0 bit. This bit is cleared when the receiver is disabled. When a SYN or DLE character is stripped this bit cannot be reset.
4	FRAMING ERROR (FE)/SYN DETECT (SD)	In the asynchronous mode this bit is set to a 1 bit if the bit after the last data bit of a synchronous character is a zero and the receiver is enabled. The Status bit is set to a 0 bit if the bit is a one. In the synchronous mode this bit is set to a 1 bit when the contents of the Receiver Register matches the contents of the SYN Register and SYN strip is not enabled. In both modes the bit is cleared when the receiver is disabled. If SYN strip is enabled this status bit is updated with the character received after the SYN character. When a SYN or DLE character is stripped this bit cannot be reset.
5	CARRIER DETECTOR	This bit is the complement of the Carrier Detector input on Pin 39.
6	DATA SET READY	This bit is the complement of the Data Set Ready input on Pin 33. With 202-type data sets it can be used for Secondary Receive.
7	DATA SET CHANGE	This bit is set to a 1 bit when there is a change in the state of the Data Set Ready or Carrier Detector inputs with DTR on, or the Ring indicator is turned on with DTR off. This bit is cleared when the Status Register is read onto the DAL.

Control Registers 1, 2 and STATUS Bit Assignments for TRUE DATA BUS, Invert for FALSE DATA BUS.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SYNC/ASYNC 0 – LOOP MODE 1 – NORMAL MODE	**ASYNC** 0 – NON BREAK MODE 1 – BREAK MODE **SYNC** 0 – NON TRANSMITTER TRANSPARENT MODE 1 – TRANSMIT TRANSPARENT MODE	**ASYNC (TRANS. ENABLED)** 0 – 1½ OR 2 STOP BIT SELECTION 1 – SINGLE STOP BIT SELECTION **ASYNC (TRANS. DISABLED)** 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0 **SYNC (CR16 = 0)** 0 – NO PARITY GENERATED 1 – TRANSMIT PARITY ENABLED **SYNC (CR16 = 1)** 0 – NO FORCE DLE 1 – FORCE DLE	**ASYNC** 0 – NON ECHO MODE 1 – AUTO ECHO MODE **SYNC (CR12 = 1)** 0 – DLE STRIPPING NOT ENABLED 1 – DLE STRIPPING ENABLED **SYNC (CR12 = 0)** 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0	**ASYNC** 0 – NO PARITY ENABLED 1 – PARITY CHECK ENABLED ON RECEIVER. PARITY GENERATION ENABLED ON TRANSMITTER **SYNC** 0 – RECEIVER PARITY CHECK IS DISABLED 1 – RECEIVER PARITY CHECK IS ENABLED	**SYNC/ ASYNC** 0 – RECEIVER DISABLED 1 – RECEIVER ENABLED	**SYNC/ ASYNC** 0 – SETS $\overline{\text{RTS}}$ OUT = 1 1 – SETS $\overline{\text{RTS}}$ OUT = 0	**SYNC/ ASYNC** 0 – SETS $\overline{\text{DTR}}$ OUT = 1 1 – SETS $\overline{\text{DTR}}$ OUT = 0

CONTROL REGISTER 1

BIT 7 6	BIT 5	BIT 4	BIT 3	BIT 2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	**MODE SELECT** 0 – ASYNCHRONOUS MODE 1 – SYNCHRONOUS MODE	**SYNC/ASYNC** 1 – ODD PARITY SELECT 0 – EVEN PARITY SELECT	**ASYNC** 1 – RECEIVER CLOCK DETERMINED BY BITS 2-0 0 – RECEIVER CLK = RATE 1 **SYNC** 0 – NO SYN STRIP 1 – SYN STRIP	**SYNC/ASYNC** CLOCK SELECT 000 – 1X CLOCK 001 – RATE 1 CLOCK 010 – RATE 2 CLOCK 011 – RATE 3 CLOCK 100 – RATE 4 CLOCK 101 – RATE 4 CLOCK ÷ 2 110 – RATE 4 CLOCK ÷ 4 111 – RATE 4 CLOCK ÷ 8

CONTROL REGISTER 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA SET CHANGE	DATA SET READY	CARRIER DETECTOR	FRAMING ERROR SYN DETECT	DLE DETECT PARITY ERROR	OVERRUN ERROR	DATA RECEIVER	TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

Reg	A1	A0	Read	Write
0	0	0	Control Register 1	Control Register 1
1	0	1	Control Register 2	Control Register 2
2	1	0	Status Register	SYN & DLE Register
3	1	1	Receiver Holding Register	Transmitter Holding Register

INTERRUPTS

The following interrupts can be generated.

Carrier On

The Carrier On interrupt occurs when the Carrier Detector input goes low and DTR is on.

Carrier Off

The Carrier Off interrupt occurs when the Carrier Detector input goes high and DTR is on.

DSR On

The DSR On interrupt occurs when the Data Set Ready input goes low and DTR is on.

DSR Off

The DSR Off interrupt occurs when the Data Set Ready input goes high and DTR is on.

Ring On

The Ring On interrupt occurs when the Ring input goes low and DTR is off.

When an interrupt condition exists the INTR output is made high. Reading the Status Register or MR will allow INTR to go high again.

DATA BUS CONTROLS

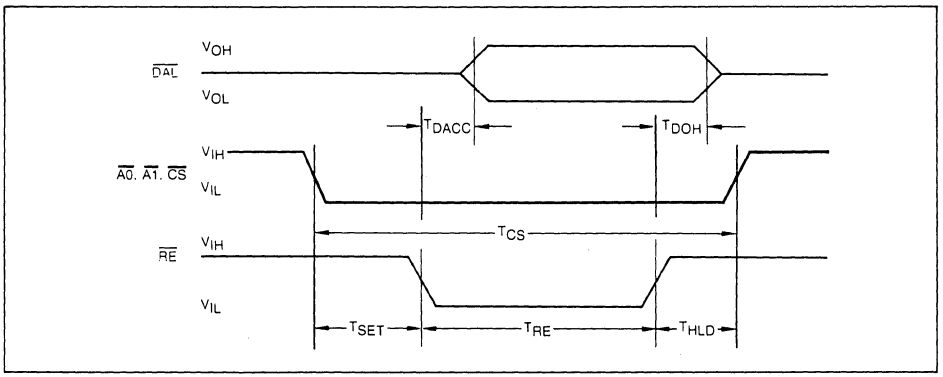
The following Data Bus controls can be generated.

Data Request Out

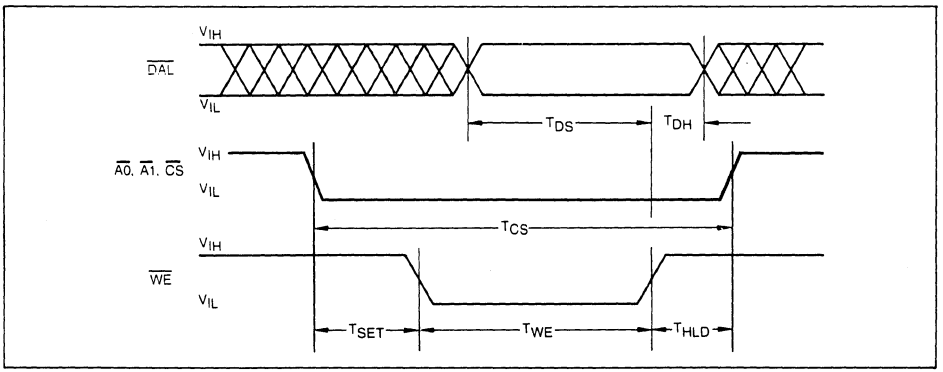
This control signal occurs when the THR is empty while the transmitter is enabled.

Data Request In

This control signal occurs when the RHR is full while the receiver is enabled.



READ TIMING



WRITE TIMING

MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+15 to −0.3V	Storage Temp. Ceramic	-65°C to +150°C
Max. Voltage to any Input with Respect to V_{SS}	+20 to −0.3V	Plastic	-55°C to +125°C
Operating Temperature	0°C to 70°C		
Power Dissipation	600 mW		

OPERATING CHARACTERISTICS

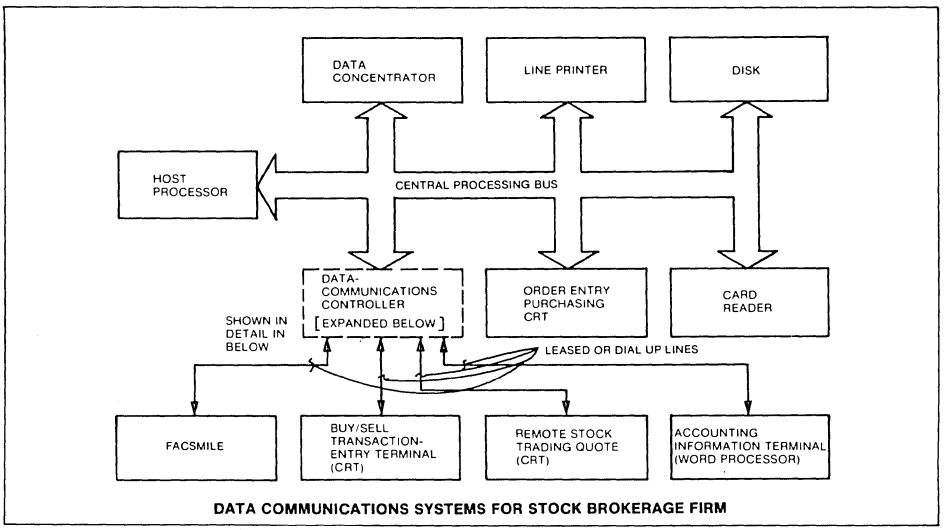
T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{CC} = +5.0V ±.25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	uA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	uA	$V_{OUT} = V_{CC}$
$I_{CC_{AVE}}$	V_{CC} Supply Current			80	mA	
$I_{DD_{AVE}}$	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 uA
V_{OL}	Output Low Voltage			.45	V	I_O = 1.6 mA

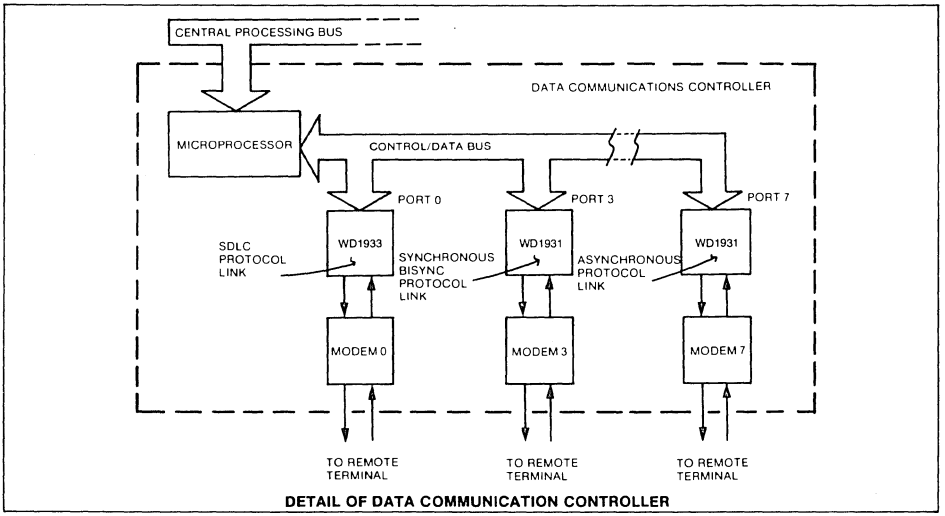
AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ±0.6V, V_{SS} = 0V, V_{CC} = +5.0 ±.25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{HLD}	A0, A1 & CS Hold Time	5			ns	
T_{CS}	A0, A1 & CS Width	495			ns	
T_{SET}	A0, A1 & CS Set-Up Time	240			ns	
T_{CYCLE}	Cycle Time	1000			ns	
T_{LOW}	A0, A1 & CS Low Time	250			ns	
T_{MR}	MR Pulse Width	450			ns	
READ						
T_{RE}	$\overline{RE}$ Width	250			ns	
T_{DACC}	Data Access from $\overline{RE}$			300	ns	CL = 25 pf
T_{DOH}	Data Hold from $\overline{RE}$	50		150	ns	CL = 25 pf
WRITE						
T_{WE}	$\overline{WE}$ Width	250			ns	
T_{DS}	Data Set-Up Time	250			ns	
T_{DH}	Data Hold Time	100			ns	



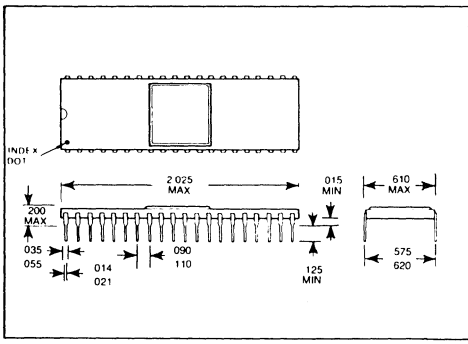
DATA COMMUNICATIONS SYSTEMS FOR STOCK BROKERAGE FIRM



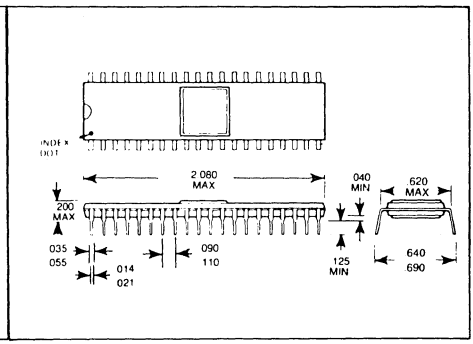
DETAIL OF DATA COMMUNICATION CONTROLLER

DIGITAL COMMUNICATIONS SYSTEM

The diagrams above illustrate a typical digital system employing several processing levels and digital protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located respectively in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers. The exploded diagram of the Data-Communications Controller exemplifies the use of one common circuit board design with one 40-pin socket. When the Port requires a character-oriented protocol (synchronous, asynchronous, or synchronous-bisync), the WD1931 is plugged into the socket. For SDLC, HDLC or ADCCP, theWD1933 is used. In addition to storing the design cycle, system flexibility and cost savings are achieved.



WD1931A CERAMIC PACKAGE



WD1931B PLASTIC PACKAGE

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