WESTERN DIGITAL
CORPORATION

WD1983 (BOART)
BUS ORIENTED ASYNCHRONOUS RECEIVER/TRANSMITTER

FEATURES

ASYNCHRONOUS MODE

- FULL DUPLEX OPERATION
- SELECTABLE 5,6,7, & 8 BIT CHARACTERS
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, or 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- OVERRUN AND FRAMING ERROR DETECTION
- DC TO 36K BITS/SEC (16X)
- DC TO 600K BITS/SEC (1X)
- 8251/8251A ASYNCHRONOUS ONLY REPLACEMENT
- REQUIRES NO ASYNCHRONOUS SYSTEM CLOCK
- 28 PIN PLASTIC OR CERAMIC
- +5 VOLT ONLY

SYSTEM COMPATIBILITY

- DOUBLE BUFFERING OF DATA
- 8 BIT BI-DIRECTIONAL BUS FOR DATA, STATUS, AND CONTROL WORDS
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- CHIP SELECT, $\overline{RE}$, $\overline{WE}$, C/$\overline{D}$ INTERFACE TO CPU
- ON-LINE DIAGNOSTIC CAPABILITY
- THREE STATE DATA BUS

BAUD RATE-DC TO 36K BITS/SEC (16X)
SELECTABLE CLOCK RATES

- 1X, 16X, 64X, BAUD RATE CLOCK INPUTS
- UP TO 47% DISTORTION ALLOWANCE WITH 64X CLOCK

APPLICATIONS

ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL INTERFACE

GENERAL DESCRIPTION

The WD1983 is an N channel silicon gate MOS/LSI device that interfaces a digital asynchronous channel with a parallel channel. It is available in a ceramic or plastic standard 28 pin dual in line package.

The WD1983 is a fully programmable microprocessor I/O peripheral with two control registers and a status register. It is capable of full duplex operations.

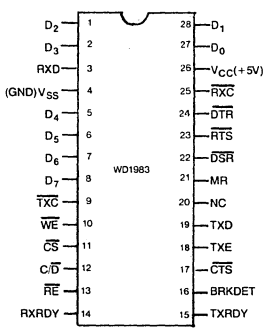


FIGURE 1 WD1983 PIN-OUT

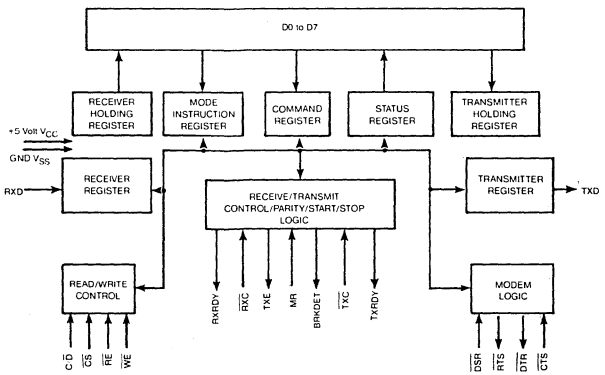


FIGURE 2 WD1983 BLOCK DIAGRAM

PIN. NO.	PIN NAME	SYMBOL	FUNCTION
4	POWER GND	VSS	Ground
26	POWER SUPPLY	VCC	+5 Volts
11	CHIP SELECT	$\overline{CS}$	This input, when low, enables READ or WRITE operations.
13	READ ENABLE	$\overline{RE}$	This input, when low, accesses the contents of the addressed register.
10	WRITE ENABLE	$\overline{WE}$	This input, when low, writes the data on the DATA BUS into the addressed register.
21	MASTER RESET	MR	This input, when high, initializes the device and clears the COMMAND and MODE REGISTERS.
12	CONTROL/DATA	C/$\overline{D}$	This input selects the CONTROL or DATA register. It is used in conjunction with a READ or WRITE enable.
19	TRANSMIT DATA	TXD	This output is the transmit serial data. When no data is being transmitted or after MASTER RESET, this output is high (a marking condition). COMMAND CONTROL word bit 3 is used to program a break condition by forcing the TXD output to a low (spacing condition).
9	TRANSMIT CLOCK	$\overline{TXC}$	This input is the source clock for transmission. MODE INSTRUCTION word bits MR0 & MR1, control 1X, 16X, or 64X, times the transmitted bit rate.
18	TRANSMIT EMPTY	TXE	This output is set high after MASTER RESET and is automatically reset when a character is written into the TRANSMITTER HOLDING REGISTER. It returns high at the end of a transmitted character indicating the end of transmission if the TRANSMIT HOLDING REGISTER has not been loaded.
15	TRANSMIT READY	TXRDY	This output is set high after MASTER RESET. It indicates that the transmitter is ready to accept a character and is automatically reset whenever a character is written into the TRANSMITTER HOLDING REGISTER.

PIN NO.	PIN NAME	SYMBOL	FUNCTION
3	RECEIVE DATA	RXD	This input is the received serial data.
25	RECEIVE CLOCK	$\overline{RXC}$	This input is the receiver clock. MODE INSTRUCTION word bits MR0 & MR1 control whether this input is 1X, 16X or 64X times the received bit rate.
14	RECEIVER READY	RXRDY	This output is set low after MASTER RESET. When set high it indicates that the receiver has assembled a character and transferred it to the RECEIVER HOLDING REGISTER. It is automatically reset when the RECEIVER HOLDING REGISTER is read.
16	BREAK DETECT	BRKDET	This output is reset after MASTER RESET. It is set high when the receiver detects a string of zeros equal to the programmed character length including start, parity and stop bits. Upon detecting a valid one data bit it's reset. Assembly of the next character is begun after detecting a valid start bit.
17	CLEAR TO SEND	$\overline{CTS}$	This input is set low to enable the transmitter. When set high it disables transmission. If the transmitter is transmitting a character, it will terminate transmission after the TRANSMITTER REGISTER is empty.
24	DATA TERMINAL READY	$\overline{DTR}$	This is a general purpose output which is set and cleared by COMMAND word bit CR1. It is reset after MASTER RESET.
23	REQUEST TO SEND	$\overline{RTS}$	This is a general purpose output which is set and cleared by COMMAND word bit CR5. It is reset after MASTER RESET.
1, 2, 5, 6, 7, 8, 27, 28	DATA BUS	D0 THRU D7	These are input/output pins. Data on the DATA BUS is written into the selected register during a WRITE operation. During a READ operation, the DATA BUS is driven by data in the selected register. When not selected, ($\overline{CS}$ high), these pins are in a high impedance state.
22	DATA SET READY	$\overline{DSR}$	This is a general purpose input which is sensed in STATUS REGISTER bit #7.
20		NC	No internal connection, pin not used.

ORGANIZATION

The WD1983 Block Diagram is illustrated on Page 1. The WD1983 (BOART) is an eight bit bus-oriented device. Communication between the BOART and the controlling CPU occurs via the 8 bit DATA BUS. There are 2 accessible DATA REGISTERS, which buffer Transmit and Receive DATA. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register (the TRANSMIT REGISTER) and a serial-to-parallel shift register (the RECEIVE REGISTER).

Operational control and monitoring of the BOART is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A READ/WRITE control circuit allows monitoring/programming or reading/loading in the CONTROL, STATUS or HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$) and Control or Data Select (C/$\overline{D}$).

Internal control of the BOART is by means of two internal MICROCONTROLLERS; one for transmit and one for receive. The CONTROL REGISTERS, MODEM CONTROL LOGIC, READ/WRITE CONTROL LOGIC and various counters provide inputs to the MICROCONTROLLERS, which generate the necessary control signals to send and receive serial data according to the programmed asynchronous format.

READ/WRITE OPERATIONS

The WD1983 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.

The WD1983 registers are accessed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	REGISTERS SELECTED
L	L	L	H	Read RECEIVE HOLDING REGISTER
L	L	H	L	Write TRANSMIT HOLDING REGISTER
L	H	L	H	Read STATUS REGISTER
L	H	H	L	Write CONTROL REGISTER
H	X	X	X	DATA BUS tri-stated

Note: "L" means V_{IL} at pins
"H" means V_{IH} at pins
"X" means don't care

OPERATING DESCRIPTION

The WD1983 (BOART) is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, C/$\overline{D}$, $\overline{RE}$ and $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. The appropriate $\overline{TXC}$ and $\overline{RXC}$ clock frequencies should be selected for the particular application using a programmable baud rate generator such as the BR1941.

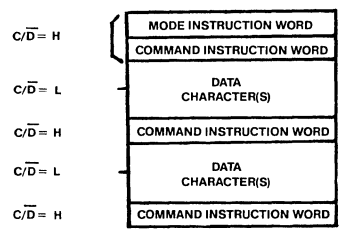
For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, TXE and BRKDET Flags may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support BOART operations.

MODEM CONTROL SIGNALS can be configured several ways as the $\overline{DTR}$, $\overline{RTS}$ and $\overline{DSR}$ signals are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS. The $\overline{CTS}$ input is used to synchronize the transmitter to external events.

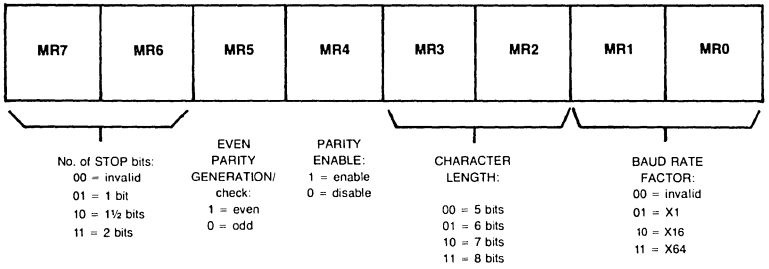
The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A break character is defined as a start bit, and all zero data, parity and stop bits). When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last word is transmitted.

The receiver is equipped with logic to look for a break character. When a break character is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to logic "1". When the receiver input line goes high again for the least "one data bit time," the receiver resets the BREAK DETECT FLAG and resumes its search for a start bit.



TYPICAL DATA BLOCK TRANSFER

MODE INSTRUCTION CONTROL WORD FORMAT



COMMAND INSTRUCTION CONTROL WORD FORMAT

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
DON'T CARE	INTERNAL RESET (IR) 1 = returns WD1983 to mode instruction word format	REQUEST TO SEND ($\overline{RTS}$): 1 = forces $\overline{RTS}$ output low 0 = forces $\overline{RTS}$ output high	ERROR RESET (ER): 1 = resets PE, OE & FE error flags 0 = normal operation	SEND BREAK CHARACTER (SBRK): 1 = forces TXD output low 0 = normal operation	RECEIVE ENABLE (RXE): 1 = enable receiver 0 = disable receiver	DATA TERMINAL READY ($\overline{DTR}$): 1 = forces $\overline{DTR}$ output low 0 = forces $\overline{DTR}$ output	TRANSMIT ENABLE TXEN: 1 = enable transmitter 0 = disable transmitter

STATUS WORD FORMAT

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{DSR}$ (SEE NOTE)	BRKDET (SEE NOTE)	FRAMING ERROR (FE): 1 = invalid stop bit detected at the end of the character 0 = No framing error detected (Reset by CR4)	OVERRUN ERROR (OE): 1 = CPU did not read the character before the next one became available 0 = No overrun error detected (Reset by CR4)	PARITY ERROR (PE): 1 = parity error detected 0 = No Parity error detected (Reset by CR4)	TXE (SEE NOTE)	RXRDY (SEE NOTE)	TXRDY (SEE NOTE)

FE, OE & PE FLAGS DO NOT INHIBIT OPERATION. THESE FLAGS ARE STATUS ONLY.

NOTE:
SR0, SR1, SR2, SR6, and SR7 HAVE IDENTICAL MEANINGS AS THE EXTERNAL OUTPUT PINS.

ABSOLUTE MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground)	+ 15 to −0.3V	Storage Temp.	
Max. Voltage to any Input with Respect to V_{SS}	+ 20 to −0.3V	Ceramic -65°C to +150°C	('E' Package)
Power Dissipation	1000 MW	Plastic -55°C to +125°C	('F' Package)

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = + 5.0V ± .25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{DL}	Data Bus Leakage			50	μA	Data Bus is in high impedence state
ICC_{AVE}	V_{CC} Supply Current		45	80	mA	5.25 VDC/f_{CLK} = 600 kHz No Loads.
V_{IH}	Input High Voltage	2.4		0.8	V	
V_{IL}	Input Low Voltage (All Inputs)	−0.3			V	
V_{OH}	Output High Voltage	2.4			V	I_O = − 100μA (source)
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA (sink)

TABLE 1 WD1983 DC CHARACTERISTICS

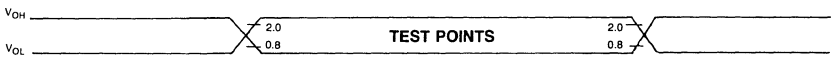


FIGURE 3 INPUT WAVEFORMS FOR AC TESTS

NOTE: ALL WAVEFORMS ARE MEASURED AT 2.0V IF RISING EDGE, AND 0.8V IF FALLING EDGE.

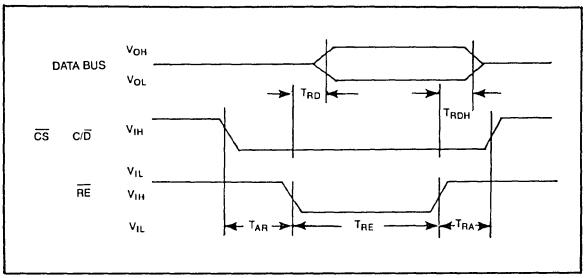


FIGURE 4 READ TIMING

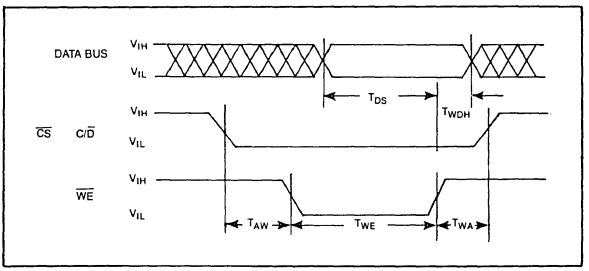


FIGURE 5 WRITE TIMING

NOTE:

8251A COMPATIBILITY

The WD1983 (BOART) is an asynchronous only device, which is compatible with the 8251A. However, in test evaluation and application, the following differences should be noted:

(1) The WD1983 utilizes the transmit and receive baud clocks in their respective internal logic sections instead of the system clock normally applied to Pin 20 on the 8251A. This Pin on the WD1983 is not used.

(2) As a result of the above condition, timings referenced to the system clock period in the 8251A specification are now specified in absolute time units or with respect to the transmit or receive baud clock.

AC Electrical Characteristics
T_A = 0°C to + 70°C; V_{CC} = 5.0 V ± 5%; GND = 0 V

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
BUS PARAMETERS READ CYCLE					
t_{AR}	Address Stable Before $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$ ($\overline{CS}$,C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50pF
		25		ns	C_L = 15pF
WRITE CYCLE					
t_{AW}	Address Stable Before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
OTHER TIMINGS					
t_{DTX}	TXD Delay from Falling Edge of TXC		200	ns	C_L = 100pF
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100pF
t_{HRX}	RX Data Hold Time to Sampling Pulse	100		ns	C_L = 100pF
f_{TX} [1]	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	500		ns	

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
f_{RX}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	500	kHz	
	16X and 64X Baud Rate	DC	600	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	1.0		μs	
	16X and 64X Baud Rate	800		ns	
t_{TX}	TXRDY Delay from Center of Data Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RXRDY Delay from Center of Data Bit		1/2	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
t_{TRD}	TXRDY Delay from Falling Edge of $\overline{WE}$		1	t_{TXC}	
t_{TOD}	TXD Output from Falling Edge of $\overline{WE}$		2	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of $\overline{WE}$ ($\overline{DTR}$, $\overline{RTS}$)		400	ns	
t_{CR}	Control to $\overline{RE}$ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		500	ns	

TABLE 2 WD1983 AC CHARACTERISTICS

At f_{TX} (max), the duty cycle should be 50%. At less than f_{TX} (max), the minimum pulse width for the high or low half is $\frac{1}{2 \bullet f_{TX}(max)}$.
Hence, at frequencies less than f_{TX} (max), the required duty cycle will be less stringout than 50%.

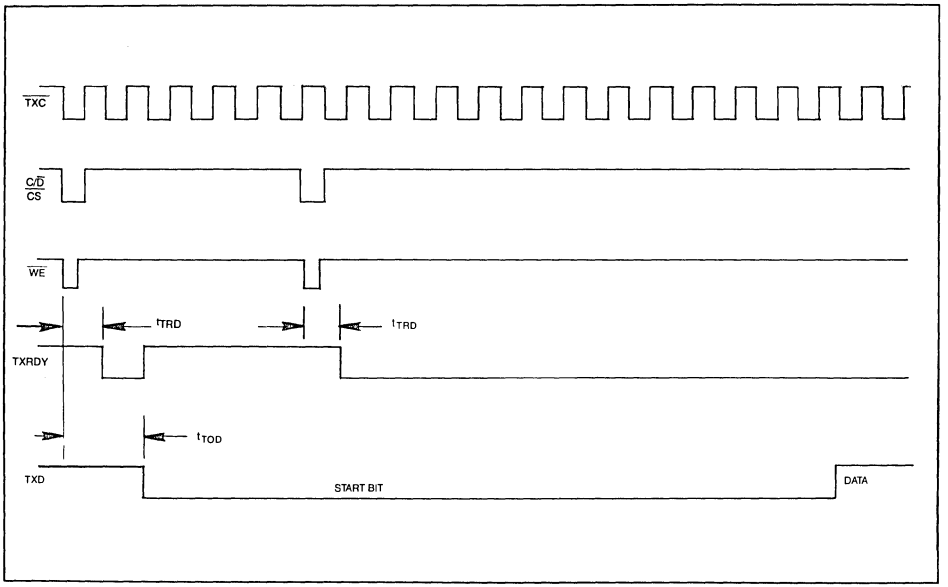


FIGURE 6

TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

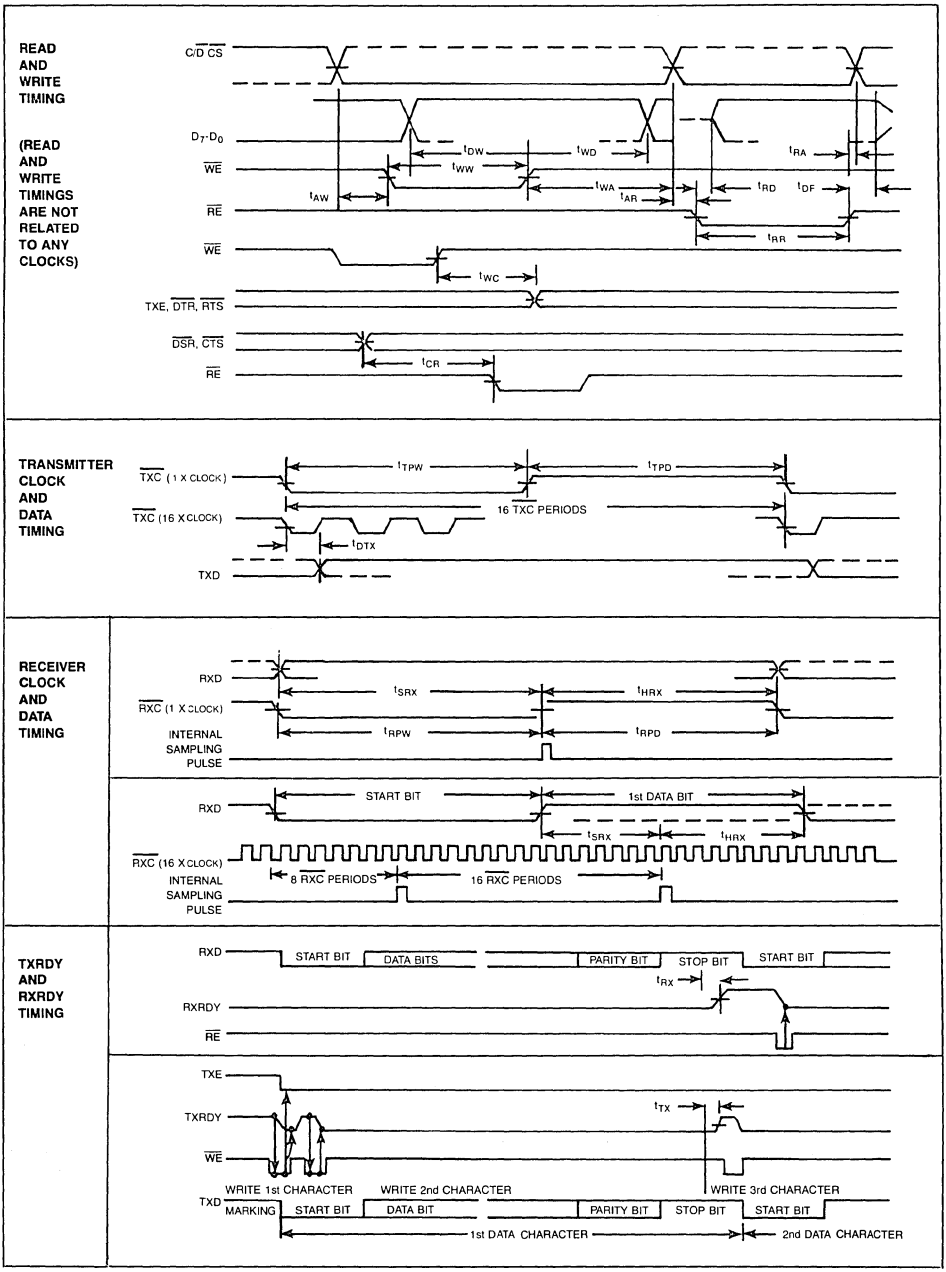
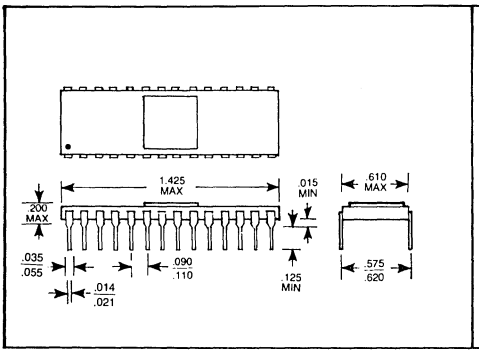
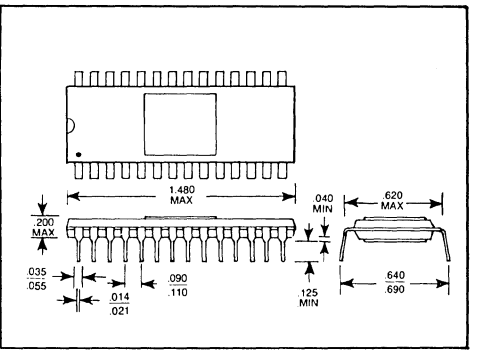


FIGURE 7 SYSTEM TIMING DIAGRAMS



WD1983 E CERAMIC PACKAGE



WD1983 F PLASTIC PACKAGE

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