WESTERN DIGITAL
CORPORATION

WD1984 MULTI-CHARACTER SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

MARCH, 1981

FEATURES

- TWO OPERATING MODES: SYNCHRONOUS & ASYNCHRONOUS
- 1 TO 8 CHARACTERS OF 5, 6, 7, OR 8 BITS PER CHARACTER TRANSMISSION
- SELECTABLE PARITY INSERTION IN OR AFTER LAST BIT OF WORD
- EVEN/ODD PARITY SELECT OR NO PARITY
- DOUBLE BUFFERED RECEIVER & TRANSMITTER
- ASYNCHRONOUS SELECTABLE CLOCK RATES (1x,16x)
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- LINE BREAK GENERATION AND DETECTION (ASYNC MODE)
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 1M BITS/SEC (1x) OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- 28 PIN CERAMIC OR PLASTIC PACKAGE
- TEMPERATURE RANGES 0°C to 70°C, −40°C TO +85°C

INTRODUCTION

The Western Digital WD1984 is designed to handle digital data transmission, according to two protocols. These are the Synchronous and Asynchronous protocols. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception.

The device can be programmed to transmit and receive words that are 1 to 8 characters in length; 5, 6, 7 or 8 bits per character. Error flags and control signals have been provided to broaden the application range of the device. The WD1984 is packaged in a 28 pin plastic or ceramic package and is available in two temperature ranges: Commercial and Industrial.

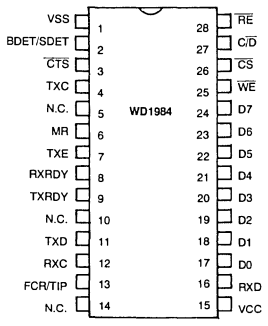


Figure 1 WD1984 PIN-OUT

N.C. No Internal Connection

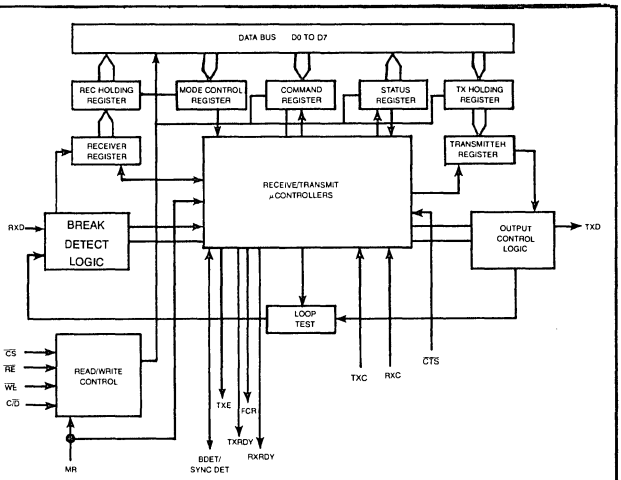


Figure 2 WD1984 BLOCK DIAGRAM

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	BDET/ SDET	BREAK DETECT/ SYNC DETECT	This pin is a bi-directional port. In ASYNC, it is an output, which goes high when the receiver logic detects a break character. In the SYNC mode, it is an input which causes the receiver to begin assembling data bytes as programmed.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ASYNC MODE = 1× or 16× bit rate SYNC MODE = 16× bit rate
5	N.C.		No internal connection.
6	MR	MASTER RESET	When high (V_{IH}), presets the WD1984. The command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1984.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1984 and can be used as an interrupt to the system.

PIN NO.	SYMBOL	SIGNAL NAME	FUNCTION
10	N.C.		
11	TXD	TRANSMIT DATA ONE	This output is the serial data output.
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR/TIP	FIRST CHARACTER READY/TRANSMISSION IN PROGRESS	In the ASYNC mode, this output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	N.C.		
15	VCC	POWER SUPPLY	+5V DC
16	RXD	RECEIVE DATA ONE	This input is the serial data input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1984 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
25	$\overline{WE}$	WRITE ENABLE	When low (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	CHIP SELECT	When low (V_{IL}), the device is selected. This enables communication between the WD1984 and a microprocessor.
27	C/$\overline{D}$	CONTROL/DATA	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	READ ENABLE	When low (V_{IL}), allows the CPU to read data or status information from the WD1984.

GENERAL DESCRIPTION

The WD1984 is a bus-oriented MOS/LSI device designed to provide two data communication protocols:

1. Asynchronous
2. Synchronous

The control registers are used to select the desired protocol and provide programmable format options within each protocol, as outlined below.

The WD1984 contains two control registers needed to specify formal options within each protocol. These registers are the command instruction register and the mode instruction register.

The format options available to the user are:

1) Parity Enable (PEN)
2) Parity Position (PIA)
   The *P*arity bit (when enabled) can either be appended to the data word *A*fter the data bits or it can be *I*nside the data word in the last bit position.
3) Odd or Even Parity Select (EPS)
4) Character Length Select 5, 6, 7 or 8 Bits/Character) (CLS2 and CLS2)

The Asynchronous mode has the option of selecting the number of contiguous characters per transmission and receive sequence. This multicharacter option may facilitate data handling between peripheral devices with a non-standard number of data bits. Therefore, the user can change the mode register to transmit and receive any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character.

Additionally, the Asynchronous mode has two options which determine the operational characteristics of the protocol:

1) Stop Bit Selection—(SPS)
   This control bit selects 1 or 2 stop bits (1 or 1½ bits in 5 bit characters) at the end of the word, which is part of the character delimiting definition.
2) Asynchronous clock rate select (1× or 16× clock rate), which describes resolution and bit rate characteristics.

The WD1984 also contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the $\overline{CTS}$ input must be low ("0"). The status and output flags operate normally.

ORGANIZATION

A block diagram of the WD1984 is shown in figure 1.

As mentioned, the WD1984 is an eight bit bus-oriented device. Communication between the WD1984 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1984 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$) and Control or Data Select ($C/\overline{D}$).

Internal control of the WD1984 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the programmed protocols.

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
EPS	IR	PEN	LTE	TXSM	REN	PIA	TEN

TEN	Transmit ENable
1	Enabled
0	Disabled
PIA	Parity Inside or After
1	After the data word
0	Inside (the last data bit) of word
REN	Receive ENable
1	Enabled
0	Disabled
TXSM	Transmit Space or Mark
1	Send break character (force TXD low)
0	Normal transmitter operation
LTE	Loop Test ENable
1	Local loop-back mode
0	Normal Operation
PEN	Parity ENable *
1	Enabled
0	Disabled
IR	Internal Reset
1	Returns WD1984 to mode instruction format
0	
EPS	Even Parity Select
1	Even parity
0	Odd parity

*Internally disabled in Synchronous mode.

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	BRKDET	FE	OE	PE	TXE	RXRDY	TXRDY

TXRDY	Transmitter Ready
1	Active (THR can be reloaded)
0	Inactive (transmitter is busy)
RXRDY	Receiver Ready
1	Active (RHR should be read)
0	Inactive
TXE	Transmitter Empty
1	Transmitter idle
0	Transmitter active
PE	Parity Error
1	Error reported
0	No error
OE	Overrun Error
1	RHR has been overwritten
0	No error
FE	Framing Error
1	Indicates a framing error has been detected.
0	No error
BRKDET	Break Character Detect
1	In ASYNC mode, this bit indicates the receiver has detected a break character.
0	Inactive
UE	Underrun Error
1	In multi-character transmissions, indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0	No error

The format and definition of the Mode Register is shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
SBS	N3	N2	N1	CLS2	CLS1	MS2	MS1

MS2	MS1	Mode Selected
X	X	Undefined
0	0	Asynchronous mode (16X)
0	1	Asynchronous mode (1X)
1	X	Synchronous mode (16X)

CLS2	CLS1	Character Length Select
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

N3	N2	N1	Characters Per Word Select
0	0	0	1 character
0	0	1	2 characters
0	1	0	3 characters
0	1	1	4 characters
1	0	0	5 characters
1	0	1	6 characters
1	1	0	7 characters
1	1	1	8 characters

SBS	Stop Bit Select
1	2 stop bits (1-1/2 bits in 5 bit characters)
0	1 stop bit

The WD1984 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Control Registers
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
t_{RX}	RxRDY Delay from Center of Data Bit (FCR Delay from Center of Data Bit)		½	R_{RXC}	
	Internal BRKDET Delay from Center of Data Bit		1	t_{RXC}	
	External SynDet Set-up time before rising edge of RXC	200		ns	
	TXEMPTY Delay from Center of Data Bit		½	t_{TXC}	C_L = 50 pF (1 × Rate)

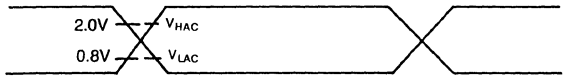


Figure 4 TEST POINTS FOR A.C. TIMING

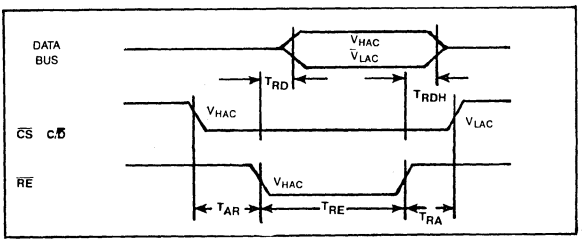


Figure 5 READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V

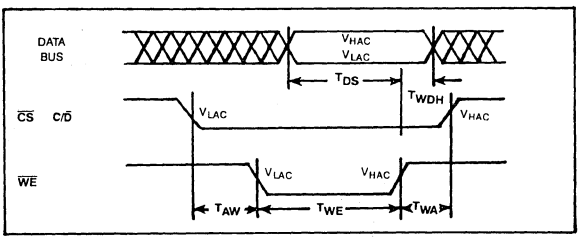


Figure 6 WRITE CYCLE TIMING

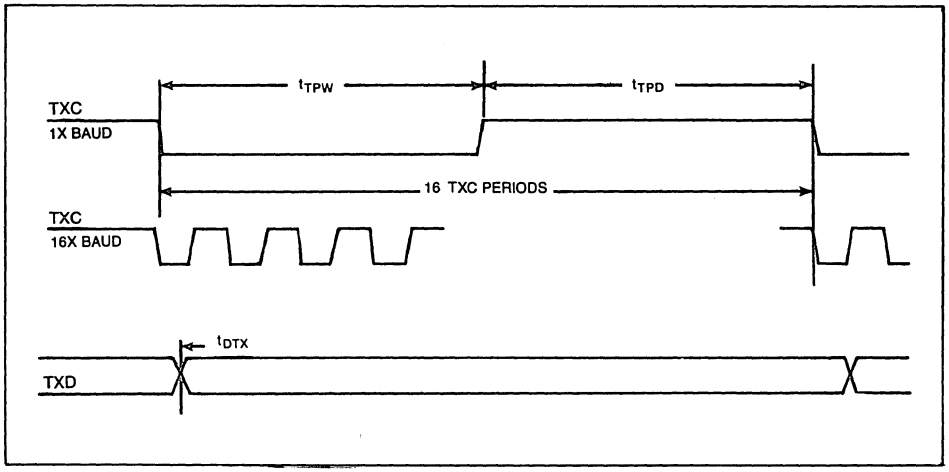


Figure 7 TRANSMITTER CLOCK AND DATA TIMINGS

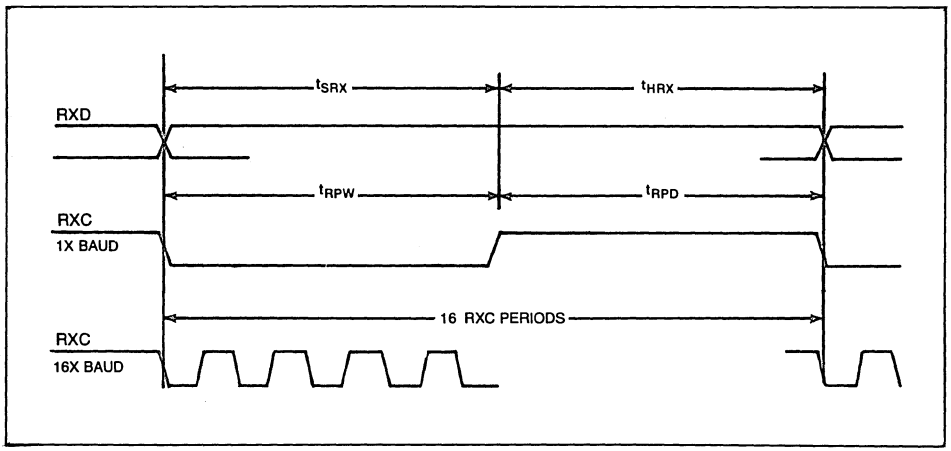


Figure 8 RECEIVER CLOCK AND DATA TIMINGS

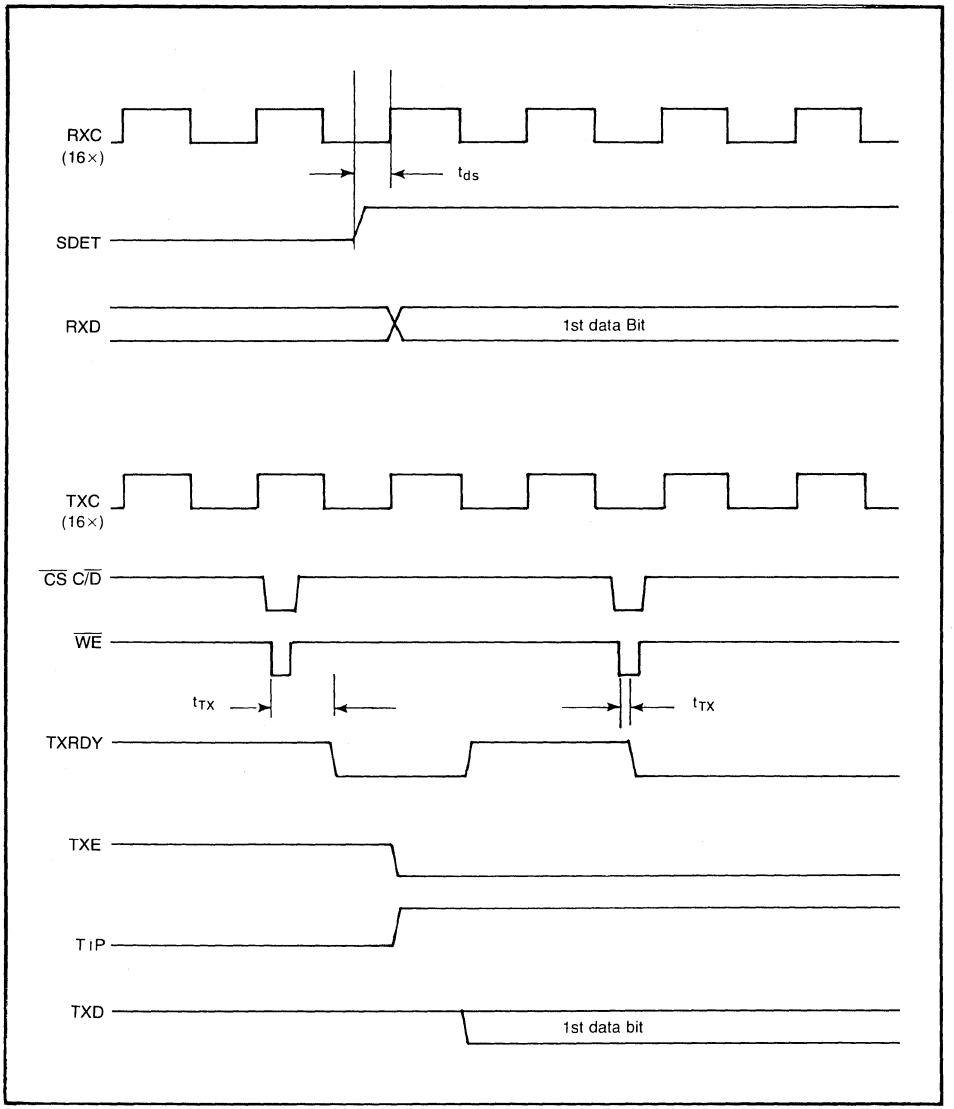


Figure 9 SYNCHRONOUS MODE TIMINGS

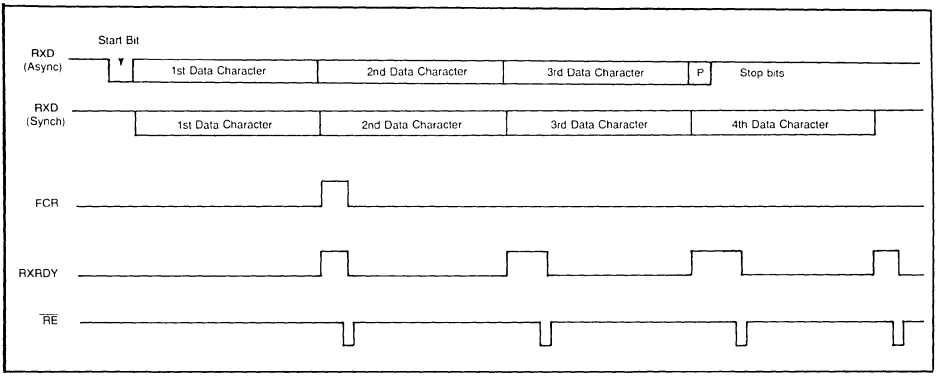


Figure 10 RXRDY AND FCR TIMING

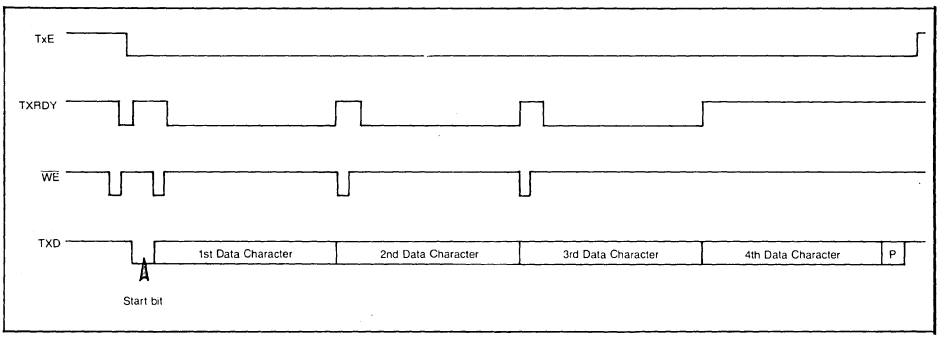


Figure 11 TXRDY AND TXE TIMINGS (4 CHARACTERS SEQUENCE)

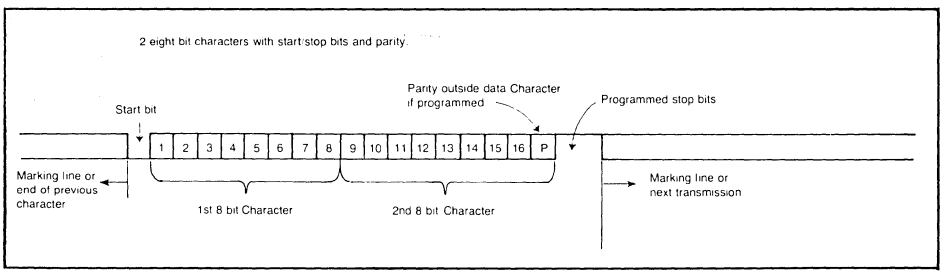


Figure 12 16 BIT ASYNCHRONOUS

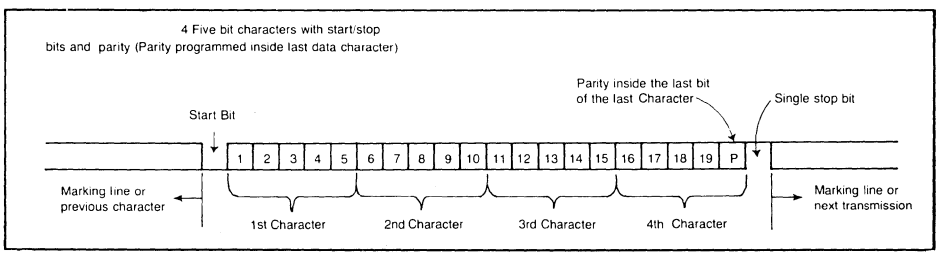


Figure 13 20 BIT ASYNCHRONOUS

ASYNCHRONOUS OPERATION

When the Asynchronous mode is selected, start, stop and parity bits are inserted as programmed. The receiver and transmitter clocks can be programmed as 1X or 16X. The transmitter output, TXD line will mark or space after transmission depending on command register programming. A line break condition can be programmed by setting the TXSM bit (command register bit CR3) to a logic "1". The TXD line will be forced to a low as long as this bit is logic "1". When the receiver detects the input line (RXD) low for a period equal to the word length including start, parity and stop bits, the break detect flag will become active.

The multi-character option is available to the Asynchronous protocol. The user can select any combination of one to eight characters per word and 5, 6, 7 or 8 bits per character. This allows a minimum word length of 5 bits and a maximum of 64 bits, plus parity, if enabled.

SYNCHRONOUS OPERATION

When the Synchronous mode is selected, start and stop bits are not transmitted. Parity is not available in Synchronous mode. The multi-character option is not available; however, the transmitter will continuously shift out data as long as the transmit holding register is buffered by the CPU. Two I/O signals are provided for synchronization, TIP (transmission in progress), an output which indicates that the transmitter is actively sending data and SYNCDET (SYNC detect), an input which notifies the receiver logic when to begin assembling characters.

Synchronization is obtained when the TIP signal from the transmitter is brought to the SYNCDET input of the associated receiver. Completion of a data transmission sequence occurs when the last character in the transmit register is sent and no further data is loaded into the transmit holding register. The TIP signal goes low. The receiver monitors the SYNCDET line and assembles data characters until it goes low, at which time it goes to an idle state.

PARITY MODES

The WD1984 is provided with some unique parity options as discussed above. If parity is enabled and the word length is eight bits, the parity is added to the transmitted word and stripped from the received word. When programmed for 5, 6 or 7 bits per character, the receiver checks and makes available the parity bit on the bus next to the MSB of data. Unused bits in an assembled character are zero when the receive holding register is read.

For example, in Asynchronous mode when two 8 bit characters are programmed with parity after the Data Word and two stop bits, 20 bits are transmitted. These are the Start bit, 16 Data bits, Parity and the 2 Stop bits. The Parity will be stripped off at the receiver since the character length is 8.

In Synchronous mode, Parity is not available and it is suggested the user provide his own software CRC as the last characters of his transmission.

OPERATING DESCRIPTION

The WD1984 is primarily designed to operate in an 8 bit micro-processor environment, although other control logic schemes are easily implemented. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and C/$\overline{D}$) should be connected to the microprocessor's data bus and system control bus. The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a BR1941. A master reset pulse initializes the WD1984 and presets the control registers to transmit and receive four 8-bit contiguous characters with the 32nd bit odd parity. If other protocols are desired, then the mode and command registers should be programmed as discussed previously.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits or a modem.

The TXRDY, RXRDY, FCR and FE/BRKDET Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1984 is designed such that a control register write operation accesses the command instruction register. The mode instruction register is accessed by performing a control write operation setting the internal reset bit high, which allows the next control write operation to program the mode register. Subsequent control write operations will again access the command register until another internal reset is performed. Internal reset commands should also disable the receiver and transmitter until the new mode instruction is programmed. The next command should then reactivate the receiver and transmitter to resume operations. This minimizes any errors that may be generated as a result of an active receive line during reprogramming.

The TXSM bit of the command register causes the transmitter output to be forced low after the last word is transmitted. This is also used in Asynchronous mode to send a break character (all zero data and parity bits).

The receiver is equipped with logic to look for a break character in the Asynchronous mode. When a break character is received, the receiver activates the break detect flag and status bit. When the receiver input line goes high again for at least "one bit time", the receiver resets the break detect flag and resumes its search for a start bit.

MULTI-CHARACTER OPERATIONS

As discussed above, the WD1984 is equipped with a multi-character option which provides the user with the means of transmitting and receiving multiple contiguous characters of data within one set of start and stop bits. Since the WD1984 is an 8 bit bus-oriented device, the controlling processor must read the WD1984 data from its holding register before the subsequent characters are assembled. This situation also exists on the transmit side, i.e., the Transmit Holding Register must be loaded before the previous 8 bits are completely shifted out of the transmit register.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) The data is loaded into the transmit register and TXRDY goes High. This indicates the first data word is being sent and the character can be loaded into the holding register. If the WD1984 is programmed for more than one character (multi-character) then an underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the receive register.

d) When the first character is completely assembled, the data is loaded into the Receive Holding Register, the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active, "1". The CPU should read the data prior to the reception of the next character or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

LOOP TEST MODE:

As mentioned, the WD1984 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and CTS should be "0". The receiver inputs are ignored and the transmitter outputs are held high V_{OH}. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

It is possible to program a test routine using the loop-back mode so that one can simulate "line breaks" and parity errors. This can be done using the TXSM command to interrupt a transmit sequence in "mid-stream", since setting the TXSM bit to a "1" while the transmitter is currently sending data will immediately cause zeroes to be sent until the TXSM bit is reprogrammed to a "0". This can only be done when in the loop-test mode, else the TXSM command is recognized only after the current transmission is complete.

For multicharacter operations, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic ("F" package) ..... −55°C to +125°C
Ceramic ("E" package) ..... −65°C to +150°C
Voltage on any Pin with respect to ground ... −0.5V to +7V
Power Dissipation 400MW

Absolute ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A=0°C to +70°C; V_{CC} =5.0V ± 5%; GND= 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
V_{IL}	Input Low Voltage	−0.5		.08	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			−50	uA	V_{OUT} = 0.45V
				10	uA	V_{OUT} = V
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

CAPACITANCE

T_A = 25°C: V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

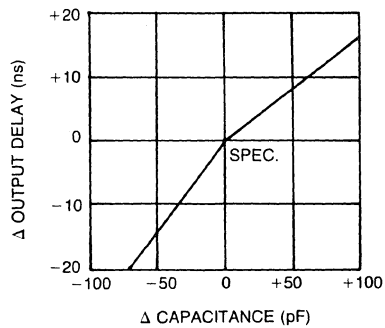
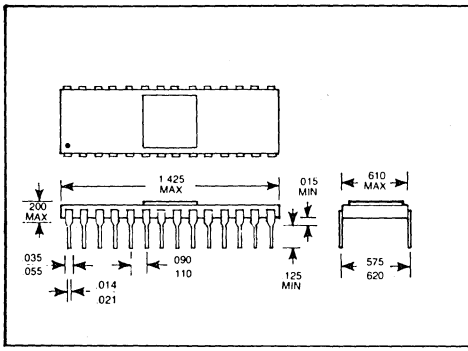


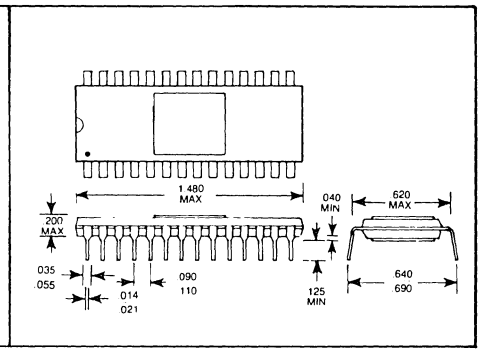
Figure 3 OUTPUT DELAY VS CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
	BUS PARAMETERS				
	Read Cycle (Reference Figure 5)				
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50pF
		25		ns	C_L = 50pF
	WRITE CYCLE (Reference Figure 6)				
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
	OTHER TIMINGS (Reference Figure 7, 8, 9)				
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	RX Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{NRX}	RX Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1× Baud Rate	1.0		us	
	16× Baud Rate	500		ns	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
t_{Rx}	Receiver Input Clock Frequency				
	1× Baud Rate	DC	500	kHz	
	4×, 16× Baud Rate	DC	750	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1× Baud Rate	1.0		us	
	16× Baud Rate	500		ns	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1× Baud Rate	1.0		us	
	16× Baud Rate	700		ns	
				ns	
t_{TX}	TXRDY Delay from center of Data Bit	200 ns	½	t_{TXC}	(1x or 16x)



WD1984E CERAMIC PACKAGE



WD1984F PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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