WESTERN DIGITAL
CORPORATION

PRELIMINARY

LSI PACKET NETWORK INTERFACE WD2501/11 *
SHORT FORM DATA SHEET

September, 1980

FEATURES

- Packet Switching Controller Compatible with CCITT Recommendation X.25, Level 2, LAP.
- Programmable Primary Timer (T1) And Retransmission Counter (N2)
- Programmable A-Field Which Provides A Wider Range Of Applications Than Defined By X.25. These Include: DTE-To-DTE Connection, Multipoint, And Loop-Back Testing
- Direct Memory Access (DMA) Transfer: Two Channels; One For Transmit And One For Receive. Send/Receive Data Accessed By Indirect Addressing Method. No External Address Latches Required. Sixteen Output Address Lines.
- Zero Bit Insert And Delete
- Automatic Appending and Testing Of FCS Field
- Computer Bus Interface Structure: 8 Bit Bi-Directional Data Bus. CS, WE, RE-Four Input Address Lines
- DC To *1.6M Bits/SEC Baud Rate
- TTL Compatible
- 48 Pin Dual In-Line Packages
- Pin-for-pin compatible with WD2511 (LAPB.)

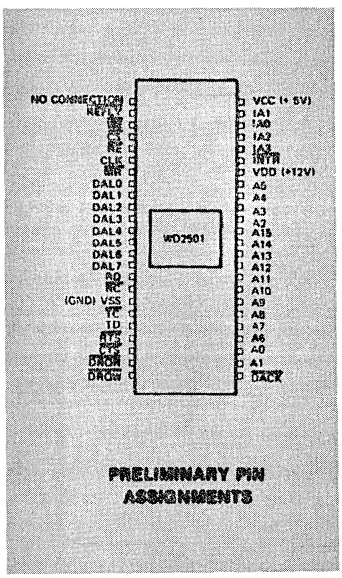
* Higher Baud Rates Available By Special Order

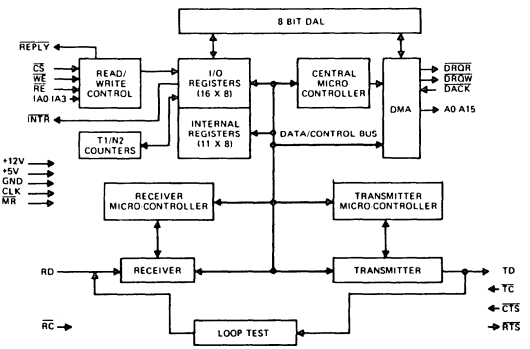
APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OF DCE
PRIVATE PACKET NETWORKS

GENERAL DESCRIPTION

The WD2501 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.
The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.





WD 2501 BLOCK DIAGRAM

*A detailed long form data sheet for this product is available from your local Western Digital Representative.

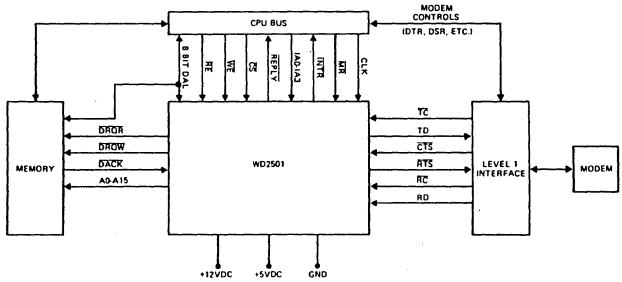
INTERFACE SIGNAL DESCRIPTION

*PIN NUMBER	SYMBOL	NAME	FUNCTION
48	VCC	Power Supply	+5VDC power supply input
42	VDD	Power Supply	+12VDC power supply input
18	VSS	Ground	Ground
6	CLK	Clock	Clock input used for internal timing. Must be square wave from 1.0 to 3.0 mHz.
7	$\overline{MR}$	Master Reset	Initialize on active low. All registers reset to zero, except control bits MDISC and $\overline{LINK}$ are set to 1. $\overline{DACK}$ must be stable high before MR goes high.
4	$\overline{CS}$	Chip Select	Active low chip select for CPU control of I/O registers.
8-15	DAL0-DAL7	Data Access Lines	An 8 bit bi-directional three-state bus for CPU and DMA controlled transfers.
5	$\overline{RE}$	Read Enable**	The contents of the selected register are placed on DAL when $\overline{CS}$ and $\overline{RE}$ are low.
3	$\overline{WE}$	Write Enable	The data on the DAL are written into the selected register when $\overline{CS}$ and $\overline{WE}$ are low. $\overline{RE}$ and $\overline{WE}$ must not be low at the same time.
2	$\overline{REPLY}$	Reply	An active low output to indicate that either a $\overline{CS}\bullet\overline{WE}$ or $\overline{CS}\bullet\overline{RE}$ input is present.
43	$\overline{INTR}$	Interrupt Request	An active low interrupt service request output, and returns high when Status Register #1 is read.
47-44	IA0-IA3	Address Lines In	Four address inputs to the 2501 for CPU controlled read/write operation with registers in the 2501. If ADRV = 0, these may be tied to A0 - A3.
26-41	A0-A15	Address Lines Out	Sixteen address outputs from the 2501 for DMA operation. If the control bit ADRV is 1, the outputs are TTL drives at all times. If ADRV is 0, the ouputs are 3-state, and are HI-Z whenever $\overline{DACK}$ is high. (ADRV is in Control Register #1.)
23	$\overline{DRQR}$	DMA Request Read	An active low output signal to initiate CPU bus request so the 2501 can output onto the bus.

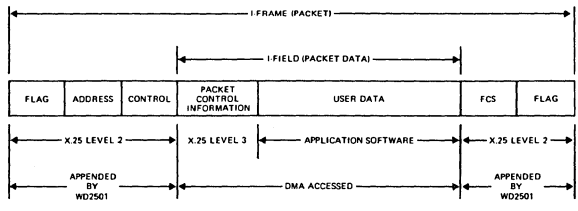
*PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
24	$\overline{DRQW}$	DMA Request Write	An active low output signal to initiate CPU bus request so that data may be written into the 2501. $\overline{DRQW}$ and $\overline{DRQR}$ cannot be low at the same time.
25	$\overline{DACK}$	DMA Acknowledge	An active low input from the CPU in response to $\overline{DRQR}$ or $\overline{DRQW}$. $\overline{DACK}$ must not be low if $\overline{CS}$ and $\overline{RE}$ are low or if $\overline{CS}$ and $\overline{WE}$ are low.
20	TD	Transmit Data	Transmitted serial data output
16	RD	Receive Data	Receive serial data input
19	$\overline{TC}$	Transmit Clock	A 1X clock input. TD changes on the falling edge of $\overline{TC}$.
17	$\overline{RC}$	Receive Clock	This is a 1X clock input, and RD is sampled on the rising edge of $\overline{RC}$. Adjustment of the sample is by quadrant. The sampling may be monitored by the $\overline{RCO}$ output.
21	$\overline{RTS}$	Request-To-Send	An open collector (drain) output which goes low when the 2501 is ready to transmit either flags or data. May be hard-wired to ground.
22	$\overline{CTS}$	Clear-To-Send	An active low input which signals the 2501 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.

* PIN NUMBERS ARE PRELIMINARY

** Throughout this document, the term "read" refers to data out of the 2501 and "write" refers to data going into the 2501.



SYSTEM CONNECTION



According to the X.25 protocol, there are three types of frames: supervisory (S-frame), unnumbered (U-frame), and information (I-frame). All S- and U-frames are generated and tested by the 2501. The user's CPU handles only the I-field of I-frames, which are packets.
NOTE: X.25 Level 1 is the physical interface.

FRAME FORMAT CONTROL

The WD2501 is controlled and monitored by sixteen I/O registers.
Control, status, and error bits will be referred to as CR, SR, or ER, respectively, along with two digits. For example, SR16 refers to status register #1 and bit 6, which is "XBA".

REG. #	IA3	IA2	IA1	IA0	REGISTER	REGISTER GROUPING
0	0	0	0	0	CR0	
1	0	0	0	1	CR1	OVERALL CONTROL
2	0	0	1	0	*SR0	AND
3	0	0	1	1	*SR1	MONITOR
4	0	1	0	0	*SR2	
5	0	1	0	1	*ER0	
6	0	1	1	0	*CHAIN MONITOR	RECEIVER
7	0	1	1	1	*RECEIVED C-FIELD	MONITOR
8	1	0	0	0	T1	TIMER
9	1	0	0	1	N2/T1	
A	1	0	1	0	TLOOK H1	
B	1	0	1	1	TLOOK LO	DMA SET-UP
C	1	1	0	0	CHAIN/LIMIT	
D	1	1	0	1	(UNUSED)	
E	1	1	1	0	XMT COMMAND "E"	"A" FIELD
F	1	1	1	1	XMT RESPONSE "F"	

*CPU READ ONLY. (Write not possible)

CONTROL,STATUS,ERROR REGISTERS

REGISTER	7	6	5	4	3	2	1	0
CR0	0	0	0	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	0	RECR	MDISC
CR1	0	0	0	ADRV	RRT1	0	0	SEND
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX
SR1	[1]PKR	[1]XBA	[1]ERROR		NE2	NE1	NE0	
SR2	T1OUT	$\overline{\text{IRTS}}$	REC IDLE				RANC	$\overline{\text{LINK}}$
ER0	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

[1]Causes Interrupt ($\overline{\text{INTR}}$ Goes Low).

BIT	DESCRIPTION
CR07	Unused control bits, like CR07, should be 0.
CR04	This bit will cause the 2501 to initiate link set-up if CR04 = 1, or to wait for a link set-up from the remote device if CR04 = 0.
CR03	The LOOP TEST bit will connect the transmitted data output to the receiver input. The receiver input pin, RD, is gated-out. The "E" and "F" registers of the A-field should be equal.
CR01	This bit is RECR which defines the CPU's receiver buffer as Ready (CR01 = 1) or as Not Ready (CR01 = 0). If RECR = 0, this bit indicates that the CPU has a temporary inability to accept more I-frames, or packets, and the 2501 will transmit an RNR S-frame.
CR00	MDISC is a mandatory disconnect command. MDISC will cause a logical disconnect in the DTE/DCE link. No DMA accessed data may be transferred as long as MDISC = 1. After Master Reset ($\overline{\text{MR}}$ pin transition from low to high), MDISC will be set. The 2501 will neither transmit nor accept received data until MDISC = 0.
CR14	The ADRV bit (CR14) is the control for the 16 bit output addresses (A0-A15). If ADRV = 0, the outputs are 3-state and are in HI-Z, except when $\overline{\text{DACK}}$ goes low. If ADRV = 1, the outputs are always low impedance (TTL), and are high when $\overline{\text{DACK}}$ is high.

BIT	DESCRIPTION
CR13	RRT1 will cause the 2501 to transmit an RR (RECR = 1) or RNR (RECR = 0) at T1 intervals provided the 2501 is not sending a command or waiting for an acknowledgement.
CR10*	The SEND bit (CR10) is used to command the 2501 to send the next packet or packets. If SEND = 1, the 2501 will read from TLOOK the BRDY bit of the next segment for transmission. If BRDY = 0, the 2501 will clear SEND and no action occurs. If BRDY = 1, the 2501 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the 2501 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and transmission of packets is stopped.
SR07-SR05*	NA2-NA0. Next block of transmitted data to be Acknowledged.
SR04	RNRR. An RNR has been received.
SR03-SR01*	NB2-NB0. Next block to be transmitted.
SR00	RNRX. As a result of RECR (CR01) = 0, an RNR has been transmitted.
SR17	The PKR bit stands for Packet Received. This means that a packet has been received error-free and in correct sequence according to the received N (S) count. The data (I-field) has been placed in the CPU's RAM memory. NE is advanced. The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an interrupt request ($\overline{INTR}$ goes low) when that bit goes to a 1. After SR1 is read, all three bits are reset to 0, and $\overline{INTR}$ returns high.
SR16	The XBA bit means that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK'ED bit is set to "1" for each segment in TLOOK which was acknowledged.
SR15	The ERROR bit indicates: 1) An error has occurred which is not recoverable by the 2501, or 2) A significant event has occurred. The "significant events" are: change in link status (link-up or down), the 2501 is progressing to the next segment in a chained receive buffer, or one direction of the link has been reset. The exact nature of the reason for the ERROR bit is given in ER0.
SR13-SR11*	NE2-NE0. Next Expected packet segment number of RLOOK.
SR27	T1OUT bit means that timer T1 has timed-out. This bit returns to 0 when T1 is re-started.
SR26	$\overline{IRTS}$ stands for the Internal Request-To-Send bit, and indicates that the transmitter is attempting (successful or not) to send either data or flags. If the $\overline{RTS}$ pin is not tied to ground or WIRE-ORED with another signal, then $\overline{IRTS}$ = $\overline{RTS}$.
SR25	REC IDLE indicates that the 2501 has received at least 15 contiguous 1's.
SR21	RANC means that the Received Address field is Not Correct. Either the A-field was from "E" but should have been "F" or vice versa. A CMDR will be transmitted if link was in the information transfer phase. NOTE: If an A-field is neither "E" nor "F", the entire packet is disregarded and not brought into memory by DMA. No action is taken.
SR20	If the link is established, $\overline{LINK}$ = 0. If the link is logically disconnected, $\overline{LINK}$ = 1.

*See "Memory Access Method" Section

ERROR REGISTER (ER0)

ER07	ER06	ER05						
0	0	0	ER00 - NOSFR ER01 ROR ER02 TUR ER03 - RPKNR ER04 RLNR					
0	0	1	ER04 0 1 0 0	ER03 0 0 0 0	ER02 0 0 1 0	ER01 0 0 0 1	ER00 1 0 0 0	LINK is up. (Was down) Received DISC while LINK up. DISC sent, sent SARM sent N2 times without UA. DISC sent, REC IDLE for T1xN2.
0	1	0	CHAIN STATUS ER00 - GNCS ER01 - CNR					
1	0		LINK RESET RECEIVED if ER05 - ER00 - 000000 LINK RESET TRANSMITTED if ER05 - ER00 = non-zero ER00 similar to W ER01 similar to X ER02 similar to Y ER03 similar to Z ER05 means received F = 1, but did not send P = 1 ER04 means I-frame was sent N2 times without acknowledge					
1	1		COMMAND REJECT RECEIVED if ER05 - ER00 = 000000 TRANSMITTED if ER05 - ER00 = non-zero ER00 = W ER01 = X ER02 = Y ER03 = Z ER04 = Z1					

NOTES:

1. Whenever a command reject (CMDR) is received, the I-field will have been placed in appropriate memory by DMA, and a link reset SARM will be transmitted. The NB is not advanced.
2. Definitions of W,X,Y,Z as stated in CCITT X.25. Z1 indicates received N(S) is invalid (not part of X.25).

TERMS USED IN ERROR REGISTER

GNCS Going to Next Chain Segment

RLNR RLOOK Not Ready. REC RDY bit of next segment is 0.

ROR Receiver Over-Run. The Receiver Register (RR) had a character to load into the FIFO, but the FIFO was full.

RPKNR Received Packet but Memory Block was Not Ready.

TUR Transmitter Under-Run. The Transmitter Register (TR) needed a character from the Transmitter Holding Register (THR), but the THR was not ready.

NOSFR No S-frame received for T1 x N2. Used only if RRT1 = 1.

MEMORY ACCESS METHOD

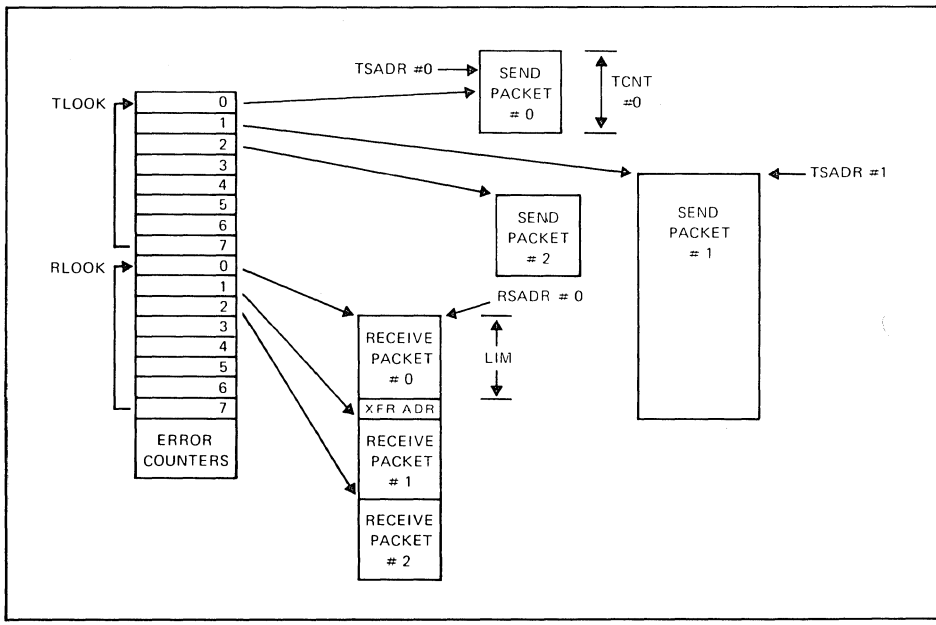
The memory access method, which includes DMA, is designed to take full advantage of the bit-oriented protocol which allows up to 7 I-frames to be outstanding (i.e., unacknowledged) in each direction of a communications link. The memory access method used two "look-up" tables: One for transmit and one for receive. These tables contain addresses and control for the individual send/receive packets. Thus, packet data are DMA addressed indirectly. This method is best suited for most software applications.

The 16 bit starting address for the look-up table TLOOK is loaded into the 2501 by the CPU. (I/O Registers "A" and "B"). RLOOK must immediately follow TLOOK in contiguous fashion. TLOOK and RLOOK are in the RAM memory external to the 2501. There are a total of 8 segmented control sections for each table. Each segment contains eight bytes. Four bytes are used for data memory starting address and length, two bits of one byte are used for control, one byte defines variable bit length and residual, and the other two bytes are open for user definition.

In transmit, the 2501 will have read from TLOOK the starting address and length of the first packet to be transmitted. The 2501 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory. At the end of the information field, the 2501 will automatically send the FCS and closing Flag. The 2501 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the 2501 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

To receive, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit. After the packet is received error-free and in proper N(S) sequence count, an interrupt is generated, and the 2501 is ready for the next packet which will be placed in the next location.



MEMORY ACCESS SCHEME

"DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the 2501. Therefore, to prevent the "deadly embrace", the following rule is obeyed by the 2501 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK, and to the I/O registers. The Error Counters do not apply to this rule.

> RULE: If a bit is set by the CPU, it will not be set by the 2501, and vice versa. If a bit is cleared by the 2501, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segment is set by the CPU, only, but cleared by the 2501, only.

ERROR COUNTERS

Following continguously after RLOOK is ten 8 bit error counters. The 2501 will increment each counter at the occurrence of the defined event. However, the 2501 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

ERROR COUNTER	COUNT
1	Received Frames with FCS Error
2	Received Short Frames (less than 32 bits)
3	Number of times T1 ran-out (completed)
4	Number of I-Frame Retransmissions
5	REJ Frames Received
6	REJ Frames Transmitted
7	Invalid Commands Received
8	Invalid Responses Received
9	Number of frames which I-field exceeded total Limit.
10	Number of Null Packets Received

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	ACK'ED	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	BRDY
2	TSADR HI							
3	TSADR LO							
4	SPARE				TCNT HI			
5	TCNT LO							
6*	SBL2	SBL1	SBL0	BL1	RES2	RES1	RES0	BL0
7	SPARE FOR USER DEFINITION							
8	SPARE							

TLOOK SEGMENT

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0
1	FRCML	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	REC RDY
2	RSADR HI							
3	RSADR LO							
4					RCNT HI			
5	RCNT LO							
6*	SBL2	SBL1	SBL0	BL1	RES2	RES1	RES0	BL0
7	SPARE FOR USER DEFINITION							
8	SPARE							

*Byte #6 defines variable bit length and residual bits.

RLOOK SEGMENT

BRDY means that the transmit buffer is ready. The 2501 will send the block only after the CPU makes BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the 2501 will make BRDY = 0, and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknowledgement is contained in the received N (R) count of an I-frame, RR frame, or RNR frame. Upon acknowledgement, the 2501 will make ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the 2501 that the receive buffer is ready. The 2501 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the 2501 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet in proper sequence, the 2501 will set FRCML, clear REC RDY, and generate a Packet Received Interrupt. The 2501 will also write the value of the binary length of the received packet in RCNT HI and RCNT LO. The NE count is advanced. The 2501 will acknowledge received packets at the first opportunity. This will be in either the next transmitted I-frame, or by an RR frame if RECR = 1, or by an RNR frame if RECR = 0. (RECR is in CRO.)
In the address bytes, HI represents the upper 8 bits and LO represents the lower 8 bits. In the count bytes, HI represents the upper 4 bytes.

TSADR is the starting address of the buffer to transmit, and TCNT is the binary count of the number of characters in the I-field.

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the 2501 will write the value of RCNT which is the binary count of the number of characters in the I-field.

Whether the 2501 accesses a look-up table or a memory block, a DMA Cycle is required for each access.

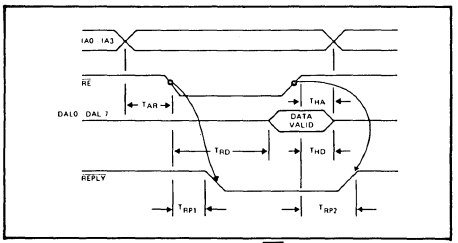
TLOOK AND RLOOK POINTERS

There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SRO) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted, and is advanced at the end of each DMA transmission. NA is the value of the segment of the next block which will be acknowledged. If all transmitted blocks have been acknowledged, then NA = NB.

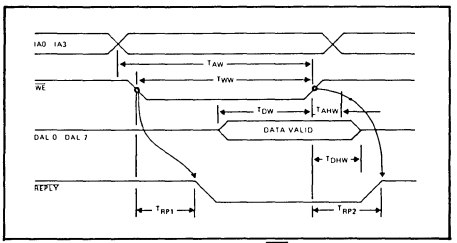
In SR1 is a 3-bit counter, NE, used with RLOOK. NE is the value of the segment number where the next received packet will be placed.

PRELIMINARY TIMING SPECIFICATIONS

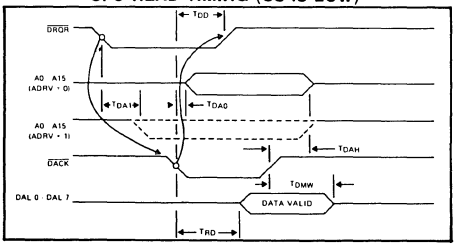
SYMBOL	PARAMETER	MIN. (NS)	MAX. (NS)	COMMENT
T_{AR}	Input Address Valid to $\overline{RE}$	0		
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid	200 375		C (DAL) = 50 pf C (DAL) = 100 pf
T_{HD}	Data Hold Time from Read Strobe		80	
T_{HA}	Address Hold Time from Read Strobe	80		
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	200		
T_{WW}	Minimum $\overline{WE}$ Pulse	200		
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100		
T_{AHW}	Address Hold Time after $\overline{WE}$	80		
T_{DHW}	Data Hold Time after $\overline{WE}$ or after $\overline{DACK}$ for DMA Write	80		
T_{DA1}	Time from $\overline{DRQR}$ (or $\overline{DRQW}$) to Output Address Valid if ADRV = 1		80	C (ADDRESS) = 100 pf
T_{DA0}	Time from $\overline{DACK}$ to Output Address Valid if ADRV = 1		360	C (ADDRESS) = 100 pf
T_{DD}	Time from Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQR}$ (or $\overline{DRQW}$)		200	C ($\overline{DRQ}$) = 50 pf
T_{DAH}	Output Address Hold Time from $\overline{DACK}$		120	
T_{DMW}	Data Hold Time from $\overline{DACK}$ for DMA Read		80	
T_{RP1}	$\overline{REPLY}$ Response Leading Edge		160 240	C_{LOAD} = 50 pf C_{LOAD} = 100 pf
T_{RP2}	$\overline{REPLY}$ Response Trailing Edge		200 260	C_{LOAD} = 50 pf C_{LOAD} = 100 pf



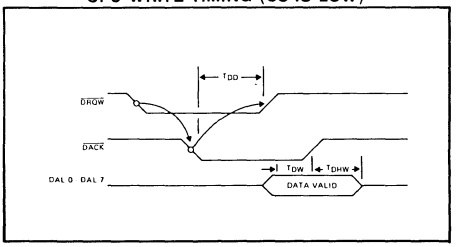
CPU READ TIMING ($\overline{CS}$ IS LOW)



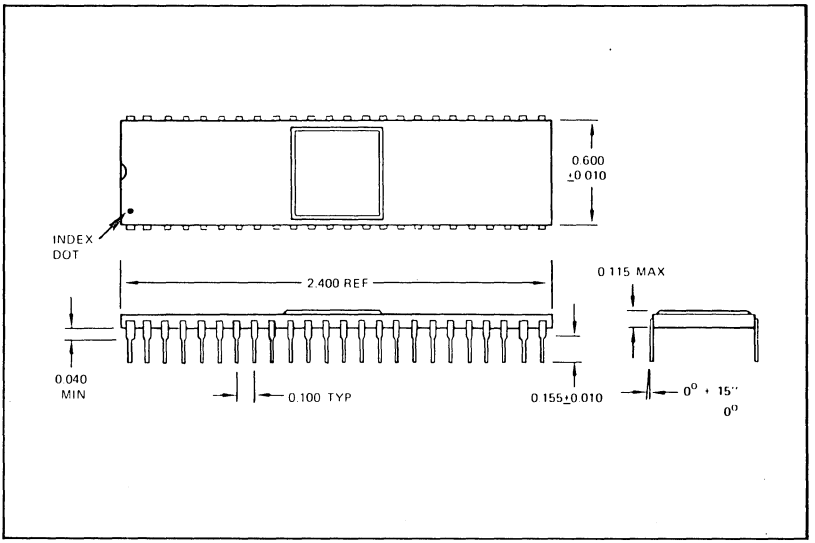
CPU WRITE TIMING ($\overline{CS}$ IS LOW)



DMA READ TIMING



DMA WRITE (A0-A15 SAME AS DMA READ)



WD2501 CERAMIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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