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WD33C95A, WD33C96A

Enhanced Single-ended and Differential SCSI Bus Interface Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This document describes two versions of a single chip VLSI SCSI bus controller. The WD33C96A is a 100-pin device that can act only as a single-ended SCSI controller, and the WD33C95A is a 132-pin device that can act as both a single-ended and a differential SCSI controller.

In this document, the term ESBC (Enhanced SCSI bus controller) is used as a term when referring to both parts.

The ESBC can perform both as an initiator and target. The data path for this device is programmable to be either 8-bits or 16-bits wide. All the features and timings described below are preliminary and subject to change without notice.

1.2 REFERENCE DOCUMENTS

The following reference documents may be of help:

- Draft proposed American National Standards for Information Systems-Small Computer System Interface-2 (SCSI-2), X3T9.2 Task Group number X3T9/89-042 revision 10c dated March 2, 1990.
- WD33C93A SCSI Protocol Chip Specification 96-105393.
- WD61C40 Intelligent Disk Controller and Buffer Manager Chip Specification.
- WD33C95A and WD33C96A Product Bulletin.

1.3 FEATURES

- High speed SCSI bus transfers, 8-bits or 16-bits wide
- Minimum SCSI bus latency/overhead
- Automatic response to a bus initiated selection/reselection
- Flexible combination commands through writeable control store
- Automatic decoding of the transfer length of commands
- 16-word FIFO to support synchronous offset up to 16-words or 32-bytes
- Programmable synchronous transfer period
- Includes single-ended 48 mA drivers for SCSI interface
- Includes control signals to support external differential drivers and receivers (WD33C95A)
- Supports low-level SCSI bus control
- Efficient interaction with the WD61C40 with less microprocessor overhead
- Supports fast DMA transfers up to 10M transfers/second
- Supports host adapter application on the motherboard
- Flexibility to support most DMA controllers or buffer managers
- Dedicated 8-bit port for high speed microprocessor
- Pipelined 24-bit transfer counter (two-level)
- Transfers may be specified in bytes or logical blocks
- Minimum microprocessor intervention required
- Single +5 volt supply with low power mode
- 100-pin PQFP package for single-ended interface (WD33C96A)
- 132-pin package for differential and single-ended interface (WD33C95A)
- Target-mode LRC generation/checking

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1.4 GENERAL DESCRIPTION

The ESBC is a high performance CMOS VLSI device that controls data transfers between the SCSI bus and the local data buffer.

2.0 ARCHITECTURE

2.1 PERFORMANCE

The SCSI and DMA interfaces are independently programmable between 16-bits and 8-bits wide. The interface can transfer data at a rate up to 10M transfers/second, that is 20 MByte/s mode in 16-bit mode. The total time required to perform arbitration, selection, command transfer, and message transfer is less than 20 µs. The ESBC includes a dedicated 8-bit port for a high performance microprocessor, such as 25 MHz 80C188/186 and 16 MHz 80C196. The ESBC requires supervision from the microprocessor only in exception conditions. The device includes a 16 word by 18-bit FIFO to support an offset of 16-words or 32-bytes in a SCSI synchronous transfer.

2.2 FLEXIBILITY

The ESBC handles SCSI protocol and data transfer through a 128-word Writeable Control Store (WCS), allowing the user to program any sequence of bus phases on the SCSI bus. The ESBC can act as a target as well as an initiator. The WCS has enough capacity to fit both initiator and target instruction sequences. The device can interface with various buffer managers, such as the WD60C40, WD60C40A, WD61C40 and the WD42C22. It can also interface with various types of DMA controllers.

2.3 MICROPROCESSOR INTERFACE

The device has a dedicated microprocessor interface. This port supports 8-bit microprocessors with a multiplexed address/data AD[0-7] bus. The microprocessor can access the internal registers and FIFO through this port. The ESBC can interface with various high performance microprocessors, such as 80C196, 80C188, and 80C186. $\overline{RE}$ and $\overline{WE}$ control access through this port.

The ESBC has another access mode, where the microprocessor can access the internal registers through DMA bus pins BD[0-7]. This mode is useful in applications where a dedicated microprocessor is not available and the ESBC is controlled directly by the main processor. The microprocessor accesses the internal registers in 8-bit mode; only the lower DMA port is used. The register address is supplied into the AD bus (dedicated microprocessor bus). $\overline{DRE}$ and $\overline{DWE}$ control the access. $\overline{DACK}$ must not be active.

2.4 DMA INTERFACE

The on-board DMA controller is programmable to act as bus master or slave. The polarity of DRQ and DACK is also programmable to be active high or low. The data can be transferred in 8-bit or 16-bit mode. The maximum transfer rate is 10M transfers/s. The ESBC automatically performs byte/word conversions.

2.5 DUAL PORT REGISTERS

The ESBC uses a 32-word by 9-bit (8-bit plus parity) Dual Port Register to store special information such as commands, messages and status. The information is transferred between the SCSI bus and the registers under control of the WCS sequence. The microprocessor can randomly access these registers like any other register. The dual port structure allows simultaneous accesses by the microprocessor and the WCS.

2.6 DIFFERENTIAL DRIVER CONTROL

One configuration of the ESBC, the WD33C95A, provides all signals needed for interface to a 8-bit or 16-bit differential SCSI bus. All commonly used SCSI interface devices are supported.

2.7 POWER MANAGEMENT

The ESBC automatically goes into a power-down mode when the WCS has not been active and the device has not been accessed for a period of time defined in the SLEEP register. A wakeup time of less than 200 ns is required to return to full operating speed.

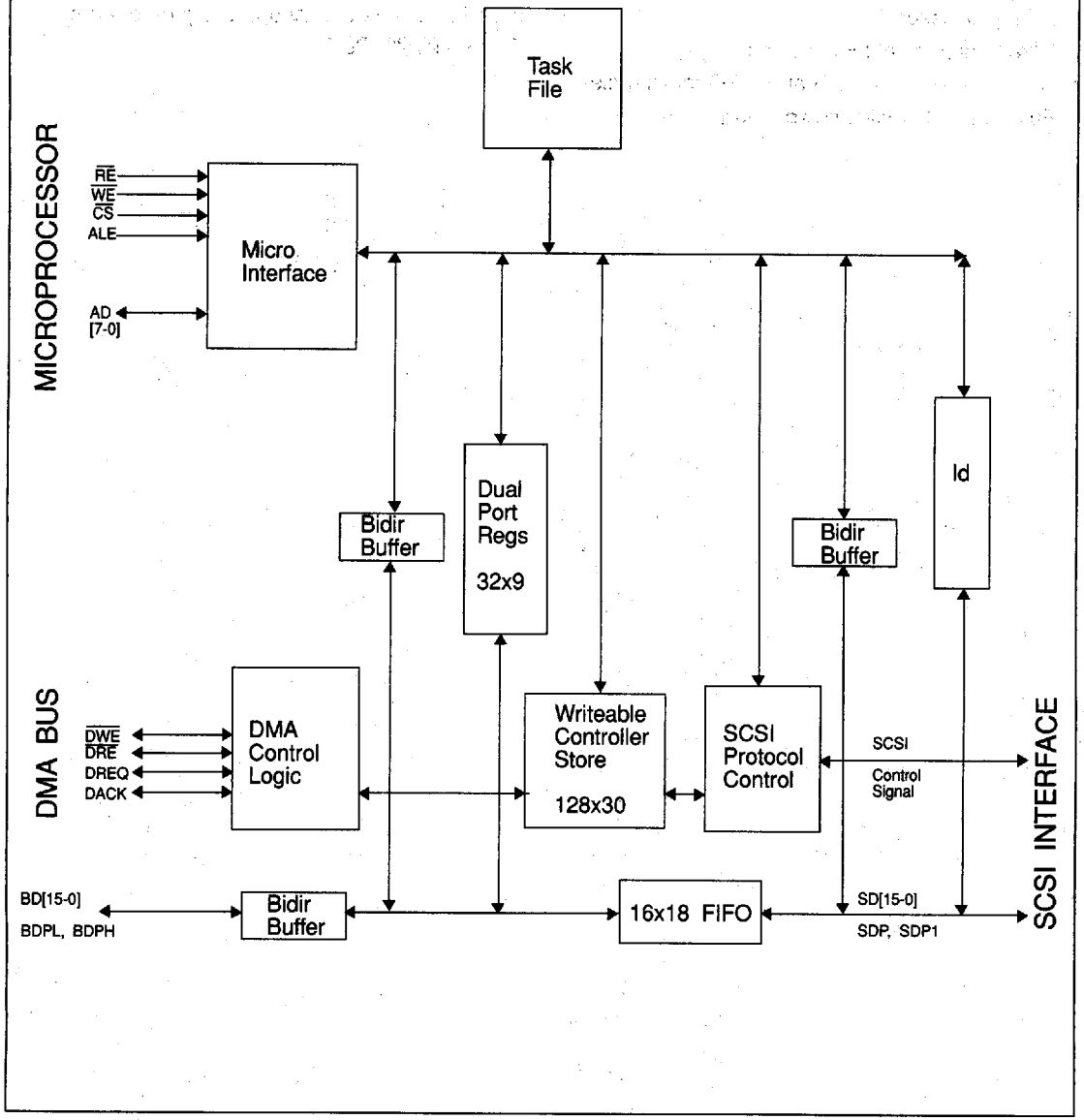

FIGURE 2-1. ESBC BLOCK DIAGRAM

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2.8 TESTABILITY

The ESBC includes several features to improve testability of the device:

- All registers are readable
- WCS RAM is readable and writeable by the microprocessor
- Wire bond/pin solder checking
- BIST for the WCS, DPR and FIFO register files
- Full scan path logic implemented

2.9 COMPATIBILITY with WD33C93 FAMILY

The architecture of the ESBC is substantially different from that of the WD33C93 family. However, the ESBC has the ability to emulate all the combination commands supported by the WD33C93. In addition, the firmware that controls the device may be adapted to support higher performance through pipelining.

3.0 SIGNAL DESCRIPTION

This section contains two figures and accompanying tables which describe the signal to pin locations.

In addition there is a detailed description of each signal.

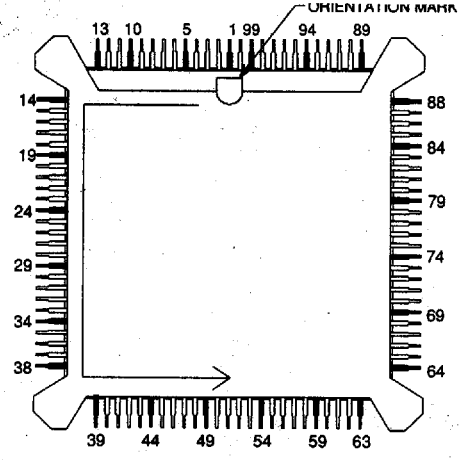

FIGURE 3-1. 100-PIN PACKAGE

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-GND	26-N.C.	51-BD10	76-VCC
2-I/O	27-TST	52-BD11	77-SD11
3-MSG	28-VCC	53-BD12	78-N.C.
4-C/D	29-GND	54-BD13	79-SD10
5-GND	30-AD0	55-BD14	80-GND
6-ACK	31-AD1	56-BD15	81-SD9
7-REQ	32-AD2	57-BDPH	82-N.C.
8-GND	33-AD3	58-GND	83-SD8
9-RST	34-AD4	59-DRE	84-GND
10-ATN	35-AD5	60-DWE	85-SD7
11-BSY	36-AD6	61-DRQA	86-N.C.
12-SEL	37-AD7	62-DRQB	87-SD6
13-VCC	38-VCC	63-VCC	88-VCC
14-GND	39-GND	64-GND	89-GND
15-CLK	40-BD0	65-DACKA	90-SD5
16-MUX	41-BD1	66-DACKB	91-SD4
17-DIRECT	42-BD2	67-TSTSE	92-GND
18-CS	43-BD3	68-N.C.	93-SD3
19-WE	44-BD4	69-SD15	94-SD2
20-RE	45-BD5	70-N.C.	95-GND
21-ALE	46-BD6	71-SD14	96-SD1
22-HRST	47-BD7	72-GND	97-SD0
23-RDY	48-BDPL	73-SD13	98-GND
24-RSTF	49-BD8	74-N.C.	99-SDP1
25-INT	50-BD9	75-SD12	100-SDP

TABLE 3-1. WD33C96A PIN ASSIGNMENTS

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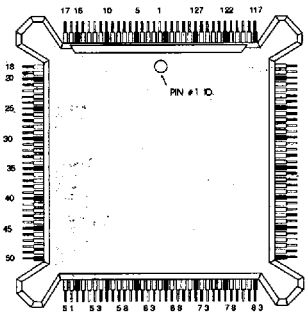

FIGURE 3-2. 132-PIN PACKAGE

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-GND	34-SD1OE	67-BD10	100-VCC
2-N.C.	35-SD2OE	68-GND	101-SD11
3-I/O	36-TST	69-BD11	102-SD11OE
4-MSG	37-VCC	70-BD12	103-SD10OE
5-C/D	38-GND	71-GND	104-SD10
6-GND	39-SD3OE	72-BD13	105-GND
7-ACK	40-AD0	73-BD14	106-SD9
8-REQ	41-AD1	74-BD15	107-SD9OE
9-GND	42-AD2	75-BDPH	108-SD8OE
10-RSTIN	43-SD4OE	76-GND	109-SD8
11-RST	44-AD3	77-DRE	110-N.C.
12-ATN	45-AD4	78-DWE	111-GND
13-BSYIN	46-AD5	79-DRQA	112-SD7
14-BSY	47-AD6	80-DRQB	113-SD7OE
15-SELIN	48-AD7	81-VCC	114-SD6
16-SEL	49-VCC	82-N.C.	115-DSENS
17-VCC	50-N.C.	83-N.C.	116-VCC
18-N.C.	51-N.C.	84-N.C.	117-N.C.
19-N.C.	52-GND	85-GND	118-GND
20-GND	53-BD0	86-DACKA	119-SD5
21-CLK	54-N.C.	87-DACKB	120-SD4
22-MUX	55-BD1	88-TSTSE	121-GND
23-DIRECT	56-BD2	89-SD5OE	122-SD3
24-CS	57-BD3	90-SD6OE	123-SD2
25-WE	58-BD4	91-SD15	124-GND
26-RE	59-BD5	92-SD15OE	125-SD1
27-ALE	60-BD6	93-SD14OE	126-SD0
28-SE	61-N.C.	94-SD14	127-IGS
29-HRST	62-BD7	95-GND	128-TGS
30-RDY	63-BDPL	96-SD13	129-GND
31-RSTF	64-GND	97-SD13OE	130-SDP1
32-INT	65-BD8	98-SD12OE	131-SDPOE
33-SD0OE	66-BD9	99-SD12	132-SDP

TABLE 3-2. WD33C95A PIN ASSIGNMENTS

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
		MICROPROCESSOR INTERFACE		
30-37	40-42 44-48	AD[0-7]	I/O	**Microprocessor Address/Data Bus**
21	27	ALE	I	**Address Latch Enable** The falling edge of ALE is used to latch the address of the desired register.
18	24	$\overline{CS}$	I	**Chip Select** $\overline{CS}$ is active low and is used to qualify $\overline{RE}$ and $\overline{WE}$ when the microprocessor is accessing a register.
17	23	DIRECT	I	Selects direct microprocessor access protocol.
22	29	$\overline{HRST}$	I	**Hardware Reset** Active low hardware reset.
25	32	INT	O	**Interrupt Request** INT is active high, and is asserted to indicate an error condition or completion of a command.
16	22	MUX	I	Selects multiplexed microprocessor address/data protocol.
23	30	RDY	O	**Chip Ready** RDY is an open-drain output. RDY will be pulled low whenever the device is being accessed and is not ready to end the bus access cycle.
20	26	$\overline{RE}$	I	**Read Enable** This signal is active low and is used with $\overline{CS}$ to read the registers.
24	31	RSTF	O	**SCSI Reset Follower** RSTF is a debounced version of $\overline{RST}$/RSTIN. It is active high, and will be asserted as long as a valid SCSI reset is detected.
N/A	28	SE	I	Single-ended SCSI select. (10K pullup)
19	25	$\overline{WE}$	I	**Write Enable** This signal is active low and is used with $\overline{CS}$ to write the registers.
		DMA INTERFACE		
40-47	53,55-60, 62	BD[0-7]	I/O	**DMA Bus** The lower 8 bits of the DMA bus.
48	63	BDPL	I/O	Parity for BD[0-7].

TABLE 3-3. SIGNAL DESCRIPTION

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

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PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
49-56	65-67, 69-70, 72-74	BD[8-15]	I/O	**DMA Bus** DMA bus for upper 8 bits.
57	75	BDPH	I/O	Parity for BD[8-15].
65	86	DACKA	I/O	**Port A DMA Acknowledge** This pin is used to acknowledge DMA requests on port A.
66	87	DACKB	I/O	**Port B DMA Acknowledge** This pin is used to acknowledge DMA requests on port B.
59	77	$\overline{DRE}$	I/O	**DMA Read Enable** This signal is active low, and is used to strobe on the DMA bus.
61	79	DRQA	I/O	**Port A DMA Request** This pin is used to request DMA transfers on port A.
62	80	DRQB	I/O	**Port B DMA Request** This pin is used to request DMA transfers on port B.
60	78	$\overline{DWE}$	I/O	**DMA Write Enable** This signal is active low, and is used to strobe data on the DMA bus.
SCSI INTERFACE				
6	7	$\overline{ACK}$	I/O	**Data Acknowledge**
10	12	$\overline{ATN}$	I/O	**Attention**
11	N/A	$\overline{BSY}$	I/O	**Busy** Bidirectional busy signal.
N/A	14	BSY	O	**Busy** Output busy signal.
N/A	13	$\overline{BSYIN}$	I/O	**Busy** Input busy signal.
4	5	$\overline{C}$/D	I/O	**Command/Data** Command/data select.
N/A	115	DSENS	I	**Differential SCSI Sense**
2	3	$\overline{I}$/O	I/O	**Input/ Output** Select input or output direction.
N/A	127	IGS	I/O	**Initiator Group Select** Asserted whenever the WD33C95A is connected as an initiator.

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
3	4	$\overline{MSG}$	I/O	**Message** Selects message phase.
7	8	$\overline{REQ}$	I/O	**Data Request**
9	N/A	$\overline{RST}$	I/O	**SCSI Reset** Resets SCSI bidirectional signal.
N/A	11	RST	O	**SCSI Reset** Resets SCSI output only signal.
N/A	10	$\overline{RSTIN}$	I	**SCSI Reset** Resets SCSI input only signal.
85, 87, 90, 91, 93, 94, 96, 97	112,114, 119,120, 122,123, 125, 126	$\overline{SD[0\text{-}7]}$	I/O	**SCSI Data** Lower byte (0-7) SCSI data signals.
100	132	$\overline{SDP}$	I/O	Parity for $\overline{SD[0\text{-}7]}$
69, 71 73, 75 77, 79 81, 83	91, 94, 96, 99, 101, 104 106, 109	$\overline{SD[8\text{-}15]}$	I/O	**SCSI Data** Upper byte (8-15) SCSI data signals.
99	130	$\overline{SDP1}$	I/O	Parity for $\overline{SD[8\text{-}15]}$
N/A	33-35, 39, 43, 89, 90, 92, 93, 97, 98, 102, 103,107, 108,113	SDOE[0-15]	O	**Output Enable** These output enables are active high.
N/A	131	SDPOE	O	**Output Enable** Output enable for SDP and SDP1
12	N/A	$\overline{SEL}$	I/O	**Select** Bidirectional select.
N/A	16	$\overline{SEL}$	O	**Select** Output only select.
N/A	15	SELIN	I	**Select** Input only select
N/A	128	TGS	O	**Target Group Select** High whenever a target.

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

PIN*	PIN**	MNEMONIC	I/O	DESCRIPTION
				MISCELLANEOUS
15	21	CLK	I	**INPUT CLOCK** 20 MHz to 50 MHz
13, 28, 38, 63, 76, 88	17, 37, 49, 81, 100, 116	VCC	--	**Power Supply** +5V Power Supply Pins
1, 5, 8, 14, 29, 39, 58, 64, 72, 80, 84, 89, 92, 95, 98	1, 6, 9, 20, 38, 52, 64, 68, 71, 76, 85, 95, 105, 111, 118, 121, 124, 129	GND	---	**GROUND PINS**
26, 68, 70, 74, 78, 82, 86	2, 18, 19, 50, 51, 54, 61, 82-84, 110, 117	N.C.	I	**NO CONNECTS** Do **not** connect these pins to any signal.
27	36	TST	I	**TEST MODE ENABLE** Enables the test mode.
67	88	TSTSE	I	**TEST MODE SCAN ENABLE** Enables the test scan mode.

TABLE 3-3. SIGNAL DESCRIPTION (CONTINUED)

NOTE:
* Pin numbers are for the WD33C96A
** Pin numbers are for the WD33C95A.

A.0 GLOSSARY AND CONVENTIONS

The following is a list of terms and conventions used throughout the ESBC data sheet.

A.1 GLOSSARY

TERM	MEANING
0x00	Hexadecimal number
CDB	Command Descriptor Block
DMA	Direct Memory Access
DPR	Dual Port Register
FIFO	First In First Out Memory
HLR	High Level Response bits (SELH, RSELH, AUTOR)
LLR	Low Level Response bits (SELL, RSELL)
LSB	Least Significant Bit
MSB	Most Significant Bit
RAM	Random Access Memory
RRS	Reselection Response Sequence
SRS	Selection Response Sequence
WCS	Writeable Control Store

A.2 CONVENTIONS

TERM	CONVENTION
asserted	the signal is driven active by the ESBC
negated	the signal is driven inactive by the ESBC
released	the signal is released by the ESBC; external bias circuitry will bring the signal to the inactive state
micro	refers to the microprocessor controlling the ESBC
DMAC	refers to the DMA controller connected to the DMA port

A.3 RESERVED REGISTERS

All registers marked as "Reserved" must not be written, and if read, will produce either 0's or 1's.

All bits marked as "Reserved" must only be written with 0's, and if read, will produce either 0's or 1's.

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