WESTERN DIGITAL
CORPORATION

WD4020 ROMless N-Channel Microcontrollers

September, 1980

FEATURES

- LOW COST
- EXACT CIRCUIT EQUIVALENT OF WD4200
- STANDARD 40-PIN DUAL-IN-LINE PACKAGE
- INTERFACES WITH STANDARD PROM OR ROM
- 64 x 4 RAM, ADDRESSES UP TO 1K x 8 ROM
- POWERFUL INSTRUCTION SET
- TRUE VECTORED INTERRUPT, PLUS RESTART
- THREE-LEVEL SUBROUTINE STACK
- 4.0 μs INSTRUCTION TIME
- SINGLE SUPPLY OPERATION (4.5 V TO 6.3 V)
- INTERNAL TIME-BASE COUNTER FOR REALTIME PROCESSING
- INTERNAL BINARY COUNTER REGISTER WITH SERIAL I/O CAPABILITY
- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF WD4000 FAMILY

GENERAL DESCRIPTION

The WD4020 ROMless Microcontrollers are members of the Control Oriented Processor (COP) family, fabricated using N-channel, silicon gate MOS technology. Each part contains CPU, RAM and I/O, and is identical to a WD4200 device, except the ROM has been removed; pins have been added to output the ROM address to input ROM data. In a system, the WD4020 performs exactly like the WD4200; this important benefit facilitates development and debug of a WD4200 program prior to masking the final part. These devices are also appropriate in low volume applications, or when the program may require changing.

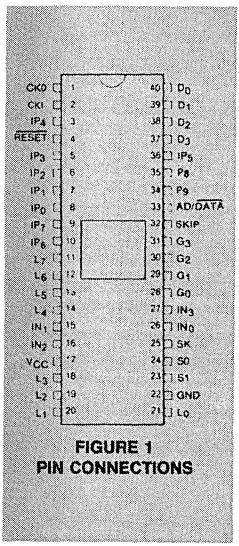


FIGURE 1
PIN CONNECTIONS

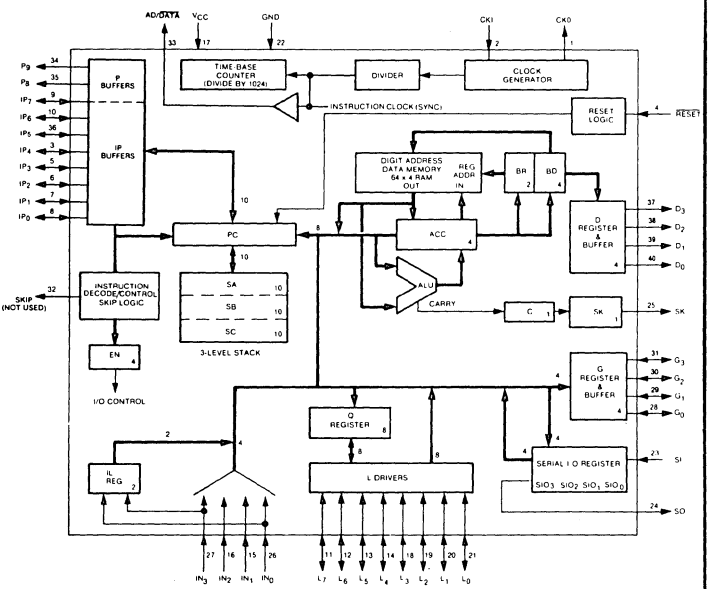


FIGURE 2 WD4020 BLOCK DIAGRAM

SECTION 4

Pin No.	Symbol	Description
1	CKO	System oscillator output
2	CKI	System oscillator input
3,5,6,7,8, 9,10,36	$IP_0 - IP_7$	8 bidirectional ROM address and data ports
4	$\overline{RESET}$	System reset input
11,12,13,14, 18,19,20,21	$L_0 - L_7$	8 bidirectional I/O ports with TRI-STATE®
15,16,26,27	$IN_0 - IN_3$	4 general purpose inputs
17	V_{CC}	Power supply
22	GND	Ground
23	SI	Serial input (or counter input)
24	SO	Serial output (or general purpose output)
25	SK	Logic-controlled clock (or general purpose output)
28,29,30,31	$G_0 - G_3$	4 bidirectional I/O ports
32	SKIP	Instruction skip output
33	AD/$\overline{DATA}$	Address out/data in flag
34, 35	$P_8 - P_9$	2 ROM address outputs
37,38,39,40	$D_0 - D_3$	4 general purpose outputs

Absolute Maximum Ratings

Voltage at Any Pin Relative to GND:	−0.5V to + 7V
Ambient Operating Temperature WD4020A,B	0°C to +70°C
WD4020AE, BE:	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C
	0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	V_{CC} = 5V, T_A = 25°C (all inputs and outputs open)		30	mA
Input Voltage Levels				
CKI Input Levels				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
RESET Input Levels				
Logic High		0.7 V_{CC}		V
Logic Low			0.6	V
RESET Hysteresis		1.0		V
SO Input Level (Test mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = max	3.0		V
Logic High	V_{CC} = 5V ± 5%	2.0		V
Logic Low			0.8	V
Output Voltage Levels (Note 2)				
TTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = 100μA	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6mA		0.4	V
CMOS Operation				
Logic High (V_{OH})	I_{OH} = 10μA	V_{CC} − 1		V
Logic Low (V_{OL})	I_{OL} = −10μA		0.2	V
Output Current Levels				
LED Direct Drive Output	V_{CC} = 6V			
Logic High (I_{OH})	V_{OH} = 2.0V	2.5	14	mA
TRI-STATE® Output Leakage Current		−10	+10	μA

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time—t_c	figure 3a	4	10	μs
CKI Using Crystal				
Input Frequency—f_I	+16 mode	1.6	4	MHz
Duty Cycle (Note 2)	figure 3a	30	55	%
INPUTS:				
IN_3–IN_0, G_3–G_0, L_7–L_0				
t_{SETUP}		1.7		μs
t_{HOLD}		100		ns
SI, IP_7–IP_0				
t_{SETUP}		0.3		μs
t_{HOLD}		100		ns
OUTPUTS:				
COP TO CMOS PROPAGATION DELAY	$4.5V \leq V_{CC} \leq 6.3V$, C_L = 50 pF, $V_{OH} = 0.7\ V_{CC}$, $V_{OL} = 0.3\ V_{CC}$			
SK as a Logic-Controlled Clock				
t_{PD1}			1.1	μs
t_{PD0}			0.3	μs
SO, SK as a Data Output				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
t_{PD1}	V_{OH} = 2V		0.7	μs
D_3–D_0, G_3–G_0				
t_{PD1}			1.6	μs
t_{PD0}			0.6	μs
L_7–L_0 (LED Direct Drive)				
t_{PD1}	V_{OH} = 2V		2.4	μs
t_{PD0}			0.4	μs
COP TO TTL PROPAGATION DELAY	fanout = 1 Standard TTL Load V_{CC} = 5V ± 5%, C_L = 50pF, V_{OH} = 2.4V, V_{OL} = 0.4V			
$\overline{AD/DATA}$				
t_{PD1}			0.5	μs
t_{PD0}			0.5	μs
SKIP				
t_{PD1}			0.6	μs
t_{PD0}			0.6	μs
SK as a Logic-Controlled Clock				
t_{PD1}			0.8	μs
t_{PD0}			0.8	μs
SK as a Data Output, SO				
t_{PD1}			1.0	μs
t_{PD0}			1.0	μs

AC ELECTRICAL CHARACTERISTICS (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
OUTPUTS (cont.):				
D_3-D_0, G_3-G_0				
t_{PD1}			1.3	μs
t_{PD0}			1.3	μs
L_7-L_0				
t_{PD1}			1.4	μs
t_{PD0}			0.4	μs
IP_7-IP_0, P_9, P_8				
t_{PD1}			1.5	μs
t_{PD0}			1.5	μs
CKO (figure 3b)				
t_{PD1}			0.2	μs
t_{PD0}			0.2	μs

Note 1: Duty Cycle = $t_{WI}/(t_{WI} + t_{WO})$.

Note 2: See WD4200 data sheet for additional I/O characteristics and instruction set description

Note 3: I/O options on WD4020 are: CKI/CKO = "xtal osc," L-PORT = "LED direct drive," IN-PORT, SI, RESET = "pullup," G, D-PORTS, SO, SK = "standard out," FUNCTION = "non-microbus™."*

*TRI-STATE, MICROBUS are copyrighted by National Semiconductor Corporation

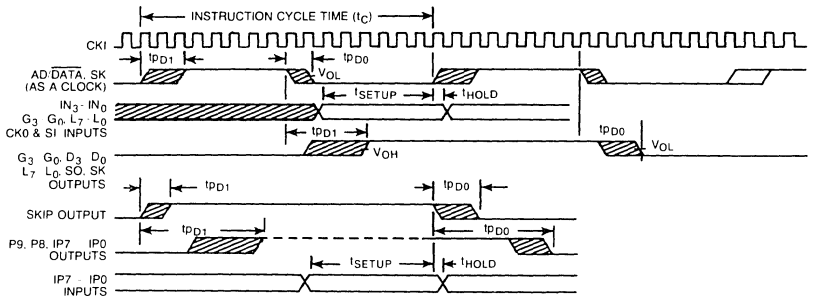


Figure 3a. Input/Output Timing Diagrams (Crystal ÷ 16 Mode)

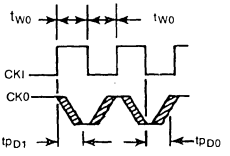


Figure 3b. CKO Output Timing

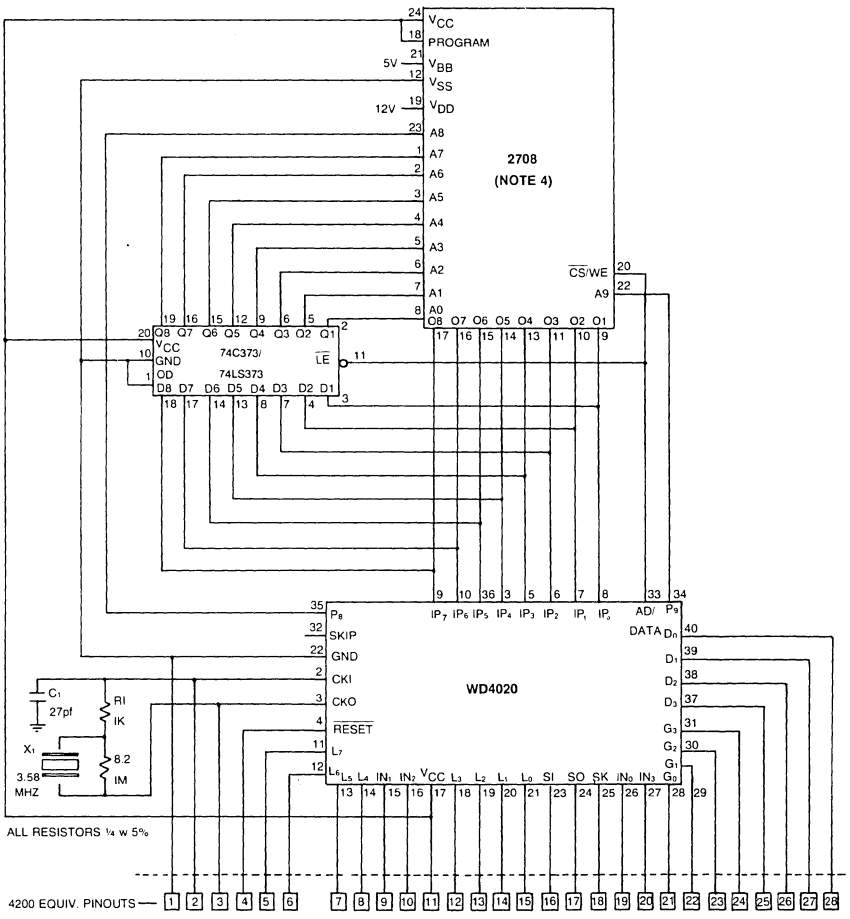
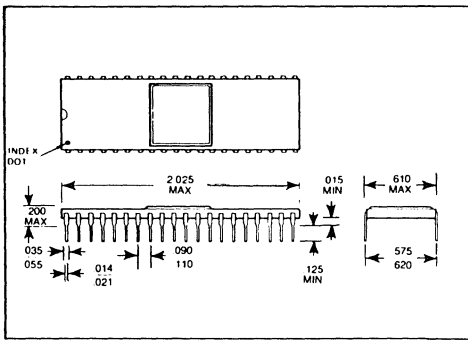
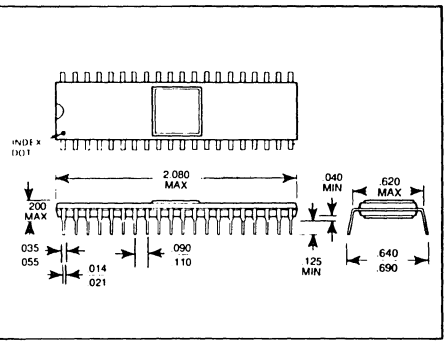


FIGURE 4 WD4020 WITH EPROM USED TO EMULATE WD4200 OR AS A LOW COST "3-CHIP" MICROCOMPUTER



WD4020A CERAMIC PACKAGE



WD4020B PLASTIC PACKAGE

ORDERING INFORMATION:

WD4020A: −0 → + 70°C, CERAMIC PACKAGE
WD4020AE: −40 → + 85°C, CERAMIC PACKAGE
WD4020B: −0 → + 70°C, PLASTIC PACKAGE
WD4020BE: −40 → + 85°C, PLASTIC PACKAGE

SECTION 4

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