WESTERN DIGITAL
CORPORATION

WD5869 Dynamic Shift Register

MARCH, 1981

FEATURES

- DUAL 640 BIT
- ADDITIONAL TAPS AT 512 ON EACH REGISTER
- INTERNAL CLOCKING
- HIGH SPEED
- 3 STATE OUTPUT BUFFER

GENERAL DESCRIPTION

The WD5869 Dual 640 Bit Dynamic Shift Register is a monolithic MOS integrated circuit designed for use in computer display peripherals. The clocks and recirculate logic are internal to reduce system component count, and 3 state output buffers provide bus interface. The WD5869 is available in a 16 pin molded plastic package, or a 16 pin ceramic package.

APPLICATIONS

- CRT DISPLAYS
- COMPUTER PERIPHERALS
- CRYPTOGRAPHY

DUAL IN-LINE PACKAGE

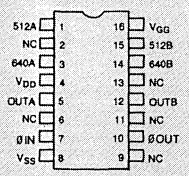


Figure 1
WD5869 PIN CONNECTIONS

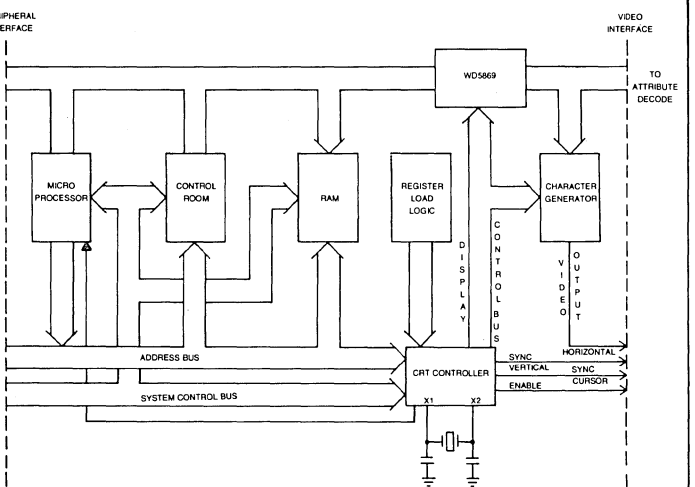


Figure 2 WD5869 TYPICAL APPLICATION BLOCK DIAGRAM

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Data and Clock Input Voltage and Supply Voltages with respect to VSS	+0.3V to −20V
Power Dissipation	800mW at TA = 25°C
Storage Temperature	−55°C to +125°C (Plastic Package) −65°C to +150°C (Ceramic Package)

ELECTRICAL CHARACTERISTICS (DC)

TA = 0°C to + 50°C, V_{SS} = +5V ± 5%, V_{DD} = −5V + 5%, V_{GG} = −12V ± 5%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I_{DD}	POWER SUPPLY CURRENT		−50	mA	
	DATA INPUT LEVELS				
V_{IL}	Logical Low Level	V_{SS}−17.9	V_{SS}−4.2	V	
V_{IH}	Logical High Level	V_{SS}−1.7	V_{SS}+0.3	V	
I_{IL}	DATA INPUT LEAKAGE		10	μA	V_{IN} = −5V; All other Pins GND
C_{di}	DATA INPUT CAPACITANCE		10	pf	V_{IN} = 0V; f = 1MHZ, All other Pins GND
	CLOCK INPUT LEVELS				
V_{OH}	Logical High Level	V_{SS}−1.0	V_{SS}+0.3	V	
V_{OL}	Logical Low Level	V_{SS}−17.9	V_{SS}−14.5	V	
I_{CL}	CLOCK INPUT LEAKAGE		10	μA	V_O = −17.9V; All other Pins GND
C_{ci}	CLOCK INPUT CAPACITANCE		200	pf	V_O = 0V; f = 1MHZ, All other Pins GND
	DATA OUTPUT LEVELS				
V_{OH}	Logical High Level	2.4		V	I Source = −50mA
V_{OL}	Logical Low Level		V_{SS}−0.4	V	I Sink = 1.6 mA

TABLE 1 D.C. PARAMETERS

YMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
	CLOCK FREQUENCY	10	2000	KHz	Øtr = Øtf = 20 ns
ɔw in	CLOCK PULSE WIDTH, In	0.15	1.0	uS	Øtf + Øpw + Øtr ≤ 3.0 uS
pw out	CLOCK PULSE WIDTH, Out	1	1	Øpw in	
d	CLOCK PHASE DELAY TIME, from rising edge	10		ns	
d	CLOCK PHASE DELAY TIME, from falling edge	10		ns	
tr	CLOCK TRANSITION TIME, rising edge		1.0	us	Øtf + Øpw + Øtr ≤ 3.0 uS
tf	CLOCK TRANSITION TIME, falling edge		1.0	us	
ds	DATA INPUT SET-UP TIME	80		ns	
dh	DATA INPUT HOLD TIME	40		ns	
pdl	DATA OUTPUT PROPAGATION DELAY, to low level		200	ns	
pdh	DATA OUTPUT PROPAGATION DELAY, to high level		200	ns	

TABLE 2 A.C. PARAMETERS

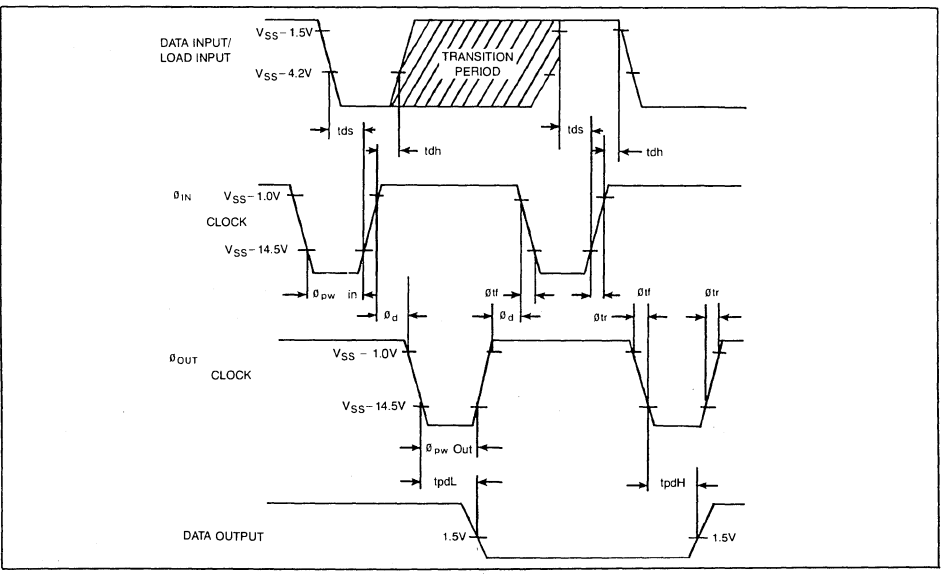
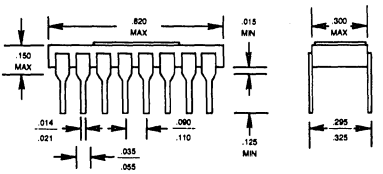
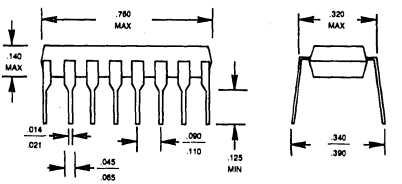


Figure 3 WD5869 TIMING DIAGRAM



WD5869J CERAMIC PACKAGE



WD5869K PLASTIC PACKAGE

WESTERN DIGITAL CORPORATION
3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139