1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

This document describes a single chip VLSI Peripheral Cache Manager, SCSI bus controller, and Disk Controller device, the WD61C96A, for target mode of operation. The WD61C96A is a highly integrated CMOS VLSI device which combines the functionality of the WD61C40A Disk Manager and the WD33C96A SCSI Manager. All of the features of the two separate devices are retained, including:

- 8-bit Parallel Disk Data Bus.
- 4M by 16-bit Buffer Memory Interface.
- 16-bit Wide SCSI Interface.
- Fast SCSI timing.
- Internal DMA transfer between devices.
- External DMA port for connecting a second WD61C40A (208-pin device only).
- Single 8-bit, 25 MHz 80186 Microprocessor port.

1.1.1 Features NOT Included

The only microprocessor bus type supported is multiplexed direct addressing. The other modes supported by the WD33C96A are not available.

1.1.2 Deviations

There are several deviations from the device specifications provided for the WD33C96A and the WD61C40A. These are:

- The I/O Map Test modes are different.
- The DMA (Host) bus is not observable during normal operation on Host Channel A. A test mode is provided to enable the bus to the output. The bus behaves normally for Host Channel B operation, but only for an external WD61C40A slave.
- The WD61C40A portion of the device operates in the burst slave mode and single cycle master mode only and the WD33C96A portion operates in burst and single cycle master mode only.

1.1.3 Microprocessor Interface

The dedicated microprocessor interface supports 8-bit microprocessors with multiplexed address/ data busses. The microprocessor can access the internal registers and FIFO through this port by using the five following control signals: WEB, REB, ALE, CS0, CS2, and RDYB. The device must be externally mapped into a 384 byte space. A chip select, CS0 or CS2, must be presented to this device for any read or write access. CS0 accesses the registers associated with the WD61C40 functions (256-byte space). CS2 accesses the registers associated with the WD33C96 functions (128-byte space).

The WD61C96A sends a Ready signal, RDYB, to the microprocessor whenever an extended read or write strobe is required. This is done when the microprocessor wishes to access the buffer memory.

1.1.4 Host Port Interface

The Host Port is exactly as defined for the WD33C96A: there are two DMA channels available, DREQA/DACKA and DREQB/DACKB. Channel A is dedicated to the internal WD61C40A function which should be programmed as a slave. Channel B is available for use by a second, external WD61C40A device (programmed as a slave), or other generic DMA slave.

Data can be transferred in 8-bit or 16-bit mode. The maximum transfer rate is 10 megatransfers per second.

1.1.5 SCSI Interface

The WD61C96A uses a 32-word by 9-bit (8 bits plus parity) Dual Port Register to store special information such as commands, messages, and status. The information is transferred between the SCSI bus and the registers under control of a writable control store sequence. The microprocessor can randomly access these registers.

1.1.6 Buffer Interface

The buffer port is designed to support 16-bit DRAM configurations up to 4MWords. Memory

size and bus timing are all programmable.

The Buffer Manager reduces microprocessor support and provides buffer segmentation hardware assist logic. Skip mask modes reduce microprocessor interrupts.

1.1.7 Testability

The WD61C96A includes several features to improve testability of the device:

- All RAM and Register files contain internal BIST logic.
- Full scan test methodology.
- Most microprocessor registers are readable.
- Test modes exist for the large transfer counters, address pointers and major internal logic blocks.
- The I/O pins include the I/O Mapping Test feature for PCB testing.
- The Disk Port contains logic which guarantees data integrity (LRC, CRC, ECC checking).
- The Writable Control Store RAMs are read-writable by the microprocessor.
- A host bus test pin allows the internal DMA bus between the WD61C40A and WD33C96A cores to be observed on the host bus pins.

1.2 FEATURES

- High Flexibility
- Programmable SCSI data bus width.
  - — Programmable synchronous transfer period.
  - — Programmable DMA data bus width.
  - — Programmable DMA transfer period.
  - — Programmable DRQ and DACK polarities.
  - — Sequencer with a writable control store.
  - — Capability for direct control of the SCSI signals by the microprocessor.
  - — Support for specifying transfer lengths in logical and physical blocks.
- High Performance
  - — High-speed SCSI transfers, up to 10 Mtransfers/s.
  - — Fast DMA transfer rate, up to 10 Mtransfers/s.
  - — Dedicated eight-bit port for a high-speed microprocessor.
  - — Pipelined 24-bit transfer counter.
  - — Two DMA ports (one internal, one external) to support striping and mirroring.
  - — Sixteen-word FIFO supports synchronous offsets up to sixteen words or thirty-two bytes.
- Low Overhead
  - — Minimal SCSI bus overhead and latency.
  - — Automatic response to selection and reselection.
  - — Automatic decoding of SCSI command descriptor block lengths.
  - — Automatic response to DMA requests.
  - — Efficient interaction with the external and internal WD61C40A Disk Controller to minimize microprocessor overhead.
  - — Interrupt masking capability.
- Data Integrity
  - — Longitudinal Redundancy Check (LRC) feature maximizes data transfer integrity.
  - — Support for data mirroring and striping.
  - — Parity on all internal data busses and on the FIFO and Dual Port registers.
  - — Built-in Self Test (BIST) logic for the Writable Control Store, FIFO, and Dual Port registers.
- Other Features
  - — 48 mA drivers for direct connection to a single-ended SCSI interface.
  - — Support for external drivers and receivers for single-ended and differential applications (WD33C96A).
  - — Single +5 V supply.
  - — Sleep mode minimizes power consumption.
  - — 176-pin SQFP and PQUAD packages
  - — 208-pin MQFP packages

1.3 ORDERING INFORMATION

The WD61C96A is available in three package options (SW, QW and MZ) with four different bonding options (A, B, C, and D). See Table 3-1, OPTIONAL PACKAGE FEATURES, on page 5 for a description of the packing options. Following are the device order numbers:

ORDER P/N	DESCRIPTION
61C96ASWA01	SQFP, 176 pins, bonding Option A
61C96ASWC01	SQFP, 176 pins, bonding Option C
61C96AQWA01	PQUAD, 176 pins, bonding Option A
61C96AQWC01	PQUAD, 176 pins, bonding Option C
61C96AMZB01	MQFP w/heat spreader, 208 pins, bonding Option B
61C96AMZD01	MQFP w/heat spreader, 208 pins, bonding Option D

1.4 REFERENCE DOCUMENTS

For additional information, please consult the following Western Digital publications:

- WD33C96A SCSI Protocol Chip Specification 96 - 100242.
- WD61C40A High-Performance Disk Manager Engineering Specification 96-106140.
- WD10C01 Disk Controller Specification 96-101474.

1.5 DOCUMENT SCOPE

This document provides an architectural overview, signal descriptions, register descriptions, theory of operations, and timing specifications for the WD61C96A. This device is used to control SCSI disks in the target mode of operation. Other topics covered are: Disk/SCSI Control Store, Disk/SCSI LRC operations, error correction, Disk/SCSI interrupts, and test modes.

2.0 ARCHITECTURE OVERVIEW

The WD61C96A is a combination of the WD61C40A (Disk Manager) and WD33C96A (SCSI Bus Manager) devices.

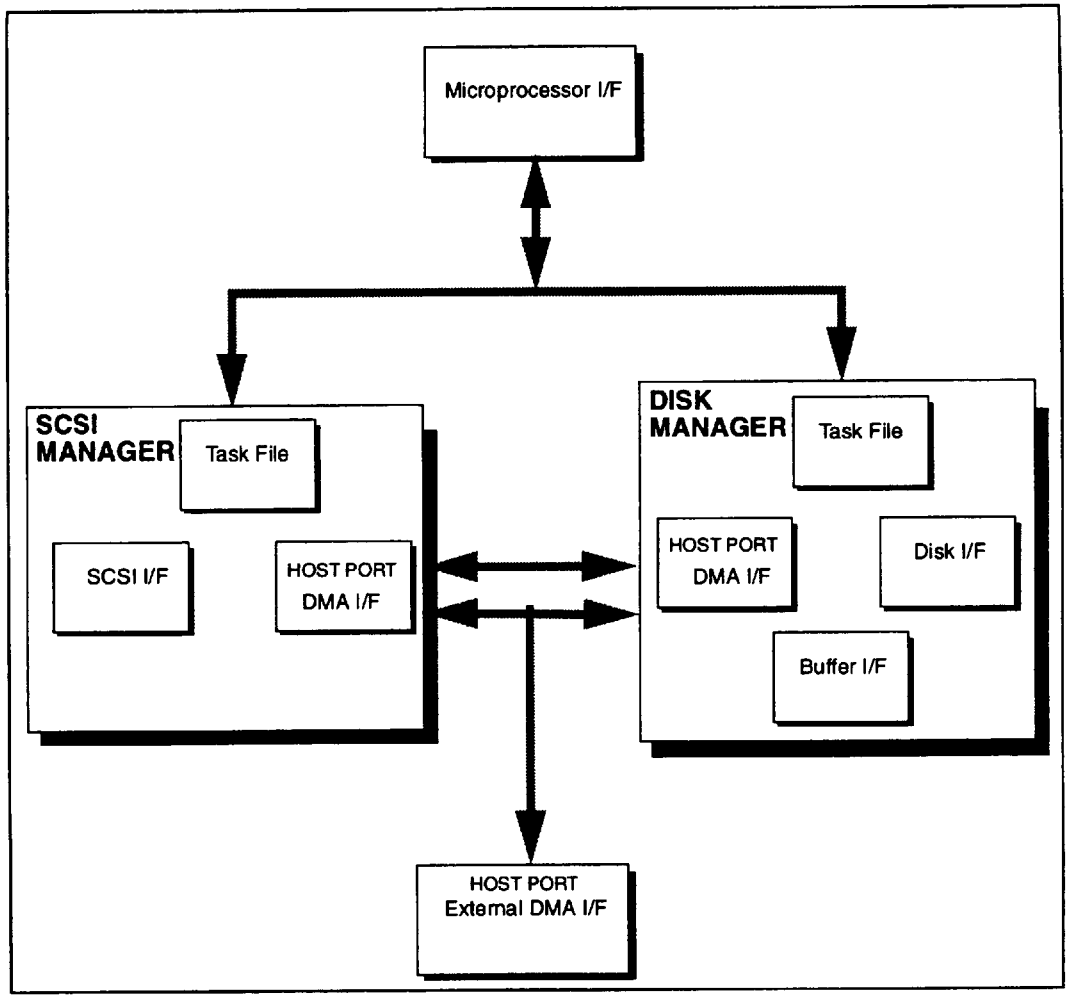

FIGURE 2-1 BLOCK DIAGRAM OF WD61C96A

The SCSI Block contains all of the functions of the WD33C96A, including a Task File of microprocessor accessible registers, a 16-bit Wide/Fast SCSI Interface, and a 16-bit DMA Interface.

The Disk Block contains all of the functions of the WD61C40A, including a Task File of microprocessor accessible registers, a 16-bit Buffer Interface, an 8-bit Disk Interface and a 16-bit DMA Interface.

The External DMA Interface is used to connect a second WD61C40A as a DMA slave.

The Microprocessor Interface contains logic which supports a multiplexed data/address bus microprocessor with wait state capabilities. Note that this is the only mode supported. This includes Intel 80196 and 80186 devices.

3.0 SIGNAL DESCRIPTION

The WD61C96A device has four bonding options. These options make trade-offs between:

1. Single-ended Only and Single-ended/Differential SCSI support
2. Single and Dual LUN support
3. Quantity of GPX, GPY, POR latch pins, Optional Functional features

Table 3-1 describes the features of each package type. Tables 3-2 through 3-5 list the pin/signals for each option. Refer to Appendix A for more information concerning packaging.

FEATURES	OPTION A	OPTION B	OPTION C	OPTION D
Package Pins	176	208	176	208
Single Ended SCSI	yes	yes	yes	yes
Differential SCSI	no	yes	no	yes
Single LUN	yes	yes	yes	yes
Dual LUN	no	yes	no	yes
GPX Pins	8 (GPX7:0)	5 (GPX4:0)	8 (GPX7:0)	0
GPY Pins	4 (GPY3:0)	4 (GPY3:0)	4 (GPY3:0)	4 (GPY3:0)
POR Pins	Total: 12 (BD15:11, BDP10:9, BDP4:3, BD2:0) Not bonded: BD8:5	Total: 16 (DB15:0)	Total: 7 (BD15:13, BDP10, BDP4:3, BD0) Not bonded: BD8:5, BDP9, BD2:1, BD12:11	Total: 16 (BD15:0)

TABLE 3-1 OPTIONAL PACKAGE FEATURES

All outputs are tristated when the Power on reset, RESETB, is active (low) **except:**

- RDYB is released open-drain.
- RSTF is low.
- SDOE[15:0], SDPOE, TGS, and IGS are low.

PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL
1 - DGND	37 - CGND	73 - SD11	109 - RST	145 - GPY1
2 - BF5	38 - RDGATE	74 - SD10	110 - TST2B	146 - GPY0
3 - BF6	39 - WRTGATE	75 - SD9	111 - CVDD	147 - GPX0
4 - DGND	40 - DATA0	76 - DGND	112 - CGND	148 - A8
5 - BF7	41 - DATA1	77 - SD8	113 - SCTL	149 - DGND
6 - BFPL	42 - DATA 2	78 - DVDD	114 - WEB	150 - A7
7 - DGND	43 - DGND	79 - CVDD	115 - REB	151 - A6
8 - BF8	44 - DATA3	80 - CGND	116 - CS0	152 - A5
9 - GPX3	45 - DATA4	81 - SDP1	117 - CS2	153 - A4
10 - BF9	46 - DVDD	82 - SDP	118 - ALE	154 - BCLK
11 - DGND	47 - DATA5	83 - DGND	119 - RESETB	155 - DVDD
12 - BF10	48 - DATA6	84 - SD7	120 - GPX7	156 - CVDD
13 - BD11	49 - DGND	85 - SD6	121 - AD7	157 - CGND
14 - BF11	50 - DATA7	86 - SD5	122 - DGND	158 - A3
15 - CVDD	51 - DATAP	87 - DGND	123 - AD6	159 - A2
16 - CGND	52 - GPX4	88 - REQ	124 - AD5	160 - DGND
17 - DGND	53 - AMDET	89 - SD4	125 - GPX6	161 - A1
18 - BD12	54 - RRCLK	90 - SE	126 - AD4	162 - A0
19 - BF12	55 - GPX5	91 - SD3	127 - DGND	163 - GPX1
20 - DVDD	56 - WRAP	92 - DGND	128 - AD3	164 - BD0
21 - BD13	57 - DRVFLT	93 - SD2	129 - AD2	165 - BF0
22 - BF13	58 - BDP9	94 - SD1	130 - DVDD	166 - DGND
23 - DGND	59 - SMDET	95 - CVDD	131 - AD1	167 - BD1
24 - BD14	60 - BDP4	96 - CGND	132 - BDP10	168 - BF1
25 - BF14	61 - CVDD	97 - SD0	133 - DGND	169 - BD2
26 - BD15	62 - CGND	98 - DGND	134 - AD0	170 - BF2
27 - BF15	63 - IDXDET	99 - SEL	135 - RSTF	171 - DGND
28 - DGND	64 - BDP3	100 - DVDD	136 - CVDD	172 - BF3
29 - BFPH	65 - TST1B	101 - IO	137 - CGND	173 - BF4
30 - GPX2	66 - SCLK	102 - ATN	138 - INT2	174 - CVDD
31 - MEMW	67 - SD15	103 - DGND	139 - INT1	175 - CGND
32 - CAS	68 - DGND	104 - BSY	140 - INT0	176 - DVDD
33 - RAS	69 - SD14	105 - ACK	141 - RDY	
34 - DGND	70 - SD13	106 - CD	142 - DGND	
35 - WRTCLK	71 - SD12	107 - DGND	143 - GPY3	
36 - CVDD	72 - DGND	108 - MSG	144 - GPY2	

TABLE 3-2 PIN TO SIGNAL (OPTION A - 176-PIN SQFP)

PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL
1 - DATA3	37 - BF9	73 - DGND	109 - DGND	145 - SDOE1	181 - DGND
2 - DGND	38 - BD9	74 - A2	110 - AD4	146 - CGND	182 - SD12
3 - DATA2	39 - GPX3	75 - DRQB	111 =- AD5	147 - CVDD	183 - SDOE12
4 - DATA1	40 - BF8	76 - A3	112 - AD6	148 - SD1	184 - SDOE13
5 - DATA0	41 - BD8	77 - DACKB	113 - DGND	149 - SDOE2	185 - SD13
6 - WRTGATE	42 - DGND	78 - CGND	114 - AD7	150 - SD2	186 - SDOE14
7 - RDGATE	43 - BFPL	79 - CVDD	115 - RESETB	151 - DGND	187 - SD14
8 - CGND	44 - BDPL	80 - DVDD	116 - ALE	152 - SD3	188 - DGND
9 - CVDD	45 - BF7	81 - BCLK	117 - CS2	153 - SDOE3	189 - SD15
10 - WRTCLK	46 - BD7	82 - A4	118 - CS0	154 - SE	190 - SDOE15
11 - DGND	47 - DGND	83 - A5	119 - REB	155 - SDOE4	191 - SCLK
12 - RAS	48 - BF6	84 - A6	120 - WEB	156 - SD4	192 - TST1B
13 - CAS	49 - BD6	85 - A7	121 - SCTL	157 - REQ	193 - BDP3
14 - MEMW	50 - BF5	86 - DGND	122 - CGND	158 - DGND	194 - IDXDET
15 - GPX2	51 - BD5	87 - A8	123 - CVDD	159 - SD5	195 - CVDD
16 - BFPH	52 - DGND	88 - DWEB	124 - TSTB	160 - SDOE5	196 - SMDET
17 - BDPH	53 - DVDD	89 - DREB	125 - RSTIN	161 - SDOE6	197 - DRVFLT
18 - DGND	54 - CGND	90 - GPX0	126 - RST	162 - SD6	198 - WRAP
19 - BF15	55 - CVDD	91 - GPY0	127 - MSG	163 - SDOE7	199 - RRCLK
20 - BD15	56 - BF4	92 - GPY1	128 - DGND	164 - SD7	200 - AMDET
21 - BF14	57 - BD4	93 - GPY2	129 - CD	165 - DGND	201 - GPX4
22 - BD14	58 - BF3	94 - GPY3	130 - ACK	166 - SDP	202 - DATAP
23 - DGND	59 - BD3	95 - DGND	131 - DSENSE	167 - SDPOE	203 - DATA7
24 - BF13	60 - DGND	96 - RDY	132 - TGS	168 - SDP1	204 - DGND
25 - BD13	61 - BF2	97 - INT0	133 - BSYIN	169 - SDOE8	205 - DATA6
26 - DVDD	62 - BD2	98 - INT1	134 - BSY	170 - CGND	206 - DATA5
27 - BF12	63 - BF1	99 - INT2	135 - DGND	171 - CVDD	207 - DVDD
28 - BD12	64 - BD1	100 - CGND	136 - ATN	172 - DVDD	208 - DATA4
29 - DGND	65 - DGND	101 - CVDD	137 - IO	173 - SD8	
30 - CGND	66 - BF0	102 - RSTF	138 - IGS	174 - DGND	
31 - CVDD	67 - BD0	103 - AD0	139 - DVDD	175 - SD9	
32 - BF11	68 - GPX1	104 - DGND	140 - SELIN	176 - SDOE9	
33 - BD11	69 - DRQA	105 - AD1	141 - SEL	177 - SDOE10	
34 - BF10	70 - A0	106 - DVDD	142 - DGND	178 - SD10	
35 - BD10	71 - DACKA	107 - AD2	143 - SD0	179 - SDOE11	
36 - DGND	72 - A1	108 - AD3	144 - SDOE0	180 - SD11	

TABLE 3-3 PIN TO SIGNAL (OPTION B - 208-PIN MQFP)

PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL
1 - DGND	37 - CGND	73 - SD11	109 - RST	145 - GPY1
2 - BF5	38 - RDGATE	74 - SD10	110 - TST2B	146 - GPY0
3 - BF6	39 - WRTGATE	75 - SD9	111 - CVDD	147 - GPX0
4 - DGND	40 - DATA0	76 - DGND	112 - CGND	148 - A10
5 - BF7	41 - DATA1	77 - SD8	113 - SCTL	149 - A9
6 - BFPL	42 - DATA 2	78 - DVDD	114 - WEB	150 - A8
7 - DGND	43 - DGND	79 - CVDD	115 - REB	151 - DGND
8 - BF8	44 - DATA3	80 - CGND	116 - CS0	152 - A7
9 - GPX3	45 - DATA4	81 - SDP1	117 - CS2	153 - A6
10 - BF9	46 - DVDD	82 - SDP	118 - ALE	154 - A5
11 - DGND	47 - DATA5	83 - DGND	119 - RESETB	155 - A4
12 - BF10	48 - DATA6	84 - SD7	120 - GPX7	156 - BCLK
13 - BF11	49 - DGND	85 - SD6	121 - AD7	157 - DVDD
14 - CVDD	50 - DATA7	86 - SD5	122 - DGND	158 - CVDD
15 - CGND	51 - DATAP	87 - DGND	123 - AD6	159 - CGND
16 - DGND	52 - GPX4	88 - REQ	124 - AD5	160 - A3
17 - BF12	53 - AMDET	89 - SD4	125 - GPX6	161 - A2
18 - DVDD	54 - RRCLK	90 - SE	126 - AD4	162 - DGND
19 - BD13	55 - GPX5	91 - SD3	127 - DGND	163 - A1
20 - BF13	56 - WRAP	92 - DGND	128 - AD3	164 -A0
21 - DGND	57 - DRVFLT	93 - SD2	129 - AD2	165 - GPX1
22 - BD14	58 - CMPLT	94 - SD1	130 - DVDD	166 - BD0
23 - BF14	59 - SMDET	95 - CVDD	131 - AD1	167 - BF0
24 - BD15	60 - BDP4	96 - CGND	132 - BDP10	168 - DGND
25 -BF15	61 - CVDD	97 - SD0	133 - DGND	169 - BF1
26 - DGND	62 - CGND	98 - DGND	134 - AD0	170 - BF2
27 - BFPH	63 - IDXDET	99 - SEL	135 - RSTF	171 - DGND
28 - GPX2	64 - BDP3	100 - DVDD	136 - CVDD	172 - BF3
29 - MEMW	65 - TST1B	101 - IO	137 - CGND	173 - BF4
30 - CAS	66 - SCLK	102 - ATN	138 - INT2	174 - CVDD
31 - RAS	67 - SD15	103 - DGND	139 - INT1	175 - CGND
32 - DGND	68 - DGND	104 - BSY	140 - INT0	176 - DVDD
33 - WRTCLK	69 - SD14	105 - ACK	141 - RDY	
34 - AMENA	70 - SD13	106 - CD	142 - DGND	
35 - SQOUT	71 - SD12	107 - DGND	143 - GPY3	
36 - CVDD	72 - DGND	108 - MSG	144 - GPY2	

TABLE 3-4 PIN TO SIGNAL (OPTION C - 176-PIN SQFP)

PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL	PIN - SIGNAL
1 - DATA3	37 - DGND	73 - A2	109 - DGND	145 - SDOE1	181 - DGND
2 - DGND	38 - BF9	74 - DRQB	110 - AD4	146 - CGND	182 - SD12
3 - DATA2	39 - BD9	75 - A3	111 =- AD5	147 - CVDD	183 - SDOE12
4 - DATA1	40 - BF8	76 - DACKB	112 - AD6	148 - SD1	184 - SDOE13
5 - DATA0	41 - BD8	77 - CGND	113 - DGND	149 - SDOE2	185 - SD13
6 - WRTGATE	42 - DGND	78 - CVDD	114 - AD7	150 - SD2	186 - SDOE14
7 - RDGATE	43 - BFPL	79 - DVDD	115 - RESETB	151 - DGND	187 - SD14
8 - CGND	44 - BDPL	80 - BCLK	116 - ALE	152 - SD3	188 - DGND
9 - CVDD	45 - BF7	81 - A4	117 - CS2	153 - SDOE3	189 - SD15
10 - SQOUT	46 - BD7	82 - A5	118 - CS0	154 - SE	190 - SDOE15
11 - AMENA	47 - DGND	83 - A6	119 - REB	155 - SDOE4	191 - SCLK
12 - WRTCLK	48 - BF6	84 - A7	120 - WEB	156 - SD4	192 - TST1B
13 - DGND	49 - BD6	85 - DGND	121 - SCTL	157 - REQ	193 - IDXDET
14 - RAS	50 - BF5	86 - A8	122 - CGND	158 - DGND	194 - CGND
15 - CAS	51 - BD5	87 - A9	123 - CVDD	159 - SD5	195 - CVDD
16 - MEMW	52 - DGND	88 - A10	124 - TSTB	160 - SDOE5	196 - SMDET
17 - BFPH	53 - DVDD	89 - DWEB	125 - RSTIN	161 - SDOE6	197 - CMPLT
18 - BDPH	54 - CGND	90 - DREB	126 - RST	162 - SD6	198 - DRVFLT
19 - DGND	55 - CVDD	91 - GPY0	127 - MSG	163 - SDOE7	199 - WRAP
20 - BF15	56 - BF4	92 - GPY1	128 - DGND	164 - SD7	200 - RRCLK
21 - BD15	57 - BD4	93 - GPY2	129 - CD	165 - DGND	201 - AMDET
22 - BF14	58 - BF3	94 - GPY3	130 - ACK	166 - SDP	202 - DATAP
23 - BD14	59 - BD3	95 - DGND	131 - DSENSE	167 - SDPOE	203 - DATA7
24 - DGND	60 - DGND	96 - RDY	132 - TGS	168 - SDP1	204 - DGND
25 - BF13	61 - BF2	97 - INT0	133 - BSYIN	169 - SDOE8	205 - DATA6
26 - BD13	62 - BD2	98 - INT1	134 - BSY	170 - CGND	206 - DATA5
27 - DVDD	63 - BF1	99 - INT2	135 - DGND	171 - CVDD	207 - DVDD
28 - BF12	64 - BD1	100 - CGND	136 - ATN	172 - DVDD	208 - DATA4
29 - BD12	65 - DGND	101 - CVDD	137 - IO	173 - SD8	
30 - DGND	66 - BF0	102 - RSTF	138 - IGS	174 - DGND	
31 - CGND	67 - BD0	103 - AD0	139 - DVDD	175 - SD9	
32 - CVDD	68 - DRQA	104 - DGND	140 - SELIN	176 - SDOE9	
33 - BF11	69 - A0	105 - AD1	141 - SEL	177 - SDOE10	
34 - BD11	70 - DACKA	106 - DVDD	142 - DGND	178 - SD10	
35 - BF10	71 - A1	107 - AD2	143 - SD0	179 - SDOE11	
36 - BD10	72 - DGND	108 - AD3	144 - SDOE0	180 - SD11	

TABLE 3-5 PIN TO SIGNAL (OPTION D - 208-PIN MQFP)

The following table shows the four different pinout options available for the WD61C96A:

- Option A - 176-pin, SQFP
- Option B - 208-pin, MQFP
- Option C - 176-pin SQFP
- Option D - 208-pin, MQFP

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
MICROPROCESSOR INTERFACE						
118	116	118	116	ALE	I	**ADDRESS LATCH ENABLE.** This signal is used to load the address of desired register.
115	119	115	119	REB	I	**READ ENABLE.** This signal is active low and it is used with CS0 or CS2 signal to read the registers.(Active Low)
114	120	114	120	WEB	I	**WRITE ENABLE.** This signal is active low and it is used with the CS0 or CS2 signal to write into the registers. (Active Low)
116	118	116	118	CS0	I	**CHIP SELECT 0.** This signal is active low and is used to qualify REB and WEB signals when the microprocessor is accessing a register. CS0 is used to select DISK Manager functions.
117	117	117	117	CS2	I	**CHIP SELECT 2.** This signal is active low and is used to qualify REB and WEB signals when the microprocessor is accessing a register. CS2 is used to select SCSI Manager functions.
138 139 140	99 98 97	138 139 140	99 98 97	INT 2 INT 1 INT 0	O	**INTERRUPT REQUESTS.** These output signals are active high. They are asserted to alert the microprocessor indicating a completion or termination of a command. INT0 and INT1 are used for Disk Manager interrupts. INT2 is used for SCSI interrupts.
121 123 123 126 128 129 131 134	114 112 111 110 108 107 105 103	121 123 123 126 128 129 131 134	114 112 111 110 108 107 105 103	AD[7:0]	I/O	**MICROPROCESSOR DATA/ADDRESS BUS**

TABLE 3-6 SIGNAL DESCRIPTION

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
MICROPROCESSOR INTERFACE (Continued)						
141	96	141	96	RDY	O	**READY.** This is an open drain output that controls the microprocessor's wait logic. (Active High)
HOST (DMA) INTERFACE						
-	69	-	68	DRQA	I/O	**DMA REQUEST A.** The function of this pin is programmable and is defined by the control bits. In normal operation, this pin is tristated since this signal is dedicated to the internal DMA channel. This pin is only driven externally when in a test mode.
-	70	-	71	DACKA	I/O	**DMA ACKNOWLEDGE A.** The function of this pin is programmable and is defined by the control bits. In normal operation, this pin is tristated since this signal is dedicated to the internal DMA channel. This pin is only driven externally when in a test mode
-	75	-	74	DRQB	I/O	**DMA REQUEST B.** The function of this pin is programmable and is defined by the control bits. This pin is normally driven by an external DMA slave.
-	77	-	76	DACKB	I/O	**DMA ACKNOWLEDGE B.** The function of this pin is programmable and is defined by the control bits. This pin is normally driven out to an external DMA device
-	88	-	89	DWEB		**DMA WRITE ENABLE**, (Active low). This pin is only driven externally when in a test mode, or when an external DMA device is being serviced.
-	89	-	90	DREB		**DMA READ ENABLE**, (Active low). This pin is only driven externally when in a test mode, or when an external DMA device is being serviced.

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
HOST (DMA) INTERFACE (Continued)						
26 24 21 18 13 - - - - - - - - 169 167 164	20 22 25 28 33 35 38 41 46 49 51 57 59 62 64 67	24 22 19 - - - - - - - - - - - - 166	21 23 26 29 34 36 39 41 46 49 51 57 59 62 64 67	BD[15:0]	I/O	**HOST DMA BUS.** These pins are only driven externally when in a test mode, or when an external DMA device is being serviced.
-	44	-	44	BDPL	I/O	**PARITY OF THE LOWER DMA BUS.** This pin carries the odd parity for the BD7 through BD0. This pin is only driven externally when in a test mode, or when an external DMA device is being serviced.
-	17	-	18	BDPH	I/O	**PARITY OF THE UPPER DMA BUS.** This pin carries the odd parity for the BD15 through BD8. This pin is only driven externally when in a test mode, or when an external DMA device is being serviced

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
DISK INTERFACE						
50	203	50	203	DATA[7:O]	I/O	**DISK DRIVE PARALELL DATA BUS**
48	205	48	205			
47	206	47	206			
45	208	45	208			
44	1	44	1			
42	3	42	3			
41	4	41	4			
40	5	40	5			
51	202	51	202	DATAP	I/O	**DISK PARALLEL DATA BUS PARITY.** Odd or even parity is selectable. See section 4.3.5 on page 32.
54	199	54	200	RRCLK	I	**READ REFERENCE CLOCK.** This clock is generated by the Disk Read Channel. All WD61C96A disk control and data pins are synchronized to this clock.
35	10	33	12	WRTCLK	O	**WRITE CLOCK.** This pin is the inversion of the RRCLK.
38	7	38	7	RDGATE	O	**READ GATE.** This signal is controlled by the Control Store.
39	6	39	6	WRTGATE	O	**WRITE GATE.** This signal is controlled by the Control Store.
63	194	63	193	IDXDET	I	**INDEX DETECT.** This signal is generated by the Read/Write logic when an index mark is detected.
59	196	59	196	SMDET	I	**SECTOR MARK DETECT.** This generated by the Read/Write logic when a sector mark is found.
-	-	34	11	AMENA	O	**ADDRESS MARK ENABLE.** In write mode, this signal indicates to the write channel that an address mark byte is being send on the DATA[0:7] lines. In read mode, this signal flags the read channel on the type of sync bytes is to be detected. When RDGATE and WRTGATE are inactive, this signal indicates a search for an ID Address mark. (Not tristated on reset conditions)

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
DISK INTERFACE (Continued)						
53	200	53	201	AMDET	I	**ADDRESS MARK DETECT.** The Read Channel generates this signal when an ID address mark (or optional Sync Bytes) are detected.
-	-	58	197	CMPLT	I	**SEEK COMPLETE.** This is a general purpose flag from the drive electronics. This signal is active only when the WCS is in operation. When this signal is active an interrupt can be generated by the WD61C96A.
-	-	35	10	SEQOUT	O	**SEQUENCE OUT.** This is a general purpose control line that is controlled directly from the Control Store.
57	197	57	198	DRVFLT	I	**DRIVE FAULT.** This is a general purpose flag from the drive electronics. This is typically an indication of a drive failure. When this signal, is active an interrupt is generated by the WD61C96A. As an option, the Control Store can respond to this error condition and jump to the error routine.
120 125 55 52 9 30 163 147	- - - 201 39 15 68 90	120 125 55 52 9 28 165 147	- - - - - - - -	GPX[7:0]	I/O	**GENERAL PURPOSE PORT.** These pins can be configured as generic input or output pins.
143 - 146	94 - 91	143 - 146	94 - 91	GPY[3:0]	I/O	**GENERAL PURPOSE PORT.** These pins can be configured as generic input or output pins.

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
56	198	56	199	WRAP	I	**WRAP CHECK.** In options C and D, this pin is used to verify that the RDGATE, WRTGATE, and AMENA signals are properly connected to the drive electronics. In options A and B, this pin is used to verify that RDGATE and WRTGATE are properly connected to the drive electronics. An Interrupt is also generated when an error is detected.
SCSI INTERFACE						
105	130	105	130	ACK	I/O	**SCSI ACKNOWLEDGE.**
102	136	102	136	ATN	I/O	**SCSI ATTENTION.**
104	134	104	134	BSY	I/O	**SCSI BUSY** (Single ended) or **BUSY OUTPUT** (Differential)
-	133	-	133	BSYIN	I	**SCSI BUSY INPUT** (Differential mode only, active low.)
106	129	106	129	C/D	I/O	**SCSI COMMAND/DATA.**
101	137	101	137	I/O	I/O	**SCSI INPUT/OUTPUT.**
108	127	108	127	MSG	I/O	**SCSI MESSAGE.**
88	157	88	157	REQ	I/O	**SCSI REQUEST.**
109	126	109	127	RST	I/O	**SCSI RESET I/O** (Single ended) or **RESET OUTPUT** (Differential).
-	125	-	125	RSTIN	I	**SCSI RESET IN** (Differential mode only, active low)
99	141	99	141	SEL	I/O	**SCSI SELECT** (Single ended) or **SELECT OUTPUT** (Differential).
-	140	-	140	SELIN	I	**SCSI SELECT INPUT** (Differential mode only, active low.)
84	164	84	164	SD[7:0]	I/O	**SCSI DATA BUS** (lower byte).
85	162	85	162			
86	159	86	159			
89	156	89	156			
91	152	91	152			
93	150	93	150			
94	148	94	148			
97	143	97	143			

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
SCSI INTERFACE (Continued)						
82	166	82	166	SDP	I/O	**SCSI DATA PARITY** (for lower byte).
67	189	67	189	SD[15:8]	I/O	**SCSI DATA BUS** (higher byte).
69	187	69	187			
70	185	70	185			
71	182	71	182			
73	180	73	180			
74	178	74	178			
75	175	75	175			
77	173	77	173			
81	168	81	168	SDP1	I/O	**SCSI DATA PARITY** (for higher byte).
-	131	-	131	DSENSE	I	**SCSI DIFFERENTIAL SENSE** (10K pullup).
90	154	90	154	SE	I	**SINGLE ENDED** (10K pullup)
-	138	-	138	IGS	O	**INITIATOR GROUP SELECT.**
-	132	-	132	TGS	O	**TARGET GROUP SELECT.**
-	190	-	190	SDOE[15:0]	O	**SCSI DATA OUTPUT ENABLES.**
	186		186			
	184		184			
	183		183			
	179		179			
	177		177			
	176		176			
	169		169			
	163		163			
	161		161			
	160		160			
	155		155			
	153		153			
	149		149			
	145		145			
	144		144			

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
SCSI INTERFACE (Continued)						
-	167	-	167	SDPOE	O	**SCSI DATA PARITY OUTPUT ENABLE.**
BUFFER PORT INTERFACE						
5	45	5	45	BF[7:0]	I/O	**BUFFER DATA BUS (LSB)**
3	48	3	48			
2	50	2	50			
173	56	173	56			
172	58	172	58			
170	61	170	61			
168	63	169	63			
165	66	167	66			
27	19	25	20	BF[15:8]	I/O	**BUFFER DATA BUS (MSB)**
25	21	23	22			
22	24	20	25			
19	27	17	28			
14	32	13	33			
12	34	12	35			
10	37	10	38			
8	40	8	40			
6	43	6	43	BFPL	I/O	**BUFFER DATA PARITY BIT LSB.** Odd parity.
29	16	27	17	BFPH	I/O	**BUFFER DATA PARITY BIT MSB.** Odd parity.

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
BUFFER PORT INTERFACE (Continued)						
-	-	148	88	A[10:0]	O	**BUFFER ADDRESS.**
-	-	149	87			
148	87	150	86			
150	85	152	84			
151	84	153	83			
152	83	154	82			
153	82	155	81			
158	76	160	75			
159	74	161	73			
161	72	163	71			
162	70	164	69			
31	14	29	16	MEMW	O	**MEMORY WRITE (Active low).**
32	13	30	15	RAS	O	**ROW ADDRESS STROBE (Active low).**
33	12	31	14	CAS	O	**PRIMARY COLUMN ADDRESS STROBE (Active low).**
MISCELLANEOUS						
119	115	119	115	RESETB	I	**HARD RESET.** This input sets the WD61C96A in power on reset condition. All the drivers are set into inactive state. (Active Low)
135	102	135	102	RSTF	O	**SCSI RESET FOLLOWER.** RSTF is a debounced version of the SCSI $\overline{\text{RST}}$/ RSTIN input, and is asserted as long as a valid SCSI reset is detected (active high).
154	81	156	80	BCLK	I	**BUFFER CLOCK.** Maximum 50 MHz.
66	191	66	191	SCLK	I	**SCSI CLOCK.** Minimum 20 MHz, maximum 40 MHz.
110 65	124 192	110 65	124 192	TST2B TST1B	I	**I/O TEST ENABLES 1 AND 2.** When active (low) the WD61C96A is placed into special test modes. See Section 5.12.
113	121	113	121	SCTL	I	**SCAN SHIFT/LOAD CONTROL**

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
64	193	64	-	BDP3	I	**POWER ON LATCH INPUTS.** The data on these pins are latched into the WD61C40A power on latch registers. Refer to Table 3-1, OPTIONAL PACKAGE FEATURES, on page 5.
60	-	60	-	BDP4		
58	-	-	-	BDP9		
132	-	132	-	BDP10		
15	31	14	32	CVDD		**+5 VOLTS**
36	9	36	9			
61	195	61	195			
79	171	79	171			
95	147	95	147			
111	123	111	123			
136	101	136	101			
156	79	158	78			
174	55	174	55			
16	30	15	31	CGND		**GROUND**
37	8	37	8			
62	-	62	194			
80	170	80	170			
96	146	96	146			
112	122	112	122			
137	100	137	100			
157	78	159	77			
175	54	175	54			
20	26	18	27	DVDD		**+5 VOLTS**
46	207	46	207			
78	172	78	172			
100	139	100	139			
130	106	130	106			
155	80	157	79			
176	53	176	53			

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

PINS A	PINS B	PINS C	PINS D	MNEMONIC	I/O	DESCRIPTION
1,4,7,	52, 47,	1,4,7,	52, 47,	DGND		GROUND
11,17,	42, 36,	11,16,	42, 37,			
23, 28,	29, 23,	21, 26,	30, 24,			
34, 43,	18, 11,	32, 43,	19, 13,			
49, 68,	2, 204,	49, 68,	2, 204,			
72, 76,	188,	72, 76,	188,			
83, 87,	181	83, 87,	181			
92, 98,	174	92, 98,	174			
103,	165	103,	165			
107	158	107	158			
122	151	122	151			
127	142	127	142			
133	135	133	135			
142	128	142	128			
149	113	151	113			
160	109	162	109			
166	104	168	104			
171	95, 86,	171	95, 85,			
	73, 65,		72, 65,			
	60		60			

TABLE 3-6 SIGNAL DESCRIPTION (Continued)

4.0 REGISTER DESCRIPTIONS

4.1 GENERAL REGISTER MAP

The registers are mapped into the I/O space of the 80C186, or other microprocessor, as shown in the table below. For specific register definitions, see the following sections.

Chip Select	Address Range (hex)	Registers Assigned to Range (hex)
CS0	xxx00-xxxFF	Disk Manager Register 00-FF hex
CS2	xxx00-xxx7F	SCSI Manager Register 00-7F hex

TABLE 4-1 REGISTER MAPPING

4.1.1 Disk Manager Register Map

The register map as listed below contains the complete list of microprocessor accessible locations for the Disk Manager register map. In general, there are four types of registers.

1. R/W - Read/Write
2. R/C - Read/Clear
3. R - Read only
4. W - Write only

Within these registers, the default power on condition is reset to zero unless noted. All unassigned register bits are defaulted to be reset, zero.

ADDRESS	REGISTER	DIR	FUNCTION	
General Configuration Registers				
00_{hex}	CFG1	R/W	Configuration	page 28
02	INTSTAT1	R	Interrupt Summary 1	page 28
04	INTSTAT2	R	Interrupt Summary 2	page 29
06	INTMSK1	R/W	Interrupt Mask 1	page 29
08	INTMSK2	R/W	Interrupt Mask 2	page 30
0A	HSTLD1	R	Host Power On Latch - MSB	page 30
0C	HSTLD2	R	Host Power On Latch - LSB	page 30
0E	HSTLD3	R	Host Power On Latch - Parity	page 30
Disk Controller Registers				
10_{hex}	DCNF1	R/W	Disk I/F Configuration 1	page 30
12	DCNF2	R/W	Disk Configuration 2	page 31
14	PRTXDIR	R/W	Port X Direction Control	page 32
16	PRTXDAT	R/W	Port X Data	page 32
18	PRTYDIR	R/W	Port Y Direction Control	page 32
1A	PRTYDAT	R/W	Port Y Data	page 33
1C	DSEQI	R/C	Disk Sequencer Interrupts	page 33
1E	DERRI	R/C	Disk Error Interrupts	page 34
20_{hex}	DSEQMSK	R/W	Disk Sequencer Mask	page 35
22	DERRMSK	R/W	Disk Error Mask	page 35
24	SEQSTAT	R	Disk Sequencer Status	page 35
26	WCSCTL	R/W	WCS Control	page 36
28	WCSERR	R	WCS Error Status	page 37
2A	START	R/W	Sequencer Start Address	page 38
2C	LOOP	R/W	Sequencer Loop Address	page 38
2E	SKPADR1	R/W	Skip Address	page 39
30_{hex}	SKPADR2	R/W	Skip Address	page 39
32	SKPADR3	R/W	Skip Address	page 39
34	IDSEGAD	R/W	ID/Segment Address	page 39
36	IDSEGDT	R/W	ID/Segment Data	page 39
38	CSERR	R/W	Control Store Error	page 41
3A	CSCTL	R/W	Control Store Control	page 42
3C	CSVAL	R/W	Control Store Value	page 43
3E	CSCNT	R/W	Control Store Count	page 44
40_{hex}	DEFSKP	R/W	Defect Skip Size Counter	page 45
42	DFIFOH	R/W	Disk FIFO Read/Write - MSB	page 45

TABLE 4-2 DISK MANAGER REGISTER MAP

ADDRESS	REGISTER	DIR	FUNCTION	
44	DFIFOL	R/W	Disk FIFO Read/Write - LSB	page 45
46	DFSTAT	R/W	Disk FIFO Status/Control	page 46
48	DFTHRES	R/W	Disk FIFO Threshold	page 46
4A	DFB	R/W	Disk FIFO BIST Control	page 46
4C	CECTL	R/W	CRC/ECC Control	page 47
4E	ECCSTAT	R	ECC Status	page 48
50_{hex}	ECCSYN	R	ECC Syndrome	page 48
54	EILV0	R/W	ECC Interleave Size	page 49
5A	ECCSM	R/W	ECC Sector Size	page 49
5C	ECCSL	R/W	ECC Sector Size	page 49
5E	LPR	R/W	Logical to Physical Ratio	page 50
60_{hex}	LRCHI	R/W	LRC High Bytes	page 50
62	LRCLO	R/W	LRC Low Bytes	page 50
64	IDCAP	R/W	ID Capture Control/Data	page 51
66	IDB	R/W	ID BIST Control/Status	page 51
68	OTF	R	On The Fly Counter	page 51
Host Control Registers				
70_{hex}	HCNF1	R/W	Host Configuration 1	page 52
72	HCNF2	R/W	Host Configuration 2	page 52
74	HFIFOH	R/W	Host FIFO Read/Write - MSB	page 53
76	HFIFOL	R/W	Host FIFO Read/Write - LSB	page 53
78	HFSTAT	R	Host FIFO Status/Control	page 53
7A	HCECTL	R/W	Host FIFO BIST Control	page 51
Buffer Manager Registers				
80_{hex}	MCFG1	R/W	Memory Configuration 1	page 54
82	MCFG2	R/W	Memory Configuration 2	page 55
84	MSPD	R/W	Memory Speed	page 55
86	BSSIZE	R/W	Buffer Segment Size	page 56
88	PBSHM	R/W	Physical Block Size (Host)- MSB	page 56
8A	PBSHL	R/W	Physical Block Size (Host) - LSB	page 56
8C	PBSDM	R/W	Physical Block Size (Disk) - MSB	page 49
8E	PBSDL	R/W	Physical Block Size (Disk) - LSB	page 49
90_{hex}	HBINT	R/C	Host Buffer Interrupt Status	page 56
92	DBINT	R/C	Disk Buffer Interrupt Status	page 57
94	HMSK	R/W	Host Buffer Interrupt Mask	page 59
96	DBMSK	R/W	Disk Buffer Interrupt Mask	page 59

TABLE 4-2 DISK MANAGER REGISTER MAP (Continued)

ADDRESS	REGISTER	DIR	FUNCTION	
98	BUFCTLH	R/W	Host Buffer Access Control	page 59
9A	MEMSEGH	R/W	Host Memory Segment Select	page 59
9C	RADHH	R/W	Host Relative Buffer Address MSB	page 60
9E	RADMH	R/W	Host Relative Buffer Address	page 60
$A0_{hex}$	RADLH	R/W	Host Relative Buffer Address LSB	page 60
A2	BCNTH	R/W	Host Block Count	page 60
A4	HSTSS	W	Host Start/Stop Control	page 60
A6	HBUFFH	R/W	Host Buff Count Capture - MSB	page 61
A8	HBUFFL	R/W	Host Buff Count Capture - LSB	page 61
AA	BUFCTLD	R/W	Disk Buffer Access Control	page 61
AC	MEMSED	R/W	Disk Memory Segment Select	page 62
AE	RADHD	R/W	Disk Relative Buffer Address MSB	page 62
$B0_{hex}$	RADMD	R/W	Disk Relative Buffer Address	page 62
B2	RADLD	R/W	Disk Relative Buffer Address LSB	page 62
B4	BCNTD	R/W	Disk Block Count	page 62
B6	SKPMSKM	R/W	Skip Mask	page 62
B8	SKPMSKL	R/W	Skip Mask	page 62
BA	DSS	W	Disk Start/Stop Control	page 63
BC	DBUFFH	R	Disk Buffer Count Capture - MSB	page 63
BE	DBUFFL	R	Disk Buffer Count Capture - LSB	page 63
$C0_{hex}$	BSTAT	R	Buffer DMA Status	page 63
C2	PADH	R/W	Microprocessor Active Address - MSB	page 64
C4	PADM	R/W	Microprocessor Active Address	page 64
C6	PADL	R/W	Microprocessor Active Address - LSB	page 64
C8	PBODDA	R/W	Microprocessor Autoincrement Odd Data Byte	page 64
CA	PBEVENA	R/W	Microprocessor Autoincrement Even Data Byte	page 64
CC	PBODD	R/W	Microprocessor Data Buffer Latch Odd	page 64
CE	PBEVEN	R/W	Microprocessor Data Buffer Latch Even	page 64
$D0_{hex}$	ECCADH	R	ECC Block Start Address - MSB	page 65
D2	ECCADM	R	ECC Block Start Address	page 65
D4	ECCADL	R	ECC Block Start Address - LSB	page 65
D6	BFCTL	W	Buff Count Capture Control	page 65
D8	DBCC	R/W	Disk Block Count Compare	page 65

TABLE 4-2 DISK MANAGER REGISTER MAP (Continued)

4.1.2 SCSI Bus Controller Register Map

The register map below contains the complete list of microprocessor accessible locations. In general, there are two modes for registers.

- Setup Mode
- Normal Mode

Within these registers, the default power-on condition is reset to zero unless noted. All unassigned register bits are defaulted to be reset zero.

Register Map in Setup Mode

ADDRESS	REGISTER	R/W	DESCRIPTION	
00	CTL	R/W	Control Register	page 66
02	SCNF	R/W	SCSI Configuration	page 66
04	OWNID	R/W	Own ID Register	page 67
06	TIMOUT	R/W	Selection and Reselection Time-out Period	page 67
08	SLEEP	R/W	Sleep Countdown Register	page 68
0A	TIMER	R	SCSI Timeout Countdown Residue	page 69
0C	CDBSIZ1	R/W	Special CDB Size Register (groups 3,4)	page 69
0E	CDBSIZ2	R/W	Special CDB Size Register (groups 6,7)	page 69
10	IDFLAG0	R/W	SCSI-ID Specific Flags (IDs 0..7)	page 69
12	IDFLAG1	R/W	SCSI-ID Specific Flags (IDs 8..15)	page 69
14	DMACNF	R/W	DMA Configuration	page 70
16	DMATIM	R/W	DMA Timing Control	page 70
18	TEST0	R/W	Factory Test Register	page 71
1A	SC0	R, R/W	SCSI Low-level Control	page 72
1C	SC1	R/W	SCSI Low-level Control	page 72
1E	SC2	R/W	SCSI Low-level Control	page 72
20	SC3	R/W	SCSI Low-level Control	page 72
22	CSADR	R/W	WCS Address Register for Microprocessor Access	page 74
24	CSPRT0	R/W	WCS Port for Window 0	page 74
26	CSPRT1	R/W	WCS Port for Window 1	page 74
28	CSPRT2	R/W	WCS Port for Window 2	page 74
2A	CSPRT3	R/W	WCS Port for Window 3	page 74
2C	SQSEL	R/W	WCS Selection Response Start Address Register	page 74
2E	SQRSL	R/W	WCS Reselection Response Start Address Register	page 75
30	SQDMA	R/W	WCS Start Address in Response to DMA Request	page 75
32	DPRADD	R	DPR Address Pointer	page 75

TABLE 4-3 SCSI BUS CONTROLLER REGISTER SETUP MODE

ADDRESS	REGISTER	R/W	DESCRIPTION	
34	DPRTC	R	Dual-Port Register Transfer Counter	page 75
36	PLR	R/W	Physical-to-Logical Block Ratio	page 76
38	PSIZE0	R/W	Physical Block Size	page 76
3A	PSIZE1	R/W	Physical Block Size	page 76
3C	PING	R/W	Mirroring Ping-pong Value Register	page 76
3E	CMPIX	R/W	Data Compare Index	page 77
40	CMPVAL	R/W	Data Compare Value Register	page 77
42	CMPMSK	R/W	Data Compare Mask Register	page 77
44	BBDL	R	Buffered BD[0-7]	page 78
46	BBDH	R	Buffered BD[8-15]	page 78
48	CVER	R	Chip/Design Version	page 78
4A	TEST1	R	Factory Test Register	page 79
4C	OFFSET	R	REQ/ACK Offset Counter	page 79
4E-7E			Reserved†	

TABLE 4-3 SCSI BUS CONTROLLER REGISTER SETUP MODE (Continued)

†All registers marked *reserved* should not be written, and if read, will produce either 0's or 1's.

Register Map in Normal Mode

ADDRESS	REGISTER	R/W/C	DESCRIPTION	
00	CTL	R/W	Control Register	page 66
02	CTLA	R/W	Control Register, Auxiliary	page 80
04	ISR	R/C, R	Interrupt Status Register	page 80
06	STOPU	R/C	Unexpected Stop Status Register	page 81
08	UEI	R/C	Unexpected Event Interrupt Register	page 82
0A	ISRM	R/W	ISR Mask Register	page 82
0C	STOPUM	R/W	STOPU Mask Register	page 82
0E	UEIM	R/W	UEI Mask Register	page 82
10	RESPONSE	R/W	Automatic Response Control	page 83
12	SQINT	R	WCS Sequencer Interrupt Address	page 84
14	SQADR	R/W	Current Address WCS Is Executing	page 84
16	STC	R/W	SCSI Transfer Control Register	page 85
18	SPW	R/W	SCSI Pulse Width Control Register	page 85
1A	DESTID	R/W	Destination ID Register	page 86
1C	SRCID	R	Source ID Register	page 86

TABLE 4-4 SCSI BUS CONTROLLER REGISTERS NORMAL MODE

ADDRESS	REGISTER	R/W/C	DESCRIPTION	
1E	FLAG	R/W	Flag Register	page 86
20	TC[0-7]	R/W	Transfer Count Register, Low Byte	page 87
22	TC[8-15]	R/W	Transfer Count Register, Middle Byte	page 87
24	TC[16-23]	R/W	Transfer Count Register, High Byte	page 87
26	DATA	R/W	Data Access Port	page 87
28	SR	R	Status Register	page 87
2A	FIFOS	R	FIFO Status Register	page 88
2C	PBR	R/W	Physical Block Residue	page 88
2E	BR0	R/W	Byte Residue	page 88
30	BR1	R/W	Byte Residue	page 88
32	PINGR	R/W	PING Residue	page 88
34	LRCR0	R/W	LRC Residue Register (Low)	page 89
36	LRCR1	R/W	LRC Residue Register (High)	page 89
38	ODDR	R/W	Odd-byte Reconnect Register	page 89
3A			Reserved†	
3C			Reserved†	
3E			Reserved†	
40-7E	DPR[0-31]	R/W	Dual Port Registers 0 through 31	page 89

TABLE 4-4 SCSI BUS CONTROLLER REGISTERS NORMAL MODE (Continued)

4.2 DISK MANAGER GENERAL CONTROL REGISTERS

4.2.1 General Configuration

CFG1 Register address = 00							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV3	REV2	REV1	REV0		RDY1	RDY0	POR

When the microprocessor writes to this address after power up, the WD61C96A always generates a µRDY for six to seven BCLK cycles after the low going edge of REB or WEB. The µRDY pulse width is changed when RDY[1:0] is loaded. When RDY[1:0] is changed, the microprocessor must not read or write the WD61C96A registers for 4 BCLKs.

REV [3:0] = Revision Number (Read Only)

These bits indicate the revision of the WD61C96A. These bits, hex code, are read only and are fixed. (XA is 1000b).

RDY[1:0] = Microprocessor Ready Control

Refer to Section 7.1.2, PIO Read with RDYB - CS0, on page 177 and Section 7.1.3, PIO Write with RDYB - CS0, on page 177 for microprocessor timing. REB or WEB to RDYB high is 4 to 6 clocks.

(An 80C186 running at 20 - 25 Mhz requires RDY[1:0] = 10.)

RDY1	RDY0	µRDY CLOCKS
0	0	6 x BCLK
0	1	5 x BCLK
1	0	4 x BCLK
0	0	0 x BCLK

POR = Power On Reset

When this bit is set, the entire WD61C40 portion of the WD61C96A is reset. This reset condition is identical to an active RESETB pin condition on the WD61C40A. This bit must be cleared by the microprocessor to complete the reset.

4.2.2 Interrupt Summary 1

INTSTAT1 Register address = 02 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AINT1			PDBP ER	HSTB INT	DERR INT	DSCB INT	DESQ INT

This register contains the summation of all possible WD61C96A interrupt flags. Each bit simply indicates the general location of the interrupt source. The interrupt must be cleared at the interrupt source or the individual interrupt mask can be reset. (Refer to Section 5.7.3, Disk Interrupt Structure, on page 152.)

AINT1 = Any Interrupt

Any of the following interrupts are active. This bit reflects the active condition of the external interrupt pin.

PDBPER = Processor Buffer Parity Error

This bit is set when a parity error is detected during a microprocessor buffer read.

Refer to section 4.5.7, Host Buffer Interrupt Status, on page 56.

HSTBINT= Host Buffer Interrupt

The Host Buffer control logic has generated an interrupt. (Refer to Section 4.5.7, Host Buffer Interrupt Status, on page 56.)

DERRINT= Disk Error Interrupt

When this bit is set a disk related error interrupt is pending. The interrupt are described in Section 4.3.8, Disk Error Interrupts, on page 34. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

DSCBINT= Disk Buffer Interrupt (Read Only)

When this bit is set, an interrupt is pending from the Disk Buffer Manager Control. For details on the cause of the interrupt, refer to Section 4.5.8, Disk Buffer Interrupt Status, on page 57. For details on the interrupt structure, refer to Sec-

tion 5. 7.3.2, Interrupt Generation, on page 155.

DSEQINT= Disk Sequencer Interrupt

When this bit is set, an interrupt is pending from the Disk Control. Refer to the Disk Interrupt Status 1 and 2 registers. For details on the cause of the interrupt, refer to Section 4.3.7, Disk Sequencer Interrupts, on page 33. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

4.2.3 Interrupt Summary 2

2 INTSTAT2 Register address = 04 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
AINT2			PDBP ER	HSTB INT	DERR INT	DSCB INT	DSEQ INT

This register contains the summation of all possible WD61C96A interrupt flags. Each bit simply indicates the general location of the interrupt source. The interrupt must be cleared at the interrupt source or the interrupt mask can be reset. (Refer to the Section 5.7.3, Disk Interrupt Structure, on page 152)

AINT2 = Any Interrupt

Any of the following interrupts are active. This bit reflects the active condition of the external interrupt pin.

PDBPER = Processor Buffer Parity Error

This bit is set when a parity error is detected during a microprocessor buffer read. (Refer to section 4.5.7, Host Buffer Interrupt Status, on page 56.)

HSTBINT = Host Buffer Interrupt

The Host Buffer control logic has generated an interrupt. (Refer to Section 4.5.7, Host Buffer Interrupt Status, on page 56

DERRINT = Disk Error Interrupt

When this bit is set a disk related error interrupt is pending. The interrupt are described in Section 4.3.8, Disk Error Interrupts, on page 34. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

DSCBINT= Disk Buffer Interrupt (Read Only)

When this bit is set, an interrupt is pending from the Disk Buffer Manager Control. For details on the cause of the interrupt, refer to Section 4.5.8, Disk Buffer Interrupt Status, on page 57. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

DSEQINT = Disk Sequencer Interrupt

When this bit is set, an interrupt is pending from the Disk Control. Refer to the Disk Interrupt Status 1 and 2 registers. For details on the cause of the interrupt, refer to Section 4.3.7, Disk Sequencer Interrupts, on page 33. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

4.2.4 Interrupt Mask 1

INTMSK1 Register address = 06							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
			PBPE N1	HBEN 1	DERR EN1	DSCB EN1	DSQ EN1

When any bit is set, the interrupt is enabled. The interrupt group is observable in the Interrupt Summary 1 register and presented to the INT1 pin. For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

PBPEN1 = Processor Parity Mask

HBEN1 = Host Buffer Interrupt Mask

DERREN1 = Disk Error Interrupt Mask

DSCBEN1 = Disk Buffer Interrupt Mask

DSQEN1 = Disk Sequencer Interrupt Mask

4.2.5 Interrupt Mask 2

IINTMSK1 Register address = 08							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
			PBP EN2	HB EN2	DERR EN2	DSCB EN2	DSQ EN2

When any bit is set, the interrupt is enabled. The interrupt group is observable in the Interrupt Summary 2 register and presented to the INT2 pin. For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

PBPEN2 = Processor Parity Mask

HBEN2 = Host Buffer Interrupt Mask

DERREN2 = Disk Error Interrupt Mask

DSCBEN2 = Disk Buffer Interrupt Mask

DSQEN2 = Disk Sequencer Interrupt Mask

4.2.6 Host Power On Latch

IHSTLD1 Register address = 0A (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BD15	BD14	BD13	BD12	BD11	BD10	BD9	BD8

IHSTLD2 Register address = 0C(Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0

IHSTLD3 Register address = 0E (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
						BDPL	BDPH

BD[15:0] = Host Bus Power On Latch Data

BDP[H,L] = Host Bus Power On Parity Latch

The Power On Latch stores the data that is available on the Host Data Bus, BD[15:0], BDPL, and BDPH. The Power On latch is enabled when the RESETB pin is low. The latch is closed when RESETB is high. These bits are general purpose and have no effect on the internal function of the device. The BD[15:0] have internal pullup resistors of about 30 to 50K. The user should provide a bank of external pulldown resistors with jumper on the BD[15:0] bus. When the BD bit wants to be a one, the user leaves the associated bus bit open. When the BD bit wants to see a zero, the user should jumper the associated BD pin to the pulldown resistor. Refer to Section 6.0, ELECTRICAL CHARACTERISTICS, on page 174. BDPL and BDPH are valid during special IC tester operations only. These two signals do not have pull-ups at the pins.

4.3 DISK MANAGER PORT REGISTERS

4.3.1 Disk Configuration

DCNF1 Register address = 10							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IDIEN	DRVF LEN	LRCC HK	DPAR EN		DIAG 2	DIAG 1	SRST

IDIEN = ID Increment Enable

When this bit is set, the expected ID can be incremented. The BLKMODE, bit 6 of the Disk Configuration 2 register, identifies what portion of the ID field is incremented. If BLKMODE is reset, only the sector count is incremented. If BLKMODE is set, the Logical Block Address, 30 bits or 24 bits as defined by the ID3OR4 bit, are incremented. The ID is incremented *when CHK bit is active and CRCEN is inactive* or the Buffer Manager detects a skip mask bit of zero and skip mask operation is enabled. When this bit is reset the ID field is not incremented when requested. For more details refer to Section 5.6.9, Disk DMA Operation - Standard Mode, on page 135 and Section 5.6.10, Disk DMA Operation - Skip Mask Mode, on page 136.

DRVFLEN = Drive Fault Enable

Normally, this is reset. In this condition an active DRIVE FAULT signal only generates an interrupt to the microprocessor at the time of detection. The microprocessor is responsible for

controlling the effects of the error condition. When this bit is set, the Drive Fault input pin is also an input parameter to the WCS FAIL bit condition. When the FAIL bit is active and a DRVFAULT occurs, the WCS aborts its operation and the SEQSTP interrupt is generated. For interrupt details, refer to Section 5. 7.3.2, Interrupt Generation, on page 155. An Abort condition causes WRTGATE, READGATE, and AMENA output pins to be reset.

LRCCHK = LRC Check Enabled

When this bit is set, the logical block LRC check bytes are checked. This control bit is used in conjunction with the WCS "LRC" bit and the Logical to physical ratio counter. The physical block count is reinitialized at every WCS start operation. When the FAIL bit is active and an LRC error occurs, the WCS aborts its operation and an LRC interrupt and SEQSTP interrupts are generated. Residue and other LRC options are not valid if this bit is disabled. For interrupt details, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

DPAREN = Disk Parity Check Enable

When this bit is set, the Disk port parity checker is enabled on disk reads. When the FAIL bit is active and a Disk Port parity error is detected, the WCS aborts its operation and a Disk Port parity interrupt and SEQSTP interrupt are generated. For interrupt details, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

DIAG2 = Diagnostic Mode Select 2 - Read Pointer Increment Mode

When this bit is reset, the WCS read pointer operates normally. When this bit is set, the read pointer increments whenever the microprocessor reads the CSCNT Microprocessor register location. This mode is used when the microprocessor wants to read the contents of the WCS. The start address should be initialized preceding these events.The reading of the start address register outputs the current WCS pointer value. For more information, refer to Section 5.9.8, WCS Register File Access, on page 166.

NOTE

This diagnostic mode is only valid if the WCS is aborted or IDLE.

DIAG1 = Diagnostic Mode Select 1- START register read control

When this bit is reset, the Disk is in a normal mode operation. In this mode, the START read register value represents the uP written data. When this bit is set, the START read register represents the present active WCS read pointer. This is used when the programmer needs to find the last active WCS location. For more information, refer to Section 5.9.8 on page 166.

SRST = Soft Reset Mode

When this bit is set, the WCS and all associated error status bits are reset.

NOTE

The Port X and Y Data and Direction bits are not changed by this bit. for more details, refer to Section 5.9.6, Disk Manager Soft Reset Operations, on page 165.

4.3.2 Disk Configuration 2

DCNF2 Register address = 12							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ID3 OR4	BLK MODE		WD MODE			WRPE REN	

ID3OR4 = ID 3 or 4 Byte

When this bit is set, the ID block count is four bytes deep. If BLKMODE is set, the Logical Block Address, 30 bits or 24 bits as defined by the ID3OR4 bit, are incremented. For more details on the Expected ID value within the internal RAM storage refer to Section 4.3.20, ID/Segment Data, on page 39.

BLKMODE = ID Block Mode Selected

When this bit is set, the first three or four bytes of the LBA contain a 24 or 30 bit count value

which is used to identify this sector. The size of the count value is defined by ID3OR4. When the BLOCKMODE bit is reset, the sector is identified is the more traditional Cylinder high, Cylinder Low, Head, Sector format. For details pertaining to ID incrementing in Block and Non-Block Modes refer to Section 4.3.1, Disk Configuration, on page 30.

WDMODE = WD ID Format Mode

When this bit is set, the WD defect skipping disk format is enabled. The data field within the sector can be divided into multiple segments. The ID field contains the size of each segment. For more details on the expected ID format values within the internal RAM storage refer to Section 4.3.20, ID/Segment Data, on page 39.

WRPEREN = WRAP Error Enable

When this bit is set, the WRAP input pin is also an input parameter to the WCS FAIL bit condition. When the FAIL bit is active and a WRAP is detected, the WCS aborts its operation and a WRAP interrupt and SEQSTP interrupt are generated. When reset, the internal wrap function is not implemented. For interrupt details, refer to Section 5. 7.3.2, Interrupt Generation, on page 155. An Abort condition causes WRTGATE, READGATE, SEQOUT, and AMENA output pins to be reset.

4.3.3 Port X Direction

PRTXDIR Register address = 14							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

XD[7:0] = Port X Direction Control

These bits are used to control the general purpose Port X direction. When a bit is set, the associated port bit is an output, else the associated port bit is an input. The microprocessor directs the data in the Port X register to the output pins.

NOTE

The Port X and Y Data and Direction bits are not changed by the SRST bit.

4.3.4 Port X Data

PRTXDIR Register address = 16							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

X[7:0] = Port X Data

These bits reflect the input Port X pin condition when there respective Port X direction bits is reset. These bits define Port X output data when there respective Port X direction bits are set.

NOTE

The Port X and Y Data and Direction bits are not changed by the SRST bit.

4.3.5 Port Y Direction Control/Configuration

PRTYDAT Register address = 18							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PAR EV	AMSY	IXSY	SMSY	YD3	YD2	YD1	YD0

PAREV = Disk Port Even Parity Select

When this bit is set, the disk port parity is even parity. In this mode the data from the buffer is converted to even parity. Disk input data is checked for even parity and converted to odd parity for the buffer. When this bit is reset the disk port parity is odd. In this mode the parity is just passed through the disk port to and from the buffer.

AMSY = Synchronous AMDET Select

When this bit is set, this input pin is defined as a synchronous input with relationship to the RRCLK. This signal must maintain a 30ns setup time to the rising edge of RRCLK. This bit is set when the programmer requires the minimum time from the active condition detection of this signal and the Control Store reacting to this signal. This means the Control Store can change instructions as soon as the next RRCLK. When this bit is reset the input signal is considered an asynchronous input. This means that the

WD61C96A must synchronize this signal before presenting this input to the Control Store. This means that there is a nominal two RRCLK delay before the Control Store reacts the active condition of this signal.

IXSY = Synchronous IXDET Select

When this bit is set, this input pin is defined as a synchronous input with relationship to the RRCLK. This signal must maintain a 30ns setup time to the rising edge of RRCLK. This bit is set when the programmer requires the minimum time from the active condition detection of this signal and the Control Store reacting to this signal. This means the Control Store can change instructions as soon as the next RRCLK. When this bit is reset the input signal is considered an asynchronous input. This means that the WD61C96A must synchronize this signal before presenting this input to the Control Store. This means that there is a nominal two RRCLK delay before the Control Store reacts the active condition of this signal.

SMSY = Synchronous SMDET Select

When this bit is set, this input pin is defined as a synchronous input with relationship to the RRCLK. This signal must maintain a 30 ns setup time to the rising edge of RRCLK. This bit is set when the programmer requires the minimum time from the active condition detection of this signal and the Control Store reacting to this signal. This means the Control Store can change instructions as soon as the next RRCLK. When this bit is reset the input signal is considered an asynchronous input. This means that the WD61C96A must synchronize this signal before presenting this input to the Control Store. This means that there is a nominal two RRCLK delay before the Control Store reacts the active condition of this signal.

YD[3:0]= Port Y Direction Control

These bits are used to control the general purpose Port Y direction. When a bit is set, the associated port bit is an output else the associated bit is an input. The microprocessor directs the data in the Port Y register to the output pins.

NOTE

The Port X and Y Data and Direction bits are not changed by the SRST bit.

4.3.6 Port Y Data

PRTYDAT Register address = 1A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
				Y3	Y2	Y1	Y0

Y[3:0] = Port Y Data

These bits reflect the input Port Y pin condition when there respective Port Y direction bits is reset. These bits define Port Y output data when there respective Port Y direction bits are set.

NOTE

The Port X and Y Data and Direction bits are not changed by the SRST bit.

4.3.7 Disk Sequencer Interrupts

DSEQI Register address = 1C (Read/Clear)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	ID FULL	DX FER	COM PLT	SEQ STP	IX	SM	

These are Disk Controller related interrupts. Any one of the following interrupts can generate an active flag in the Interrupt Summary Status 1 or 2 bit 0. These bits are cleared by writing a one to the respective interrupt bit. These status bits are also reset when the WCS SRST is set. For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

IDFULL = ID Field Read Complete

This bit is set when a complete ID field is captured and the ID CRC is good.For more details, refer to Section 4.3.37, ID Capture Address/ Data/Control, on page 51. This status bit is also reset when the WCS SRST is set.

DXFER = Data Transfer Start (*10C01 compatible*)

This bit is set when the Control Store NOXFER bit or BUFF bit transitions from a 0 to a 1 condi-

tion. This status bit is also reset when the WCS SRST is set.

COMPLT = COMPLT input pin active

This interrupt is set when the COMPLT input pin transitions from a low to high. This bit is typically used as the Servo's SEEK Complete Flag.

SEQSTP = WCS Stop Interrupt

This bit is set when the WCS reaches a CS word which contains an active STOP bit or when an abort condition occurs.

IX = Index Mark Detected

This bit is set when an Index mark is detected and the *WCS is Active.*

SM = Sector Mark Detected

This bit is set when a Sector Mark is detected and the *WCS is Active.*

4.3.8 Disk Error Interrupts

DERRI Register address = 1E (Read/Clear)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CMP ERR	CMPI ERR	ID ERR	WRAP ER	DPP ER	ECC INT	LRC ER	FAULT

These are Disk Controller related interrupts. Any one of the following interrupts can generate an active flag in the Interrupt Status1 register bit 2. These bits are cleared by writing a one to the respective interrupt bit.

NOTE

These interrupts are generally generated when the corresponding error bit is set and the FAIL bit is active in the present Control Store instruction.

For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152 and Section 4.3.13, WCS Error Status, on page 37.

CMPERR = Compare Error

This bit is set when a CMPERR error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

CMPIERR = Compare Immediate Error

This bit is set when a CMPIERR error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

IDERR = ID CRC Error

This bit is set when a IDERR error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

WRAPER = WRAP error

This bit is set when a WRAPERR error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

DPPER = Disk Port Parity Error Interrupt

This bit is set when a DPPER error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

ECCINT = ECC Interrupt *(ECC error / Test Done)*

When this bit is set an uncorrectable ECC error has occurred. For details on the cause of the interrupt, refer to Section 4.3.31, ECC Status, on page 48. For details on the interrupt structure, refer to Section 5. 7.3.2, Interrupt Generation, on page 155.

NOTE

This interrupt is not locked to the FAIL bit.

LRCER = LRC Error Detected

This bit is set when a LRCER error flag (see Section 4.3.13, WCS Error Status, on page 37) and a Control Store FAIL bit is detected. This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

FAULT = Drive Fault

This bit is immediately set when the DRIVE FAULT input pin is active high (see Section 4.3.13, WCS Error Status, on page 37). This bit is reset when the microprocessor writes a one to this location. This status bit is also reset when the WCS SRST is set.

NOTE

This interrupt is not locked to the FAIL bit.

4.3.9 Disk Sequencer Mask

DSEQMSK Register address = 20							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	IDF EN	XF EN	CPLT EN	STP EN	IX EN	SM EN	

When a bit is set in this register, the corresponding interrupt generation is enabled. When a bit is reset, the corresponding interrupt generation is disabled. However, the interrupt is not cleared if the mask is disabled (reset). For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

IDFEN = ID Field Read Complete Mask

XFEN = Transfer Complete Mask

CPLTEN = Complete Input Pin Active Mask

STPEN = Sequencer Stop Mask

IXEN = Index Detect Mask

SMEN = Sector Mark Detect Mask

4.3.10 Disk Error Mask

DERRMSK Register address = 22							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CMP EN	CMPI EN	ID EN	WRAP EN	DP EN	ECC EN	LRC EN	FLT EN

When a bit is set in this register, the corresponding interrupt generation is enabled. When a bit is reset, the corresponding interrupt generation is disabled. However, the interrupt is not cleared if the mask is disabled (reset). For more details refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

CMPEN = Data Compare Error Mask

CMPIEN = Compare Immediate Error Mask

IDEN = ID CRC Error Mask

WRAPEN = WRAP Mask

DPEN = Disk Port Parity Mask

ECCEN = ECC Interrupt Mask

LRCIEN = LRC Error Detect Mask

FLTEN = Drive Fault Enable Mask

4.3.11 Sequencer Status 1

SEQSTAT Register address = 24 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ECCB	ECCA	ACTB	ACTA	WCS ACT	WSPD	AM DET	SEQ OUT

These bits indicated the general status of the Control Store.

ECCB = ECC Error Pending for Active B ID

This bit is set when 1) an ECC error flag is detected, 2) the Active B ID field stores the ID field from that sector, and 3) the ECCA flag is *not pending*. This bit is reset when the ECC error has been corrected. This bit is also reset by the SRST bit.

ECCA = ECC Error Pending for Active A ID

This bit is set when 1) an ECC error flag is detected, 2) the Active A ID field stores the ID

field from that sector, and 3) the ECCB flag is *not pending*. This bit is reset when the ECC error has been corrected. This bit is also reset by the SRST bit.

ACTB = Active B ID Busy

When this bit is set the Active B space within the ID/Segment Data register file contains an ID. This bit is typically set when the WCS ID bit transitions from a zero to a one and the ACTA flag is set. This bit is cleared *when there are no outstanding Drive errors* and the ECC is defined as good or the data has been corrected. Refer to Sections 4.3.19, ID/Segment Address, on page 39 and 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139. This bit is also reset by the SRST bit.

ACTA = Active A ID Busy

When this bit is set the Active A space within the ID/Segment Data register file contains an ID. This bit is typically set when the WCS ID bit transition from a zero to a one. This bit is cleared *when there are no outstanding Drive errors* and the ECC is defined as good or the data has been corrected. Refer to Sections 4.3.19, ID/Segment Address, on page 39 and 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139. This bit is also reset by the SRST bit.

WCSACT = Control Store Active

When this bit is set, the Control Store has begun executing and is presently active. The bit remains set until a Control Store STOP bit is detected or an abort condition has been detected.

WSPD = WCS is Paused

This bit is active when the Control Store is paused. A pause condition can occur during a skip mask. The conditions for a pause are a JUMP instruction has been detected and the disk buffer manager has request a pause during a skip mask operation. For details on skip mask operations refer to Section 5.6.10, Disk DMA Operation - Skip Mask Mode, on page 136.

AMDET = Address Mark Detected

This bit reflects the active status of the AMDET pin

SEQOUT = Sequence Out Flag Active

This bit reflects the active status of the SEQOUT pin and SEQOUT bit of the Control Store instruction.

4.3.12 WCS Control

WCSCTL Register address = 26							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
WSPD	WWT	WCST 1	WCST 0	NUKE WCS	STOP WCS	RCMP EN	WCS PS

WSPD = WCS is Paused (Read Only)

When this bit is set, the WCS is paused at a JMPEN instruction.

WWT = WCS in Wait state (Read Only)

When this bit is set, the WCS is waiting for a special event. These events are Wait for ID address Mark, Wait for sector mark, or Wait for Index Mark.

WCST[1:0] = WCS Present Control State (Read Only)

These bits define the general condition of the WCS.

STATES		CONDITION DESCRIPTION
0	0	WCS is in Reset condition OR SRST is active
0	1	WCS is IDLE (waiting for a START request)
1	0	WCS is presently Active (includes wait and pause conditions)
1	1	WCS is in the Abort state

NUKEWCS = Halt WCS Immediate (Read/Write)

When this bit is set the Control Store is immediately aborted. The WRTGATE, READGATE, and AMENA output pins are reset within three RRCLKs of the microprocessor write strobe going high. The microprocessor must reset this bit before the WCS can execute any other operations. The microprocessor must restart the DMA pipeline before the Control Store can begin again. A SEQSTP interrupt is generated when the WCS stops.

STOPWCS = Halt WCS only at JMPEN or RETRY (Read/Write)

When this bit is set, the WCS aborts when the WCS reaches an active JMPEN or RETRY bit. The WRTGATE, READGATE, and AMENA output pins are reset at the jump instruction. The WCS address remains at the present location. This bit must be reset before the Control Store can execute again. The microprocessor must restart the DMA pipeline before the Control Store can begin again. A SEQSTP interrupt is generated when the WCS stops.

RCMPEN = Read Compare Enable (Read/Write)

When this bit is set, the Control Store executes a read verify byte for byte comparison operation. In this operation, the Disk read data is compared byte for byte against buffer data when the WCS BUFF bit is set.

WCSPS = Wait the WCS (Read/Write)

When this bit is set the WCS pauses at the next JMPEN instruction. The WCS continues when this bit is reset.

4.3.13 WCS Error Status

WCS ERR Register address = 28 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CMP ERR	CMPI ERR	ID ERR	WRAP ER	DPP ER	DOV UN	LRC EN	FAULT

These bits reflect the active WCS error conditions. These bits are set when the error is encountered. In general, these status bits are reset when the WCS SRST is set or the corresponding interrupt is reset.

CMPERR = Compare Error

When this bit is set a data byte compare error has been detected. This includes all bytes for byte compare operations when SVSEL and CMPEN are set. This internal flag is examined when a WCS RETRY bit is active. An active CMPER status flag causes the WCS to jump to the loop instruction address if the RETRY bit is set. The CMPER status flag is reset when the jump is made. If this internal error flag is set and a FAIL bit is active, the control store aborts. The status bit is also reset when the WCS SRST is set. In addition this flag is reset when the microprocessor writes a one to the corresponding interrupt.

CMPIERR = Compare Immediate Error

When this bit is set, a valid byte compare has not occurred when SVSEL is reset and CMPEN is set. This occurs when byte synchronization has failed. This internal flag is examined when a WCS RETRY bit is active. An active CMPIER status flag causes the WCS to jump to the loop instruction address if the RETRY bit is set. The CMPIERR status flag is reset when the jump is made. If this internal error flag is set and a FAIL bit is active, the control store aborts. The status bit is also reset when the WCS SRST is set. In addition, this flag is reset when the microprocessor writes a one to the corresponding interrupt.

IDERR = ID CRC Error.

When this bit is set, an ID field CRC compare error has been detected. An internal status flag is set. This internal flag is examined when a WCS RETRY bit is active. An active IDER status flag causes the WCS to jump to the loop instruction address if the RETRY bit is set. The IDER status flag is reset when the jump is made. If this internal error flag is set and a FAIL bit is active, the control store aborts. The status bit is also reset when the WCS SRST is set. In addition, this flag is reset when the microprocessor writes a one to the corresponding interrupt.

WRAPER = WRAP error

If this bit is set a WRAP error has occurred. This bit is set if the WRAP pin status does not match the internal generated WRAP signal from Write gate, Read gate, and AMENA. This status bit is also reset when the WCS SRST is set. In addition, this flag is reset when the microprocessor writes a one to the corresponding interrupt.

DPPER = Disk Port Bus Parity Error

This bit is set when a parity error has been detected on the 8 bit disk port during a disk read operation. This error is examined by the Control Store when the FAIL bit is set in the present WCS instruction. This status bit and its corresponding interrupt status are reset when the microprocessor writes a one to its respective interrupt status register. This status bit is also reset when the WCS SRST is set.

DOVUN = Disk FIFO Overrun / Underrun

This bit is set when a Disk FIFO Over/Underrun condition is detected. This error occurs whenever the disk has read data from FIFO when the FIFO is empty or the Disk port has written to the FIFO when the FIFO is FULL. This status bit and its corresponding interrupt status are reset when the microprocessor writes a one to its respective interrupt status register.This status bit is also reset when the WCS SRST is set.

LRCER = LRC Error Detected

This bit is set when an LRC error has been detected. During disk write operations the LRC checker can be enabled (Disk Configuration 1, bit 5). An error is detected when the generated LRC bytes (2) do not match the LRC bytes at the end of the physical block. The LRC bytes can span more than a physical block boundary. Refer to Sections 5.10.1, DISK PORT LRC OPERATION, on page 168, and 5.10.2, SCSI LRC OPERATION, on page 169. This status bit and its corresponding interrupt status are reset when the microprocessor writes a one to its respective interrupt status register. This status bit is also reset when the WCS SRST is set.

FAULT = Drive Fault

This error flag and interrupt is set when the DRVFLT input pin is active high. This interrupt remains active until the FAULT condition is externally cleared and the interrupt flag is reset when the microprocessor writes a one to its respective interrupt status register. This status bit is also reset when the WCS SRST is set.

4.3.14 Sequencer Starting Address

START Register address = 2A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		STC5	STC4	STC3	STC2	STC1	STC0

STC[5:0] = WCS Start Address

These bits define the location of the WCS start address. This address is the point where the WCS begins its operation or WCS loading begins. In diagnostic mode 1, the present WCS pointer address is read out from this location. In diagnostic mode 2, the next WCS pointer address is read out from this location. For more details on WCS loading refer to Section 5.9.7, Disk Register File Access, on page 165.

4.3.15 Loop Address

LOOP Register address = 2C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		LCS5	LCS4	LCS3	LCS2	LCS1	LCS0

LCS[5:0] = WCS Loop Address

When the WCS JMPEN bit is set, the internal Block count is nonzero, no errors are pending (if the FAIL bit is active), and the end of the present instruction is reached, the WCS jumps to this address. The Loop Address is used by the control store during a JUMP or RETRY execution.

4.3.16 Skip Address 1

SKPADR1 Register address = 2E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		SK15	SK14	SK13	SK12	SK11	SK10

SK1[5:0] = WCS Skip Address 1

Skip Address No. 1 for the WCS program. The control store will skip to this instruction address when SKPEN and CSERR[5:4] = 00_{bin} are detected in the executing instruction.

4.3.17 Skip Address 2

SKPADR2 Register address = 30							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		SK25	SK24	SK23	SK22	SK21	SK20

SK2[5:0] = WCS Skip Address 2

Skip Address No. 2 for the WCS program. The control store will skip to this instruction address when SKPEN and CSERR[5:4] = 01_{bin} are detected in the executing instruction.

4.3.18 Skip Address 3

SKPADR3 Register address = 32							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		SK35	SK34	SK33	SK32	SK31	SK30

SK3[5:0] = WCS Skip Address 3

Skip Address No. 3 for the WCS program. The control store will skip to this instruction address when SKPEN and CSERR[5:4] = 10_{bin} are detected in the executing instruction.

4.3.19 ID/Segment Address

IDSEGAD Register address = 34							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IDCE			IDA4	IDA3	IDA2	IDA1	IDA0

The WD61C96A contains a 32-byte register file which stores the ID Field data from the disk during a normal read/write operation or the buffer supplied data format operation. The Expected ID is also stored in this register file. This register controls the microprocessor access of this register file.

NOTE

The microprocessor should only access the register file when the WCS is not active and rrclk is running.

Access should be limited to error recovery operations and Expected ID changes. For more details on ID/Segment Access loading refer to Section 5.9.7, Disk Register File Access, on page 165.

IDCE = ID Register File External Access Enable

When this bit is set, the normal WCS access to the ID Field register file is disabled and the IDA[4:0] address lines have priority. This occurs when the microprocessor needs to examine the ID field data that has just been read or the microprocessor wishes to force the ID Register file to a fixed value. This bit must be RESET to allow internal access by the disk controller.

IDA[4:0] = ID Register Address

This is the address which the microprocessor is accessing by reading or writing the ID/Segment Data Register.

4.3.20 ID/Segment Data

IDSEGDT Register address = 36							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IDD7	IDD6	IDD5	IDD4	IDD3	IDD2	IDD1	IDD0

IDD[7:0] = ID/Segment Data

The ID RAM stores the expected ID Identifier (Block Count or C/C/H/S), the actual ID Identifier (Active A and B ID fields), and the Data Segment Count values or the ID flag field. The microprocessor can modify or observe these bytes through this register. ID Regfile is **top justified**, always starting at the first location of the designated block and filling consecutive locations without any gaps, regardless of the type or size of the ID. For more details on the type of ID data stored refer to Section 5.9.9, ID Capture

Register File Access, on page 167. This ID RAM is mapped as shown in Table 4-5.

The ID/Segment register file stores expected data (prewritten ID information) and disk data written or read to/from the disk port during an ID field operation. The Expected ID, address 24 - 27, is data which is typically stored in preparation of disk read/write operation. The Active A and B ID fields contain the present ID passing to/from the disk. These ID fields are identical. These fields are used when an ECC or drive error is detected. The sector's ID field is stored in the Active A or B fields until the error is corrected. For details on the ACTA, ACTB, ECCA, ECCB flags refer to Section 4.3.11, Sequencer Status 1, on page 35). In WDMODE a complete Active A field consists of the Active field, address 0 - 3, and the Data Segment Count, address 8 - 15. A complete Active B field consists of the Active field, address 4 - 7, and the Data Segment Count, address 16 -23.

There are two parameters which define how data is stored and manipulated in the ID/Segment registers. These parameters are BLKMODE and WDMODE. The BLKMODE bit, refer to Section 4.3.2, Disk Configuration 2, on page 31, defines the configuration of the Expected ID field. The Expected ID is define as 1) a Logical Block Address (LBA) or 2) physical format (Cylinder High Cylinder Low, Head, and Sector). When BLOCKMODE is set the format is LBA. In addition the ID3OR4 bit, (Refer to Section 4.3.2, Disk Configuration 2, on page 31), select the size of the LBA field. When ID3OR4 is set there are four bytes in the expected LBA field. When ID3OR4 is reset there are three bytes in the expected LBA field. The position of the expected LBA field in the ID/Segment register file always starts at address 27. The Active A, Active B and Expected ID fields are always **top justified and contiguous**. I.E. the first ID byte is placed into address 0, 12 or 24 respectively. Any additional information (flags etc.) are placed immediately after the ID in consecutive locations, without any gaps in between.

Address	$\overline{\text{WDMODE}}$		WDMODE	
	BLKMODE	$\overline{\text{BLKMODE}}$	BLKMODE	$\overline{\text{BLKMODE}}$
0 - 3	Active A ID	Active A ID	Active A ID	Active A ID
4 - 7	Active A ID	Active A ID	Data Seg A Cnt	Data Seg A Cnt
8 - 11			Data Seg A Cnt	Data Seg A Cnt
12 - 15	Active B ID	Active B ID	Active B ID	Active B ID
16 - 19	Active B ID	Active B ID	Data Seg B Cnt	Data Seg B Cnt
20 - 23			Data Seg B Cnt	Data Seg B Cnt
24 - 31	Expected ID Bytes	Expected ID	Expected ID Bytes	Expected ID Bytes
24	LBA-MSB (bits 30-24)	Cylinder High	LBA - MSB (bits 30-24)	Cylinder High
25	LBA - (bits 23-16)	Cylinder Low	LBA - (bits 23 - 16)	Cylinder Low
26	LBA - (bits15-8)	Head	LBA - (bits15-8)	Head
27	LBA - LSB (bits 7-0)		LBA - LSB (bits 7-0)	
28 - 31	Expected ID Flags	Expected ID Flags	Expected ID Flags	Expected ID Flags

TABLE 4-5 ID/SEGMENT REGISTER MAP

4.3.21 WCS - CSERR Register

CSERR Register address = 38							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WDID	RS ECC	SKAD 1	SKAD 0	FAIL	RTY	DAC	SQ OUT

A write operation to this location defines the next data to be written to the WCS. For more details on WCS loading refer to Section 5.9.7, Disk Register File Access, on page 165.

WDID = WD ID Mode (Data Sector Segmentation Mode)

When the WDMODE bit is set, refer to section 4.3.2, Disk Configuration 2, on page 31, this bit is used as part of the Defect skipping function. When this bit is set, it triggers the defect skipping function and skip-mask state machine to prepare for data segmentation.

When WDMODE is set, the data field can be divided into multiple data segments. When this happens the data segment count and flags which have been stored in the ID register during an ID read operation are used to define the size of each data field segment. Refer to Theory of Operations Section 5.3.4, Read/Write Sector without Segmentation - 10C01 Backward Compatibility Mode, on page 107 for more details. The instruction with WDID bit must be followed by at least four rrclks before the WG or RG bits are activated. This time is necessary to prepare the WDMODE state machine and counters with the next setup.

RSECC = Calculate Reed Solomon ECC

When this bit is set, the ECC generator logic is enabled. The source of the data may be the disk, if READGATE, BUFF, are active and RCMPEN is reset; 2) the Disk FIFO if WRTGATE is active and BUFF is set; 3) the WCS immediate field CSVAL is selected, if WRTGATE is active and BUFF is reset; or 4) the disk if READGATE, BUFF, RCMPEN are set.

SKAD1, SKAD0/ES = Skip Address Select and End of Sector Flag (3 possible skip locations)

When WDMODE is set, these bits define which address the WCS shall move at the end of the present instruction. There are 3 possible skip addresses. Skip Address of 00 selects the Skip address 1. Skip address of 01 selects skip address 2. Skip address of 10 selects skip address 3. These addresses are initialized by the microprocessor before the Control Store is activated.

When SKPEN is reset, SKAD0 is used as ES, End of Sector bit. This bit is used to generate the end of sector flag for the buffer manager, indicating that a true end of sector has been reached. If FAIL is set this ESPEND flag is qualified with no disk errors and no ECC errors. This bit is used to enable a Buff Count and external Block Count update. This bit is also used to qualify the reasons for failure detection. When this bit is reset and the FAIL bit is set, all errors except the ECC errors are examined by the WCS. When the ES and FAIL bits are set, all errors including the ECC error are examined by the WCS.

SKPEN and FAIL or SKPEN and ES or SKPEN, FAIL, and ES cannot be set concurrently.

FAIL = Fail Recovery Control

When this bit is set and any of the following errors are set, the Control Store aborts its present operation and generated a SEQSTP interrupt and the corresponding error interrupt. The error conditions which cause an abort operation at a FAIL instruction are:

a) Parity Error detected at the Disk port during disk read if enabled

b) Parity Error detected at the Buffer port during a buffer read if enabled.

c) LRC Error detected during a disk write operation if enabled

d) DRVFAULT is detected if enabled

e) Disk FIFO overrun/underrun condition

f) LRC Error

g) COMPARE Error

h) WRAP error if enabled

i) CMPIER Error

Most of above mentioned errors also generate a corresponding interrupt when the FAIL bit is set and the Control Store aborts. The Drive Fault, Buffer parity error, and Disk Overrun/ underrun interrupts are not linked to the FAIL bit. These error interrupts are generated as soon as the error is detected.

These interrupt error flags are reset when the microprocessor writes to its corresponding interrupt register bit or sets the SRST bit, refer to Section 4.3.1, Disk Configuration, on page 30.

NOTE

IF the FAIL bit and ES bit are set an ECC error is also checked by the FAIL bit. The timing relationship an ECC error and the FAIL/ES bit combination is critical. Refer to Sections 5.3.3, Read/Write Sector with Data Segmentation, on page 102 and 5.3.4, Read/Write Sector without Segmentation - 10C01 Backward Compatibility Mode, on page 107 for more details.

An abort condition at a FAIL instruction also causes the WRTGATE, READGATE, SEQOUT, and AMENA signals to be reset at the pins. The WCS resets its instruction field when the abort occurs.

RTY = Retry control

When this bit is set, the Control Store shall jump to the LOOP instruction and continue executing when any of the following errors are detected.

a) ID CRC Error

b) CMPIER Error

c) Compare Error

When the RETRY jump is performed the above mentioned internal error flags are reset. The corresponding interrupt is only reset when the microprocessor writes to its corresponding interrupt register bit or sets the SRST bit, refer to Section 4.3.1, Disk Configuration, on page 30.

DAC = Data Field Active

This bit is used to identify the location of the data field within the control store sequence. This bit when combined with RSECC define when the LRC is to be calculated.

SEQOUT = Enable SEQOUT pin

When this bit is set the SEQOUT output pin is set. This bit is also reset when the WCS aborts.

4.3.22 WCS - CSCTL Register

CSCTL Register address = 3A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SV SEL	CW SEL	WG	RG	AM	CMP ENW	SKP EN	JMP EN

A write operation to this location defines the next data to be written to the WCS. For more details on WCS Access loading refer to Section 5.9.7, Disk Register File Access, on page 165.

SVSEL = CSVAL Register Control

When this bit is set, the CSVAL byte represents the bits described in the CSVAL register. When this bit is a zero, the CSVAL byte is considered an immediate value. This immediate value can be used to write to the disk or compare to data from the disk.

CWSEL = CSCNT Register Control

When this bit is set, the CSCNT byte represents the bits described in the CSCNT register. When this bit is a zero, the CSCNT is considered an immediate value. This immediate value is used to define the quantity of RRCLKs that the control store shall remain at the present address.

WG = Write Gate Pin Active

When this bit is set, the WRTGATE output pin is active high. WRTGATE remains high for as long as the Control Store remains at this location or an abort occurs due to an error condition.

RG = Read Gate pin Active

When this bit is set, the RDGATE output pin is active high. RDGATE remains high for as long as the Control Store remains at this location or an abort occurs due to an error condition.

AM = AMENA pin Active

When this bit is set, the AMENA output pin is active high. AMENA remains high for as long as the Control Store remains at this location or an abort occurs due to an error condition.

CMPENW = Compare Enable

When this bit is set, the input disk data is compared to:

1. a CSVAL immediate field (SVSEL is reset)

   If no valid compares occur before the CS count exhausts a CMPIER flag is set.

2. The buffer data (BUFF is set and SVSEL is set)

   The Control Store performs a byte for byte comparison with FIFO data until the CSCNT is exhausted. If the bytes do not compare a CMPER flag is set.

3. The ID data (ID is set and SVSEL is set)

   The Control Store performs a byte for byte comparison with expected ID data until the CSCNT is exhausted. If the bytes do not compare a CMPER flag is set.

The default compare data is the CSVAL immediate data.

SKPEN = Skip Enable

When this bit is set the WCS shall skip to the address specified in the selected skip address, SKPSEL[1:0] at the end of the present control store instruction. The qualities which define the end of the instruction are 1) CSCNT is zero if CWSEL is a 0, or 2) any Wait condition is met if CWSEL is a 1.

JMPEN = Jump Enable

When this bit is set, the WCS shall jump to the address specified in the LOOP address register if the internal Block Count, the quantity of sectors to be transferred is nonzero and there are no outstanding Pause requests. The buffer manager generates a pause request when it has the Skip mode enabled and a "0" has been detected in the next skip mask bit. When the pause request is removed, the WCS jumps to the LOOP address and continues execution.

4.3.23 WCS - CSVAL Register

CSVAL Register address = 3C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BUFF	NO XFR	LAST	ID	CHK			WDAC

If SVSEL, bit 7 of CSCTL, is reset, this value is considered the immediate count/data value. When SVSEL is high, this register generally controls the WCS ID/Data Compare logic. A write operation to this location defines the next data to be written to the WCS.A read operation of this location simply reads the WCS register file. For more details on WCS Access loading refer to Section 5.9.7, Disk Register File Access, on page 165.

BUFF = Buffer Enable

When this bit is set, data moves to or from the Disk FIFO. When this bit transitions from a 0 to a 1 the internal block count is decremented by one. For details refer to Section 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139.

NOXFR = No Transfer

When this bit transitions from a 0 to a 1 the internal block counter decrements by 1. There is no transfer from the Disk FIFO. For details refer to Section 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139.

LAST = Last Data

When this bit is set, the WCS is flagged that this is the last Control Store word of the data field. This bit is used in conjunction with the CS counter. The last byte of the data field is identi-

fied by the LAST bit being set and the immediate CS counter is exhausted.

ID = ID Enable

When this bit is set, the internal ID registers are used to store the disk data on ID reads or FIFO data during ID writes. This bit is used with the READGATE, WRITEGATE, and BUFF bits. The following is a list of typical combinations:

ID * WRTGATE * $\overline{\text{BUFF}}$ * $\overline{\text{READGATE}}$

In this mode the ID which was previously initialized is written to the disk.

ID * WRTGATE * BUFF * $\overline{\text{READGATE}}$

In this mode the ID is coming from the Disk FIFO. This data is being written to the disk and being stored in the ID registers. (WDMODE primarily)

ID * $\overline{\text{WRTGATE}}$ * $\overline{\text{BUFF}}$ * READGATE

In this mode the ID is being read from the disk and being stored in the ID registers. This data can also be compared with the expected ID which is stored in the ID registers.

ID * $\overline{\text{WRTGATE}}$ * BUFF * READGATE

In this mode the disk ID is stored in the ID/Segment registers, and sent to the Disk FIFO.

CHK = ID CRC and ECC Verify Enable

When CHK and CRCEN are set, the internally calculated ID CRC is written to the disk if WRTGATE is active or compared to the disk read CRC if READGATE is active. When this bit is set and CRCEN is reset the internally calculated data CRC/ECC is written to the disk if WRTGATE is active or compared to the disk read CRC/ECC if READGATE is active.

NOTE

If CHK is set and CRCEN is reset the Expected ID field is also incremented.

LRCEN = LRC Check Enable

This bit is set when the LRC bytes are written to the disk. This bit identifies the location of the LRC bytes and enables the internal compare logic. LRC calculation is active whenever DAC and WRTGATE are active. The LRC calculator is initialized at the WCS Start location. The LRC is reset to AAAA whenever a Logical boundary is detected and no errors are found. Refer to Section 5.10.1, DISK PORT LRC OPERATION, and Section 5.10.2, SCSI LRC OPERATION, for more details.

CRCEN = ID CRC Calculation & Check enable

When this bit is set, the ID CRC calculator is enabled. The ID CRC calculator is disabled when CRCEN and CHK bits are active.

WDAC = Wait for Defect Skip Count Zero or Sector Mark

This bit is used during the WDMODE. In WDMODE the ID format contains flags, LSEG and WSCT. These flags are used to define how the data field has been divided. The data field can be split because the data field spans a sector mark, a defect area, or no segmentation at all. The WDAC is used when a data segment boundary is expected. This wait instruction can exit due to a sector mark detection or a defect skip count of zero.

4.3.24 WCS - CSCNT Register

CSCNT Register address = 3E							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	WIAM	WIX	WSM	STOP			WGCZ

If CWSEL, bit 7 of CSCTL, is reset, this value is considered the immediate count value. When CWSEL is high, this register generally controls the WCS Wait logic. A write to this location loads the CSERR, CSCTL, CSVAL, and CSCNT values into the WCS. The WCS write address is also incremented. For more details on WCS Access loading refer to Section 5.9.7, Disk Register File Access, on page 165.

WIAM = Wait for ID Address Mark

When this bit is set the Control Store waits for an AMDET signal. When AMDET is received the Control Store moves to the next instruction.

The Control Store only changes when this condition is met.

If WIAM and CMPEN are set the Control Store waits for an AMDET and a valid compare of the disk data to the CSVAL immediate data byte. The Control Store only changes when this condition is met.

WIX = Wait for Index Detect

When this bit is set the Control Store waits for an Index Detect to be received.

WSM = Wait for Sector Mark

When this bit is set the Control Store waits for an Sector Mark Detect to be received.

STOP = Stop WCS at Present Address

When this bit is set the Control Store stops operation at this instruction and goes to the idle state, resetting its instruction register.

WGCZ = Wait Until Generic Counter is Zero

When this bit is set the control store waits for the end of the present WD data segment to be reached. See Section 5.3, WRITE CONTROL STORE: DISK CONTROL, on page 93.

4.3.25 Defect Skip Size

DEFSKP Register address = 40							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0

DF[7:0] = Defect Size

Defect skip byte count for the control store in wdmode operation.

4.3.26 Microprocessor Disk FIFO Access

DFIFOH Register address = 42							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DFH7	DFH6	DFH5	DFH4	DFH3	DFH2	DFH1	DFH0

DFIFOL Register address = 44							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DFL7	DFL6	DFL5	DFL4	DFL3	DFL2	DFL1	DFL0

DFH[7:0] = Disk Data FIFO High Byte

DFL[7:0] = Disk Data FIFO Low Byte

The FIFO can execute a 60C40-like loop back mode. In this mode the Disk buffer manager logic is set to complement microprocessor operation. This means the microprocessor should never share the same side of the FIFO. The buffer should only read the FIFO when the microprocessor is writing the FIFO.

The Disk FIFO is a word-based FIFO. Since the microprocessor bus is byte based, the microprocessor must construct words for transfer into the FIFO. It is important to note that no Disk DMA transfer should occur during a microprocessor Read or Write. No Buffer DMA writes to the FIFO should occur when the microprocessor writes to the FIFO.

Writing to the FIFO is performed in two steps. First, the microprocessor writes the FIFO low byte, DFIFOL. This data byte is loaded into a holding register. Next, the microprocessor writes to the FIFO high byte, DFIFOH. This action does two things, 1) loads the data into a holding register and 2) flags the FIFO that a word is ready for transfer.

NOTE

There is a delay of 4 BCLKs from the rising edge of WEB before the word is written to FIFO. The previously written data will be corrupted if the microprocessor writes to these register before this time.

Reading from the Disk FIFO are performed in two steps. First, the microprocessor reads the low byte, DFIFOL. Next, the microprocessor reads the FIFO high byte, DFIFOH.

NOTE

When the microprocessor read strobe REB, goes from low to high the FIFO pointer is changed 4 BCLKs later. This means that the FIFO data is invalid for this period of time.

4.3.27 Disk FIFO Status/Control

DFSTAT Register address = 46							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DLP EN	DFULL	DEM PTY	DF CNT4	DF CNT3	DF CNT2	DF CNT1	DF CNT0

DLPEN = Loop Back Enable

When this bit is set the microprocessor has access to the FIFO and all Disk Control Store operations are disabled. For normal DMA operations this bit must be reset. Refer to Section 5.6.5, Loopback Mode, on page 129.

DFULL = FIFO is Full (Read Only)

When this bit is set the FIFO, 16 words deep is full.

DEMPTY = FIFO is Empty (Read Only)

When this bit is set the FIFO, 16 words deep is empty.

DFCNT[4:0] = FIFO up/down count (Read Only)

This is the FIFO *word* count. This count value indicates the number of words still in the FIFO. (This bit is independent of data direction).

4.3.28 Disk FIFO Threshold

DFTHRES Register address = 48							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
			FT4	FT3	FT2	FT1	FT0

FT[4:0] = FIFO Threshold

These bits define the threshold at which the Disk FIFO requests immediate service to avoid an under/overrun condition. A value of 10h will hold off an 'Urgent' request until the fifo is full for disk read operations. A value of 1h will force the fifo to make an 'Urgent' request when 1 or more words are in the FIFO during a disk read operation. Same evaluation is applicable for a disk write from the buffer. (Refer to section 5.6.4, Buffer Arbitration, on page 129 for more information on 'Urgent' requests).

For optimum system performance the value programmed in this register should accurately reflect the demands being made of the Buffer Manager. Refer to section 5.6.2, Disk FIFO Threshold Programming, on page 128.

4.3.29 Disk FIFO BIST Control Status

DFB Register address = 4A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DB FLG	DBC	DFF ENA			DCLK SW	DBF CHK	DBIST ST

For more detail on the BIST controls and flags, (BFLG, BC,BFCHK, and BISTST), refer to section 5.9.11, Register File BIST (Built In Self Test), on page 168.

DBFLG = BIST Flag (Read Only)

DBC = BIST Complete (Read Only)

DFFENA = FIFO enable (Read/Write)

When this bit is set the FIFO read/write pointers and FIFO counters are enabled. When this bit is reset, these counter are held in a reset condition.

DCLKSW = Data FIFO Clock Switch

This bit must be reset during normal data transfers to/from the disk data FIFO. This bit is set when the FIFO is to undergo BIST testing and the normal data transfers are idle.

NOTE

No data transfers to/from the FIFO are valid when this bit is set.

DBFCHK = BIST Flag Check (Read/Write)

DBISTST = BIST Test Mode (Read/Write)

4.3.30 CRC/ECC Control

CECTL Register address = 4C							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EC RST			CRC VD	R CONT	ECB EN	ECO EN	SHLD

ECRST = Reset all ECC

When set by the microprocessor, both the Syndrome and Relative Offset/Mask Generators are reset. The SRST bit, refer to Section 5.9.6, Disk Manager Soft Reset Operations, on page 165, also resets all ECC logic. This bit is not used in normal OTF operation. If the user should need to reset the ECC logic without affecting the rest of the device, the microprocessor must set this bit. To negate the ECC reset, the microprocessor must write a zero to the ECRST bit.

Reset state: 0

CRCVD = CRC Field Valid

When set, the disk format also includes a four byte CRC field for the data field. When reset, no CRC field is included for the format.

Reset state: 1

RCONT = Read Continuous Mode

When this bit set the ECC expects to check the incoming read data and generate the syndrome and generate an offset/mask if an error is detected. If the error is correctable the ECC corrector performs the correction in the data buffer. If the data is considered uncorrectable no correction is performed and the data transfer continues. An ECC error interrupt is generated if enabled.

Reset state: 0

ECBEN = Enable Buffer Corrector

This bit Enables/Disables On The Fly (OTF) error correction for disk read operations. When set, the appropriate data condition status will be reported and the Relative Offset/Mask Generator will transfer the masks and relative offset to the buffer corrector if the error is on-the-fly correctable. When reset, the appropriate data integrity status is still reported but the masks and relative offsets will not be transferred to the buffer corrector, i.e. no correction will be performed.

Reset state: 1

ECOEN = Enable Relative Offset/Mask Generator

When reset, the syndrome generator maintains its last condition. This mode is primarily used during a sector reread. No new sector can be read. When this bit is set, the syndrome generator is automatically reset when the syndrome is passed to the offset/mask logic. The microprocessor must set this bit to return to normal ECC operation.

Reset state: 1

SHLD = Syndrome Generator Hold

When set, the Syndrome Generator will not automatically reset after the composite syndromes are transferred to the Relative Offset/Mask Generator. This means that all reads must halt if there is an error in the composite syndromes that may or may not be on-the-fly correctable. Normal ECC operation will continue after the Relative Offset/Mask Generation is complete, i.e. if the error is on-the-fly correctable or if not on-the-fly correctable the composite syndromes have been read. When the SHLD bit is zero, the Syndrome Generator will automatically reset after the composite syndromes have been transferred.

Reset state: 0

The microprocessor may set ECRST at anytime but all ECC activities will abort and all contents will be lost. The other bits may not be changed while SACT or OACT bits are set in the ECC status register.

4.3.31 ECC Status

ECCSTAT Register address = 4E (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ECCBD	ECCGD	REQ	SACT	OACT	ECCER	CRCER	OMER

ECCBD = ECC Bad

This bit indicates whether or not the sector read had an ECC and/or CRC error. This bit is set after the last byte of the ECC field if an error has been detected. If the error is On The Fly correctable this bit will be reset when the correction in the buffer is complete. This bit will never be set while ECCGD bit is set.

Reset state: 0

ECCGD = ECC Good

This bit indicates whether the sector read is free of CRC/ECC errors. This bit may be set after the last byte of the ECC field is read if there were no errors. It can also be set after the buffer corrector performs the correction. This bit is never set while the ECCBD bit is set.

Reset state: 0

REQ = Request for Buffer Corrector

When set, the error is on-the-fly correctable and requesting an acknowledge from the buffer corrector. The acknowledge will reset the REQ bit and the relative offsets and masks are then transferred. If the ECBEN bit is reset or if the error is not on-the-fly correctable then REQ will remain reset.

Reset state: 0

SACT = Syndrome Generator Active

When set, the Syndrome Generator is active. When reset, the syndrome generator is not active and is ready for the next read. If SHLD is set, SACT will be set during both syndrome generation and Relative Offset/Mask generation.

Reset state: 0

OACT = Relative Offset/Mask Generator Active

When set, the Relative Offset/Mask Generator is active. When reset, the O/M Generator is not active. This bit indicates that on-the-fly correction is being attempted.

Reset state: 0

ECCER = Data ECC Error Detected

When set, the composite syndrome is non-zero, resulting from an ECC error. An ECC error has been detected in the data field. When reset, the composite syndrome is zero indicating no ECC error. This bit is valid only after the Syndrome Generation is complete, i.e. SACT is reset, or if SHLD is set then when SACT and OACT are both set.

Reset state: 0

CRCER = Data CRC Error Detected

This bit is enabled if CRCVD is set, i.e. CRC field included in format. When the CRCER is set, the CRC detected an error in the data field. When reset, no CRC error was detected in the data field. This bit is valid only after the Syndrome Generator is complete, i.e. SACT is reset, or if SHLD is set then when SACT and OACT are both set.

Reset state: 0

OMER = Error Relative Offset/Mask Error

When set, on-the-fly correction failed. When reset, on-the-fly correction performed. This bit is only valid after Syndrome Generation is completed and OACT negates.

Reset state: 0

4.3.32 ECC Syndrome Bytes

ECC SYN Register address = 50 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0

ES[7:0] = ECC Syndrome Bytes

The microprocessor reads this register in one of two conditions. The first condition is with the ECOEN bit zero (single sector read mode), SACT negated, and ECCER is set. If the ECCER and CRCER are reset then the initial error was a soft error in which case the composite syndromes cannot be read and ECC operations continue. The second condition is when the SHLD bit is one and the error is not "On-the-Fly" correctable. The microprocessor must read all the composite syndromes. The total number of reads will be 18. The higher order bytes will be read first to the lowest order and in each order the highest interleave is read first to the lowest interleave. If CRC is included in the data field the user reads 22 bytes. The last four bytes are the data CRC, starting with the highest order bytes.

4.3.33 ECC Largest Interleave Size

EILVO Register address = 54							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
					LILV2	LILV1	LILV0

LILV[2:0] = ECC Largest Interleave Size

When set the bits represent the largest interleave number with the largest interleave size. The following figure is an example of how the data sector may occupy the ECC interleaves. In this example, the bits LILV1 = LILV0 = 1 and LILV2 = 0 because interleave 0 and 1 are the largest interleaves.

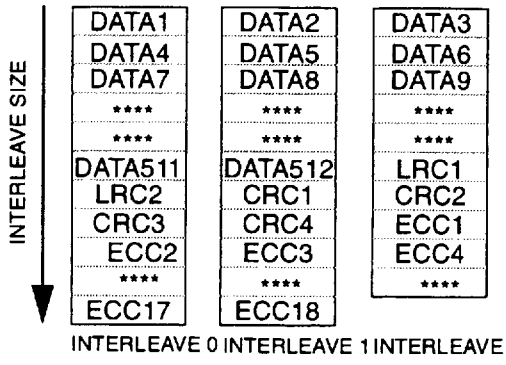

FIGURE 4-1 INTERLEAVE SIZE EXAMPLE

4.3.34 ECC Sector Size

ECCSM Register address = 5A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
						EPB9	EPB8

ECCSL Register address = 5C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
EPB7	EPB6	EPB5	EPB4	EPB3	EPB2	EPB1	EPB0

EPB[9:0] = ECC Sector Size

These registers are programmed to reflect the total number of bytes over which ECC is calculated. This count includes the Data field *and* an optional LRC field.

Valid range = 1_{10}-747_{10}

4.3.35 Logical to Physical Block Ratio for LRC

LPR Register address = 5E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PL3	PL2	PL1	PL0	LP3	LP2	LP1	LP0

PL[3:0] = Partial logical block start count

These values define the quantity of physical blocks in the first logical block data transfer after this register is written. The quantity of physical blocks per logical block for all subsequent transfers defaults to LP[3:0]. This register must be written whenever: 1) the logical block changes size, 2) the first logical block transfer is a partial block transfer, or 3) following a power on reset condition.

If N is the total number of physical blocks per logical block, then PL[3:0] is programmed with a range of N-1 to zero. For example, a logical block of eight physical blocks has a range of 7 to 0. The first physical block is defined by PL[3:0] = 7. The last physical block is defined by PL[3:0] = 0. The higher PL[3:0] value defines an earlier physical block position within the logical block. (Remember, this value only applies to the first logical block after this register is written.)

LP[3:0] = Logical to Physical Block Count Ratio

These bits define the quantity of physical blocks (sectors) for each logical block. These bits are use with the WCS LRC bit and WRITGATE bit. This combination of control signals when the LRC bytes, are checked during write operations. The WCS LRC bit defines the location of each LRC field. A calculated LRC is compared against the LRC which is written to the disk.Each time the WCS LRC bit is active the Logical to Physical Counter decrements by one unless LP[3:0] is zero. When this counter reaches zero (a logical boundary is reached), the calculated LRC bytes are reset to $AAAA_{hex}$. LP[3:0] define how often the calculated LRC bytes are reinitialized.

LP[3:0] = N -1; Number of physical blocks per logical block

= 7_{10}; 8 physical blocks per logical block

= 15_{10}; 16 physical blocks per logical block

If WCS aborts, a read of the Logical to Physical Register gives the LPR ratio to be programmed for continuing the calculation, starting at the aborted block sector.

The Default value for LPR register is 00hex or one physical block per logical block. For more details refer to Section 5.10.1, Section 5.10.2, and Section 4.6.1.19.

4.3.36 LRC Preset Bytes

LRCHI Register address = 60							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LR15	LR14	LR13	LR12	LR11	LR10	LR9	LR8

LRCLO Register address = 62							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0

LR[15:0] = LRC Preset Bytes

When these bits are loaded the next Disk write operations begins the LRC calculation with this seed. This is primarily used when the disk transfers begins on a partial logical block boundary. When the next logical block boundary is reached *the LRC is reinitialized to a fixed pattern, AAAAhex.*

If the WCS aborts, a read of these registers gives the LRC residue that can be used for presetting on the next start command. In case of a LRC error, the residue will be incorrect. In this case the preset bytes must be retrieved from the buffer.

When reset, these registers initialize to AAAA-hex pattern.

For more details, refer to Section 5.10.1, DISK PORT LRC OPERATION, Section 5.10.2, SCSI LRC OPERATION, and Section 4.6.1.19 on page 76.

4.3.37 ID Capture Address/Data/Control

IDCAP Register address = 64							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0

When the microprocessor writes a one to bit 7, the ID capture feature is armed. The content of ID[2:0] will be the starting address for the read of ID Capture data after an IDFULL interrupt has been generated. An IDFULL interrupt occurs when a complete ID field is read and the ID CRC is good. When the IDFULL interrupt is generated, this register contains a **valid** ID field.

The captured ID is always **top justified**, starting at address 00 and is loaded in consecutive locations without any gaps, regardless of the ID type or size. A valid ID consists of a complete ID field and a good ID CRC. Their are eight ID values at this one microprocessor address. To read these values the microprocessor must first write the first address, 00 to 07hex, to this location. The microprocessor then reads this location. After reading a byte the internal read address autoincrements. The next value can be read after 4 BCLKs from the rising edge of the microprocessor read strobe.

The size of the ID field is defined by the ID bit in the WCS instruction sequence. Refer to Section 5.9.9, ID Capture Register File Access, on page 167 and Section 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139.

IC[2:0] = ID Capture Control/Address / ID data [2:0] (Read/Write)

IC[6:3] = ID Capture data [6:3] (Read Only)

IC[7] = ID Capture Arm Control / ID data [7] (Read/Write)

4.3.38 ID BIST Control Status

IDB Register address = 66							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BFC	BIST	WCS BF	WCS BC	IDCBF	IDCBC	IDSBF	IDSBC

Refer to Section 5.9.11, Register File BIST (Built In Self Test), on page 168 for more details.

BFC = BIST Flag Check

BIST = BIST Test Enable Mode

WCSBF = WCS BIST Error Flag (READ ONLY)

WCSBC = WCS BIST Complete (READ ONLY)

IDCBF = ID Capture BIST Error Flag (READ ONLY)

IDCBC = ID Capture BIST Complete (READ ONLY)

IDCBF = ID/Segment BIST Error Flag (READ ONLY)

IDSBC = ID/Segment BIST Complete (READ ONLY)

4.3.39 On-the-Fly Counter

OTF Register address = 68							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
OTF7	OTF6	OTF5	OTF4	OTF3	OTF2	OTF1	OTF0

This register counts the number of on-the-fly error corrections. This counter increments whenever a successful correction is performed. The Counter wraps from FFh to 00h. This counter is reset by an active POR bit condition (see CFG1, Section 4.2.1 on page 28), by an active SRST bit (see DCNF1, Section 4.3.1 on page 30) or by a microprocessor 00h byte write operation.

4.4 DISK MANAGER HOST CONTROL REGISTERS

4.4.1 Host Configuration 1

HCNF1 Register address = 70							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HFF ENA	PAWZ	DACK H	DRQH	DPEN	PGEN	MAS SEL	BURS T

For more information on DMA port operations, refer to Section 5.5 on page 120.

HFFENA = FIFO enable

When this bit is set the FIFO read/write pointers and FIFO counters are enabled. When this bit is reset, these counters are held in a reset condition. For more information, refer to Section 5.9.6, Disk Manager Soft Reset Operations, on page 165.

PAWZ = Pause Host DMA

When this bit is set, the DRQ pin is synchronously disabled.On Power on, this bit is reset. In slave mode, this bit when set disables the generation of DRQ to the master. In master mode, this bit when set disables the DRQ to the DMA control logic.

NOTE

In either case, setting this bit disables DMA control only at the end of an active DMA Cycle or when DRQ is inactive.

DACKH = DACK Active Level Selection

When this bit is set the DACK is active high. When this bit is reset, DACK is active low.

DRQH = DRQ Active Level Selection

When this bit is set the Host DRQ is active high. When this bit is reset, DRQ is active low.

DPEN = Parity Checker Enable

When this bit is set, the internal disk manager checks parity on Host port input data bus.

PGEN = Parity Generator Enable

When this bit is set, the internal disk manager generates parity on Host port data. When this bit is reset, the Host port parity is simply passed through the FIFO to/from the Buffer. Parity is always generated when the microprocessor writes to the FIFO.

MASSEL = Master Mode Select

When this bit is set the internal disk manager operates the host bus as the master. This means that the internal disk manager generates DACK, Host write strobes, and the Host read strobes. When this bit is reset, the Host Bus operates as a slave.

BURST = Burst Cycle DMA Enable

When this bit is set the Host Port is placed in a Burst DMA cycle mode. When this bit is reset the Host Port is placed in a single cycle DMA mode. This means that there is a DACK transition for every transition of DRQ.

4.4.2 Host Configuration 2

HCNF2 Register address = 72							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DMA EN	DSRW	STRL2	STRL1	STRL0	STH2	STRH 1	STRH 0

Refer to Section 5.5 on page 120 for more information on host DMA operations.

DMAEN = DMA output Drivers Enabled

When this bit is set, the internal DRQA, DACKA, DWEB, and DREB signals are driven based upon the MASSEL bit. When DMAEN and MASSEL are set the DACK, DWEB, and DREB pins are active outputs. When DMAEN is set and MASSEL is reset the DRQ output pin is driven.

DSRW = DACK to R/W Strobe Delay

When this bit and MSSEL are set there is a three clock delay from DACK going active and the first read/write strobe.

STRH[2:0]= Master Mode Read/Write Strobe High Time

These bits define the number of clocks that the

Host DMA Strobe is high.

*High time = 2 * BCLK + (STRH[2:0] * BCLK); BCLK is primary input clock*

STRL[2:0] = Master Mode Read/Write Strobe Low Time

These bits define the number of clocks that the Host DMA Strobe is low.

*Low time = (2 * BCLK) + (STRL[2:0] * BCLK); BCLK is primary input clock.*

4.4.3 Host FIFO Microprocessor

HFIFOH Register address = 74							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
HFH7	HFH6	HFH5	HFH4	HFH3	HFH2	HFH1	HFH0

HFIFOL Register address = 76							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
HFL7	HFL6	HFL5	HFL4	HFL3	HFL2	HFL1	HFL0

The FIFO can execute a 60C40-like loop back mode. In this mode the Host buffer manager logic is set to complement microprocessor operation. This means the microprocessor should never share the same side of the FIFO. The buffer should only read the FIFO when the microprocessor is writing the FIFO.

The Host FIFO is a **word** based FIFO. Since the microprocessor bus is byte based, the microprocessor must construct words for transfer into the FIFO. It is important to note that no Host DMA transfer should occur during a microprocessor Read or Write. No Buffer DMA writes to the FIFO should occur when the microprocessor writes to the FIFO.

Writing to the FIFO is performed in two steps. First, the microprocessor writes to the FIFO low byte, HFIFOL. This data byte is loaded into a holding register. Next, the microprocessor writes to the FIFO high byte, HFIFOH. This action does two things. It loads the data into a holding register and flags the FIFO that a word is ready for transfer. There is a delay of four BCLKs before the word is written to FIFO. The previously written data will be corrupted if the microprocessor writes to these registers before this time.

Reading from the FIFO is also performed in two steps. First the microprocessor reads the low byte, FIFOL. Next, the microprocessor reads the FIFO high byte, FIFOH. When the microprocessor read strobe, REB, goes from low to high the FIFO pointer is changed four BCLKs later. This means that the FIFO data is invalid for this period of time.

The Host FIFO can be used in a "60C40 Loopback" like mode. Refer to Section 5.6.5, Loopback Mode, on page 129.

4.4.4 Host FIFO Status/Control

HFSTAT Register address = 78 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DBR	HFULL	HEMPTY	HFNT4	HFCNT3	HFCNT2	HFCNT1	HFCNT0

DBR = Data Buffer Ready

When this bit is set, the host FIFO register contains a data word.

HFULL = FIFO is Full

When this bit is set the FIFO, 16 words deep is full.

HEMPTY = FIFO is Empty

When this bit is set the FIFO, 16 words deep is empty.

HFCNT[4:0] = FIFO Up/down Count

This is the FIFO word count. This count value indicates the **number of words** still in the FIFO.

4.4.5 Host FIFO BIST Control Status

HCECTL Register address = 7A							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HB FLG	HBC	DRQ IN	DACK IN	HLP EN	HCLK SW	BF CHK	BIS TST

For more detail on the BIST controls and flags, (BFLG, BC,BFCHK, and BISTST), refer to section 5.9.11, Register File BIST (Built In Self Test), on page 168.

HBFLG = BIST Flag (Read Only)

HBC = BIST Complete (Read Only)

DRQIN = DRQ Input Condition (Read Only)

This bit reflects the condition of the Host DRQ pin. DRQ is active if this bit is high.

DACKIN = DACK Input Condition (Read Only)

This bit reflects the condition of the Host DACK pin. DACK is active if this bit is high.

HLPEN = Loop Back Enable (Read/Write)

When this bit is set the Host FIFO is configured in the loopback mode. The microprocessor has access to the FIFO and all DMA operations are disabled on the Host interface. For normal DMA operations this bit must be reset. Refer to Section 5.6.5, Loopback Mode, on page 129.

HCLKSW = Host FIFO Clock Switch (Read/Write)

This bit must be reset during normal FIFO reads and writes. When this bit is set the FIFO is prepared for BIST operation. No valid FIFO accesses are possible when this bit is set.

BFCHK = BIST Flag Check (Read/Write)

BISTST = BIST Test Mode (Read/Write)

4.5 DISK MANAGER BUFFER REGISTERS

4.5.1 Memory Configuration - Primary

MCFG1 Register address = 80							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MPAR	CAW2	CAW1	CAW0	RRC3	RRC2	RRC1	RRC0

NOTE

This register must be programmed before any buffer accesses are performed.

The Buffer Manager control logic ignores all buffer accesses until this register is written by the microprocessor. Some DRAMs may require up to 8 RAS cycles before proper operation. No refresh RAS cycles will occur until this register has been written.

MPAR = Memory Parity Disable

When this bit is set, the memory parity checker is disabled.

CAW[2:0] = Column Address Width

2	1	0	Column Width		Addr during CAS
0	o	o	8 bit column addr	64K	A[7:0]
0	0	1	9 bit column addr	256K	A[8:0]
0	1	0	10 bit column addr	1M	A[9:0]
0	1	1	11 bit column addr	4M	A[10:0]

The Column Address Width defines the active address pins. The Buffer is word wide.

RRC[3:0] = Refresh Rate

The number of clocks between refresh requests is given by:

1024 - (VAL * 64) = CLKS between refresh requests

where VAL is the decimal value of RRC[3:0].

For example, If RRC[3:0] is programmed with a value of 5 (0101b), then *1024 - (5 * 64) = 704*, meaning 704 BCLK System clocks would occur

before the next refresh request.

A table showing refresh interval ranges with variable frequencies and RRC combinations follows:

3	2	1	0	Freq. Low	Freq. High	Interval Range
0	1	0	1	45 Mhz	50	15.6 - 14.1 µs
0	1	1	0	42	45	15.5 - 14.2
0	1	1	1	40	42	14.4 - 13.7
1	0	0	0	36	40	14.2 - 12.8
1	0	0	1	30	36	14.9 - 12.4
1	0	1	0	26	30	14.7 - 12.8
1	0	1	1	22	26	14.6 - 12.3
1	1	0	0	20	22	12.8 - 11.6

4.5.2 Memory Configuration - Secondary

MCFG2 Register address = 82							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDYS	BYWD	WAIT	WAITE	F MODE			

RDYS = Microprocessor Buffer Access Ready Status (Read Only)

When this bit is set, data is available in the Buffer data Latches. Refer to Sections 4.5.26, Microprocessor Autoincrement Access Registers, on page 64.

BYWD = Byte/Word Access

When this bit is set, each write to an odd or even byte causes the WD61C96A to write the holding registers to the buffer. When this bit is reset, data is only written to the buffer when the microprocessor writes to the odd byte. For details, refer to Section 5.6.6, Microprocessor Buffer Access, on page 130.

WAIT = Wait the Microprocessor

When this bit is reset the WD61C96A assumes a waitable microprocessor. The external RDYB line is connected to the microprocessor and extends the Write and Read strobe timing accordingly. When this bit is set the WD61C96A assumes a nonwaitable microprocessor. In this mode the WD61C96A does not gate RDYB with CSB. Thus, the RDYB pin is used as status to a PIO pin on the microprocessor or the RDYB status bit is polled by a microprocessor. For details, refer to Section 5.6.6, Microprocessor Buffer Access, on page 130.

WAITE = Wait Enable

This bit is the master enable control for the RDYB output pin. When this bit is reset the RDYB is enabled. When this bit is set the RDYB pin is disabled. This control does not effect the internal operation of the buffer manager ready functions. For details, refer to Section 5.6.6, Microprocessor Buffer Access, on page 130.

FMODE = Full Disk Qualification Mode

When this bit is set the Disk Buffer manager changes state only when there are no outstanding ECC errors.

4.5.3 Memory Speed

MSPD Register address = 84							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				RASH	CASH	CASL1	CASL0

RASH = RAS High TIme Extension

When this bit is set the RAS to CAS time is extended from 2 clocks to 3 clocks. Refer to Section 7.4.1, DMA Read/ Write RAS/CAS Cycle, on page 185.

CASH = CAS High Time Extension

When this bit is set the Fast Page CAS cycle high time is extended from one clock to two clocks. Refer to Section 7.4.3, Fast Page Write Mode, on page 186.

CASL[1:0] = CAS Low Time Extension

When this bit is set the Fast Page CAS cycle low time is extended from two clocks to five clocks. Refer to Section 7.4.3, Fast Page Write Mode, on page 186.
*CAS Low = 2 * BCLK + (CASL[1:0] * BCLK)*

4.5.4 Buffer Segment Size

BSSIZE Register address = 86							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				SIZE3	SIZE2	SIZE1	SIZE0

SEG[3:0] = Memory Segment Selection

3	2	1	0	Segment Size
0	1	0	1	4 M
0	0	0	1	8 K
0	0	1	0	16 K
0	0	1	1	32 K
0	1	0	0	64 K
0	1	0	1	128 K
0	1	1	0	256 K
0	1	1	1	512 K
1	0	0	0	1 M
1	0	1	0	2 M

These bits define the size of the buffer segment per its address size. The buffer width is always 16 bits plus two parity bits.

4.5.5 Physical Block Size - Host

PBSHM Register address = 88							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
						HPB9	HPB8

PBSHL Register address = 8A							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPB7	HPB6	HPB5	HPB4	HPB3	HPB2	HPB1	HPB0

HPB[15:0] = Physical Block Size

Valid range = 1_{10} - 1023_{10} (747_{10} with ECC)

This value represents the complete sector byte size. Typically, this includes the Data field and LRC bytes per sector.

NOTE

This count must NEVER be set to zero for a host data transfer.

4.5.6 Physical Block Size - Disk

PBSDM Register address = 8C							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
						DPB9	DPB8

PBSDL Register address = 8E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DPB7	DPB6	DPB5	DPB4	DPB3	DPB2	DPB1	DPB0

DPB[15:0] = Physical Block Size

Valid range:

= 0_{10} - 743_{10} with CRC
= 0_{10} - 747_{10} without CRC

This value represents the complete sector byte size. Typically, this includes the Data field and LRC bytes per sector. As an example, a count of ZERO is used during a FORMAT operation when no data is supplied from the buffer. All other operations require a nonzero count value.

4.5.7 Host Buffer Interrupt Status

HBINT Register address = 90							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPP ER	HBP ER	HVVB ER	UPP ER			HV BSY	H BSY

These interrupt bits reflect the condition of the Host buffer manager logic. Each bit reflects the condition of an internal interrupt status flag. These interrupt bits are cleared by writing a one to its appropriate bit at this address. For more details on system operations of these interrupts refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

HPPER = Host Bus Parity Error

This bit is set when a host bus parity error has been detected during a Host Bus transfer.

HBPER = Data Buffer Bus Parity Error

This bit is set when a buffer port parity error has been detected during a Host Buffer Read transfer.

HVVBER = Very Very Busy Error

When this bit is set the microprocessor has requested another DMA start while the Host DMA pipeline is already in a Very Busy state.

UPPER = Microprocessor Buffer Parity Error

When this bit is set a parity error has been detected during a microprocessor buffer read operation.

HVBSY = Host Very Busy Interrupt

This bit is set when the DMA pipeline moves from a VERY BUSY to BUSY condition. On a buffer read, this occurs when the Transfer counter is zero (both block count and physical count) and no parity error has occurred. On a buffer write, this occurs when the Transfer counter is zero, no Host port parity error, and the FIFO is empty.

HBSY = Host Busy Interrupt

This bit is set when the DMA pipeline moves from a BUSY to IDLE condition. On a buffer read, this occurs when the Transfer counter is zero (both block count and physical count) and no parity error has occurred. On a buffer write, this occurs when the Transfer counter is zero, no Host port parity error, and the FIFO is empty.

4.5.8 Disk Buffer Interrupt Status

DBINT Register address = 92							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DBCC INT	DB PER	DVVB ER	DOV UN	DDV BSY	DD BSY	DV BSY	DBSY

These interrupt bits reflect the condition of the disk buffer manager logic. Each bit reflects the condition of an internal interrupt status flag. These interrupt bits are cleared by writing a one to this address. For more details on system operations of these interrupts refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

DBCCINT = Disk Block Count Compare Interrupt.

This bit is set when the value loaded into the DBCC register equals the current Disk block count.

DBPER = Disk Data Buffer parity Error

This bit is set when a buffer parity error has been detected during a Disk Buffer Read transfer or an ECC read operation during data correction.

DVVBER = Very Very Busy Error Interrupt

When this bit is set the microprocessor has requested another DMA start while the Disk DMA pipeline is already in a Very Busy state.

DOVUN = Disk FIFO Over/Underrun Error Interrupt

When this bit is set, a Disk FIFO overrun or underrun has been detected during a disk transfer. An *overrun* condition is generated when the disk port attempts to write to a FULL Disk FIFO. An *underrun* condition is generated when the disk port attempts to read from an EMPTY Disk FIFO.

DDVBSY = Disk Delayed Very Busy Interrupt

This bit is set when the DMA pipeline moves from a VERY BUSY to BUSY condition.

On a buffer read, this occurs when:

1. The Transfer Counter is zero (both block count and physical count) for this pipeline load
2. An End of Sector Flag is pending for this pipeline load.
3. No buffer parity errors occurred during this pipeline load

On a buffer write, this occurs when:

1. The Transfer Counter is zero, (both block count and physical count) for this pipeline load
2. An End of Sector Flag is pending for this

pipeline load.

3. There are no outstanding ECC corrections pending for this pipeline load. If an ECC correction is pending, this interrupt is generated when this correction is successfully completed.
4. No ECC correction buffer parity error occurred during this pipeline load.

DDBSY = Disk Delayed Busy Interrupt

This bit is set when the DMA pipeline moves from a BUSY to IDLE condition.

On a buffer read, this occurs when:

1. The Transfer counter is zero (both block count and physical count) for this pipeline load.
2. An End of Sector Flag is pending for this pipeline load.
3. No buffer parity errors occurred during this pipeline load.

On a buffer write, this occurs when:

1. The Transfer counter is zero, (both block count and physical count) for this pipeline load.
2. An End of Sector Flag is pending for this pipeline load.
3. There are no outstanding ECC corrections pending for this pipeline load. If an ECC correction is pending, this interrupt is generated when this correction is successfully completed.
4. No ECC correction buffer parity errors occurred during this pipeline load

DVBSY = Disk Very Busy Interrupt

This bit is set when the DMA pipeline moves from a VERY BUSY to BUSY condition.

On a buffer read, this occurs when:

1. The Transfer counter is zero (both block count and physical count) for this pipeline load.
2. An End of Sector Flag is pending for this pipeline load.
3. No buffer parity errors occurred during this pipeline load.

On a buffer write, this occurs when:

1. The Transfer counter is zero, (both block count and physical count) for this pipeline load.
2. No disk errors during this pipeline load
3. An End of Sector Flag is pending for this pipeline load.
4. If FMODE is set, there are no pending ECC errors.

DBSY = Disk Busy Interrupt

This bit is set when the DMA pipeline move from a BUSY to IDLE condition.

On a buffer read, this occurs when:

1. The Transfer counter is zero (both block count and physical count) for this pipeline load.
2. An End of Sector Flag is pending for this pipeline load.
3. No buffer parity errors occurred during this pipeline load.

On a buffer write, this occurs when:

1. The Transfer counter is zero, (both block count and physical count) for this pipeline load.
2. No disk errors during this pipeline load.
3. An End of Sector Flag is pending for this pipeline load.
4. If FMODE is set, there are no pending ECC errors.

4.5.9 Host Buffer Interrupt Mask

HMSK Register address = 94							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPEN	HBP EN	HVVB EN	UPP EN			HVBS YEN	HBSY EN

The interrupt mask bits permit the internal interrupt flag to be sent to the summary register and then to the appropriate Interrupt output pin, INT1 or INT2. Setting or resetting the mask bits does not clear the interrupt flags. For more details on system operations of these interrupts refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

HPEN = Host Bus Parity Error Mask

HBPEN = Host Buffer Parity Error Mask

HVVBEN = Very Very Busy Error Mask

UPPEN = Microprocessor Parity Error Mask

HVBSYEN = Host Very Busy Interrupt Mask

HBSYEN = Host Busy Interrupt Mask

4.5.10 Disk Buffer Interrupt Mask

DBMSK Register address = 96							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DBCC EN	DBP EN	DVVB EN	DOVU NEN	DDVB SYEN	DDBS YEN	DVBS YEN	DBSY EN

The interrupt mask bits permit the internal interrupt flag to be sent to the summary register and then to the appropriate Interrupt output pin, INT1 or INT2. Setting or resetting the mask bits does not clear the interrupt flags. For more details on system operations of these interrupts refer to Section 5.7.3, Disk Interrupt Structure, on page 152.

DBCCEN = Disk Block Count Compare Mask

DBPEN = Data Buffer parity Error Mask

DVVBEN = Very Very Busy Error Mask

DOVUNEN = Disk Over/Underrun Error Mask

DDVBSYEN = Disk Delayed Very Busy Mask

DDBSYEN = Disk Delayed Busy Mask

DVBSYEN = Disk Very Busy Mask

DBSYEN = Disk Busy Mask

4.5.11 Host Buffer Access Control

BUFCTLH Register address = 98							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HDIAG SEL	HSTR ST			HDDIR			HBUF EN

These bits configure the Host DMA pipeline. These bits **must not** change when the DMA pipeline is active.For a system perspective refer to section 5.7.3, Disk Interrupt Structure, on page 152.

HDIAGSEL = Host Diagnostic Select

This bit is set when the Block counter is executing a special diagnostic mode. Refer to Section 4.5.14, Host Block Count, on page 60.

HSTRST = Host DMA Soft Reset

When this bit is set the Host DMA control logic and status is reset. The Host DMA control logic remains reset until this bit is reset. Refer to Section 5.9.6, Disk Manager Soft Reset Operations, on page 165.

HDIR = DMA Buffer Access Direction

When this bit is set the data transfer is to the buffer. When reset, the data transfer is from the buffer.

HBUFEN = Buff Count Enable

When this bit is set the common Buffer Counter decrements with every contiguous "good" block transferred to/from the buffer.

4.5.12 Host Memory Segment Selection

MEMSEGH Register address = 9A							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
			HSEG 4	HSEG 3	HSEG 2	HSEG 1	HSEG 0

These bits are typically loaded with each pipeline load. The pipeline reuses this value if this value is

not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

HSEG[4:0] = Memory Segment Select (PIPELINE VARIABLE)

These bits define the memory segment is to be accessed in the buffer during a host transfer. The buffer memory can have a maximum of 32 segments. The absolute memory address is calculated based upon a) the Relative Address, b) the segment size, and c) the selected Memory Segment.

Absolute Address = ((HSEG[4:0]) * SEGSIZE) + Relative Address

4.5.13 Host Relative Segment Address

RADHH Register address = 9C							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	HA22	HA21	HA20	HA19	HA18	HA17	HA16

RADMH Register address = 9E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HA15	HA14	HA13	HA12	HA11	HA10	HA9	HA8

RADLH Register address = A0							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HA7	HA6	HA5	HA4	HA3	HA2	HA1	HA0

These address bits are typically loaded with each pipeline load. The pipeline continues from the last absolute address if this value is not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

HA[22:0] = Relative Segment Address (Pipeline Variable)

The three above mentioned registers are loaded with an address which is related to the beginning of the active data segment. The least significant address, HA00, is ignored due to the word wide buffer structure.

Valid Address range = 0 - (Segment Size - 1).

4.5.14 Host Block Count

BCNTH Register address = A2							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HBC7	HBC6	HBC5	HBC4	HBC3	HBC2	HBC1	HBC0

These count bits are typically loaded with each pipeline load. The pipeline reuses this value if this value is not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

HBC[7:0] = Block Count (Pipeline Variable)

The Logical Block Count defines the quantity of data which is to be transferred. Two counters are readable via this address location. When HDIAGSEL, bit 7 of the BUFCTLH register, is set the internal block counter is read. When HDIAGSEL, bit 7 of the BUFCTLH register, is reset the external block counter is read. Normally, HDIAGSEL is reset. During microprocessor read, this register reflects the last count which was captured by issuing a HCAP from the BFCTL register. Refer to Section 4.5.29, Buff Count Capture Control, on page 65.

4.5.15 Host Start/Stop Control

HSTSS Register address = A4 (Write Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				HDIAG LD	DIAG LD	H STOP	H STRT

For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

HDIAGLD = Internal Block Count Diagnostic Load

When this bit is set the internal block counter is loaded with the uP loaded block count, BCNTH. This counter is readable via the BCNTH register when HDIAGSEL, bit 7 of the BUFCTLH register is set.

DIAGLD = Relative Address Diagnostic load

When this bit is set the Relative Address, all three bytes, is moved from the microprocessor holding register to the Address Counter. This is only used as a counter diagnostic.

HSTOP = Stop Host Buffer Request

When this bit is set the Host DMA operation is aborted. The DMA pipeline goes to the IDLE state. This bit must be reset to release the DMA pipeline for another DMA operation.

HSTRT = Execute Host Buffer Request

When this bit is set the Host DMA operation begins. The Block Count, Segment select, and relative address are translated to absolute address and transfer count. The DMA pipeline moves up a state, IDLE to BUSY, or BUSY to VERY BUSY depending upon the present pipeline state.

4.5.16 Host Buff Count Capture

HBUFFH Register address = A6							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DIFF	BCH14	BCH13	BCH12	BCH11	BCH10	BCH9	BCH8

HBUFFL Register address = A8							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BCH7	BCH6	BCH5	BCH4	BCH3	BCH2	BCH1	BCH0

DIFF = Difference Flag

Refer to section 4.5.23, Disk Buff Count Capture, on page 63.

BCH[14:0] = Host Buff Capture

These bits reflect the last Buff Count value. Refer to Section 4.5.23, Disk Buff Count Capture, on page 63. On microprocessor write operations to the High byte, HBUFFH, this count value is loaded into the internal BUFF counter. Refer to Section 4.5.29, Buff Count Capture Control, on page 65.

4.5.17 Disk Buffer Access Control

BUFCTLD Register address = AA							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
VW MODE	SMEN		NO DAT	DDIR		WR SAM	DBUF EN

These bits configure the Host DMA pipeline. These bits **must not** change when the DMA pipeline is active.

VWMODE

When this bit is set, a pipeline transfer should not occur if an uncorrectable ECC error occurs on the second to last sector of a pipeline boundary.

SMEN = Skip Mask Enable

When this bit is set, the disk DMA control only transfer data to/from the buffer when a bit is set in the Skip mask field. The Disk Block Count is limited to a maximum of 16 blocks per pipeline load when this feature is enabled. Refer to Section 5.6.10, Disk DMA Operation - Skip Mask Mode, on page 136 for more details.

NODAT = No Buffer Data Transfers

When this bit is set there are no transfers of data from the disk FIFO to/from the Buffer. This bit is primarily used when the WCS is performing ECC verification. Refer to Section 5.6.12, Disk DMA Operation - Disk Verify Mode, on page 138.

DDIR = DMA Buffer Access Direction

When this bit is set the data transfer is to the buffer. When reset, data transfer is from the buffer.

WRSAM = Write Same Enable

When this bit is set, the disk buffer manager operates in the Write Same mode. Refer to Section 5.6.11, Disk DMA Operation - Write Same Mode, on page 138 for more details.

DBUFEN = Buff Count Enable

When this bit is set the common Buffer Counter *increments* with every disk block transferred

to/from the buffer.

4.5.18 Disk Memory Segment Selection

MEMSED Register address = AC							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
			DSEG 4	DSEG 3	DSEG 2	DSEG 1	DSEG 0

These bits are typically loaded with each pipeline load. The pipeline reuses this value if this value is not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

DSEG[4:0] = Memory Segment Select (Pipeline Variable)

These bits define the memory segment is to be accessed in the buffer during a disk transfer. The buffer memory can have a maximum of 32 segments. The absolute memory address is calculated based upon a) the Relative Address, b) the segment size, and c) the selected Memory Segment.

Absolute Address = ((SEG[4:0]) * SEGSIZE) + Relative Address

4.5.19 Disk Relative Segment Address

RADHD Register address = AE							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DA22	DA21	DA20	DA19	DA18	DA17	DA16

RADMD Register address = B0							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

RADLD Register address = B2							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

These address bits are typically loaded with each pipeline load. The pipeline continues from the last absolute address if this value is not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

DA[22:0] = Relative Segment Address (Pipeline Variable)

The three above mentioned registers are loaded with an address which is related to the beginning of the active data segment.

Valid Address range = 0 - (Segment Size - 1).

4.5.20 Disk Block Count

BCNTD Register address = B4							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DBC7	DBC6	DBC5	DBC4	DBC3	DBC2	DBC1	

These count bits are typically loaded with each pipeline load. The pipeline reuses this value if this value is not reloaded. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

DBC[7:0] = Block Count (Pipeline Variable)

The Block Count defines the number of data to be transferred during a disk DMA transfer. During a microprocessor read, reflect the data in the block count capture register, which was captured by issuing a DCAP request from the BFCTL register.

4.5.21 Skip Mask

SKPMSKM Register address = B6							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SGM15	SGM14	SGM13	SGM12	SGM11	SGM10	SGM9	SGM8

SKPMSKL Register address = B8							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SGM7	SGM6	SGM5	SGM4	SGM3	SGM2	SGM1	SGM0

SGM[15:0] = DMA transfer mask (Pipeline Variable)

The Disk Write Same and Skip Mask modes use these bits. For details refer to Section 5.6.10, Disk DMA Operation - Skip Mask Mode, on page 136 and Section 5.6.11, Disk DMA Operation - Write Same Mode, on page 138.

4.5.22 Disk Start/Stop Control

DSS Register address = BA (Write Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
					DIAG LD	D STOP	DST RT

These bits initiate or abort a Buffer DMA operation. For a system perspective refer to section 5.6, DATA PATH CONTROL: BUFFER INTERFACE, on page 127.

DIAGLD = Relative Address Diagnostic Load

When this bit is set the Relative Address, all three bytes, are moved from the microprocessor holding register to the Address Counter. This is only used as a counter diagnostic. The microprocessor must reset this bit. Normal data transfers require this bit to be reset.

DSTOP = Stop Disk Buffer Request

When this bit is set the Disk DMA operation is aborted. The DMA pipeline goes to the IDLE state. This bit must be reset to release the DMA pipeline for another DMA operation. A SRST to the disk is recommended before starting a new DMA transfer.

DSTRT = Execute Disk Buffer Request

When this bit is set the Disk DMA operation begins. The Block Count, Segment select, and relative address are translated to absolute address and transfer count. The DMA pipeline moves up a state, IDLE to BUSY, or BUSY to VERY BUSY depending upon the present pipeline state.

4.5.23 Disk Buff Count Capture

DBUFFH Register address = BC (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DIFF	BCD14	BCD13	BCD12	BCD11	BCD10	BCD9	BCD8

DBUFFL Register address = BE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BCD7	BCD6	BCD5	BCD4	BCD3	BCD2	BCD1	BCD0

DIFF = Difference Flag

When this bit is zero no Buffer counter change request is pending.When this bit is active the Buffer counter has a pending change request. The pending change request is active when the DMA pipeline transitions from VERY BUSY to BUSY and an ECC correction is pending. This bit is inactive when the ECC correction has completed successfully. This bit is reset when SRST is set.

BCD[14:0] = Disk Buff Capture

These bits reflect the last Buff Count value which was captured by issuing a DCAP request from the BFCTL register. Refer to Section 4.5.23, Disk Buff Count Capture, on page 63.

4.5.24 Buffer DMA Status

BSTAT Register address = C0 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	HBP ER	DBP ER	PPAR ER	DV BSY	DBSY	HV BSY	HBSY

The following status bits reflect the present active condition of the Disk and Host DMA pipelines. This status is subject to change at any time.

HBPER = Host Buffer Parity Error

A parity error has been detected on the Buffer Memory Bus during a Host DMA buffer read.

DBPER = Disk Buffer Parity Error

A parity error has been detected on the Buffer

Memory Bus during a Disk DMA buffer read or an ECC correction cycle.

PPARER = Processor Parity Error

A parity error has been detected on the Buffer Memory Bus during a microprocessor buffer read.

DVBSY = Disk Very Busy

Disk DMA pipeline is presently in a Very Busy State.

DBSY = Disk Busy

Disk DMA pipeline is presently in a Busy State.

HVBSY = Host Very Busy

Host DMA pipeline is presently in a Very Busy State.

HBSY = Host Busy

Host DMA pipeline is presently in a Busy State.

4.5.25 Active Microprocessor Address

PADH Register address = C2							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	PA22	PA21	PA20	PA19	PA18	PA17	PA16

PADM Register address = C4							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

PADL Register address = C6							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

PA[22:0] = Microprocessor Address

The microprocessor must load the buffer absolute address preceding the first microprocessor buffer access. If autoincrement registers are used, the address increments each time the microprocessor reads or writes the buffer, or else a new address must be written before any buffer access. Refer to Section 4.5.2, Memory Configuration - Secondary, on page 55 and Section 5.6.6, Microprocessor Buffer Access, on page 130.

4.5.26 Microprocessor Autoincrement Access Registers

PBODDA Register address = C8							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UP15	UP14	UP13	UP12	UP11	UO10	UP9	UP8

PBEVENA Register address = CA							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UP7	UP6	UP5	UP4	UP3	UP2	UP1	UP0

Microprocessor accesses to the buffer via this port will invoke the autoincrement feature, refer to Section 5.6.6, Microprocessor Buffer Access, on page 130 for more details.

4.5.27 Microprocessor Buffer Data Latch Registers

PBODD Register address = CC							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UPL7	UPL6	UPL5	UPL4	UPL3	UPL2	UPL1	UPL0

PBEVEN Register address = CE							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UPL7	UPL6	UPL5	UPL4	UPL3	UPL2	UPL1	UPL0

Microprocessor accesses to the buffer via this port will not affect the microprocessor memory address pointer. Refer to Section 5.6.6, Microprocessor Buffer Access, on page 130 for details.

4.5.28 ECC Start Block Address

ECCADH Register address = D0 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	EA22	EA21	EA20	EA19	EA18	EA17	EA16

ECCADM Register address = D2 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA15	EA14	EA13	EA12	EA11	EA10	EA9	EA8

ECCADL Register address = D4 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0

EA[22:0] = ECC Block Start address

This value is the start address for the first uncorrectable data block. This is internally used by the ECC corrector to perform "ECC on-the-fly". This address is valid when a SEQSTP interrupt is sent due to an abort condition.

4.5.29 Buff Count Capture Control

BFCTL Register address = D6 (Write Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				BUF DN	BUF UP	DCAP	HCAP

These bits control the Buff Counter. For system details refer to Section 5.6.13, Disk Block Count, Buff Count, and ID Capture Registers (Read Operation), on page 139.

BUFDN = Buff Count Down Count

When this bit is set, the Buff Count decrements by one count. There is no need to reset this bit. The microprocessor must wait 4 BCLKs after the rising edge of WEB before another Buff count change can occur.

BUFUP = Buff Count Up Count

When this bit is set, the Buff Count increments by one count. There is no need to reset this bit. The microprocessor must wait 4 BCLKs after the rising edge of WEB before another Buff count change can occur.

DCAP = Disk Buff/Block Count Capture

When this bit is set the Disk Difference Flag, Disk Block and Buff Counts are stored in the Disk Buff Count Capture (refer to Section 4.5.23, Disk Buff Count Capture, on page 63) register and the Block Count (refer to Section 4.5.20, Disk Block Count, on page 62). There is no need to reset this bit.

HCAP = Host Buff/Block Count Capture

When this bit is set the Disk Difference Flag, the Host Block and Buff Counts are stored in the host Buff Count Capture registers (refer to Section 4.5.16, Host Buff Count Capture, on page 61) and the Block Count (refer to Section 4.5.14, Host Block Count, on page 60). There is no need to reset this bit.

4.5.30 Disk Block Count Compare

DBCC Register address = D8							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DBCC 7	DBCC 6	DBCC 5	DBCC 4	DBCC 3	DBCC 2	DBCC 1	DBCC 0

DBCC[7:0] = Disk Block Count Compare Value

This Register is cleared on Hard Reset and Disk Soft Reset. The value programmed into this register is synchronously compared with the current Disk block count value. When the two are equal the DBCCINT will be set (bit 7 of the DBINT register). The microprocessor must write a non-zero value to the DBCC to arm operation. Only one interrupt will be generated per value loaded, i.e. one-shot type comparison. To re-arm, another non-zero value must be loaded. Writing a zero to the DBCC will Disarm comparison operation and no interrupts will be generated.

4.6 SCSI BUS REGISTERS

4.6.1 Setup Page Registers

The setup page is usually used once for initialization following a reset condition. The normal page is used during actual SCSI operations. The switching between these two pages is accomplished by using the SETUP bit of the control register that appears on both pages at all times.

4.6.1.1 SCSI Bus Control Register

CTL Register address = 00							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	FRST	RSTO	LD TCL	LD TC	KILL	ABOR T	SET UP

FRST = FIFO RESET

When set, this bit clears the data FIFO. It should only be used in conjunction with the ABORT bit if a previous abort operation has failed to reach completion.

RSTO = Reset the SCSI Bus

The microprocessor sets RSTO to reset the SCSI bus. As long as RSTO is set, all SCSI outputs on the WD61C96A, except the RST output, are disabled. To end the reset condition, the microprocessor must reset this bit. This ensures that the UEI bit is set to correspond to bit 7 of the Unexpected Event Register if the mask is enabled. When the mask is disabled, the pending interrupt will appear later when the mask is enabled. This may cause some undesirable effects. Therefore, the user should issue the reset after enabling the mask and appropriately handling the interrupt before resuming any manual operations.

LDTCL = Load Transfer Counter Last

The microprocessor sets LDTCL to load the transfer counter pipeline with a new transfer count and to indicate that the LAST flag should be set upon successful completion of the corresponding transfer. Setting LDTC and LDTCL simultaneously resets the transfer setup. This is useful for ending a DMA in progress without needing to issue any abort/kill directives.

LDTC = Load Transfer Counter

The microprocessor sets LDTC to load the transfer counter pipeline with a new transfer count. Completion of a transfer with a count loaded using this bit has no effect on the LAST flag. Setting LDTC and LDTCL simultaneously resets the transfer setup.

KILL = Kill Transfer

Setting this bit has the same effects as setting the ABORT bit, but any transfer is halted immediately, i.e. the FIFO is reset instead of flushed. Refer to Section 5. 7.2.1, Response to Abort / Kill (ABORTI), on page 146.

ABORT = Halt Transfer

ABORT is used by the microprocessor to CLEANLY halt any transfer in progress and to subsequently stop the sequencer. Refer to Section 5. 7.2.1, Response to Abort / Kill (ABORTI), on page 146 for details.

SETUP = Setup Pages

The SETUP bit allows the microprocessor to choose between the normal and setup pages. If this bit is zero, the normal page is selected; if this bit is one, the setup page is selected.

4.6.1.2 SCSI Configuration Register

SCNF Register address = 02							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SCLK2	SCLK1	SCLK0	RSTF M	SPUE	SPDE N	SCSIL	LRCC E

SCLK[2:0] = SCSI Clock Divider (Bits 7:5)

The SCLK field specifies the number of input clock cycles that will generate at least a 100 ns period. The following table decodes the possible values:

SCLK			Input Clock (Mhz)
0	1	0	20.00
0	1	1	20.01 - 30.00
1	0	0	30.01 - 40.00
1	0	1	Default - incoming clock divides by 5

For maximum performance, input clocks of 20, 30, or 40Mhz should be used.

RSTFM = RSTF Output Mask

The Reset Follower Mask bit controls whether the RSTF pin mirrors the state of the RSTINT bit in the Interrupt Status register or is held inactive. Setting this bit allows RSTINT to propagate to the RSTF pin.

SPUE = SCSI Pullup Enable

To select between single-ended or differential modes, SPUE/E48 must be properly set. Setting SPUE enables low-strength pullups on the SCSI signals where the following properties apply:

SPUE	E48	Activated Driver Type
When SE = 1, single-ended setup		
0	1	60 mA REQ, ACK; 48 mA Open Drain, all pins
1	1	48 mA Active Negation on SD[0:15], SDP, SDP1; 60 mA on REQ, ACK. All other pins 48 mA Open Drain.
When SE = 0, differential setup		
1	0	6 mA TTL level output driver (only applicable setting for this mode).

SPDEN = Enable Checking for SCSI Parity

Setting this bit enables parity checking on incoming SCSI data. When it is zero, it disables SCSI parity checking during selection and reselection phases.

SCSIL = Low Level SCSI Bus Control

The SCSIL bit, when set, gives the microprocessor direct control over the SCSI bus via the SCSI Low-Level Control registers. It is mainly used for diagnostic/debug purposes. See 4.6.1.12, SCSI Low-Level Control Registers, on page 72.

LRCCE = LRC Checking Enable

The LRC Checking Enable bit when set allows checking of the LRC word appended to each physical block on incoming DMA data. This bit only has effect when the LRC feature is enabled, i.e. LRCGS set to one. Normally, it is enabled for target mode applications, seldom for initiator mode setup. See Section 5. 10.2.1, Programming The SCSI Section For LRC, on page 169 for details.

4.6.1.3 Own ID Register

OWNID Register address = 04							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				OWN ID3	OWN ID2	OWN ID1	OWN ID0

OWNID[3:0] Own ID (Bits 3:0)

This field specifies the SCSI bus ID of the WD61C96A, which is used during the arbitration, selection, and reselection phases.

4.6.1.4 Timeout Register

TIMOUT Register address = 06							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM OUT7	TIM OUT6	TIM OUT5	TIM OUT4	TIM OUT3	TIM OUT2	TIM OUT1	TIM OUT0

TIMOUT[7:0] = Timeout Register

The value in this register specifies, in units of SCLK×32768 clock cycles, the maximum time to wait for the intended initiator or target to respond with BSY during a reselection or selection attempt. A value of zero disables the timeout feature. A value of 153 corresponds to the recommended timeout value of approximately

250 ms. Refer to FIGURE 4-2 on page 68.

4.6.1.5 Sleep Register

SLEEP Register address = 08							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SLEEP 7	SLEEP 6	SLEEP 5	SLEEP 4	SLEEP 3	SLEEP 2	SLEEP 1	SLEEP 0

SLEEP[7:0] = Sleep Register

The value in this register specifies, in units of SCLK×32768 clock cycles, the time to wait after certain conditions are met before the device enters a sleep (low-power) mode. The SCSI section of the WD61C96A loads an internal counter and starts counting down as soon as all of the following conditions are true.

- If MUX = 1:
  - — $\overline{REB}$ and $\overline{CS0}$ are not both asserted.
  - — $\overline{WEB}$ and $\overline{CS0}$ are not both asserted.
- There is no pending data transfer
- The SCSI reset pin (RST) is not asserted.
- The SCSI section of the WD61C96A is not connected on the SCSI bus.
- The SCSI timeout register is not counting.
- The WCS is idle.
- Self-test is not being performed.
- Hardware reset is not being performed.

The SCSI section halts the internal sleep counter and wakes up as soon as any of the above conditions becomes false, or any of the following conditions occurs to the SCSI section:

- the SCSI section is selected.
- the SCSI section is reselected.

NOTES

An interrupt may be pending when the SCSI section goes to sleep. The microprocessor cannot read the value of the sleep counter to see how close the device is to sleep because the counter is reloaded before the counter is read. Also, the state of the external busses is not disturbed when the SCSI section goes to sleep. Tristated outputs remain tristated and active outputs continue driving the values output before going to sleep.

See FIGURE 4-2 on page 68 and the following table.

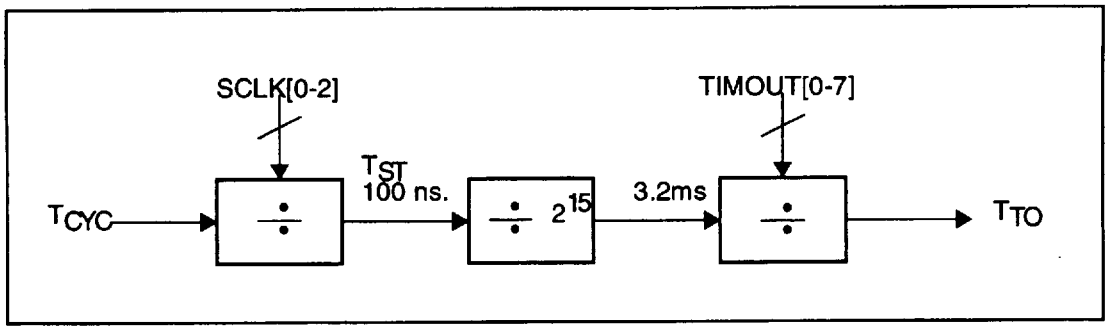

FIGURE 4-2 SLEEP REGISTER DIAGRAM

TIMOUT Value	Timeout Period (assuming T_{ST} = 100ns
0	Timeout is disabled.
1	3.2 ms
77	153 ms
153	255 ms
255	835 ms

TIMOUT is loaded only when starting a (re)selection, and counts down only while the (re)selection is in progress. (The counter halts as soon as connection is completed or timeout occurs).

$T_{TO} = SCLK \bullet T_{CYC} \bullet 32768 \bullet TIMOUT$

The TIMER register contains the time remaining before timeout would have occurred. The SLEEP Timer works in a similar manner.

4.6.1.6 Timer Register

TIMER Register address = 0A (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TIMER 7	TIMER 6	TIMER 5	TIMER 4	TIMER 3	TIMER 2	TIMER 1	TIMER 0

This register allows the microprocessor to view the contents of the selection/reselection timeout counter, which begins counting down from the value specified in the Timeout register from the start of the selection or reselection phase until the destination SCSI device responds by asserting BSY.

TIMER[7 - 0] = Timer Register

4.6.1.7 CDB Size Registers

These registers are used to set up the CDB lengths that are not explicitly defined by the ANSI standard. The normal range of values is 6 to 12 bytes. This allows the WCS to transfer the requested number of command bytes requested by the target without generating an interrupt. If the exact number of programmed bytes is not transferred, an unexpected phase change interrupt will be generated.

CDBSIZ1 Register address = 0C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CDB4 G3	CDB4 G2	CDB4 G1	CDB4 G0	CDB3 G3	CDB3 G2	CDB3 G1	CDB3 G0

CDBSIZ2 Register address = 0E							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CDB7 G3	CDB7 G2	CDB7 G1	CDB7 G0	CDB6 G3	CDB6 G2	CDB6 G1	CDB6 G0

CDB3G[3:0] = CDB Group 3 Size Commands

CDB length for group 3 commands. The actual value of the field is the length less one.

CDB4G[3:0] = CDB Group 4 Size Commands

CDB length for group 4 commands. The actual value of the field is the length less one.

CDB6G[3:0] = CDB Group 6 Size Commands

CDB length for group 6 commands. The actual value of the field is the length less one.

CDB7G[3:0] = CDB Group 7 Size Commands

CDB length for group 7 commands. The actual value of the field is the length less one.

4.6.1.8 IDFLAG Registers

IDFLAG1 Register address = 12							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ID FLAG 15	ID FLAG 14	ID FLAG 13	ID FLAG 12	ID FLAG 11	ID FLAG 10	ID FLAG 9	ID FLAG 8

IDFLAG0 Register address = 10							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ID FLAG 7	ID FLAG 6	ID FLAG 5	ID FLAG 4	ID FLAG 3	ID FLAG 2	ID FLAG 1	ID FLAG 0

The IDFLAG register is used by the WCS to stop or jump on the SCSI device-dependent information. The following table shows what SCSI ID is used as the index:

ID Flag Index	Event
DESTID	SCSI section started due to microprocessor start/step or DMA request.
SRCID	SCSI section started due to 2-bit re(selection).
OWNID	SCSI section started due to 1-bit selection.

IDFLAG[15:8] = ID Flag Register 15 - 8

Flag bits corresponding to SCSI devices eight through fifteen.

IDFLAG[7:0] = ID Flag Register 7 - 0

Flag bits corresponding to SCSI devices zero through seven.

4.6.1.9 DMA Configuration Register

DMACNF Register address = 14							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SWAP	DMA 16	DAC AH	DRQ AH	DPEN	PGEN	MAS TER	BUR ST

Refer to 5.5, DATA PATH CONTROL: HOST INTERFACE, on page 120 for more information about host DMA operations.

Swap High and Low Bytes

The SWAP bit controls whether the high and low bytes on wide DMA transfers are swapped as the word moves between the FIFO and the DMA data bus. Setting this bit causes the swapping to occur. This bit is normally used for odd byte transfers.

DMA16 = DMA Transfer Size 8/16 Bits

The DMA16 bit controls the width of the DMA data bus. Setting this bit selects a sixteen-bit data bus as opposed to an 8-bit wide bus.

DACAH = Active High Polarity for DACK

The DACAH bit determines the polarity of the DACKA and DACK B pins in both master and slave modes. Setting this bit selects active high levels for the DACK signals.

DRQAH = Active High Polarity For DRQ

The DRQAH bit determines the polarity of the DRQA and DRQB pins in both master and slave modes. Setting this bit selects active high levels for the DRQ signals.

DPEN = Enable Parity Checking

Setting DPEN enables parity checking on incoming DMA data.

PGEN = Generate Parity

The Parity Generation bit when set causes the WD61C96A to regenerate parity on received DMA data before writing the data and parity bits to the FIFO. When this bit is reset, received parity, regardless of whether it is correct or not, is simply passed through to the output. The direction of transfer determines whether the SCSI or the host side is being used for parity generation.

MASTER = Master/Slave DMA

The MASTER bit when set selects the internal SCSI manager as the bus master on the DMA interfaces.

BURST = Burst/Single Cycle DMA

The BURST bit, when set, selects a burst protocol for the DMA interface. No DMA REQ/ACK handshake is needed, resulting in a faster DMA transfer.

4.6.1.10 DMA Timing Control Register

DMATIM Register address = 16							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DMA OE	DSRW	DCLK L2	DCLK L1	DCLK L0	DCLK H2	DCLK H1	DCLK H0

Refer to 5.5, DATA PATH CONTROL: HOST INTERFACE, on page 120 for more information about host DMA operations.

DMAOE = DMA Output Enable

The DMAOE bit, when zero, disables the output buffers on all DMA signals. When set to one, the device drives the appropriate signals, depending on the setting of the MASTER bit.

DSRW = DACK Setup Read/Write Strobe

The DSRW bit controls the setup time of DACK to $\overline{DRE}$ or $\overline{DWE}$ when the device acts as a DMA bus master. If the bit is set to zero, the setup time is two clock cycles; otherwise, there are three clock cycles from DACK asserted to $\overline{DRE}$ or $\overline{DWE}$. This bit must be set to one if performing master DMA burst transfer at the highest speed such that DCLKH = DCLKL = 0.

DCLKL[2:0] = DMA Read/Write Low Pulse Width

DCLKL has the same function as DCLKH but for the low pulse width. Together, these two fields set the maximum transfer rate on the DMA interface.

DCLKH[2:0] = DMA Read/Write High Pulse Width

DCLKH specifies the number of clock cycles in addition to the two clock cycle minimum which defines the width of the $\overline{DRE}$ and $\overline{DWE}$ high output pulses. This signal is decoded in this way:

DCLKH	Negation Pulse Width
0	2
-	-
7	9

4.6.1.11 Test 0 Register

TEST0 Register address = 18							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ATNHI	E48	TEST2	TEST1	TEST0	CRST	BIST	BFC

ATNHI = Attention Halt Attention

This bit is used to invoke a special ATN handling. During a data phase transfer (message and command phases are excluded) when connected as a target, ATN input is asserted when the WCS instruction has ENATN enabled. If ATNHI is set, the REQ ACK protocol continues until the initiator stops or transfer completes, but the data is ignored. It completes the protocol only to avoid hanging up the initiator. It works independent from ATNHD, but mixing these two bits are not recommended. See Section 5. 7.2.3, Response to ATNI (Target Mode), on page 149 for more details on ATN input handling.

E48 = Enable 48mA pulldowns

E48 is used to enable SCSI 48mA drivers. For single-ended SCSI only.

TEST[2:0]] = Factory Testing (Bits 5:3)

The TEST field is used for factory testing. The microprocessor should never write a value other than 0 to the field.

Mode	Test
0	Normal Mode
1	Reserved
2	This mode may only be used on a single-ended SCSI bus and when SPUE = 1. When test mode 2 is selected, each SCSI bus pullup is enabled only until the voltage on the SCSI bus rises up to 2.4V, at which point, the pullup turns off.
3	This mode tristates the INT, RSTF, SDOE[15:0], SDPOE, IGS and TGS outputs. For a thorough test, the SCSI section should not be connected on the SCSI bus (IGS, TGS bits are zero), and the DMA port should be disabled (DMAOE = 0), and no register accesses should occur (RDY is tristate).
4	Reserved
5	Reserved
6	This mode forces the SCSI section into the initiator state. It should only be used during factory test.
7	This mode forces the SCSI section into the target state. It should only be used during factory test.

CRST = Chip Software Reset

The CRST bit allows the microprocessor to reset the SCSI device by writing a one to this bit.

BIST = BIST Test Start

The BIST bit, when set, causes a self-test of the Writable Control Store, the FIFO, and the Dual Port Registers.

BFC = BIST Fail Check Test

The BFC bit allows the microprocessor to test the integrity of the WBF, FBF, and DBF bits in the TEST1 register. Setting BFC forces these bits high. The microprocessor should set BFC bit after running the BIST test and setting BIST.

4.6.1.12 SCSI Low-Level Control Registers

SC0 Register address = 1A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SDP1	SDP	RSTI		BSYI	BSYO	SELI	SELO

SC1 Register address = 1C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
IGS	TGS	ATNL	IO	CD	MSG	ACK	REQ

SC2 Register address = 1E							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

SC3 Register address = 20							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8

The SCSI Low-level Control registers gives the microprocessor a high-degree of manual control of the SCSI bus signals.

When low-level registers are read, a zero indicates that the signal on the SCSI bus is not asserted, and a one indicates that the signal on the SCSI bus is asserted. The low-level registers must be debounced by the microprocessor, as the SCSI signals can change at any time.

When the low-level registers are written, writing a zero negates the signal; writing a one asserts the signal. The low-level control registers may be written at any time; however, the values written will not appear on the SCSI bus unless SCSIL = 1.

SDP1 = SCSI Parity SD15 - SD8(Read/Write)

The SDP1 bit, when read, reflects the logical state of the SDP1 signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if I/O is in the appropriate state (depending upon whether the device is connected to the bus as an initiator or as a target).

SDP = SCSI Parity SD0 - SD7 (Read/Write)

The SDP bit, when read, reflects the logical state of the SDP signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if I/O is in the appropriate state (depending upon whether the device is connected to the bus as an initiator or as a target).

RSTI = Current Value on RST Line (Read Only)

The RSTI bit reflects the logical state of the RST signal on the SCSI bus.

BSYI = Current Value on BSY Line (Read Only)

The BSYI bit reflects the logical state of the BSY signal on the SCSI bus.

BSYO = BSY Output Driver (Read/Write)

The BSYO bit is the logical output value of BSY when in low-level mode.

SELI = Current Value on SEL Line (Read Only)

The SELI bit reflects the logical state of the SEL signal on the SCSI bus.

SELO = SEL Output Driver (Read/Write)

The SELO bit is the logical output value of SEL when in low-level mode.

IGS = Initialization Group Select (Read/Write)

The IGS bit, when set, indicates that the device is connected to the SCSI bus as an initiator. Setting this bit enables the initiator group signals ACK and ATN.

TGS = Target Group Select (Read/Write)

The TGS bit, when set, indicates that the device is connected to the SCSI bus as a target. Setting this bit enables the target group signals REQ, MSG, C/D-, and I/O-.

ATNL = ATN Output Driver (Read/Write)

The ATNL bit, when read, reflects the logical state of the ATN signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if IGS is set.

IO = I/O Output Driver (Read/Write)

The IO bit, when read, reflects the logical state of the I/O- signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if TGS is set.

CD = C/D Output Driver (Read/Write)

The CD bit, when read, reflects the logical state of the C/D- signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if TGS is set.

MSG = MSG Output Driver (Read/Write)

The MSG bit, when read, reflects the logical state of the MSG signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if TGS is set.

ACK = ACK Output Driver (Read/Write)

The ACK bit, when read, reflects the logical state of the ACK signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if IGS is set.

REQ = REQ Output Driver (Read/Write)

The REQ bit, when read, reflects the logical state of the REQ signal on the SCSI bus. When written, it controls the value driven onto the SCSI bus, if TGS is set.

SD[7-0] = SCSI Data Signal SD7:SD0 (R/W)

The SD[7:0] bits, when read, reflect the state of the lower byte of the SCSI data bus. When written, they control the value driven onto the SCSI bus, if I/O is in the appropriate state depending upon whether the device is connected to the bus as an initiator or as a target.

SD[15-8] = SCSI Data Signal SD15:SD8 (R/W)

The SD[15:8] bits, when read, reflect the state of the upper byte of the SCSI data bus. When written, they control the value driven onto the

SCSI bus, if I/O is in the appropriate state depending upon whether the device is connected to the bus as an initiator or as a target.

4.6.1.13 Writable Control Store Registers

CSADR Register address = 22							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CS ADR6	CS ADR5	CS ADR4	CS ADR3	CS ADR2	CS ADR1	CS ADR0

CSPRT0 Register address = 24							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WCS7	WCS6	WCS5	WCS4	WCS3	WCS2	WCS1	WCS0

CSPRT1 Register address = 26							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WCS 15	WCS 14	WCS 13	WCS 12	WCS 11	WCS 10	WCS 9	WCS 8

CSPRT2 Register address = 28							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WCS 23	WCS 22	WCS 21	WCS 20	WCS 19	WCS 18	WCS 17	WCS 16

CSPRT3 Register address = 2A							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		WCS 29	WCS 28	WCS 27	WCS 26	WCS 25	WCS 24

CSADR[6:0] = WCS Address for Micro Access

The CSADR field provides the address to the WCS for microprocessor accesses.

WCS[29:0] = Writable Control Store word bits WCS29 - 0

The Writable Control Store registers provide the means for the microprocessor to read and write the WCS. The CSADR register contains the current address to the WCS of the word which the microprocessor can access via the CSPRT registers. The CSADR automatically increments, modulo 127, after each microprocessor access of the CSPRT3 register.

The CSPRT registers are 8-bit data ports through which the microprocessor can access the WCS. Each word of the WCS is divided into four bytes, each byte corresponding to a CSPRT register.

To load the WCS, the user sets the initial starting address (usually 0) in the CSADR register and then provides the 32-bit data word via the CSPORTS 0:3. When the last byte is loaded, the WCS address is automatically incremented. The next 32-bit word can then be loaded by resequencing through CSPORTS 0:3 until the entire WCS has been loaded. The user may subsequently repeat the process to reload a new sequence, if desired, or verify that the WCS is properly loaded.

Reset previews the contents of the WCS, thus a reload of the WCS is not usually required.

The WCS is manually loaded just once following a power-up-reset condition phase or during initialization/setup before manual operations are resumed.

The WCS assembler is available for PC/AT-based systems under DOS. This facilitates the writing/coupling of the desired WCS sequences.

For more details on the WCS, refer to Section 5.2, WRITE CONTROL STORE: SCSI CONTROL.

4.6.1.14 Selection Response Start Address Register

SQSEL Register address = 2C							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SQ SEL6	SQ SEL5	SQ SEL4	SQ SEL3	SQ SEL2	SQ SEL1	SQ SEL0

This register defines the start address of the SRS (Selection Response Sequence). The WCS will begin executing at SQSEL if SELH = 1 and the SCSI section is in the process of being selected.

SQSEL[6:0] = Selection Response Start Address.

SQSEL specifies the starting address of the selection response sequence. When the device is selected and the SELH bit is set, the sequencer executes the instruction sequence starting at this address.

4.6.1.15 Reselection Response Start Address Register

SQRSL Register address = 2E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SQ RSL6	SQ RSL5	SQ RSL4	SQ RSL3	SQ RSL2	SQ RSL1	SQ RSL0

This register defines the start address of the RRS (Reselection Response Sequence). The WCS will execute the RRS sequence automatically as an initiator after it has been successfully reselected and RSELH = 1.

SQRSL[6:0] = Reselection Response Start Address

SQRSL specifies the starting address of the reselection response sequence. When the device is reselected and the RSELH bit is set, the sequencer executes the instruction sequence starting at this address.

4.6.1.16 DMA Response Start Address Register

SQDMA Register address = 30							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SQ DMA6	SQ DMA5	SQ DMA4	SQ DMA3	SQ DMA2	SQ DMA1	SQ DMA0

This register defines the start address of the DMA Response Sequence. The SCSI section will begin executing at this location under certain conditions. See the AUTOR bit in the RESPONSE register.

SQDMA[6:0] = DMA Response Start Address

SQDMA specifies the starting address of the DMA response sequence. When the external DMA device asserts DRQ and AUTOR is set, the sequencer executes the instruction sequence starting at this address.

4.6.1.17 DPR Address Pointer Register

DPRADD Register address = 32 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		DPR ADD5	DPR ADD4	DPR ADD3	DPR ADD2	DPR ADD1	DPR ADD0

The DPR Address Pointer is a read-only register that indicates the location of the DPR being accessed. It is useful for debug purposes.

DPRADD points to the next location to be written in the DPR (in the case of writes to the DPR) or to the next byte to be read out of the DPR (in the case of reads from the DPR). It is incremented after each byte is transferred into or from the DPR. At the start of each data transfer instruction, it is loaded with the value in the DPRADR field of the WCS instruction.

When writing to the SCSI bus from the DPR, data in the DPR will be burst-loaded into FIFO and then the FIFO will transfer the data onto the bus. As a result, DPRADD will appear as if the transfer has completed almost instantaneously. To tell the number of bytes that have actually been transferred on the bus, read the FIFOs register. When the FIFO is empty, all bytes have been transferred.

When reading from the SCSI bus into the DPR, data passes from the SCSI bus into the FIFO and then to the DPR. DPRADD will increment only as bytes are input to the DPR from the FIFO.

DPRADD[5:0] = DPR Address Pointer Register

DPRADD points to the next location to be accessed in the DPR. It is loaded with the value of the DPRADR field of the sequencer instruction at the beginning of a DPR transfer and is incremented after byte is transferred.

4.6.1.18 DPR Transfer Counter Register

DPRTC Register address = 34 (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				DPR TC3	DPR TC2	DPR TC1	DPR TC0

This read-only register contains the number of

bytes remaining to be transferred into/from the DPR. Note that the FIFO is used as a buffer between the DPR and SCSI bus.

In the case of writes to the SCSI bus, the data in the DPR will be burst-loaded into the FIFO, and DPRTC will be 0 almost instantaneously. The actual transfer of data on the SCSI bus will be complete only when the FIFO is empty (see the FIFOS register).

In the case of reads from the SCSI bus, DPRTC will only go to 0 when the DPR has received the last byte of the transfer.

DPRTC[3:0] = DPR Transfer Counter

DPRTC indicates the number of bytes left to be transferred in a DPR transfer instruction.

4.6.1.19 Physical-to-Logical Block Ratio Register

PLR Register address = 36							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
				PLR3	PLR2	PLR1	PLR0

This register is programmed with the number of physical blocks contained within each logical block minus one. Refer to sections 4.3.36, LRC Preset Bytes, on page 50; 4.3.37, ID Capture Address/Data/Control, on page 51; Section 5.10.1, DISK PORT LRC OPERATION, and Section 5.10.2, SCSI LRC OPERATIONfor more information.

PLR[3:0] = Physical Logical Ratio

PLR specifies the number of physical blocks which make up one logical block. The actual value of the field should be this ratio less one. This register is decoded using these values:

PLR Value	Physical/Logical Ratio
0	1
1	2
...	...
15	16

4.6.1.20 Physical Block Size Register

PBSIZ0 Register address = 38							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
PB SIZ7	PB SIZ6	PB SIZ5	PB SIZ4	PB SIZ3	PB SIZ2	PB SIZ1	PB SIZ0

PBSIZ1 Register address = 3A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
				PB SIZ11	PB SIZ10	PB SIZ9	PB SIZ8

The Physical Block Size register specified the number of bytes in one physical block. The microprocessor should program this register with the number of bytes per block less one.

PBSIZ[7:0] = Physical Block Size 7 - 0

PBSIZ[7-0] are the lower eight bits of the physical block size.

PBSIZ[11:8] = Physical Block Size 11 - 8

PBSIZ[11-8] are the upper four bits of the physical block size.

4.6.1.21 PING Register

PING Register address = 3C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
				PING3	PING2	PING1	PING0

PING = PING Register

PING specifies the number of physical blocks to transfer on one DMA port before switching to the other when striping is enabled. The actual value of the field is this number less one as shown in this table.

PING	Number of Blocks Transferred Before Toggle
0	1
1	2
...	...
15	16

4.6.1.22 Data Compare Registers

CMPIX Register address = 3E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
					CMPIX 2	CMPIX 1	CMPIX 0

CMPVAL Register address = 40							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMP VAL7	CMP VAL6	CMP VAL5	CMP VAL4	CMP VAL3	CMP VAL2	CMP VAL1	CMP VAL0

CMPMASK Register address = 42							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMP MSK7	CMP MSK6	CMP MSK5	CMP MSK4	CMP MSK3	CMP MSK2	CMP MSK1	CMP MSK0

The Data Compare registers provide the microprocessor with access to the Data Compare values and Data Compare masks, which are used by the sequencer when evaluating the MASK conditions. The microprocessor should not access these registers when the sequencer is running. However, it must load these registers correctly to correspond to the WCS implemented by the user. This is normally done following the successful load of the desired WCS sequence.

CMPIX[2:0] = Data Compare Index

CMPIX is the index of the data compare value and mask accessible through the Compare Value and Compare Mask registers. The figure below shows this relationship.

CMPVAL[7:0] = Data Compare Value

CMPVAL is the data compare value corresponding to the index CMPIX. In evaluating a MASK condition, the sequencer compares one of these values, as specified by the particular MASK condition, to the DPR data addressed by the DPRADD field of the instruction

CMPMSK[7:0] = Data Compare Mask

CMPMSK is the data compare mask corresponding to the index CMPIX. In evaluating a MASK condition, the sequencer masks the results of the comparison with one of these values, as specified by the particular MASK condition. A one in a bit location requires that the corresponding bits of the DPR data and the compare value be equal for the MASK condition to be met.

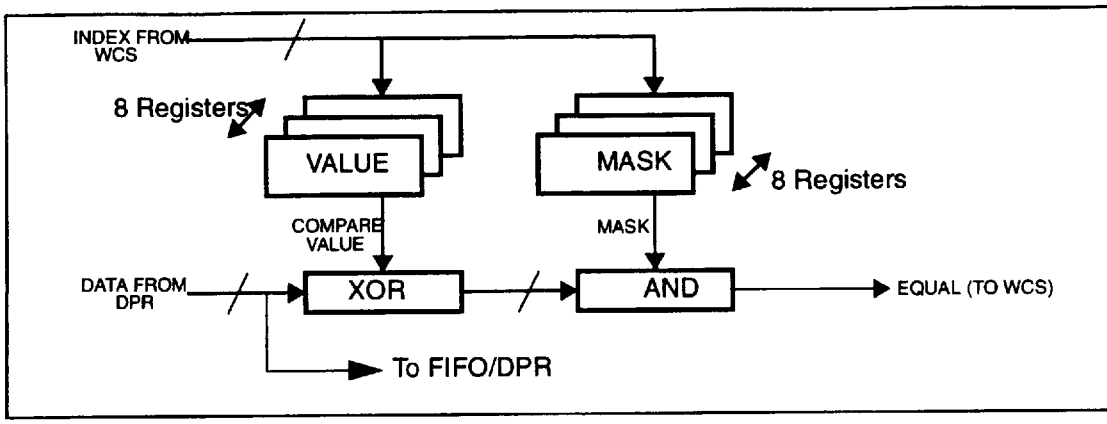

FIGURE 4-3 DATA COMPARISON FLOW DURING DATA TRANSFER

4.6.1.23 BD Bus Register

BBDL Register address = 44 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BBD7	BBD6	BBD5	BBD4	BBD3	BBD2	BBD1	BBD0

BBDH Register address = 46 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BBD15	BBD14	BBD13	BBD12	BBD11	BBD10	BBD9	BBD8

The read-only BD Bus registers give the microprocessor the ability to examine the state of the DMA data bus at any time.

BBD[15:0] is equal to BD[15:0], with only an async. prop delay. As a result, there is no default value after hardware or software reset.

BBD[7:0] = BD Bus Register Low

BBD[7:0] mirror the state of the lower byte of the DMA data bus.

BBD[15-8] = BD Bus Register High

BBD[15-0] mirror the state of the upper byte of the DMA data bus.

4.6.1.24 Version Register

CVER Register address = 48 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		SE	D SENS	CVER 3	CVER 2	CVER 1	CVER 0

The Version Register is read-only.

CVER = Revision Number

Revision number of the device. (Read as 1000b).

DSENS = DSENS Pin Value

DSENS reflects the value of the DSENS pin on the WD61C96A. On the A and D options, this bit always returns a one.

SE = SE Pin Value

SE reflects the value of the SE pin on the WD61C96A. On the A and D options, this bit always returns a one.

SE i/p	DSENS i/p	Effect
0	0	Differential bus with DIFFSENS line shorted to GND (usually caused by single-ended and differential devices connected on a single cable.
0	1	Differential bus. Normal function.
1	x	Single-ended bus. DSENS input should be tied to either VDD or VSS. Normal function.

4.6.1.25 Test 1 Register

TEST1 Register address = 4A (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		DBC	DBF	FBC	FBF	WBC	WBF

The TEST1 register contains the bits which report the results of the Built-In Self Tests (BIST) of the WCS, the FIFO, and the DPR. Table 4-6, BIST RESULTS, lists the interpretation of the bits after the microprocessor starts the BIST; Table 4-7, BIST FLAG CHECK RESULTS, gives the interpretations for the bits after the microprocessor sets the BIST flag check bits in the TEST0 register, following the BIST tests. For successful completion, the register should contain 2A; for the flag check test it should contain 3F.

DBC = DPR BIST Complete Flag

DBF = DPR BIST Flag

FBC = FIFO BIST Complete Flag

FBF = FIFO BIST Flag

WBC = WCS BIST Complete Flag

WBF = WCS BIST Flag

xBF	xBC	Description
0	0	Test is running on block.
0	1	Block successfully completely BIST.
1	x	Block failed BIST.

TABLE 4-6 BIST RESULTS

xBF	xBC	Description
0	0	xBF and xBC are stuck at 0.
0	1	xBF is stuck at 0.
1	x	xBC is stuck at 0.
1	1	xBF and xBC are functioning normally.

TABLE 4-7 BIST FLAG CHECK RESULTS

4.6.1.26 Offset Counter

OFFSET Register address = 4C (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		OFF SET5	OFF SET4	OFF SET3	OFF SET2	OFF SET1	OFF SET0

The read-only Offset Counter indicates the current REQ/ACK offset in bytes. It is only used during data-phase transfers.

OFFSET[5:0] = Offset Counter

OFFSET indicates the current SCSI synchronous offset. The possible values for this register are:

OFFSET	Valid During
0	Asynchronous SCSI Transfer
1... 32	Synchronous SCSI Transfer
> 32	Reserved

4.6.2 Normal Page Registers

This set of registers is used for normal SCSI transfers. An interrupt implies successful task completion or that an exception condition was detected. After handling the appropriate exception condition, the user may resume the WCS from any specified starting address to continue or start another SCSI session.

To start the WCS, the user loads a desired starting address in the Sequence Address Register. This same register is read to find out where an exception has occurred.

For synchronous transfers, the SCSI Pulse Width Control register (18h) must be set properly with the negotiated synchronous rates prior to restarting the WCS. This is usually accomplished via lookup tables that the user maintains.

4.6.2.1 Auxiliary Control Register

CTLA Register address = 02							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BYTEC	PBS	PAS	PPEN	PIO	LRCGS	ATNHD	MRM

BYTEC = Byte Transfer Length

The BYTEC bit controls how the contents of the transfer counter are interpreted. When set, the value in the counter specifies the transfer length in bytes; when reset, the counter specifies the transfer length in terms of logical blocks.

PBS = Port B Set

The PBS bit when set enables the device to respond to DMA requests from the DMA device on port B.

PAS = Port A Set

The PAS bit when set enables the device to respond to DMA requests from the DMA device on port A.

PPEN = Striping Enable

Setting the PPEN bit enables striping.

PIO = Processor Input/Output

The PIO bit when set selects the microprocessor as the data source or destination via the DATA register for non-DPR transfers. When reset, data is routed through the DMA interface. In conjunction with the DBR bit (FIFO status bit 7), this bit is used to implement the PIO mode of data transfer, if desired. When DBR is set, data may be transferred using the Data Register, one byte at a time. For 16-bit transfers, the user must implement external control logic as done for DMA transfers.

LRCGS = LRC Generation and Stripping

Setting the LRCGS bit enables generation and stripping of the LRC word for each physical block.

ATNHD = ATN Halt

The ATNHD bit, when set, causes a target mode data transfer to halt immediately upon detection of the SCSI ATN condition if the ENATN bit of the sequencer instruction is also set.

MRM = Mirror Restore Mode

The MRM bit, when set, enables the mirror-restore mode, where the device connected to DMA port A, acting as a master, may perform DMA transfers to the device connected to DMA port B, acting as a slave.

In mirror-restore mode, DRQA mirrors DRQB, and DACKB mirrors DACKA. All other DMA signal outputs are tristated, and all other DMA signal inputs are ignored.

4.6.2.2 Interrupt Status Register

ISR Register address = 04 (Read/Clear)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
INTO	SREJ	VBUSYI	BUSYI	UEI	STOPU	INTWCS	STOPWCS

The ISR contains the status bits indicating the exception conditions encountered by the SCSI section. The SCSI section will generate an interrupt to the microprocessor if an exception

condition occurs and its associated mask bit for the condition is masked on. The microprocessor clears the interrupt by writing a 1 to the appropriate bit. The SCSI section will assert its interrupt line until all interrupts are cleared by the microprocessor. These bits will be set regardless of the values of the mask bits in ISRM. However, the interrupt is only reflected in the INTO bit if the corresponding masks have been enabled.

Writing a 1 to these bits (except for STOPU and UEI) will clear the corresponding interrupt.

INTO = INT Pin State

The INTO bit reflects the state of the INT pin.

SREJ = Instruction Sequence Rejection

The SREJ bit indicates that the attempt by the microprocessor to start execution of an instruction sequence has been rejected. A reject may occur for the following reasons:

- the sequencer is already running;
- an interrupt is pending that was not cleared;
- a start in response to a selection or reselection overrides the microprocessor start.

VBUSYI = Very Busy to Busy State Status

The VBUSYI interrupt indicates that the Transfer Counter pipeline has transitioned from the very busy state to the busy state. The pipeline may now be loaded with the next segment of the transfer counter. Scatter/gather is implemented using external DMA logic for the host memory address.

BUSYI = Busy to Idle Status

The BUSYI interrupt indicates that the Transfer Counter pipeline has transitioned from the busy state to the idle state. Presumably, no Move Data Transfer is expected.

UEI = Assert Unexpected Event Interrupt

The UEI bit functions as the STOPU bit does but for unexpected events dictated by the SCSI bus.

STOPU = Assert Unexpected Stop Status

The STOPU bit is asserted as long as any of the unmasked bits in the STOPU register are set as dictated by events directly related to the SCSI bus.

INTWCS = WCS Interrupt Condition

The INTWCS bit is set during execution of any instruction having the INT field set just before the STOP/JUMP condition is evaluated.

STOPWCS = WCS Stop Condition

The STOPWCS bit is set at the end of execution of any instruction where the STOP condition was true and no error occurred.

4.6.2.3 Unexpected Stop Interrupt Register

STOPU Register address = 06 (Read/Clear)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		SOE	TCUND	LRCE	PARE	SCSIT	ABORTI

The interrupt bit will be set after the WCS has halted. Writing a 1 to these bits will clear the corresponding interrupt. These bits will be set regardless of the values of the mask bits in STOPUM.

SOE = SCSI Offset Error

The SOE interrupt indicates that the device detected abnormal behavior of the REQ and ACK signals.

TCUND = Transfer Count Underrun

The TCUND interrupt indicates that the sequencer tried to begin a transfer instruction but found the pipeline empty. This interrupt only occurs in target mode.

LRCE = LRC Word Error

The LRCE interrupt indicates that the last physical block transferred had an incorrect LRC word.

PARE = Parity Error

The PARE interrupt indicates that the device detected bad parity in the data received during

a transfer. The direction of transfer determines whether the SCSI or the host side experienced an error.

SCSIT = SCSI Bus Timeout During Selection or Reselection

The SCSIT interrupt indicates that the destination SCSI device did not respond to a selection or reselection attempt before the timeout counter decremented to zero as determined by the value in the Timeout Setup register.

ABORTI = Abort Interrupt

The ABORTI interrupt signals the completion of the microprocessor-issued ABORT or KILL.

4.6.2.4 Unexpected Event Interrupt Register

UEI Register address = 08 (Read/Clear)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
RST INT	UP HAS	UR SEL	U SEL	T COVR	UDISC	ATNI	FIFOE

The interrupt is cleared by writing a 1 to the appropriate bit. These bits will be set regardless of the values of the mask bits in UEIM.

RSTINT = Reset Received on SCSI Bus

The RSTINT interrupt is set when the device detects a valid SCSI reset condition, i.e. the assertion of RST for at least SCLKx4 input clock cycles.

UPHAS = Unexpected SCSI Phase

The UPHAS interrupt indicates that the target has asserted REQ to start an information transfer phase while the sequencer is idle or that the target has requested a phase that does not match the phase specified by the currently executing sequencer instruction.

URSEL = Unexpected Reselection

The URSEL interrupt indicates that another SCSI device has reselected the WD61C96A when the high-level response to reselection was not enabled. If the high level is enabled, then execution starts at the address specified in the SQRSL register.

USEL = Unexpected Selection

The USEL interrupt indicates that another SCSI device has selected the WD61C96A when the high-level response to selection was not enabled. If the high level is enabled, then execution starts at the address specified in the SQSEL register.

TCOVR = TC Pipeline Overrun

The TCOVR interrupt is set if the microprocessor attempts to load another value into the transfer counter pipeline when the pipeline is already in the very-busy state.

UDISC = Unexpected SCSI Bus Disconnect

The UDISC interrupt is set when the target disconnects while the sequencer is idle or is executing but not expecting a disconnect to occur.

ATNI = ATN Asserted

The ATNI interrupt signals the detection of the SCSI attention condition.

FIFOE = FIFO Overflow/Underflow

The FIFOE interrupt indicates that the FIFO control logic has detected an overrun or underrun condition so that the data transfer may have been corrupted.

4.6.2.5 Interrupt Mask Register

ISRM Register address = 0A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	SREJ M	VBUS YIM	BUSY IM	UEIM	STOP UM	INT WCSM	STOP WCSM

STOPUM Register address = 0C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		SOEM	TCUN DM	LRC EM	PAR EM	SCS ITM	ABOR TM

UEIM Register address = 0E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RST INTM	UPHA SM	UR SELM	U SELM	TCOV RM	U DISCM	ATNIM	FIFO EM

Each interrupt register has an associated mask register. Each bit of the mask registers corresponds to one in the interrupt status registers. When set, these bits allow the associated interrupt bits to propagate out and set the INT2 pin. If a mask bit is not set, the status register bit will still indicate if an interrupt condition has occurred, but the set status bit will not cause the INT2 pin to assert in order to interrupt the processor. However, when the mask is enabled and the bit has not been acknowledged (or cleared), the corresponding bit is set.

The bits in the ISRM register control masking of the interrupts reported in the Interrupt Status register.

The bits in the STOPUM register control masking of the interrupts reported in the Unexpected Stop Interrupt register.

The bits in the UEIM register control masking of the interrupts reported in the Unexpected Event Interrupt register.

4.6.2.6 Response Register

RESPONSE Register address = 10							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	ALLRR	AUTO D	AUTO R	R SELH	RE SELL	SELH	SELL

This register is usually used to enable the high-level or low-level responses before starting the WCS.

ALLRR = All Response to Reselection

If ALLRR = 0, bits SELL and RSELL are cleared by:

- any response to (re)selection when the SCSI section asserts BSY
- RSTINT and UDISC interrupts

If ALLRR = 1, the low-level response bits, SELL and RSELL, are also cleared when the high-level response bits SELH and RSELH are cleared.

AUTOD = Pause Data Transfer

The AUTOD bit, when set, causes the current or pending non-DPR transfer to pause at a logical block boundary. It is used in target mode to halt transfers on logical block boundaries. It is reserved in initiator mode. The SCSI section must be a DMA bus master.

Normally, the transfer portion of a sequencer instruction ends when the pipeline transitions from BUSY to IDLE. AUTOD is used to pause in the middle of a transfer so that the WCS can continue execution of the instruction. The microprocessor sets AUTOD to tell the SCSI section to halt the transfer on the SCSI bus at the next logical block boundary. After the SCSI section has halted the transfer on the SCSI bus (finishing the data transfer), it will clear AUTOD and finish executing the rest of the current WCS instruction.

Writing data onto the SCSI bus: The microprocessor sets AUTO to tell the SCSI section to halt the data transfer on the DMA port at the next logical block boundary or to stop immediately if currently on a logical block boundary. The data remaining in the FIFO is transmitted onto the SCSI bus. The WCS completes the current instruction and then begins the next WCS instruction.

Reading data from the SCSI bus: The microprocessor sets AUTOD to tell the SCSI section to halt the data transfer on the SCSI bus at the next logical block boundary. After the FIFO has been emptied (thus halting the transfer on the DMA bus on a logical block boundary), the WCS continues executing the instruction. If the SCSI bus is on a logical block boundary when AUTOD is set, the SCSI section will transfer one more logical block and then halt the transfer.

AUTOR = Enable Automatic Reconnect

The AUTOR bit when set enables the

sequencer to begin execution of the instruction sequence starting at the address in the SQDMA register upon a valid DMA request.

RSELH = Enable High-Level Response to Reselection

The RSELH bit when set enables the sequencer to begin execution at the address specified in the SQRSL register upon reselection by another SCSI device.

RSELL = Enable Low-Level Response to Reselection

The RSELL bit when set enables the device to respond to reselection by another SCSI device. An unexpected disconnect, a SCSI reset, or a connection to the SCSI bus will clear this bit.

SELH = Enable High-Level Response to Selection

The SELH bit when set enables the sequencer to begin execution at the address specified in the SQSEL register upon selection by another SCSI device.

SELL = Enable Low-Level Response to Selection

The SELL bit when set enables the device to respond to selection by another SCSI device. An unexpected disconnect, a SCSI reset, or a connection to the SCSI bus will clear this bit.

4.6.2.7 Sequencer Interrupt Address Register

SQINT Register address = 12 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	SQ INT6	SQ INT5	SQ INT4	SQ INT3	SQ INT2	SQ INT1	SQ INT0

SQINT[6:0] = Sequencer Interrupt Address

The SQINT field contains the address of the last sequencer instruction executed which has set the INT bit in the Interrupt Status register.

4.6.2.8 Sequencer Address Register

SQADR Register address = 14							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
STEP	SQ ADR6	SQ ADR5	SQ ADR4	SQ ADR3	SQ ADR2	SQ ADR1	SQ ADR0

STEP = Single-Step Mode Select

The STEP bit causes the sequencer to halt after executing one instruction in response to a write to this register with this bit set to one. The SQADR is advanced to the next address.

SQADR[6:0] = Current Sequencer Address

The SQADR field when read contains the address of the instruction currently executing if the sequencer is active or of the last instruction executed if the sequencer is idle. When the microprocessor writes the register, this field specifies the address at which the sequencer should begin execution.

WCS State	Interrupts Set*	Micro Writes	Effect
Idle	0	0aaaaaaa	Normal execution: WCS begins execution at location aaaaaaa.
Idle	0	1aaaaaaa	Single-step mode: WCS executes instruction at location aaaaaaa and then halts after updating the SQADR to the next location it would have gone to if it were not in single-step mode.
Idle	1	xxxxxxxx	SQADR is not modified. The WCS does not start. SREJ interrupt is generated. The WCS remains idle.
Run-ning	x	xaaaaaaa	SQADR is not modified; the WCS continues execution; SREJ interrupt generated. The WCS continues execution.

TABLE 4-8 SEQUENCER ADDRESS REGISTER MICRO WRITES

** If any of the 'raw' (pre-masking) bits in the ISR register are asserted, the microprocessor writes to the SQADR are blocked.*

4.6.2.9 SCSI Transfer Control Register

STC Register address = 16							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
WSCSI		OFF5	OFF4	OFF3	OFF2	OFF1	OFF0

WSCSI = Wide SCSI Transfer

The WSCSI bit specifies the data phase bus width. Setting this bit to one indicates a wide (i.e. 16-bit) data bus; setting this bit to zero selects an eight-bit data bus. Prior to setting this bit, the user must successfully send the WIDE SCSI bus message.

OFF[5:0] = Synchronous Transfer Offset

The OFF field specifies the maximum synchronous SCSI offset allowed in bytes. A zero value indicates that data should be transferred using the asynchronous transfer protocol. The non-zero value used is the negotiated offset with a specific SCSI device using the message protocol as described by the ANSI standard.

4.6.2.10 SCSI Pulse Width Register

SPW Register address = 18							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	SCLKN2	SCLKN1	SCLKN0		SCLKA2	SCLKA1	SCLKA0

SCLKN[2:0] = SCSI Synchronous Clock Negation Pulse Width

The SCLKA field specifies in clock cycles the minimum output pulse width of REQ and ACK negated for synchronous transfers.

InputCLK Mhz	SLCKN(min)	SLCKA(min)	Tn/Tsu ns	Ta/Th ns	MXfr/s
Slow Synchronous Transfer (≥200 ns)					
20	0	1	100	150	4.0
40	2	2	100	100	5.0
Fast Synchronous Transfer (<200 ns)					
40	0	0	50	50	10.0

TABLE 4-9 SYNCHRONOUS CLOCK RATES

Where:

Tn = output clock negated pulse width
Ta = output clock asserted pulse width
Tsu = data setup time to output clock assertion edge
Th = data hold time after output clock assertion.

SCLKA[2:0] = SCSI Synchronous Clock Assertion Pulse Width

The SCLKA field specifies in clock cycles the minimum output pulse width of REQ and ACK asserted for synchronous transfer.

The following two equations specify the relationship between the clock period (tsys) and the asserted/negated pulse widths of the clock and the desired sync periods.

*Sync Period = (SCLKN +2) x tsys + (SCLKA + Z) *tsys*

SCLKN = SCLKA or SCLKN = SCLKA - 1

This assumes an input clock of 40 MHz and tsys = 25 ns. For example:

SCLKN	SCLKA	SYNC PERIOD
0	0	100 ns
0	1	125 ns
1	1	150 ns
1	2	175 ns
2	2	200 ns

Using the negotiated synchronization periods, the proper values of SCLKN and SCLKA may be programmed by the user.

4.6.2.11 Destination ID Register

DESTID Register address = 1A							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				DSTID 3	DSTID 2	DSTID 1	DSTID 0

DSTID[3:0] = Destination ID

The DSTID field identifies the SCSI device to be selected or reselected.

4.6.2.12 Source ID Register

SRCID Register address = 1C (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
			SIV	SRCID 3	SRCID 2	SRCID 1	SRCID 0

SIV = Source ID Valid

The Source ID Valid bit indicates that the most recent SCSI device to select or reselect the WD61C96A asserted its own ID during the selection or reselection phase.

SRCID[3:0] = Source ID

The SRCID field identifies the SCSI device which last selected or reselected the WD61C96A. This field is valid only when the SIV bit is set.

4.6.2.13 Flag Register

FLAG Register address = 1E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F7	F6	F5	F4	F3	F2	F1	F0

F[7:0] = Flag Bits 7:0

The Flag Register contains flag bits that can be used by the WCS. The microprocessor programs F0 through F7 to control the WCS execution flow. These flags are used by the control field in the WCS instruction for jumping or halting. A typical application for these flags is to control link commands, sending or receiving extended messages or any user desired control effect. The user sets or resets these bits corresponding to the WCS sequence written to test the state of these bits.

4.6.2.14 Transfer Count Registers

TC[0-7] Register address = 20							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

TCM Register address = 22							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8

TCH Register address = 24							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16

These registers actually consist of a twenty-four bit pipeline register in front of the twenty-four bit transfer counter. Writing these locations loads values into the pipeline register which serve as the initialization value for the transfer counter. Reading these locations returns the contents of the transfer counter.

Programming the transfer count involves two steps. First, the microprocessor writes the transfer count into the TC register. Writing into the lower byte clears the higher registers; for example, if the microprocessor writes into TCl[7:0], TC[23:8] will be cleared; if the microprocessor writes into TCM[15:8], only TCH[23:16] will be cleared. In the second step, the microprocessor sets LDTC or LDTCL.

The transfer counter of the SCSI section has a two-stage pipeline. The microprocessor can write another transfer count into the pipeline while the SCSI section is working on another one as flagged by the VBUSY1 bit. Refer to the SR Register to ascertain the status of the TC pipeline.

TCL[7:0] = Transfer Count Register, Low Byte

These bits correspond to bits 7 through 0 of the transfer counter and the pipeline register. Writing to this byte clears the upper two bytes of the pipeline register.

TCM[15:8] = Transfer Count Register, Middle Byte

These bits correspond to bits 8 through15 of the transfer counter and the pipeline register. Writing to this byte clears the upper byte of the pipeline register.

TCH[23:16] = Transfer Count Register, High Byte

These bits correspond to bits16 through 23 of the transfer counter and the pipeline register.

4.6.2.15 Data FIFO Register

DATA FIFO Register address = 26							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

This register is used by the microprocessor to access the FIFO. To access the FIFO, the DMA controller must first be put in PIO mode and the WCS must be running. The FIFOS register may be read to determine the number of bytes in the FIFO.

DATA[7:0] = Data Access Port

Data byte to or from the FIFO.

4.6.2.16 Status Register

SR Register address = 28 (Read Only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
					AC TIVE	V BUSY	BUSY

ACTIVE = Active Status

The ACTIVE bit indicates that the sequencer is running.

VBUSY = Very Busy Status

The VBUSY bit indicates that there are two values in the transfer counter pipeline. No more transfer counter values can be loaded.

BUSY = Busy Status

The BUSY bit indicates that there is at least one value in the transfer counter pipeline. A second value may be loaded, if desired.

4.6.2.17 FIFO Status Register

FIFOS Register address = 2A (Read Only)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DBR	SODD	DODD	FCNT4	FCNT3	FCNT2	FCNT1	FCNT0

DBR = Data Buffer Ready

In PIO mode the Data Buffer Ready bit indicates that the microprocessor may access the DATA register.

SODD = SCSI Input/Output Data Latch Count

The SODD bit when set indicates that the SCSI input or output data latch contains one byte of data.

DODD = DMA Input/Output Data Latch Count

The DODD bit when set indicates that the DMA input or output data latch contains one byte of data.

FCNT[4:0] = FIFO Word Count

The FCNT field indicates the number of words of data in the FIFO. It does not include the staging registers used to assemble or disassemble words moving to and from the FIFO.

4.6.2.18 Physical Block Residue Register

PBR Register address = 2C							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				PBR3	PBR2	PBR1	PBR0

PBR[3:0] = Physical Block Residue

This register contains the number of whole physical blocks remaining to be transferred within the current logical block. Each time BR reaches zero, PBR is decremented. When PBR reaches zero, the main transfer counter is decremented and PBR is reloaded with the value in the PLR register. At the beginning of each data transfer instruction, if the microprocessor has not written to the PBR register since the last transfer stopped, the PBR is loaded with the value in the PLR register. If the microprocessor has written to the PBR register since the last transfer stopped, the current value in the PBR will be used for the transfer. This permits restarting a transfer in the middle of a logical block.

4.6.2.19 Byte Residue Register

BR0 Register address = 2E							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

BR1 Register address = 30							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				BR11	BR10	BR9	BR8

BR[11:0] = Byte Residue

BR contains the number of bytes plus one remaining to be transferred in the current physical block.

At the start of each WCS data transfer instruction, if the microprocessor has not written to either BR0 or BR1 since the last transfer stopped, the BR register is loaded with the value in the PBSIZ register. If the microprocessor has written to either BR0 or BR1, the current value in the BR register is used.

Each time the BR register reaches 0, the value in the PBSIZ register is loaded into the BR register and the PBR register is decremented.

4.6.2.20 Ping Residue Register

PINGR Register address = 32							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				PINGR 3	PINGR 2	PINGR 1	PINGR 0

PINGR[3:0] = Ping Residue

The PINGR register contains the number of physical blocks remaining to be transferred into or from the currently selected DMA device. PINGR is reloaded with the value in PING:

- Each time the last byte in a physical block is transferred to PINGR (previously set to zero).
- At the start of each data-transfer instruction, if the microprocessor has not written to Pinger since the last transfer stopped.
- After the last byte of a physical block has been transferred on the DMA bus, PINGR is decremented by 1.

4.6.2.21 LRC Residue Register

LRC0 Register address = 34							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
LRC7	LRC6	LRC5	LRC4	LRC3	LRC2	LRC1	LRC0

LRCR1 Register address = 36							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
LRC15	LRC14	LRC13	LRC12	LRC11	LRC10	LRC9	LRC8

LRC[15:0] = LRC Residue

This register is programmed with the LRC initialization value before a transfer and contains the LRC residue at the end of the transfer.

On byte-wide transfers, the LRC0 register will be used for even bytes and LRC1 will be used for odd bytes.

At the beginning of each transfer, the LRC residue will be initialized to 'AAAA' unless the microprocessor has written to the LRC residue since the last transfer stopped.

4.6.2.22 Odd Byte Register

ODDR Register address = 38							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ODDR 7	ODDR 6	ODDR 5	ODDR 4	ODDR 3	ODDR 2	ODDR 1	ODDR 0

ODDR[7:0] = Odd Byte Reconnect

This register is used when performing odd-byte reconnect.

4.6.2.23 Dual Port Registers

DPRx Register address = 40 - 7E (Even addresses only)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DPRx7	DPRx6	DPRx5	DPRx4	DPRx3	DPRx2	DPRx1	DPRx0

DPRx[7:0]

The Dual Port Register (DPR) can be used to store the special SCSI information such as status, message, and command description blocks. This is the only area that serves as the source/destination of information as directed by the WCS instruction word. The DPR is accessible by the microprocessor at any time, even if the SCSI section is executing an operation. Through the dual port architecture, the microprocessor can access the DPR while the SCSI section, for example, is performing a transfer to or from the DPR. The SCSI section has 32 bytes in the DPR.

5.0 THEORY OF OPERATIONS

This section discusses the following operations and functions:

- Write Control Store (SCSI Control, Disk Control)
- Data Path Control (SCSI Interface, Host Interface, Buffer Interface, Microprocessor Interface, Disk Interface)
- Data Integrity Features (ECC, Disk Port LRC Operation, SCSI LRC Operation)
- Disk Interface Wrap Control
- Test Modes

5.1 GENERAL OVERVIEW

The WD61C96A is a single chip, high-performance peripheral cache manager, SCSI manager, and disk controller. Refer to the block diagram in Section 2.0, ARCHITECTURE OVERVIEW.

Although the WD61C96A is a single device, it has the flexibility of programmable functions, such as programmable write control stores for both the SCSI protocol and disk controller, as well as programmable options and configurations for the greatest flexibility to meet individual needs.

The WD61C96A combines all of the functions of Western Digital's WD61C40 and WD33C96 devices, including task files of microprocessor accessible registers, 16-bit buffer interface, 8-bit disk interface, 16-bit DMA interfaces, and a 16-bit wide SCSI interface.

This single device controls both data transfers between the SCSI port and the disk port as well as data transfers between the SCSI bus and the local data buffer. The WD61C96A can be either an initiator or a target and has a selectable 8-bit or 16-bit programmable data path. Included with the WD61C96A are single-ended, 48/60 mA drivers that meet the proposed SCSI-3 Parallel Interface (SPI) standard, and control signals to support external differential drivers and receivers.

The external DMA interface can connect to an additional DMA buffer manager while the microprocessor interface supports a multiplexed data/address bus with wait state capabilities.

The SCSI and DMA interfaces support fast DMA transfers up to 10 megaTransfers per second, that is, 20 Mbytes per second for host and SCSI transfers and 10 Mbytes per second for disk transfers in SCSI 16-bit mode. The total time required to perform arbitration, selection, command transfer and message transfer is less than 20 microseconds.

5.1.1 Programmability

The SCSI and DMA interfaces are independently programmable between 16-bits and 8-bits wide for optimum performance and flexibility.

The WD61C96A handles SCSI protocol and data transfer through a 128-word writable control store, allowing the user to program any sequence of bus phases on the SCSI bus.

The Disk Port Writable Control Store allows the user to define the disk format rather than using a fixed sector and track format. The defect skipping option permits the dynamic variation of sector format during a read or write and works equally well with embedded or dedicated servos.

5.1.2 Testability

The WD61C96A includes several features to aid the user in testing this device in a system. To improve testability all RAM and register files have internal BIST logic and most microprocessor registers are readable. The WD61C96A provides special test modes for the large transfer counters, address pointers, internal logic blocks, and I/O pin mapping logic for PCB testing. The Disk Port contains LRC, CRC and ECC logic to guarantee data integrity. Write Control Store RAMS are read/writable by the microprocessor. A host bus test pin allows the internal DMA bus between the disk and SCSI cores to be observed by the host

5.2 WRITE CONTROL STORE: SCSI CONTROL

5.2.1 WCS Execution Started By Microprocessor (Normal Execution)

Normal mode of WCS execution goes through the following sequence.

1. Microprocessor waits until the WCS has halted.
2. Microprocessor loads SQADR register with STEP = 0.
3. WCS begins execution at SQADR.
4. If an error occurs, the WCS halts SQADR equal to the location where the error occurred.

5.2.2 WCS Execution Started By Microprocessor (Single-step)

Single step mode of WCS execution goes through the following sequence.

1. Microprocessor waits until the WCS has halted.
2. Loop: Microprocessor writes to SQADR with
   STEP = 1.
   a. WCS executes a single instruction.
   b. If WCS halts normally, SQADR is updated to point to next location and STOPWCS is set.
   c. If WCS halts due to an error, SQADR is not updated and STOPWCS is not set.
3. Microprocessor waits for interrupt
4. Microprocessor reads interrupt register to see if an abnormal halt occurred.
5. If normal halt occurred, read SQADR and goto Loop. Else evaluate error condition.

5.2.3 Response To Selection

The following tables define the behavior of SCSI section depending on the Response register settings.

The SCSI section only responds to single-bit selection, with the asserted bit in SD[7:0]. It does not respond to single-bit selection with the asserted bit in SD[15:8], or single-bit reselection.

If the SCSI section is in the process of being selected and the SELL is set by the microprocessor, the SCSI section responds to the selection.

SELL	SELH	Selection	SCSI section responds?	WCS	SIV	SRCID	Interrupt
0	x	any	no	stays idle	untouched	untouched	no
1	0	1-bit	(1)	stays idle	cleared	invalid	USEL
1	0	2-bit	yes	stays idle	set	loaded	USEL
1	1	1-bit	(1)	starts at SQSEL	cleared	invalid	no
1	1	2-bit	yes	starts at SQSEL	set	loaded	no

TABLE 5-1 WCS IS IDLE WHEN THE SCSI SECTION IS SELECTED

SELL	SELH	Selection	SCSI section responds?	WCS	SIV	SRCID	Interrupt
0	x	any	no	keeps running	untouched	untouched	no
1	0	1-bit	(1)	stops	cleared	invalid	USEL
1	0	2-bit	yes	stops	set	loaded	USEL
1	1	1-bit	(1)	branch to SQSEL	cleared	invalid	SREJ
1	1	2-bit	yes	branch to SQSEL	set	loaded	SREJ

TABLE 5-2 WCS IS RUNNING WHEN THE SCSI SECTION IS SELECTED

5.2.4 Response To Reselection

The response to reselection is exactly the same as selection, substituting RSELL for SELL, RSELH for SELH, SQRSL for SQSEL, and URSEL for USEL.

5.2.5 Response To DMA Request

Response to DMA request works in the following sequence.

1. Microprocessor programs SCSI section as DMA bus master.
2. Microprocessor loads SQDMA register
3. Microprocessor sets AUTOR

   Action: When DRQ is asserted on DMA port (indicating that data is available), the WCS begins executing at location SQDMA.

Unpredictable results may occur if the WCS starts due to a DMA request (AUTOR is set) and the Microprocessor sets the START bit. Either AUTOR should be cleared before START is set, or the system should ensure that DRQ will not be asserted at the same time as START is set.

5.2.6 Priority Of External Events

In order of priority, an idle SCSI section checks:

1. (Re)selection, if SELH or RSELH are 1.
2. DMA bus requests, if AUTOR is 1.
3. Microprocessor writes to SQADR register.

5.2.7 HLR and LLR

HLR are cleared by

- any start caused by a write to SQADR when the SCSI section is already connected
- any start caused by AUTOR when the SCSI section is already connected
- any SEL, SELA or RESEL instruction that completes connection
- any response to (re) selection, when the SCSI section asserts BSY (including when the SCSI section loses arbitration, and is (re)selected).
- all interrupts

LLR are cleared by

- any response to (re)selection, when the SCSI section asserts BSY
- RSTINT and UDISC interrupts.
- If ALLR is set, the LLR bits will also clear whenever the HLR is cleared.

Please see Section 5.7.2, SCSI Bus Interrupts, for details on the effects of interrupts.

5.2.8 Arbitration and (Re)selection

SCSI ID priority is shown below:

Priority: Highest Lowest

16-bit arbitration 7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8

During arbitration, input parity is ignored and SDP and SDP1 are not driven.

Parity checking when the SCSI section is being (re)selected:

- SDP is always checked for correct parity.
- If any bit of SD[8-15] is asserted, SDP1 parity is checked. If no bit of SD[8-15] is asserted, SDP1 parity is ignored.

Parity is always generated on SDP and SDP1 when the SCSI section is (re)selecting another device.

The SCSI section responds to selection by asserting 1 or 2 bits in SD[0-15], and it responds to reselection with exactly two asserted bits in SD[0-15]. It ignores (re)selections with other combinations of set bits or (re)selections with bad parity.

5.3 WRITE CONTROL STORE: DISK CONTROL

In general, the WD61C96A maintains a WD10C01 approach to Disk control, i.e., a writable control store platform. The Writable Control Store is 32 bits wide and 64 addresses deep. The microprocessor must load the Control Store and set the other configuration register bits before any Disk operation can begin. Five new Control Store bits have been added. (Refer to TABLE 5-3., CONTROL STORE BIT DEFINITIONS, on page 95).

WDID (CSERR bit 7)

When WDMODE is set, this bit is used when the WD ID segment registers are to be accessed. When WDID goes from low to high, the Data Segment Counter is loaded with ID Segment Register data and the Control Store State machine is set up to perform data segmentation on the current block.

RSECC (CSERR bit 6)

The Reed-Solomon Generator/Detector logic is enabled when this bit is active. This bit works in conjunction with RDGATE, and WRTGATE.

ECC is enabled when: RSECC * (RDGATE + WRTGATE)

SKPADSEL[1:0]/ES (CSERR bits 5 and 4)

When SKPEN is set, These two bits direct which Skip Address register is used at the end of the present CS instruction. There are three skip address registers, 1, 2, or 3.

When SKPEN is reset, the SKAD0 bit is used as an End of Sector flag. This flag informs the Buffer Manager logic that the true end of the sector has been reached. This flag, qualified with no Disk errors and the CS count is zero, is used to enable a Buff Count and external Block Count update. This bit is also used to qualify the reasons for failure detection. When this bit is reset and the FAIL bit is set, all errors except the ECC errors are examined by the WCS. When the ES and FAIL bits are set, all errors including the ECC error is examined by the WCS.

WDAC (CSVAL bit 0)

This bit adds another condition to the skip instruction. When this bit is set, a skip only occurs when the defect size counter is exhausted or a sector mark is detected. The WSCT bit of the ID Segmentation field defines which parameter is used. This bit is used during defect skipping.

LRCEN

This bit is active when the LRC bytes are being traversed through the control store data bus. If LRC checking is enabled, LRCCHK bit set in DCNF1 register, the data passing the LRC generator is flagged as the LRC bytes and compared against the internally calculated values. There are

always two LRC bytes per sector.

CRCEN

This bit is used to define the boundaries of the ID CRC field. The ID CRC calculation begins when CRCEN is set and CHK is reset. The ID CRC is complete and the ID CRC comparison begins when CRCEN and CHK are set.

WGCZ

This bit defines a wait condition in the WD Defect Skip mode. When this bit is set the Control Store waits for the generic counter to go to zero. This occurs when the end of a WD End of Data Segment is reached. When the counter is zero, the control can proceed to the next instruction or jump to another address based upon the conditions of SKPEN, JMPEN, and the internal LSEG bit.

7	WDID	Use WD Id Segment Registers	**CSERR**
6	RSECC	Enable Reed Solomon ECC	
5	SKAD1	Skip Register Select MSb	
4	SKAD0/ES	Skip Register Select LSb / End of Sector	
3	FAIL	Enable Error Failure	
2	RTY	Enable Read Error Retry	
1	DAC	Data Field Active	
0	SEQOUT	User Output Pin Control	
7	SVSEL	Value Byte Select (0 = immediate)	**CSCTL**
6	CWSEL	Count Byte Select (0 = immediate)	
5	WG	Write Gate	
4	RG	Read Gate	
3	AM	Address Mark Enable	
2	CMPEN	Compare Source to Data	
1	SKPEN	Jump to Skip Address	
0	JMPEN	Jump to Loop Address if Block Count >0, next if 0	
7	BUFF	Buffer Transfer	**CSVAL**
6	NOXFER	Decrement Block Count without Buffer Transfer	
5	LAST	Last CS Instruction	
4	ID	Use ID Registers (Compare, Send or Load)	
3	CHK	Check or Send ID CRC, Data CRC, or Data ECC	
2	LRCEN	Enable LRC Checker	
1	CRCEN	Enable ID CRC Generator	
0	WAITDAC	Wait for Defect or Sector Mark	
7			**CSCNT**
6	WIAM	Wait for Address Mark	
5	WIX	Wait for Index Detect	
4	WSM	Wait for Sector Mark Detect	
3	STOP	Stop All Operations	
2			
1			
0	WGCZ	Wait for Generic Counter is Zero	

TABLE 5-3 CONTROL STORE BIT DEFINITIONS

5.3.1 Track Format Basics

The WD61C96A is designed to operate with soft sectored or hard-sectored format (with or without embedded servo in the data track). In addition, defect skipping support has been added to the Disk control logic.

Traditionally, the sector format included three main fields. The first field usually defined the beginning of the sector boundary. Information included in this field is the sector mark, an optional ID Address Mark (an ESDI flag field which typically contains an encoding violation), and a gap which separates this area from the rest of the sector's information. The next field, ID Field, contained the information which identifies the sector. This field includes the VFO bytes, ID Sync Byte, ID Identifier Bytes (ID Cylinder/Head/ Sector bytes or Block address), and CRC bytes. A write splice followed which preceded the last field. The last field, Data field, is a continuous block of information containing VFO bytes, Data Sync Byte, Data Bytes, and some sort of ECC bytes with a pad. This type of format is still supported within the WD61C96A.

However, the WD61C96A defect skipping option introduces some enhancements to the standard format. With this option, the Disk controller can write data fields which are not limited to a single continuous block. A media flaw can be avoided without retiring the complete sector. In a traditional format a defect within the data field requires the complete sector to be retired. The defect skipping option makes better usage of the Disk capacity.

Defect skipping requires the following changes in the standard format. An ID Address Mark should be inserted at the beginning of the sector boundary. This is necessary when the data sector must span a sector mark. The ID Field is expanded to include additional bytes called the Data Segment field. This field is two bytes per data segment. These two bytes include a Count field, DS[0:9], and Segment Control Flags, LSEG and WSCT.

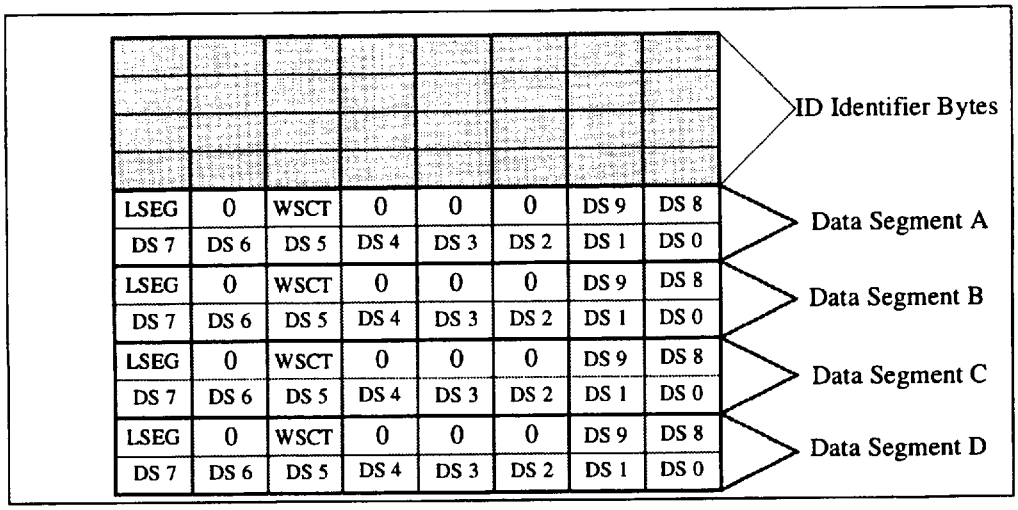

FIGURE 5-1 TYPICAL ID FIELD

There are four pairs of these bytes. These bytes indicate to the Disk controller how the following data field is to be divided. These bytes are written during a track format operation. During normal read or write operations the Disk controller reads and stores these bytes and dynamically adapts to the following data field configuration. DS[0:9] indicate the size of the data segment. LSEG indicates that this is the last segment before CRC/ ECC. WSCT indicates the type of skip that must be jumped before this segment can begin. If zero, the skip is a defect. If one, the Control Store waits for a sector mark detect before reading or writing the segment.

The Disk controller avoids the previously identified defect, sector mark, or servo burst. The data field can be divided into as many as four data segments or as few as one. Each Data Segment contains a VFO field, a Data Sync field, and a data field. The size and values for the VFO and Data Sync fields are programmable within the Control Store words.

FIGURE 5-2, SECTOR FORMAT EXAMPLE shows an example of a defect skip option format. In this example the data field is divided into two segments. The data field contains 520 data bytes plus CRC and ECC. The ID field contains the information on the size of the data segments and the type of gap, servo or defect, between segments. The following two sections in this document describe how the WD61C96A Control Store is programmed to handle this sector format.

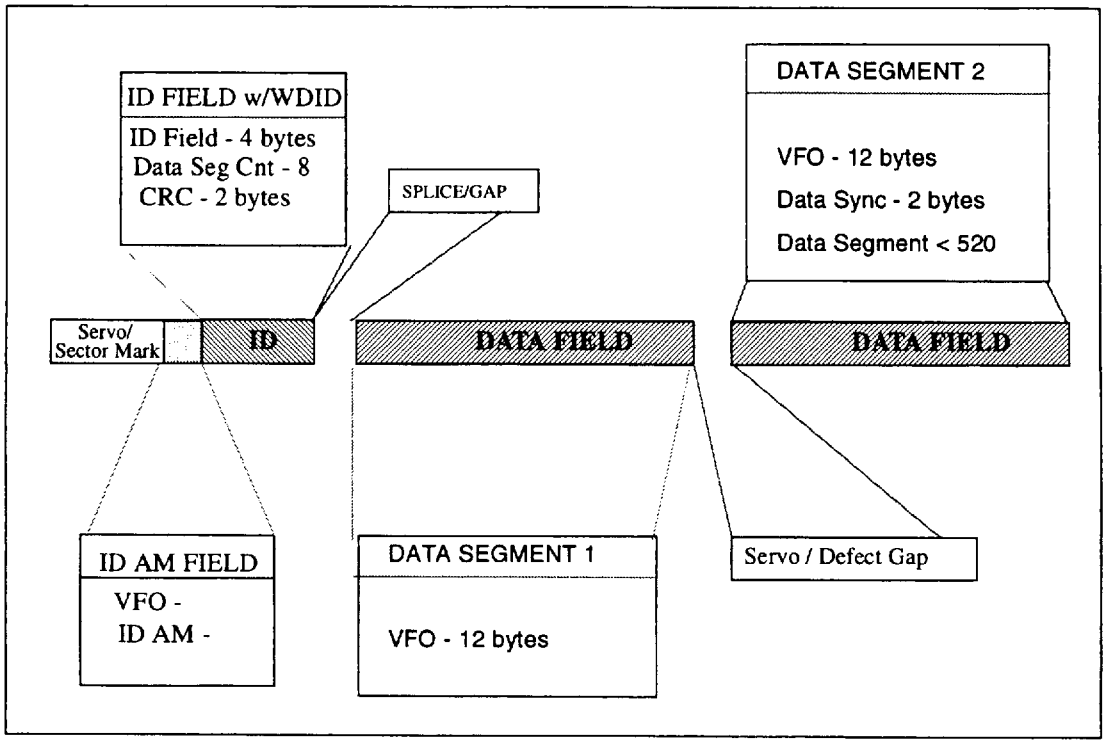

FIGURE 5-2 SECTOR FORMAT EXAMPLE

5.3.2 Disk Format Example

During a track format the Disk controller establishes the sector segmentation. Before performing a track format, the microprocessor must know:

- The location of all defects within the track
- The sector mark to sector mark spacing
- The size of any embedded servo bursts

The microprocessor must prepare the three following areas before a track format can proceed.

First, a Control Store must be loaded. Refer to TABLE 5-4, TRACK FORMAT WITH DATA SEGMENTATION. This Control Store uses immediate data to define some portions of the format and data from the buffer which dynamically defines the data segmentation of each of the sectors.

Second, the microprocessor must prepare the buffer data based upon the defect map and sector spacing. The Control Store uses these bytes when writing the ID Data Segment Field and the subsequent data field segments.

Lastly, the microprocessor must configure the Disk controller registers for a WD format operation. As a minimum, the microprocessor must initialize three skip addresses, one jump address, a defect skip count value, and configure the Control Store in WD mode. The three skip address registers and jump address register maximize Control Store flexibility with minimal Control loading.

In this example the microprocessor initializes the following registers.

JUMP ADDRESS	= 01
SKPADSEL 1	= 02
SKPADSEL 2	= 0A
SKPADSEL 3	= 10
Buffer Memory	= Sector Count x (3 Data Segment Control Pairs)
Start Address	= 00
Buffer Address	= Point to Data Segment Pairs
Buffer Count	= Sector Count x 8
ID Identifier Registers	= Cyl/Cyl/Hd/Sector or Block Address
Defect Skip Count	= 10 bytes DEFSKP Register

A basic format operation consists of the following steps. (The following steps correspond to the steps in TABLE 5-4, TRACK FORMAT WITH DATA SEGMENTATION.

1. Wait For Index Mark (CS Address = 00)

   In this example the Control Store waits for the Index Mark which establishes the beginning of the track. When the Index is found, the WCS skips to address 02.

2. Begin Format (CS Address = 02)

   Write gate is raised. A VFO/Gap field is written preceding the ID address mark byte. The CSVAL byte defines the byte that is written. The CSCNT determines the length of the VFO/GAP area. The CSCNT value is one byte less than the number of bytes to be written on the Disk. (Nine bytes of '00' are written.)

3. Write ID VFO Field (CS Address = 03)

   The VFO field is written preceding an ID Field. Typically, these bytes create a high frequency pattern on the media.

4. Write ID Address Mark (CS Address = 04)

   On a drive with soft sectoring, the WG and AM are both enabled to indicate to the drive electronics where to place the ID Address Mark.

5. Write ID Sync Byte (CS Address = 05)

   The ID Sync byte is written with this instruction. The quantity of ID Sync Bytes is defined by the CSCNT field and value is

defined by the CSVAL field of the WCS instruction.

6. Write ID Identifier - 3/4 bytes (CS Address = 06)

   The ID bytes are written to the Disk. These bytes are written from the ID registers if BUFF is reset (See Table 4-5). These values are microprocessor-loaded preceding the track format. If BUFF is set, these bytes are written from the Disk FIFO and stored in the ID/Segment Register. If enabled by IDIEN, these bytes increment at the end of each ECC read or write operation preceding the next ID field time using CHK. CRCEN enables CRC calculation for address bytes. CSCNT contains a '02', indicating a 3-byte address is to be written.

7. Write ID Data Segments (CS Address = 07)

   The Data Segment Control Bytes are written to the Disk. The buffer memory is the source of the these bytes. These bytes are also locally stored as Data Segment bytes within the Disk Controller's ID Register File, imbedded in sector's ID field for future reference. These control bytes are used when writing the following data field.

8. Write ID CRC (CS Address = 08)

   The ID CRC bytes (4) are written to the Disk. The ID CRC is internally generated over a specified field of data.

9. WCS Skip [CS Address = 09)

   The WCS skips to address in the skip address 1 register which is address '0A'. This instruction takes one RRCLK to complete. (See section 4.3.21 for Skip Address register details).

10. Write PAD/GAP (CS Address = 0A)

    A pad/gap field is written following the ID field for closure of the ID field and defining a write splice area within the sector.

11. Write Data VFO (CS Address = 0B)

    The Data VFO bytes are now written. These bytes are repeated for each and every data segment within the data field. The DAC signal should be raised during this instruction. The Data Segment counter is initialized when DAC is raised in preparation of the subsequent data segment to be written. The WDID bit can be enabled here. This bit must be enabled for at least 4 RRCLKS before enabling WG to allow the Defect Skip state machine to be setup properly.

12. Write Data Sync Byte(s) (CS Address = 0C)

    The Data Sync Byte(s) is written to the Disk. The CSCNT determines the quantity of sync bytes to be written and CSVAL determines the value to be written to the Disk.

13. Write Data Segment (CS Address = 0D)

    The Data Segment is filled from the immediate CSVAL. The quantity of bytes to be written is stored within the previously initialized data segment field in the ID Register File. The Control Store remains at this location until this counter is exhausted. A skip occurs when the count is exhausted and the LSEG flag is set. The WCS skips to the CRC/ECC instruction, address 10_{hex}. Else, if LSEG is zero and the count is exhausted the Control Store simply moves to the next address.

14. Write Pad (CS Address = 0E)

    In this example, this address is reached when LSEG is zero (this is not the last segment). PAD bytes are written after the data segment. A pad area is filled with CSCNT bytes and CSVAL data value.

15. Wait for SM or Defect (CS Address = 0F)

    The SKPEN and WDAC bits are set. The Control Store proceeds to the skip address instruction based upon one of three conditions: (1) if CSCNT value decrements to zero; (2) if WDAC is set and the Defect Skip Counter has decremented to zero, or (3) a sector mark is detected. Upon meeting the required conditions, the Control Store skips to the address defined in Skip Address 2 (address 0A) and prepares for the next data segment to be written to the

Disk. At this time the instructions repeat to address $0D_H$ where LSEG is set. The WCS skips to address 10_H

16. Write CRC/ECC (CS Address = 10 & 11)

    The CRC/ECC bytes are now transferred to the Disk. The CSCNT defines the length of this field. When CSCNT is exhausted the Control Store moves to the next address. The ID Identifier bytes are updated at the end of this instruction.

17. Write PAD, FAIL & JUMP (CS Address = 12)

    PAD bytes are written to the Disk as defined by CSVAL and CSCNT. If the Block Count is not exhausted, the Control Store executes another sector write operation by jumping to the LOOP address. In this example the WCS jumps to Loop address (01) and waits for the next sector mark to be detected before proceeding. If the Block Count is zero, the Control Store simply advances to the next instruction.

18. WCS STOP (CS Address = 13)

    The is the end of the track format. A sequencer stop interrupt is generated from DSEQI when the control store reaches this point. The Control Store waits for microprocessor intervention at this time before proceeding any further.

	CSVAL	CSCNT	CSCTL	CSERR	Comment
00	00	WIX	CWSEL, SKPEN	00	Wait for Index
01	00	WIX, WISM	00	00	Wait for Index/s
02	00	Gap Size - 1 (08)	WG		Write gap
03	VFO Bytes	VFO Size - 1	WG		Write VFO
04	00	00	WG, AM		Write ID Address Mark
05	FF	00	WG		Write ID Sync Byte
06	ID, CRCEN, (BUFF)	02	WG, SVSEL		Write 3 byte ID
07	ID, BUFF	DataSeg Info Bytes - 1	WG, SVSEL		Write Data Seg Cnt Information
08	CHK, CRCEN	03	WG, SVSEL		Write 4 byte CRC
09		00	SKPEN	SKAD0	Skips to 0A
0A	Pad Value	Pad Size 1	WG		Write Pad
0B	VFO Value	VFO Size - 1	WG	WDID	Write VFO
0C	FF	00	WG, SVSEL		Write Data Sync
0D	Data Fill Value	WGCZ	WG, SKPEN, SVSEL	RSECC, DAC, SKAD0, SKAD1	Write Data, skip if LSEG to 10
0E	Pad Value	Pad Size - 1	WG		Write Pad
0F	WDAC		SVSEL, SKPEN	SKAD0	Wait for DF/SM, Skip to 0A
10	CHK	03	WG, SVSEL	RSECC	Write CRC
11	CHK	11	WG, WVSEL		Write ECC
12	Pad Value	Pad Size - 1	WG, JMPEN	FAIL, ES	Write Pad/Fail/ Jump
13		STOP	CVSEL		STOP

TABLE 5-4 TRACK FORMAT WITH DATA SEGMENTATION

5.3.3 Read/Write Sector with Data Segmentation

During data read/write operations, modification of the Control Store instructions should be minimized. The WD61C96A meets this requirement by:

- Increasing the size of the Control Store to 64 addresses - For example, the Control Store can accommodate a primary read data routine, an error read data routine, a primary write data routine, and a primary write error routine without reloading the Control Store.
- Sharing Control Store Instruction - The three skip address registers, one jump registers, and new Control Store control bits permits better sharing of the Control Store routines. The microprocessor only has to change the skip and jump paths to establish a new combination of operation.

In the following example, the Control Store contains a primary read and write operation within one Control Store load. The Defect skipping option is also included in this operation.

In this example, the microprocessor initializes the following registers.

REGISTER	VALUE
SRESET	00_H
START	00_H (Read/Write Data)
LOOP	00_H
SKIP1	07_H (Read Data) 10_H (Write Data)
SKIP2	07_H (Read Data) 10_H (Write Data)
SKIP3	$0C_H$ (Read Data) 17_H (Write Data)
BLOCK CNT	Loaded with the number of sectors per track
Buffer Memory	Write Data
Buffer Address	Data Pointer; Read or write address pointer
ID Identifier Registers	Initial Cyl/Cyl/Hd/Sector or Block Address

A basic read/write operation consists of the following steps. These steps correspond to the steps in TABLE 5-5..

1. Wait for ID Address Mark
   (CS Address = 00)

   If defect skipping is used, the ID address mark is the primary method for determining a sector boundary. This is because the data sector can span multiple sector marks if the defects are large. The Sector marks, if any, are no longer used as the data sectors delimiter.

   The ID address mark is detected by raising AMENA without RDGATE or WRTGATE applied. The ID Address Mark is asynchronously detected by the drive Read logic. When an ID Address Mark is detected, AMDET is raised. The Control Store responses by moving to the next CS word.

2. Wait for ID Field Delay
   (CS Address = 01)

   An optional short pause is injected before RDGATE is applied.

3. Wait for ID Sync Byte(CS Address = 02)

   The Control Store waits for the detection of the ID Sync Byte. The CSVAL field contains the expected ID sync byte value. The CSCNT field determines the number of RRCLKS to wait for a sync byte. CMPEN is set. This enables the byte comparator. During a sync byte detection, AMENA can be used to indicate the type of sync byte to be found. When RDGATE is active and AMENA is zero, an ID sync byte is selected.

4. Read ID Identifier Field (CS Address = 03)

   The ID identifier field is now read and

stored. In this example, this field is 3 bytes long. These bytes contain the cylinder, head, and sector data or an LBA value. These bytes are compared to the expected ID identifier field which is programmed by the microprocessor.

5. Read ID Segment Field (CS Address = 04)

   These bytes define the segmentation of the following data field. In this example, there are 6 bytes, 3 pairs of data segment bytes. This means that the following data segment will be divided into three segments. The ID segment field remains the same size, regardless of the data segmentation of any individual data sector.

6. Compare ID CRC bytes (CS Address = 05)

   The ID CRC that is computed while reading the ID field is compared to the CRC that is read from the Disk. If there is an error, the CRCER bit in ECCSTAT register is set. The Control Store moves to the next instruction.

7. SKIP/RETRY (CS Address = 06)

   The WCS will attempt a retry of the ID field if one of the retry errors is active at this instruction. If no retry is required, the WCS will skip to Skip Address 1 and continue its operation. Note that since neither SKAD0 or SKAD1 are set, the skip address equals SKPADR1. The microprocessor sets SKPADR1 for a particular subroutine. If this is a read operation, it is set to 07_H It is set to 10_H for a write operation.

Read Data Field

8. Read Delay (CS Address = 07)

   A read delay instruction is used to avoid the write splice areas. The WDID bit is set so the Control Store can prepare for the first data segment. This data has been stored since the reading of the ID field.

9. Wait for Data Sync (CS Address = 08)

   The Control Store waits for the detection of the DATA sync byte (FF). The CSVAL field contains the expected ID sync byte value. The CSCNT field determines the sync byte quantity. CMPEN is set. This enables the byte comparator. During a sync byte detection, AMENA can be used to indicate the type of sync byte to be found. When RDGATE is active and AMENA is one, a DATA sync byte is selected.

10. Read Data Segment (CS Address = 09)

    When the Data Sync byte(s) has been detected the first data segment read operation can begin. The CSCNT field is set to zero because the Data Segment size is defined by the previous ID field. The quantity of segments and type of separation of data segments is also stored. The SKPEN is set in this Control Store instruction. If LSEG, the last segment flag, is set when the Data Segment Count is exhausted the Control Store skips to CRC/ECC verification step, address 0C. If the LSEG is not set, the Control Store proceeds to the next address.

11. Wait for Defect or Sector Mark (CS Address 0A)

    The Control Store reaches this address because this is not the last segment of the data field. If the WSCT flag (Wait for Sector Mark flag) is set, the Control Store must wait for a sector mark before proceeding. If WSCT is zero, the internal Defect Skip counter (DEFSKP) must be exhausted before the Control Store can proceed.

12. Skip (CS address = 0B)

    Skip to start the read of the next segment of the segmented sector (Address 07).

13. CRC/ECC read (CS Address = 0C,0D)

    The Control Store reaches this instruction when LSEG is set and the Data Segment counter is exhausted. The CRC and ECC are being calculated during the Data field read. During this instruction, the CRC and ECC are being compared against the values stored on the Disk. The CSCNT field defines the size of the CRC/ECC field. The ID Identifier field also increments at this time. An internal flag is also generated which indicates the status of the CRC/ECC

compare. The next data sector read operation continues, regardless of the CRC/ECC compare.

14. Jump/Fail Evaluation (CS Address = 0E)

    The Control Store checks for any Disk error failures and takes the jump if the block count is not exhausted and no errors are detected. The jump will be taken to the address specified by the LOOP register. If the block count equals zero, the WCS proceeds to the next instruction.

15. Operation STOP (CS Address = 0F)

    An operational end occurs when this CS instruction is reached. A sequencer stop interrupt is generated from the DSEQI register at this point.

Write Data Field

16. Write Delay (CS Address = 10)

    WDID is enabled here and must remain enabled for a duration of four RRCLKs before WG is enabled.

17. Write VFO (CS Address = 11)

    The Data VFO bytes are now written. These bytes are repeated for each and every data segment within the data field.

18. Write Data Sync Bytes (CS Address = 12)

    The Control Store generates the Data sync bytes from the immediate fields. The CSVAL field contains the expected ID sync byte. The CSCNT field determines the sync byte quantity. In this example, the count is one byte (FF_H). AM is set in the CSCTL to indicate that this is a data sync byte.

19. Write Data Segment (CS Address = 13)

    The Data Segment is written during this instruction. The size of the Data Segment is defined by the count that has been stored during the ID field read. DAC and RSECC are set to indicate ECC will be calculated for this instruction. BUFF is set to indicate that data moves from the buffer to the disk. WGCZ indicates the amount of bytes to be written. (This value is derived from the ID segment field.) A skip to the CRC/ECC write operation (Address 17) occurs if the Data Segment counter is exhausted and the LSEG bit is set for this segment. If not, the Control Store proceeds to the next sequential address.

20. Write Pad Bytes (CS Address = 14)

    Pad bytes are written for closure of the last data byte of the data segment. This instruction is reached if this is not the last segment. The CSVAL field contains the byte to be written. The CSCNT field contains the quantity of Pad bytes.

21. Wait for Defect or Sector Mark (CS Address = 15)

    The Control Store waits for the condition which is stored in the present data segment field, WSCT. If WSCT is set, a wait for sector mark is defined. If WSCT is reset, the defect size counter (DEFSKP) must exhaust before proceeding.

22. Skip (CS Address = 16)

    Skip to start the write of the next segment of the segmented sector. SKAD0 is set (SKPADR1, WCS Address 10). This loops until an LSEG is encountered and then skips to Address 17.

23. Write CRC/ECC(CS Address = 17, 18)

    The CRC/ECC are now written from the internally generated logic in the Disk block. When CHK and WG are both active, the internally calculated CRC and ECC are written to the disk. RSECC is set at Address 17, indicating that the ECC is calculated across the CRC bytes. The expected ID field is also incremented at this time.

24. Write Pad Bytes(CS Address = 19)

    A Pad field is written to the Disk for closure of the CRC/ECC bytes. The CSVAL field contains the byte to be written. The CSCNT field contains the quantity of Pad bytes. This instruction also includes a JUMP enable. The Control Store jumps to the defined loop address (Address 00) if the block (sector) count is not zero.

25. Operation STOP(CS Address = 1A)

This is the last instruction for the write operation. This instruction is reached when the sector count has exhausted. A sequencer stop interrupt from the DSEQI register is generated at this instruction.

	CSVAL	CSCNT	CSCTL	CSERR	Comment
00	00	WIAM	CVSEL, AM		Wait for ID Mark
01	00	Delay count - 1			RG delay
02	ID Sync Byte (FF)	Wait count - 1 (1F)	RG, SVSEL, CMPEN		Wait for ID Sync
03	ID, CRCEN	ID Size - 1 (02)	RG, SVSEL, CMPEN		Read ID LBA (3 byte ID)
04	ID	ID Flag Size - 1	RG, SVSEL		Read WDID Seg Cnt
05	CRCEN, CHK	CRC Size - 1 (03)	RG, SVSEL		Check CRC (4 bytes)
06		00	SKPEN	RETRY	Skip/Retry
07	00	Read Delay - 1		WDID	Read Delay - 1
08	Data Sync Value (FF)	Data Sync Wait Time (1F)	RG, AM, CMPEN		Data Sync (AM & RG indicate data sync)
09	BUFF	WGCZ	RG, SV/CVSL, CWSEL, SKPEN	RSECC, DAC, SKAD0, SKAD1	Data, Skip if LSEG
0A	WDAC	00	RG, SVSEL		Wait for SM/DFont = 0
0B		00	SKPEN	SKAD0	Skip to Read Seg.
0C	CHK	CRC Size - 1 (03)	RG, SVSEL	RSECC	Data CRC
0D	CHK	ECC Size - 1 (11)	RG, SVSEL		Data ECC
0E		00	JMPEN	FAIL, ES	Check Failures
0F		STOP	CWSEL		STOP
10		Write Delay - 1		WDID	Write Gate Delay
11	VFO Value	VFO Size - 1	WG		Write VFO
12	Sync Value (FF)	00	WG, AM		Data Sync
13	BUFF	WGCZ	WG, CWSEL, SVSEL, SKPEN	RSECC, DAC, SKAD0, SKAD1	Data, Skip if LSEG
14	Pad Value	Pad Size - 1	WG		Pad Bytes
15	WDAC	00	SVSEL		Wait for SM/DFont = 0
16		00	SKPEN	SKAD0	Skip to Write Seg.
17	CHK	CRC Size - 1 (03)	WG, SVSEL	RSECC	Data CRC
18	CHK	ECC Size - 1 (11)	WGSVSEL		DATA ECC
19	Pad Value	Pad Size - 1	JMPEN	FAIL, ES	Pad
1A		STOP	CSWEL		STOP

TABLE 5-5 DISK CONTROL STORE - READ/WRITE WITH SEGMENTATION

5.3.4 Read/Write Sector without Segmentation - 10C01 Backward Compatibility Mode

The WD61C96A can also operate in a 10C01 backwardly-compatible, ECC mode. In this mode the internal ECC logic generates the ECC bytes during read and write operations and generates the ECC syndrome bytes during an ECC read. In this mode all ECC errors are flagged to the microprocessor. The microprocessor is responsible for correcting the bytes in the buffer.

The 10C01 mode is invoked by changing one Control Store instruction and changing the configuration of the ECC logic. The Control Store change, line 0Fhex, adds two RCCLKs to the JMPEN delay. If an ECC error is detected, the Control Store aborts at this instruction. The jump is not made. The ECC logic is placed in a Syndrome Hold condition, the Offset/Mask logic is disabled, and the Corrector logic is disabled. In this mode, the Syndrome generator retains the last Syndrome when the Syndrome is nonzero.

	CSVAL	CSCNT	CSCTL	CSERR	COMMENT
00	--	WIX, WSM	CWSEL	--	--
01	--	04	--	--	Skew
02	--	0B	RG	--	ID Bit Sync
03	FF	1F	RG, CMPEN	RTY	ID Byte Sync
04	ID, CRCEN	02	RG, SVSEL,CMPEN	--	LBA
05	ID	02	RG, SVSEL	--	Rest of ID
06	CHK,CRCEN	03	RG, SVSEL	--	CRC
07	--	01	SKPEN	RTY	Splice
08	--	07	00	--	Redun Sync / Pad
09	--	0B	RG	--	Data Bit Sync
0A	FF	1B	RG, CMPEN	FAIL	Data Sync Bytes
0B	BUFF	FF	RG, SVSEL	DAC, RSECC	Data Field
0C	BUFF	FF	RG, SVSEL	DAC, RSECC	Data Field
0D	BUFF	09	RG, SVSEL	DAC, RSECC	Data Field + LRC
0E	CHK	11	RG, SVSEL	--	ECC Check
0F	--	00 (01, 10C01mode)	JMPEN	FAIL,ES	Jump/Fail Eval
10	--	STOP	CWSEL	--	End of Read (Stop)
11	00	18	WG	--	Bit Sync
12	FF	00	WG	--	Sync Byte
13	BUFF	FF	WG, SVSEL	DAC, RSECC	Data Field
14	BUFF	FF	WG, SVSEL	DAC, RSECC	Data Field
15	BUFF	07	WG, SVSEL	DAC, RSECC	Data Field
16	BUFF, LRCEN	01	WG, SVSEL	RSECC	(LRC Option)
17	CHK	11	WG, SVSEL	--	ECC Write
18	00	00 (01, 10C01 mode)	WG, JMPEN	FAIL, ES	Jump/Fail Eval
19	--	STOP	CWSEL	--	End of Write (Stop)
1A					

TABLE 5-6 DISK READ/WRITE - NO SEGMENTATION AND 10C01 MODE

REGISTER	VALUE
SRESET	06h
START	00h
LOOP	00h
SKIP	08h (Read Operation) 11h (Write Operation)
BLOCK CNT	Loaded with the number of sectors

Notes: Buffer contains data and LRC (2 bytes); block count = 0 is checked at every jump statement along

with the conditions.

5.4 DATA PATH CONTROL: SCSI INTERFACE

This section describes the Writable Control Store (WCS) used in the SCSI section of the WD61C96A.

The SCSI section provides 128 words WCS memory, each 30 bits long. The WCS instruction is divided into six control fields:

Field	Bits
1.Data Source/Destination control	6
2.Data Count Control	4
3.SCSI Phase Control	4
4.Instruction Execution Control	12
5.General Control	4
TOTAL	30

TABLE 5-7 WCS BIT FIELDS

The WCS in the SCSI section provides the flexibility in controlling the data transfer across the SCSI bus. The user can define the sequence and type of the data transfer by programming the WCS. Its proprietary, high-speed sequencer, whose execution resolution is four cycles of the input clock, can execute the instruction much faster than a microprocessor can interact with previous generation controller devices.

The instruction set is optimized for both initiator and target mode.

A standard WCS assembler is available for the user's application development purpose.

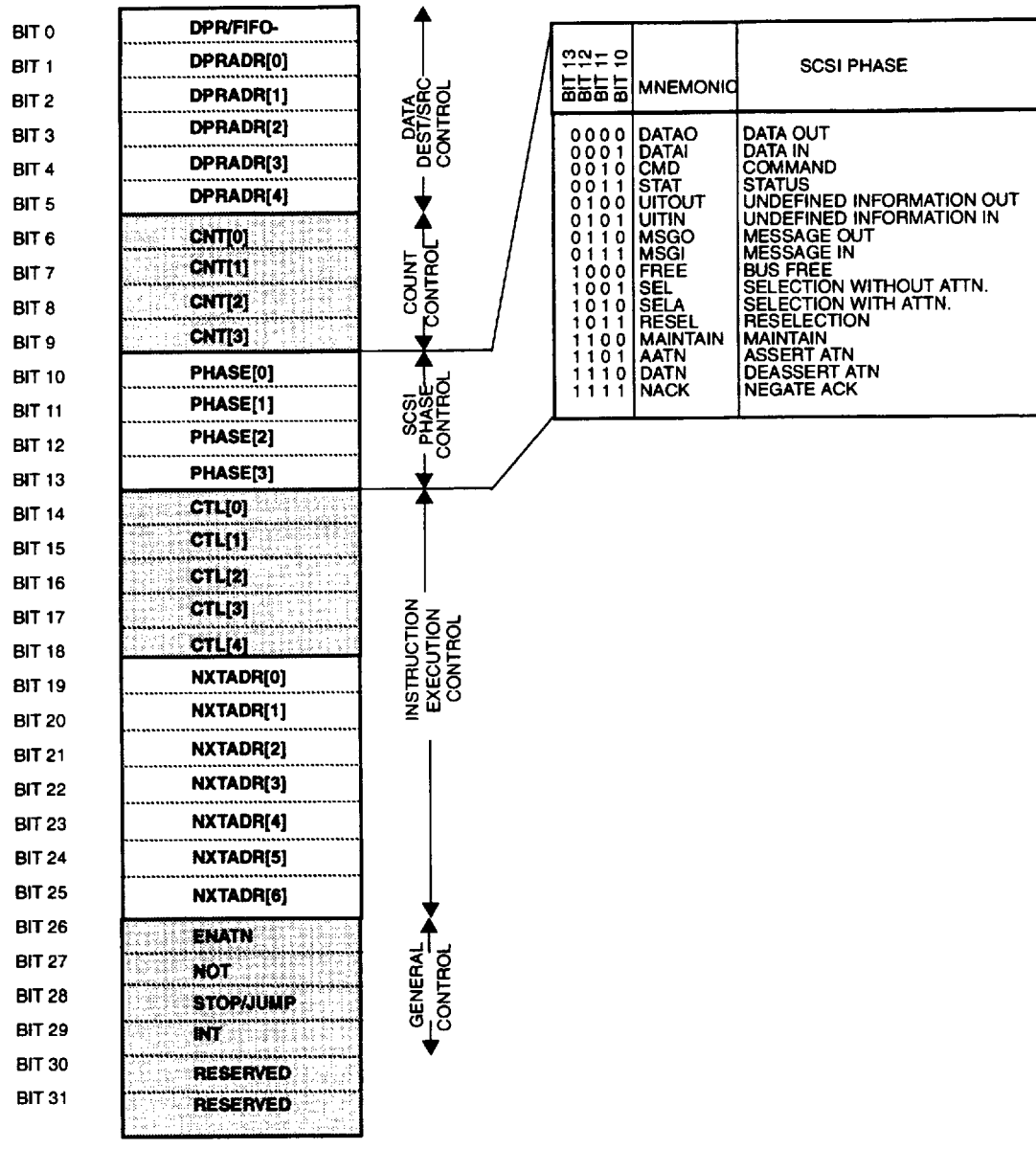

FIGURE 5-3 WRITABLE CONTROL STORE BIT DEFINITION

5.4.1 Microprocessor Access to the WCS

The SCSI section has 128 words of WCS memory. The microprocessor accesses the memory through the CSPRT0 through CSPRT3 registers. Section 4.6.1.13 on page 74 describes the CSADR and CSPRT0 through CSPRT3 registers in detail.

Accessing the WCS into the SCSI section involves two steps:

1. The microprocessor programs the starting RAM address into the CSADR register.
2. WCS Accesses:
   a. Writing to the WCS:

      The microprocessor writes a 32-bit WCS word into the CSPRT0 through CSPRT3 starting from CSPRT0. When the microprocessor writes to CSPRT0 - CSPRT2, the bytes are stored temporarily in the registers. When the microprocessor writes to CSPRT3, the SCSI section loads the 32-bit word (formed by CSPRT0-3) into the WCS-RAM. The value in the CSADR register is incremented.

   b. Reading the WCS:

      If the WCS is running, the value read out of CSPORT[0-3] is unpredictable. If the WCS is halted, the value read out of CSPORT[0-3] is the value at location CSADR.

5.4.2 Data Source/Destination Control

This control field defines the source/destination for the data being transferred in each WCS instruction. The data can be transferred to/from the FIFO or DPR. If DPR/$\overline{\text{FIFO}}$ is one, then the transfer involves the DPR. If DPR/$\overline{\text{FIFO}}$ is 0, the transfer involves the TC pipeline. Zero count transfers may be specified in all cases, with no data being transferred. Normally, zero count transfers are only used by the target when performing instructions which do not require a transfer, and the initiator normally would only use zero count transfers when testing the SCSI bus phase.

NOTE

A FIFO transfer is defined as a data transfer through the DMA port. All transfers, including DPR, actually go through the internal FIFO.

5.4.3 Data Count Control

5. 4.3.1 DPR Transfers

The DPRADR field defines the start address of the DPR register. Before the first byte is transferred, the value in the DPRADR field is loaded into the DPR address pointer and the CNT field is loaded into the DPR transfer counter. Each time a byte is transferred, the SCSI section increments the DPR address pointer and decrements the DPR transfer counter.

The transfer count field CNT[0-3] is interpreted as shown in the following table:

CNT[0-3]	Action
0	
1 - E	Transfer that number of bytes
F	PHASE = CMD:perform automatic CDB length decode (see below) PHASE = other:reserved.

TABLE 5-8 TRANSFER COUNT FIELD

When a CMD phase transfer is to occur, and the CNT field is set to F (hex), the three MSB of the first command byte is decoded to determine the command group.

CDB bits 7 6 5	Group	Number of bytes transferred after first
0 0 0	0	Five bytes.
0 0 1	1	Nine bytes.
0 1 0	2	Nine bytes.
0 1 1	3	Programmable through CDB3G field in CDBSIZ1 register.
1 0 0	4	Programmable through CDB4G field in CDB-SIZ1 register.
1 0 1	5	Eleven bytes.
1 1 0	6	Programmable through CDB6G field in CDB-SIZ2 register.
1 1 1	7	Programmable through CDB7G field in CDB-SIZ2 register.

TABLE 5-9 AUTOMATIC TRANSFER COUNT DECODING FOR CDB

For groups 3, 4, 6 and 7, if the value in CNT indicates automatic size decode, the SCSI section will transfer that many more bytes. (i.e. if group 3 was defined as a 6-byte command, the CDB3G field should be set to the value 5). If the correct number of bytes are not transferred, an unexpected phase change bit is generated.

5. 4.3.2 FIFO Transfers

Data will be transferred between the SCSI bus and DMA port in DMA mode, and between the SCSI bus and the DATA register in PIO mode, with the data passing through the FIFO in both cases. The size of the data transfer is determined by the TC pipeline and BYTEC.

5.4.4 SCSI Phase Control

This field defines the SCSI phase on the bus. The following table shows how these bits are decoded:

PHASE	MNEMONIC	TARGET	UNCONNECTED	INITIATOR
0	data_out_phase	Data Out	Reserved	Data Out
1	data_in_phase	Data In	Reserved	Data In
2	command_phase	Command Out	Reserved	Command Out
3	status_phase	Status In	Reserved	Status In
4	undefined_out_phase	Undefined Info Out	Reserved	Undefined Info Out
5	undefined_in_phase	Undefined Info In	Reserved	Undefined Info In
6	message_out_phase	Message Out	Reserved	Message Out
7	message_in_phase	Message In	Reserved	Message In
8	bus_free_phase	Bus Free	Test for Bus Free	Test for Bus Free
8	selection_phase	Reserved	Arbitrate & Select w/o ATN	Reserved
A	selection_atn_phase	Reserved	Arbitrate & Select w/ ATN	Reserved
B	reselection_phase	Reserved	Arbitrate & Reselect	Reserved
C	maintain_phase	Maintain	Reserved	Don't Care
D	assert_atn	Reserved	Reserved	Assert ATN
E	negate_atn	Reserved	Reserved	Negate ATN
F	negate_ack	Reserved	Reserved	Negate ACK

TABLE 5-10 PHASE CONTROL FIELD

NOTE

SCSI phases can be formed into four groups:

1: information transfer (DATOUT, DATIN, CMD, STAT, UITOUT, UITIN, MSGOUT, MSGIN)

2: free (FREE)

3: connection (SEL, SELA, RESEL)

4: maintenance (MAINTAIN, AATN, NATN, NACK)

5. 4.4.1 SCSI Phase Control: Target

The PHASE field tells the SCSI controller what phase to go to next, before beginning a transfer (if an immediate compare is not being performed). FREE is used to get off the SCSI bus. Maintain causes the existing SCSI phase to be maintained. Phase test may not be performed.

5. 4.4.2 SCSI Lines After Connection

The SCSI section drives the phase lines to DATOUT as soon as it is connected as a target through selection. If it is connected as a target through reselection, it drives the phase lines to DATIN.

5. 4.4.3 SCSI Phase Control: Unconnected

Only three of the phase_value is valid in this state;

SEL, SELA, RESEL: repeatedly arbitrate until

- arbitration is won (and we (re)select another device)
- arbitration is lost (and we are selected)

"Test phase" instruction may only be used with PHASE = FREE, and will return TRUE.

Only **no_data** and a count value of **0** (zero-byte transfer) may be specified in the first two fields while in the unconnected state.

5. 4.4.4 SCSI Phase Control: Active Initiator

Several phase_values are valid when connected as an initiator. This section describes the action taken by the SCSI section depending on the type of phase_value specified.

PHASE = information transfer and "test phase" specified by:

- zero-byte transfer must be specified
- wait for REQ edge or bus free
- if REQ edge seen and phase matches, return true to stop/jump test.
- if REQ edge seen and phase does not match, return false to stop/jump test.
- if bus free (i.e., BSY- and SEL- negated) seen, set UDISC

When PHASE = information transfer & "test phase" is not specified then perform the following for each byte/word in the transfer:

- wait for REQ edge or bus free
- if phase matches, perform transfer otherwise
- if ENATN is asserted, pause transfer and go to stop/jump test
- or if bus free, set UDISC
- otherwise, set UPHAS

When PHASE = FREE ("test phase" must be specified, with zero-byte transfer), then the following occurs:

- wait for the next REQ edge or bus free to occur.
- if bus-free, return true to stop/jump test.
- if REQ is asserted, return false to stop/jump test.

If PHASE = MAINTAIN ("test phase" may not be specified), then perform the following for each byte/word in the transfer:

- Wait for REQ edge or bus free
- If SCSI phase matches previous SCSI phase, perform transfer
- Otherwise, if ENATN is asserted, pause transfer and go to stop/jump test
- If bus free, set UDISC, else set UPHAS

If PHASE = AATN, NATN (zero-byte transfer must be specified; test phase not allowed), then the following sequence is performed:

- SCSI bus must currently be in an information-transfer phase.
- ATN is asserted or negated, and ACK is negated.
- If bus free occurs, it is ignored & the next instruction will deal with it. (This makes it possible to respond correctly to a fast target.)
- Evaluate stop/jump condition.

If PHASE = NACK (zero-byte transfer must be specified; test phase not allowed), then the following sequence occurs:

- SCSI bus must currently be in an information-transfer phase.
- ACK is negated.
- If bus free occurs, it is ignored & the next instruction will deal with it. (This makes it possible to respond correctly to a fast target.)
- Evaluate stop/jump condition.

5.4.5 Instruction Execution Control

This field controls WCS program execution. All condition tests are performed after the data transfer (if any) has completed, and any data error conditions have been processed (setting interrupts, halting, etc.). TABLE 5-11 on page 115 shows the transfer control functions supported by the SCSI section:

CTL	Mnemonic	Execution Control
0	flag[0]	Stop/Jump to address NXTADR[0-6] if FLAG0 is true.
1	flag[1]	Stop/Jump to address NXTADR[0-6] if FLAG1 is true.
2	flag[2]	Stop/Jump to address NXTADR[0-6] if FLAG2 is true.
3	flag[3]	Stop/Jump to address NXTADR[0-6] if FLAG3 is true.
4	flag[4]	Stop/Jump to address NXTADR[0-6] if FLAG4 is true.
5	flag[5]	Stop/Jump to address NXTADR[0-6] if FLAG5 is true.
6	flag[6]	Stop/Jump to address NXTADR[0-6] if FLAG6 is true.
7	flag[7]	Stop/Jump to address NXTADR[0-6] if FLAG7 is true.
8	mask[0]	Stop/Jump to address NXTADR[0-6] if masked compare 0 is true.
9	mask[1]	Stop/Jump to address NXTADR[0-6] if masked compare 1 is true.
A	mask[2]	Stop/Jump to address NXTADR[0-6] if masked compare 2 is true.
B	mask[3]	Stop/Jump to address NXTADR[0-6] if masked compare 3 is true.
C	mask[4]	Stop/Jump to address NXTADR[0-6] if masked compare 4 is true.
D	mask[5]	Stop/Jump to address NXTADR[0-6] if masked compare 5 is true.
E	mask[6]	Stop/Jump to address NXTADR[0-6] if masked compare 6 is true.
F	mask[7]	Stop/Jump to address NXTADR[0-6] if masked compare 7 is true.
10	phase	Stop/Jump to address NXTADR[0-6] if PHASE field = SCSI phase.
11	atn	Stop/Jump to address NXTADR[0-6] if ATN is asserted.
12	idflag	Stop/Jump to address NXTADR[0-6] if IDFLAG.
13	compare_immediate	Stop/Jump to address NXTADR[0-6] if immediate data equal. See section 5. 4.5.1
14	tc_last	Stop/Jump to address NXTADR[0-6] if TC=0 and LDTCL loaded the TC
15	tc_zero	Stop/Jump to address NXTADR[0-6] if TC pipe is empty and TC = 0.
16	always	Stop/Jump to address NXTADR[0-6] always.
17	Reserved	
18	Reserved	
19	Reserved	
1A	Reserved	
1B	Reserved	
1C	Reserved	
1D	Reserved	
1E	Reserved	
1F	Reserved	

TABLE 5-11 WCS INSTRUCTION EXECUTION CONTROL BITS

LAST is set if the current transfer was loaded with LDTCL and TC = 0. LAST is cleared as soon as a new FIFO transfer instruction is started.

5. 4.5.1 Immediate Data Comparisons

The Compare_immediate condition performs the following: The CNT and PHASE fields are considered to be a byte (CNT[0] low, PHASE[3] high), which is compared against the byte at location DPRADR:

WCS BIT	Compared to DPR[DPRADR] bit #
CNT[0]	0
CNT[1]	1
CNT[2]	2
CNT[3]	3
PHASE[0]	4
PHASE[1]	5
PHASE[2]	6
PHASE[3]	7

TABLE 5-12 IMMEDIATE DATA COMPARISONS

Jump / Stop take effect if they are equal.

5. 4.5.2 Data Comparison

All compares occur after the data transfer has been completed. If data is being written to the DPR, the comparison does not occur until all the data has been written to the DPR. The comparison is always to the DPR byte at the location specified in DPRADR.

The WCS executes each instruction as follows:

1. Perform data comparison (if any requested), and evaluate branching conditions
2. Branch to new location or halt.

NOTE

As an initiator, if the target begins to transfer bytes while the WCS is in steps 2 or 3, the WCS will not respond until the next step 1 that occurs.

5.4.6 General Control

This field contains miscellaneous control bits.

INT = Generate Interrupt

This bit causes the INTWCS bit in the ISR to be asserted and the current WCS address to be latched into the SQINT register after the data-transfer portion of the current instruction has been completed.

ENATN = Enable ATN Interrupt

There are two ways for the SCSI section (as a target) to respond to ATN while running:

1) The WCS is programmed to test for ATN asserted, and jump or stop.
2) The ENATN bit is set.

Detailed information on response to ATN is in section 5. 7.2.3 on page 149.

When the SCSI section is connected as an Initiator, this bit disables phase checking when it sets. See Section 5. 4.4.4.

NOT = Invert Branch Condition

This bit causes the WCS to branch or stop if the condition is NOT true. (i.e. if the LAST flag is tested and NOT is set, the WCS will branch if LAST is false.)

STOP/JUMP = STOP if Condition/JUMP if Condition

If STOP/JUMP is "1" and condition is true, the WCS will stop.

If STOP/JUMP is "0" and condition is true, the WCS jumps to NXTADR[0-6].

Please see TABLE 5-11. on page 115 for a list of conditions.

5.4.7 Odd-byte Transfers

The first byte in any logical transfer is the even byte (byte 0), and the next is the odd byte. If an odd byte disconnect occurs, the last byte transferred before the disconnect is an even byte, and the first byte transferred after the reconnect is an odd byte.

Odd Byte Disconnect (Initiator Only)

Sixteen-bit SCSI: The SCSI section does not know if both bytes of the last word are valid.

- 16-bit DMA: The SCSI section always transfers the last word.
- 8-bit DMA: microprocessor must back up the peripheral one byte.

8-bit SCSI: The SCSI section knows the exact number of valid bytes.

- 16-bit DMA: The SCSI section sends a word with a pad byte (value 00_{hex}).
- 8-bit DMA: no problem.

5.4.8 Hardware And Software Resets

There are two ways to cause the SCSI section to go through reset mode: asserting $\overline{HRST}$ (hardware reset) and writing a 1 to CRST (software reset). When the SCSI section enters reset mode, all bits (except CRST) are reset to their default values, only the TEST0 register may be read (CRST will equal 1), and no register may be written. CRST is reset to 0 when the SCSI section leaves reset mode.

To perform a hardware reset, $\overline{HRST}$ is set to 0. At this point, the SCSI section enters reset mode, and remains in reset mode until a short time after $\overline{HRST}$ is changed to a 1.

To perform a software reset, the microprocessor writes a 1 to CRST. The SCSI section will be in reset mode for a short time.

5.4.9 Resuming Halted Transfers

If the SCSI section is transferring data in logical blocks, and the transfer halted in the middle of a logical block, the microprocessor may wish to resume the transfer at the point where the transfer halted. To do this,

- the microprocessor must read and then write back the values in the TC, PBR, and BR registers.
- the microprocessor starts the WCS.

Values in the residue registers are valid after any event which causes the data transfer to finish cleanly, such as ABORT, ATN and parity errors. Events such as KILL, FRST or SCSI reset cause the TC residues to be invalid.

5.4.10 Interpreting Transfer-Count Values

Given a physical block size of 'P' bytes, a physical: logical ratio of 'R', and 'T' logical blocks to be transferred, program the PSIZE register with 'P-1', PLR with 'R-1', and TC register with 'T'.

Here is an example:

Given a physical block size of 2 bytes, a physical: logical ratio of 2, and 2 logical blocks to be transferred, program the PSIZE register with 1, PLR with 1, and TC register with 2. The table below shows how Transfer Count, Physical Block Residue and Block Residue register changes as the transfer progress.

TC	PBR	BR	Notes
2	1	1	Load at start of transfer; no bytes have been transferred; transfer one byte
2	1	0	Transfer one byte (end of 1st physical block)
2	0	1	Transfer one byte
2	0	0	Transfer one byte (end of 2nd physical block and 1st logical block)
1	1	1	Transfer one byte
1	1	0	Transfer one byte (end of 3rd physical block)
1	0	1	Transfer one byte
1	0	0	Transfer one byte (end of 4th physical block and 2nd logical block)
0	1	1	End of the transfer

TABLE 5-13 INTERPRETING TRANSFER COUNT VALUES

Note that TC=0 only when the transfer is completed. When a transfer is paused (the pause would always happen AFTER the counters were decremented/loaded, before the next byte is transferred)

- Bytes remaining in the current physical block = BR + 1
- Bytes in remaining complete physical blocks within current logical block = PBR * (PSIZE + 1)
- Bytes in remaining complete logical blocks = (TC - 1) * (PLR + 1) * (PSIZE + 1)
- Total bytes remaining = (BR + 1) + (PBR) * (PSIZE + 1) + (TC - 1) * (PLR + 1) * (PSIZE + 1)

5.4.11 Calculation of Minimum SCSI Timings

The following assumes two SCSI section chips, one as target, the other as initiator, performing arbitration, selection, command transfer, message transfer and disconnect.

Timings	State
0ns	Bus free state is reached (BSY and SEL have been inactive for 400ns)
+T1	Initiator determines that Bus Free condition exists
+0.8 µs	Initiator asserts BSY and its ID
+2.4 µs	Initiator checks to see that it won arbitration.
+T1	Initiator asserts SEL
+1.2 µs	Initiator asserts 2-bit selection and ATN
+T1	Initiator releases BSY
+0.4 µs	Target sees that BSY has been negated for 400ns
+T1	Target asserts BSY

TABLE 5-14 MINIMUM SCSI TIMINGS

Timings	State
+T1	Initiator releases SEL
+T1	Target sees that SEL has been negated
+T1	Target goes to CMD phase
+0.4 µs	Target waits for phase lines to settle
+n*Tdata	Target transfers n bytes of data from initiator
+0.4 µs	Target changes to message phase
+Tdata	Target transmits message byte (disconnect). Target negates BSY

TABLE 5-14 MINIMUM SCSI TIMINGS

This results in a total of 5.6 µs + 6 * T1 + (n+1) * Tdata, where T1 is approximately 200 ns and Tdata is from 200 to 400 ns, depending on the speed of asynchronous data transfers.

5.4.12 Low-level SCSI Control

Low-level SCSI control is provided as a way to clear a hung SCSI bus, or to deliberately create an illegal state on the SCSI bus. Low-level SCSI control may be entered at any time, but may only be exited by bringing the SCSI bus to bus free in low-level control and then resetting the SCSI section.

The microprocessor can read the low-level control registers at any time to verify the state of the SCSI bus. The microprocessor should debounce the signals by reading the register twice to avoid incorrect reading during a phase transition.

To enter low-level mode, the microprocessor should perform the following steps:

- bring the SCSI bus to some stable state.
- read low-level control registers, and write them to the desired values.
- set SCSIL.

PUE must be set to 0 when performing arbitration and (re)selection in low-level single-ended SCSI, and whenever both TGS and IGS are 0.

Functions disabled when in low-level control:

- WCS operation.
- FIFO transfers of any kind to or from the SCSI bus.
- DPR transfers of any kind to or from the SCSI bus.
- generation of output parity, including during (re)selection of another device.
- checking of input parity
- any automatic response that would start the WCS. (the bits are not touched; their function is disabled).

Functions enabled when in low-level control:

- SCSI section will get off SCSI bus when SCSI reset occurs.
- SCSI section will get off SCSI bus if unexpected bus free (in the initiator case) occurs.
- RSTF interrupt.

BSY, SEL and RST:

These signals are open-drain, and their output drivers are always enabled, though not necessarily driving low.

TGS, IGS:

These two bits control the SCSI bus drivers as shown in the table below.

TGS / IGS	REQ,MSG CD,IO	ATN,ACK	SD Bus*
0 / 0	enabled	enabled	enabled
0 / 1	tri-stated	enabled	enabled by I/O input high
1 / 0	enabled	tri-stated	enabled by I/O inp low
1 / 1		reserved	

TABLE 5-15 TGS, IGS DRIVER CONTROL

* SD Bus includes SD[0-15] pins and SDP, SDP1.

In differential SCSI, SDOE[0-15] and SDPOE outputs will be high any time SD[0-15], SDP and SDP1 outputs are enabled.

5.4.13 State of SCSI Section Outputs After Hardware or Software Reset

Pins	Single Ended	Differential
AD[0:7]	tri-stated	tri-stated
RDY	1	1
INT,RSTF	0	0
SD[0:15], SDP, SDP1	tri-stated	tri-stated
SDOE[0:15], SDPOE	n/a	0
TGS,IGS	n/a	0
BSY, SEL, RST	tri-stated	0
REQ, ACK, ATN	tri-stated	tri-stated
MSG, IO, CD	tri-stated	tri-stated
BD[0:15], BDPL, BDPH	tri-stated	tri-stated
DACKA, DACKB	tri-stated	tri-stated
DRQA, DRQB	tri-stated	tri-stated
DRE, DWE	tri-stated	tri-stated

TABLE 5-16 STATE OF SCSI SECTION OUTPUTS AFTER RESET

5.4.14 Starting the WCS

If the SCSI section is not connected on the SCSI bus, the first instruction that must be executed when the WCS starts is SEL, SELA or RSEL.

5.4.15 Notes on Transfers

- All SCSI data transfers go through the FIFO (data going between the DPR and SCSI bus is buffered in the FIFO).
- All types of SCSI transfers are supported by the DPR and FIFO. The only restriction is that the DPR cannot transfer to the DMA port using DMA transfers.
- Target mode: If the TC empties during a transfer, the WCS will continue to the stop/jump portion of the instruction.
- Initiator mode: If the TC is empty at the start of a transfer instruction, the WCS will wait until the TC has a value written to it. If the TC empties during an instruction, the WCS will wait until a new value is loaded into the TC. Once the WCS has begun a data-transfer instruction in initiator mode, only an error or TC=0 on a value loaded with LDTCL will cause it to end the transfer.

5.5 DATA PATH CONTROL: HOST INTERFACE

The Host Port is a generic DMA port. The host port permits data transfers between the internal SCSI manager, internal Disk Manager, and an optional external Disk Manager. The external Disk Manager is only supported in the 208-pin versions. A fully supported host port encompasses the external bus pins (BD[15:0], BDPH, BDPL). The external control pins (DRQA, DACKA, DRQB, DACKB, DWEB, DREB), an internal host bus, and internal host control signals.

Care should be taken when accessing the internal registers of WD61C96A, since the WD61C40 section and WD33C96 section access timings are slightly different. They are, however, compatible with commonly used processors such as 80196, 80186, 8051, etc. For more information, refer to sections 7.1.2, PIO Read with RDYB - CS0, 7.1.3, PIO Write with RDYB - CS0, and 7.1.4, PIO Read with RDYB - Buffer Memory Access (CS0).

Five internal registers and two input pins establish Host port configuration. HCNF1 and HCNF2 define the Disk Manager operating modes (Sections 4.4.1, Host Configuration 1 and 4.4.2, Host Configuration 2.) DMACNF, CTLA and DMATIM define the SCSI Manager operating modes (Sections 4.6.1.9, DMA Configuration Register, 4.6.1.10, DMA Timing Control Register, and 4.6.2.1, Auxiliary Control Register). TST2 and TST1 define the external Host Port pins operating modes. These registers and input pins define the following operational variables:

- Master/slave operation
- DMA Request/Acknowledge active levels
- Master Mode Read/Write Strobe ON/OFF time

- Parity checking for each 8-bit bus group
- Parity generation
- Mirror/striping/restore modes

The WD61C96A operates only two of the many 61C40/33C96 modes. The first mode is Normal Mode Transfers. In this mode the internal SCSI Manager always operates as the bus master. The internal and external Disk Managers must be programmed as bus slaves.

The internal SCSI Manager as a bus master must generate the DMA Acknowledge (DACKA and DACKB) and the DMA Strobes (DWEB and DREB). The external and internal Disk Managers must generate the DMA Request, DRQA and DRQB. The second mode is the mirror/restore mode. Normal Mode Transfers can be programmed for burst or single cycle transfers.

The second mode is Mirror/Restore Mode Transfers. In this mode the internal Disk Manager must be programmed as the masters. The external Disk Manager must be programmed as the slave. The transfer must always be in Single Cycle mode. For more information, refer to Section 5.12, TEST MODES.

5.5.1 Normal Mode Transfers

DMACNF Register address = 14, Internal 33C96							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	DMA 16	DAC AH	DRQ AH			MAS TER	BUR ST

DMA16 = 1; Host transfers are word-wide only

DACAH = 1/0; level must match Disk Manager (HCNF1 bit 5)

DRQAH = 1/0; level must match Disk Manager (HCNF1 bit 4)

MASTER = 1; SCSI Manager is always master

BURST = 1/0; level must match Disk Manager (HCNF1, bit 0)

DMATIM Register address = 16, Internal 33C96							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DMA OE	DS RW						

DMAOE = 1;

DSRW = 1

CTLA Register address = 02, Internal 33C96							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
	PBS	PAS	PPEN				MRM

PBS = 1/0; set if normal mode or striping mode transfers

PAS = 1/0; set for all transfers between internal SCSI and Disk Manager transfers

PPEN = 1/0; set if stripping is required

MRM = 0; must be 0 for normal transfers

HCNF1 Register address = 70, Internal or external WD61C40							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
		DACK H	DRQH			MAS SEL	BUR ST

DACKH = 1/0; level must match SCSI Manager (DMACNF bit 5)

DRQH = 1/0; level must match SCSI Manager (DMACNF bit 4)

MASSEL = 0; Disk Manager is always slave in normal transfer

BURST = 1/0; level must match SCSI Manager (DMACNF bit 0)

HCNF2 Register address = 70, Internal or external WD61C40							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DMA EN							

DMAEN = 1; must be set for Transfer

Test Pins TST2:1 = 1; defines normal mode transfer

5.5.2 Mirror/Restore Mode

DMACNF Register address = 14, Internal 33C96							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DMA 16	DAC AH	DRQ AH			MAS TER	BUR ST

DMA16 = 1;

DACAH = 1/0;

DRQAH = 1/0

DMATIM Register address = 16, Internal 33C96							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DMA OE	DS RW						

DMAOE = 0;

DSRW = 1;

CTLA Register address = 02, Internal 33C96							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	PBS	PAS	PPEN				MRM

PBS = 1;

PAS = 1;

PPEN = 0;

MRM = 1; mirror restore mode chalked

HCNF1 Register address = 70, Internal or external WD61C40							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		DACK H	DRQH			MAS SEL	BUR ST

DACKH = 1/0;

DRQH = 1/0;

MASSEL = 1; internal DM is master

0; external DM is slave

BURST = 0; single cycle only

HCNF2 Register address = 70, Internal or external WD61C40							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DMA EN							

DMAEN = 1;

Test Pins TST2:1 = 1

5. 5.2.1 System Setup

- One internal DMA controller (DMAA, the WD61C40); one external DMA controller (DMAB); and one SCSI section.
- The SCSI section's DACKA and DRQA pins are connected to DMAA.
- The SCSI section's DACKB and DRQB pins are connected to DMAB.
- A single DMACNF (DMA configuration register) setup value is shared between DMAA and DMAB.
- A single DMATIM (DMA timing register) setup value is shared between DMAA and DMAB.

5. 5.2.2 Mirroring

Writing:

- Both DRQs must be asserted for the SCSI section to transfer data out onto DMA bus.
- Both DMA devices get the same data.
- If either DRQ goes inactive, the data transfer will pause.

Reading:

- DRQ is asserted by one or both of the DMA ports.
- If DRQA is asserted, the SCSI section will clear PBS or else it will clear PAS.
- The data transfer begins.
- The microprocessor watches for the SCSI section to clear either PAS or PBS, and then kills the data transfer in the DMA controller that is locked out.

- The microprocessor must not kill the "losing side" channel until the "winning side" DMA transfer is completed. Clearing the one pending DMA channel while the other is in progress may abort the latter transfer as well.

5. 5.2.3 Striping

At the start of each data transfer instruction, the PINGR register is loaded with the value in PING, unless the microprocessor has written to the PINGR register since the last transfer stopped. The following loop is executed for both reading and writing. If PAS is set, the transfer starts with DMA device A, otherwise it begins with DMA device B.

While transfer is not complete:

- transfer PING + 1 physical blocks to/from initial DMA device, ignoring alternate device's DRQ.
- transfer PING + 1 physical blocks to/from alternate DMA device, ignoring initial device's DRQ.

5.5.3 Burst vs. Single Cycle Operation

The Host port can be configured for burst transfers or single cycle transfers, depending upon the value of the BURST bit in the DMACNF and HCNF1 registers. Burst accesses allow multiple data transfers during one DRQ/DACK handshake while a single cycle operation requires a full DRQ/DACK handshake process for every word that is transferred.

In burst mode, the timing handshake is very critical. A slave's DRQ is negation is based upon the DMA direction. When the data is being transferred from master to slave, the DRQ is negated with respect to the trailing edge of the DWEB and N-2 words remaining to be transferred. When the data transfer is from slave to master, the DRQ is negated with respect to the leading edge of DREB and N-2 words remaining to be transferred.

The figures which follow show the DRQ/DACK handshake timing that is required at the termination of the Read or Write DMA operation. Please note that these drawings are not to scale but only describe the relationship between the signal transitions.

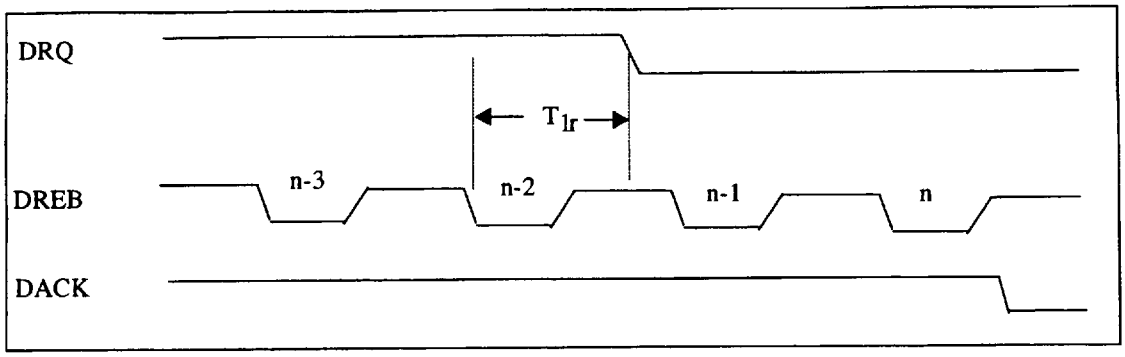

FIGURE 5-4 HOST DMA READ WITH 0 CYCLES TO TERMINATE

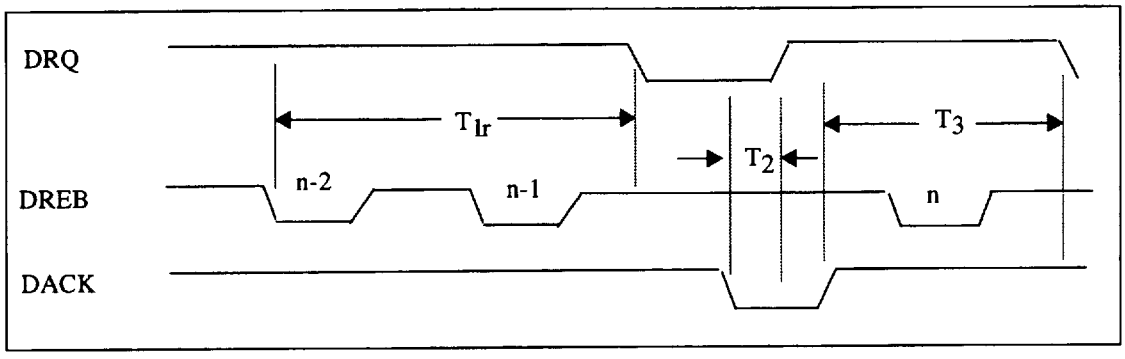

FIGURE 5-5 HOST DMA READ WITH 1 SINGLE CYCLE TO TERMINATE

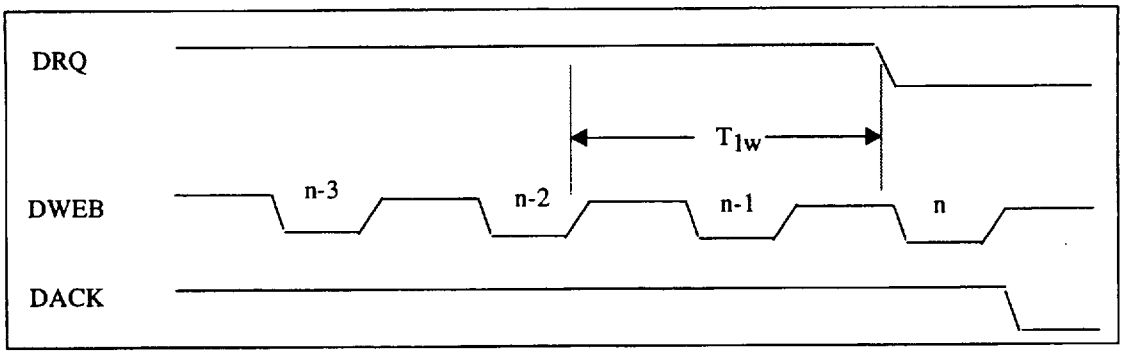

FIGURE 5-6 HOST DMA WRITE WITH 0 SINGLE CYCLES TO TERMINATE

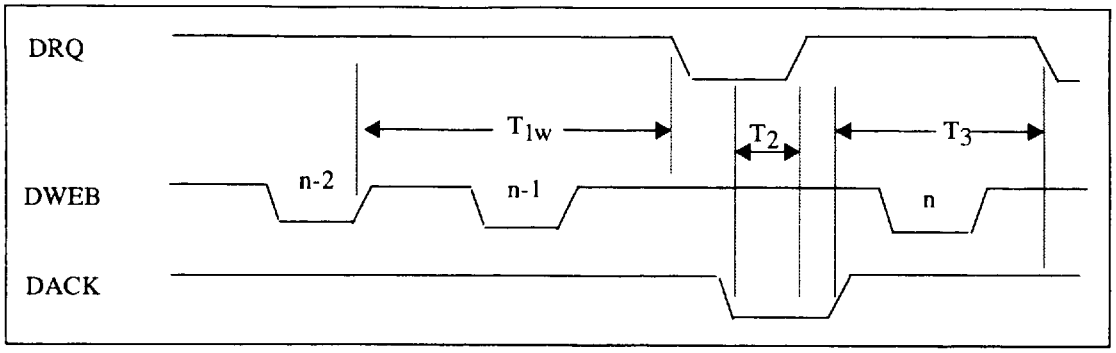

FIGURE 5-7 HOST DMA WRITE WITH 1 SINGLE CYCLE TO TERMINATE

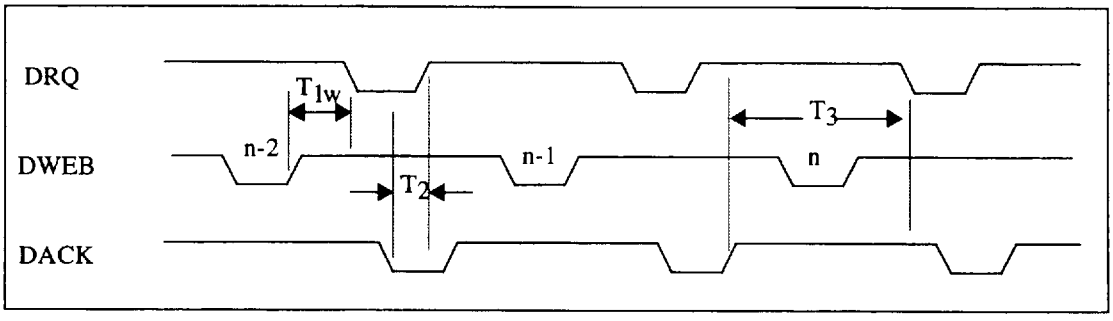

FIGURE 5-8 HOST DMA WRITE WITH 2 SINGLE CYCLES TO TERMINATE

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
T_{1r}	DREB Low to DRQ Low	(4 * t_{cyc}) + 30		ns
T_{1w}	DWEB High to DRQ Low	(4 * t_{cyc}) + 30		ns
T_2	DACK Low to DRQ High	(3 * t_{cyc}) + 30		ns
T_3	DACK High to DRQ Low	(3 * t_{cyc}) + 19		ns

TABLE 5-17 HOST PROTOCOL TIMING

5.5.4 DMA Port Values

Note that the following table assumes PIO = 0. DMA port inputs will be ignored if PIO = 1.

DMAOE	MRM	MASTER	PPEN	PAS	PBS	DACKA	DACKB	DRQA	DRQB	DRE	DWE	NOTE
0	x	x	x	x	x	Z	Z	Z	Z	Z	Z	(1)
1	0	0	0	0	0	reserved						
1	0	0	0	0	1	(2)	in	(3)	out	in	in	(5)
1	0	0	0	1	0	in	(2)	out	(3)	in	in	(5)
1	0	0	0	1	1	reserved						
1	0	1	0	0	0	reserved						
1	0	1	0	0	1	(3)	out	(2)	in	out	out	(4)
1	0	1	0	1	0	out	(3)	in	(2)	out	out	(4)
1	0	1	0	1	1	out	out	in	in	out	out	mirror
1	0	1	1	0	0	reserved						
1	0	1	1	0	1	(3)	out	(2)	in	out	out	stripe-B
1	0	1	1	1	0	out	(3)	in	(2)	out	out	stripe-A
1	0	1	1	1	1	reserved						
1	1	x	x	x	x	input	out	out	in			(6)

TABLE 5-18 DMA PORT VALUES

NOTES FOR TABLE 5-18.

(1) All outputs are tristate.

(2) In input mode, but input value is ignored. Input should be tied to negation value (as defined by DACAH and DRQAH).

(3) In output mode, but value output is steady negation value.

(4) Single-device DMA, as a master

(5) Single-device DMA, as a slave

(6) Mirror-restore mode. No FIFO transfers may be specified (only DPR transfers), and AUTOR must be 0.

AUTOR and AUTOD may only be used if MASTER = 1.

5.6 DATA PATH CONTROL: BUFFER INTERFACE

The Buffer Interface is designed for a wide array of memory configurations. The buffer interface supports 16 bit data bus. There is also an optional parity bit for each 8-bit bus grouping. The 11 address pins, A[0:10], support a maximum of 22 address lines, 8 Mbytes of memory in word mode. Three memory modes; normal read/writes, fast page read/writes, and standard RAS only refresh cycles are supported.

5.6.1 Buffer Manager Performance Overview

Peak buffer bandwidth is the determining element in total system throughput. Chip frequency determines the peak buffer bandwidth available and DRAM speed requirements when optimum system data throughput is desired. The WD61C96A is capable of DRAM Fast Page Mode cycles in 3 chip clock intervals (CAS low for 2 clocks, CAS high for 1 clock, then repeat). If maximum performance is required, then the DRAM speed grade must be selected to match the Fast Page Mode interval requirements for a given chip frequency. Specifically, at a chip frequency of 40Mhz (Fast Page Mode interval of 75ns) 100ns Drams must be used; at 47Mhz (FPM interval of 60 ns), 80ns DRAMs are required. Since the WD61C96A performs only wordwide buffer memory accesses, the peak available buffer bandwidth is two to three times chip frequency. At 40 Mhz, peak bandwidth is 26.6MB/s. Once peak bandwidth is determined, other system parameters can be analyzed.

Three major elements work together under the umbrella of peak bandwidth. They are: (1) Disk Port rate, (2) Desired Host Port rate; and (3) Buffer Management Overhead. The sum of these three elements is always less than or equal to peak buffer bandwidth. *Disk Port rate* is considered a fixed (non-pausible) data rate requirement of the buffer. This is because the disk is a mechanical instrument of fixed frequency. The *Host Port rate* is listed as a 'desired' value since this port has the ability to pause (temporarily suspend transfers) should the buffer bandwidth limit be reached. *Buffer Management Overhead* is a relatively fixed bandwidth requirement for a given system configuration. It includes such processes as Refresh accesses, DRAM Row changes between pages and RAS to CAS latencies for context switching (switching from Host to Disk to Refresh, etc.). Also included is Soft Error correction (OTF). OTF is by nature a once per sector occurrence at worst case and it consumes 48 clocks of buffer bandwidth at a time. The Buffer Overhead spans from 10% (no OTF) to 15% (OTF on each sector) of peak buffer bandwidth.

Armed with this information, the system designer can determine the expected performance from each port. For example, a system which has a 40Mhz clock and 5MB/s disk requires 100 ns DRAMs for maximum performance as stated above. The sustained Host Port rate is the peak buffer bandwidth minus Overhead and Disk. Assuming soft error correction occurs on each sector, the Buffer Overhead may be as high as 15% of peak bandwidth. At 40Mhz, peak bandwidth is 26.6MB/s. Buffer Overhead is (.15 x 26.6 =) 3.99MB/s. Disk requirements are 5MB/s. The expected sustained Host rate is 26.6 - 5 - 3.99 = 17.61MB/s. Note, this includes a worst case assumption of OTF on each sector. Actual performance may be much better.

In the course of the development cycle, several buffer performance simulations have been run to verify theoretical performance expectations. The results of this analysis are compiled in the table below.

FREQ (BCLK)	HOST RATE	DISK RATE	RAS TO CAS	REFRESH	OTF	SUSTAINED HOST RATE
50 MHz	20 MB/s	10 MB/s	3 x 1 CLKs	14.7 µs	yes	18.97 MB/s
47 MHz	20 MB/s	10 MB/s	3 x 1 CLKs	15.0 µs	yes	17.75 MB/s
47 MHz	20 MB/s	5 MB/s	3 x 1 CLKs	15.0 µs	yes	19.27 MB/s
40 MHz	20 MB/s	5 MB/s	2 x 1 CLKs	13.8 µs	yes	19.0 MB/s

TABLE 5-19 BUFFER MANAGER PERFORMANCE SUMMARY

5.6.2 Disk FIFO Threshold Programming

For peak Buffer Manager performance the Disk FIFO Threshold should accurately reflect the system requirements. An accurate value allows the Buffer Manager to efficiently service all requests for the buffer. Too pessimistic a value will lead to degraded Buffer performance via greater Buffer Overhead, while too optimistic a value may lead to FIFO Under/Overrun errors. To determine the proper value, the maximum Disk service latency needs to be calculated. The maximum latency occurs when the Disk FIFO goes Urgent when the Buffer Manager starts an OTF correction in the buffer. The Disk must wait until the correction is complete before it will be recognized. The threshold value needs to accommodate this delay without causing an Under/Overrun condition. To determine OTF induced latency, perform the following calculations:

1) Determine total number of Chip clocks (BCLK) required to perform OTF correction ⇒(OTFCLKS)

   OTFCLKS = 50 + 6*(CASL[1:0]) + 3*(RASH) Use decimal values. (Refer to section 4.5.3, Memory Speed, on page 55 for information on CASL and RASH.)

2) Determine total time required to perform OTF correction ⇒(CORTIME)

   CORTIME = OTFCLKS*(Chip clock period) (units should be ns)

3) Determine number of WORDS to transfer from Disk in this time ⇒(WORDXFR)

   WORDXFR = $\frac{\text{CORTIME}}{\text{period(ns)}}$ (2* RRCLK)

4) Add 1 to this value and round down to the next whole number. Call the result WORDS

5) Determine Threshold value ⇒(THRSHLD)

   THRSHLD = 16 - WORDS

The value THRSHLD is the decimal representation of the value to program in the DFTHRES register. If THRSHLD is a negative number, the current system configuration is not appropriate and prone to constant Under/Over run errors.

For systems using slow DRAMs or extended CAS low times, determine if any Host or Disk FIFO to Buffer data burst is greater than four refresh periods. If so, then the Refresh Burst latency must be included in the Disk service latency calculated above. To determine if a Refresh Burst is possible, perform the following calculation:

1) Determine Longest FIFO data Burst time ⇒ FBRST

   DRST(µS) = 32/((Peak Buffer Bandwidth $_{MB/s}$)-(Highest Port rate $_{Host\ or\ Disk\ MB/s}$))

2) Determine total number of refreshes that would have occurred in this time⇒NUMREF

   NUMREF = FBRST/(Programmed Refresh period $_{\mu S}$)

If NUMREF is equal to or greater than 4, the Refresh Burst Latency (RBL) must be added to the CORTIME value in the previous calculations. RBL = (32*Chip Clock period $_{nS}$).

5.6.3 Memory Configurations

Besides defining the width of the buffer interface bus, the user defines the size of memory. The following list identifies those configurations. The

column address width defines the configuration.

Address Width	Memory Size Address	Lines Used
8	64 K	A[0:7]
9	256 K	A[0:8]
10	1 M	A[0:9]
11	4 M	A[0:10]

The user also defines the memory refresh rate.

5.6.4 Buffer Arbitration

The Buffer Interface must arbitrate buffer accesses from the host port, Disk port, refresh control, the ECC buffer corrector, and microprocessor. The priority for this arbitration is as follows:

1) Microprocessor
2) Memory Refresh *
3) Disk Port *
4) Host Port
5) ECC Correction *

(* = Urgent requestor)

Except for the memory refresh control, all the above-mentioned buffer requesters have complete access to the full address range of the configured memory.

The buffer arbiter engine functions as the traffic controller for all data buffer accesses. Five possible requesters are recognized and prioritized as listed above. To begin an arbitration event, a request must be presented by one or more of the clients. If no client is currently being serviced, the arbitration process begins immediately. In the event that the buffer is busy with a client, the arbitration event is held off until the current client has completed its transfer. The length of the current client's transfer differs with each client. Refresh and microprocessor clients require only single cycle buffer transfers. The ECC Correction client requires three read-modify-write cycles per physical block of data. The longest arbitration latency occurs when the Disk or Host clients are active on the bus. Typically, arbitration is held off until the active client, host or Disk has: (a) filled its FIFO on buffer reads; (b) emptied its FIFO on buffer writes; or (c) the pipeline transfer counter has exhausted. By holding off arbitration in this fashion the maximum burst performance at the buffer interface is maintained.

There is an exception to the rule. Three of the five clients have the ability to issue "urgent" requests. ECC, Refresh, and Disk clients have this feature. Urgent requests have the ability to preempt the active client's burst transfer and force an immediate arbitration cycle. Catastrophic failure conditions can be avoided. Urgent requests are different for each requestor.

For example, the Disk FIFO could become dangerously low during a Disk write operation if the buffer is busy. A FIFO underrun could result if the FIFO goes empty during the Disk write. The system would need to execute some sort of retry operation. This situation is avoided when the Disk client makes an urgent request. The current buffer cycle is preempted and the FIFO is refilled. In the case of a Disk read operation, an urgent request is made when the FIFO becomes full.

The refresh logic has a different need for urgent request. The refresh logic has the ability to store up to four refresh requests. If access to the buffer has not been granted after that period of time, an urgent request is generated. When the request is granted, all four refresh cycles are performed.

All OTF ECC request are considered urgent. This ensures prompt data correction.

5.6.5 Loopback Mode

The microprocessor can access the buffer memory through the Loopback mode. This mode is used when the microprocessor needs to read or write large continuous data blocks to/from memory. In this mode the microprocessor reads or writes data to/from the Host or Disk FIFOs. This data is moved to/from the buffer via the Host or Disk DMA Buffer logic.

The microprocessor must make the following preparations for a Loopback mode. First, the

Loopback mode must be selected in the selected FIFO. When LPEN, loopback enable, is set the microprocessor can access the FIFO. LPEN must only be set if there are no active DMA operations in progress. If this bit is set in the Host FIFO, the Host Port DMA logic is disabled. If this bit is set in the Disk FIFO, the Disk Control Store is never activated. Second, the DMA pipeline must be configured (i.e., data direction). Third, the DMA must be initialized (relative start address, memory segment selected, physical Block size, and block count defined). For disk FIFO loopback, the block count must be 1. For host FIFO loopback, the block count can be 1 or greater. Fourth, the DMA is started. The microprocessor reads or writes the data to/from the FIFO. If the data is to the buffer, the microprocessor writes the even byte and then the odd byte. When the odd byte is written, the data is loaded into the FIFO. The initialized DMA pipeline recognizes that data is in the FIFO and a buffer transfer begins. This operation continues until the all data is transferred. If the data transfer is from the buffer, the DMA pipeline begins reading buffer data. The microprocessor reads the even byte and then the odd byte. When the odd byte is read, the FIFO status is changed. The DMA pipeline continues transferring data into the FIFO until the FIFO is full or the block and physical transfer count is zero.

5.6.6 Microprocessor Buffer Access

The microprocessor accesses the buffer in three different ways depending on the amount and type of data to be transferred. Typically, the Buffer Data Latch is used when single word transfers to/from the buffer are desired. The Autoincrement Access registers are used when small blocks of contiguous data, 2 to 20 words for example, are transferred. For large blocks of data one of the port FIFOs can be used in Loopback mode.

The Buffer Data Latch - Microprocessor accesses to the buffer via this port do not affect the Microprocessor Memory Address Pointer. After loading the desired memory address into the Memory Address Register, the microprocessor initiates a buffer access by reading the Odd byte location of this port. After reading the Odd, the Even can be read. To write data to the buffer the Even byte is first written and then the Odd. It is the access to the Odd that kicks off the transfer of the WORD to the buffer. To assist software error correction a special mode of this register is available. By setting the byte/word bit in the Secondary Memory Configuration register, any access to the Buffer Data Latch - Odd or Even - initiates a buffer transfer. The sequence of events to correct a byte in error is as follows:

a) The Byte/Word bit in MCFG2 register is set to 1.

b) The absolute address of the word containing the byte in error is loaded.

c) A read of the Buffer Data Latch Odd or Even is performed for the byte desired.

d) The microprocessor applies the correction mask to the byte just read and writes the byte back out to the appropriate Even or Odd of the Buffer Data Latch. At this point the WD61C96A writes the entire word back out to the buffer.

Be extremely careful when the Byte/Word bit is set. Always do a read first, then write the desired byte. This is because the WD61C96A always performs WORD access to the buffer. If a byte write is performed without first reading in the entire word, the other byte of the word is destroyed.

The Autoincrement Access Register - Microprocessor accesses to the buffer via this port cause the microprocessor memory address to point to the next word in memory for each word transferred. To read a word from memory, the microprocessor performs a read of the odd byte of the Autoincrement port. The WD61C96A latches the entire word internally and bumps the address pointer by one while delivering the odd byte to the microprocessor. The microprocessor can then read the even byte instantly. When the next word is desired, the Memory Address Pointer is already setup and the whole process can continue by reading the odd byte again. To write contiguous words to memory, the even byte is first written to the Autoincrement Access register followed by the odd byte. Upon writing the odd byte, the WD61C96A initiates a word write to the Buffer and then increments the microprocessor Memory

Address Pointer by two. The sequence is then repeated for each word written to memory.

Waitable Vs. Non-waitable Microprocessors - For waitable microprocessors, any access to the Buffer Data Latch or Autoincrement Access register which initiates a buffer transfer results in RDYB being negated until the word transfer is completed. The length of time RDYB is negated is system dependent. If the WD61C96A is busy servicing SCSI transfers as well as Disk transfers, the RDYB inactive time could be as large as 3.5µs for each word transferred. Non-waitable microprocessors use the external RDYB line as a status input to a PIO pin or have to poll the Ready status bit in the Secondary Memory Configuration register before initiating another buffer access.

5.6.7 Buffer Control Enhancements

The buffer control logic contains three major features which maximize performance and minimize microprocessor support. The features are:

1. Pipeline Host and Disk Control

   Each port, Disk and Host, is based upon a two-level pipeline architecture. This means that each port can support an active process, a DMA operation which is requesting access to the buffer, and a future process, an operation which is to be executed. The primary benefit of this architecture is reducing latency between processes. The change of active process to future process is executed by the hardware.

   Features:

   Multilevel pipeline - (Idle, Busy, and Very Busy Conditions)

   Idle indicates no processes in the pipeline

   Busy indicates a single process is in the pipeline and is active.

   VERY BUSY indicates that both a active and future process is in the pipeline.

   End of Process Interrupts - An interrupt is generated whenever there is a change of pipeline status. This occurs when the pipeline moves from Very Busy to Busy or Busy to Idle.

2. Memory Segmentation

   The Buffer Manager partitions the buffer memory. This partitioning is along memory address boundaries (8K,16K, 32K, 64K,.... 4M). These partitions are referred to as memory segments. When the microprocessor initiates a process, a memory segment is also defined. This means that all data transferred during this process shall remain within the limits of the selected memory segment address range.

   Features:

   Programmable Memory Segment Size

   Auto Memory Address Wraparound at Memory Segment Boundaries

   Memory Segment Relative Addressing

3. Buffer Manager/Host Counter Management

   The Buffer Manager and Host control maintains three counters. These counters are:

   a. Block Count (Internal)

   The internal Block Count is located in the Buffer Manager. The microprocessor loads the Block Count into the Host DMA pipeline. This count is examined by the Host DMA pipeline and the Control Store. The pipeline examines this value whenever the Physical Transfer Count, Physical Byte Count, is zero.

   b. Block Count (External)

   The external Block count is a qualified internal Block Count. The external Block Count only changes when the BUFF count increments. This occurs when a block transfer is considered "good". A good transfer is one in which no errors (buffer parity or host bus parity errors) are detected and the complete data block (if applicable) has entered or exited the buffer. The external Block Count is also reloaded when the pipeline transitions from VERY BUSY to

BUSY.

c. BUFF Count

The BUFF Count represents the difference between the number of "good" blocks which have exited and entered. A "good" transfer is one in which no errors (buffer parity or host bus parity errors) are detected and the complete data block (if applicable) has entered or exited the buffer. The BUFF count is always decremented by the Host DMA pipeline, regardless of the data direction. The decrement of BUFF Count is concurrent with the transition of the Host external Block Count. This counter is primarily used when the data blocks are exiting or entering the same Memory Segment.

4. Buffer Manager/Disk Control Store Counter Management

The Buffer Manager and Disk Control Store must maintains four counters. These counters are:

a. Block Count (Internal)

The internal Block Count is part of the Buffer Manager DMA pipeline. The microprocessor loads the Block count into the Disk DMA pipeline. This count is examined by the Disk DMA pipeline and the Control Store. The pipeline examines this value whenever the Physical Transfer Count, Sector Byte count, is zero. The Control Store examines this count whenever the Control Store JMPEN bit is active. If the block count is zero the Control Store does not jump to the Loop address.

The internal Block Count is decremented from two sources. The first source is the Control Store bits. Whenever a zero to one transition of NOXFER or BUFF is detected, the Disk module requests a block count decrement. The internal Block Count is also decremented by the Buffer Manager during a special condition of the Skip Mask operation.

b. Block Count (External)

The external Block count is a qualified internal Block Count. In a normal read/write operation the external Block Count only changes when the BUFF Count is updated. This occurs when a block transfer is considered "good". A "good" transfer is:

Complete Data Block has entered or exited the buffer

No pending ECC correction

No Buffer parity errors

— During Disk reads, if correction is necessary

— During Disk writes no errors during buffer data reads

An ES Pending Flag has been generated by the Control Store. The ESPEND flag is qualified by an active ES bit in the present control store word and any Disk-related errors. These errors can be:

— Disk port parity errors during Disk reads

— General Disk errors:

DRIVE FAULT

WRAP errors

LRC errors

Disk FIFO overrun/underrun errors

Compare Immediate errors

ID CRC errors

Compare Errors

ECC errors in 10C01 mode.

The Disk port parity errors and Disk errors are monitored in the Disk module. If these errors are detected the End of Sector Pending Flag, ESPEND, is never set.

The external Block Count is reloaded on any pipeline transition which initiates an active process. These transitions include a VERY BUSY to BUSY or IDLE to BUSY transition. A flag, DIFF flag, indicates that either of these pipeline transitions have

occurred and an outstanding ECC correction is pending.

In a Skip mask mode the external Block Count update is modified. The concurrent change of the External Block Count and the BUFF count is qualified by the condition the Skip Mask bits. When the Skip Mask bit is one, the Block and BUFF counts operate in the normal read/write operation, as described above. When the Skip Mask bit is zero, only the external block count update is changed. The External Block is only updated when (1) there are no errors and an ESPEND is active or (2) a pipeline idle condition is detected. Remember, the External Block Count represents the total number of blocks loaded into the pipeline, not the blocks in memory.

c. BUFF Count

The BUFF Count represents the difference between the number of "good" blocks which have exited and entered the buffer. A "good" transfer is:

Complete Data Block has entered or exited the buffer

No pending ECC correction

No Buffer parity errors

During Disk reads, if correction is necessary

During Disk writes no errors during buffer data reads

An ES Pending Flag has been generated by the Control Store. The ESPEND flag is qualified by an active ES bit in the present control store word and any Disk related errors. These errors can be:

Disk port Parity Errors during Disk reads

General Disk errors

DRIVE FAULT

WRAP errors

LRC errors

Disk FIFO overrun/underrun errors

Compare Immediate errors

ID CRC errors

Compare Errors

ECC errors in 10C01 mode.

The Disk port parity errors and Disk errors are monitored in the WCS. If these errors are detected, the End of Sector Pending Flag, ESPEND, is never set.

The BUFF count is always incremented by the Disk DMA pipeline when the DBUFEN is set, regardless of the data direction. In a normal read/write, the BUFF count change is concurrent with the Disk External Block Count change. The BUFF count is always decremented by the Host DMA pipeline, regardless of the data direction. The decrement of BUFF count is concurrent with the transition of the Host external Block Count. This counter is primarily used when the data blocks are exiting or entering the same Memory Segment.

In a Skip mask mode the BUFF count is not always changed. The concurrent change of the External Block Count and the BUFF count is qualified by the condition the Skip Mask bits. When the Skip Mask bit is one, the Block and BUFF counts operate in the normal read/write operation, as described above. When the Skip Mask bit is zero, the BUFF count is not changed. Remember, the External Block is decremented for every Skip Mask bit, 0 or 1.

d. Expected ID

The Expected ID reflects the next ID field on the Disk to be read. The Expected ID is maintained by the WCS. This count is incremented when the end of a data sector is reached. The Control Store bit, CHK, triggers the change in the Expected ID.

However, during a Skip Mask operation the Buffer Manager shares that responsibility.

5. Enhanced Disk Mode - Skip Mask

   The Skip Mask Mode adds the ability to jump over or skip contiguously numbered sectors without microprocessor intervention. The Skip Masks are two bytes of information which are appended to the DMA control block. These two bytes of data are then functionally combined with the Block Count. The Skip Mask bytes permit a maximum of 16 blocks to pass to/from the buffer in one pipeline transfer, therefore, the maximum block count per pipeline load is 16.

   The Block count defines how many IDs are to be spanned in a given pipeline load. The Skip Mask bytes define which IDs have associated data block transfers. The order of the Skip Mask, Skip Mask MSB bit 15, is related to the first sector to be read. A one in the Skip Mask indicates a data transfer should occur and the expected ID value should be incremented. When the Skip Mask is a zero, no data is transferred and the expected ID is still incremented. The Block counts are decremented for all Skip Mask bits, 1 or 0. The BUFF Count is only incremented when the Skip Mask is a 1.

   For example, when loading a Block Count of 07h and the Skip Masks of F7h, (Skip Mask MSB) and 00h, (Skip Mask LSB), the Disk port reads four contiguous data sectors, passing the data to/from the buffer. It passes through the next sector without a data transfer to/from the buffer and then transfers the next three contiguous sectors.

   The Skip Mask bytes can also be used to perform special Disk operations such as the SCSI Write Same operation.

6. Enhanced Disk Mode - Write Same with Skip Mask Byte Usage

   The Write Same operation is a special Disk Buffer Manager mode. In this mode, the buffer can be set to perform repeated Disk sector write operations using the same logical block data. When the Write Same mode is selected the Buffer Address Pointer, Block Count and Skip Mask bytes are used differently. At each Logical Block boundary the Buffer Address pointers are reinitialized to the starting DMA address. The Block Count is now a Logical Block Count rather than a Physical Block Count. The Skip Mask now defines the quantity of Physical Blocks there are for one Logical Block.

   Let's first make some assumptions:

   Physical Block size=512 bytes

   Logical Block size=4096 bytes

   If the microprocessor receives a request for a nine logical block Write Same operation, the DMA control block is set to the following values:

   Block Count =9

   Skip Mask-MSB =FFh

   Skip Mask-LSB = 00h

   Relative Address =000000h

5.6.8 Buffer DMA Operation Basics

Typically, the following registers are initialized after each Power On Reset:

- Memory Speed
- Memory Configuration
- Memory Segment Size

In preparation of any DMA transfer to/from the buffer, the microprocessor can initialize the following values.

- Physical Block Size
- Buff Count Initialization (if necessary)
- DMA Direction (Host and Disk)
- Special DMA Option Mode Control bits (Skip Mask Enable, Write Same.)

For each DMA operation, the microprocessor loads the WD61C96A with the following control block information:

- Memory Segment Selection
- Relative Start Address
- Block Count

Optional:

Skip Mask Bytes (Disk Only)

If the preceding registers are not reloaded, the Buffer manager reuses these values. If the Relative Address is not reloaded, the next DMA transfer continues from the last DMA absolute address.

The DMA begins by writing to the Host or Disk Start/Stop register.

Process Initiation (Start):

When the process is initiated, (DMA Start), the Buffer Manager logic preprocesses the command block. In this preprocess cycle, the relative address and selected memory segment are converted to an absolute start address. If the Relative Address is not reloaded, the next DMA transfer continues from the last DMA absolute address. In addition, a minimum and maximum memory segment address is calculated. The maximum address defines the limits of the select memory segment and the point where data is wrapped back to the beginning of the memory segment.

When a DMA operation is initiated, the WD61C96A is responsible for updating the:

- Internal/External Block Counts
- BUFF Count
- Physical Size Transfer Count
- Expected ID
- Address Pointers

and monitoring the:

- Bus Parity Errors
- ECC Errors
- Disk Errors
- FIFO Status
- Host Bus DRQ/DACK condition

5.6.9 Disk DMA Operation - Standard Mode

During all Disk DMA operations the WD61C96A maintains five important variables. These variables are the Expected ID, BUFF Count, the internal Block Count, the External (or Visible) Block Count, and the Physical Block Byte Count.

In standard DMA operation the typical steps are as follows:

1. The WCS reads and verifies the ID field.
2. If the ID is valid, a Data field read/write begins. The Control Store contains the appropriate bit combination to induce an internal block count update. (BUFF or NOXFER.)
3. If an ECC error flag is pending in a Disk read operation, the external block count changes only when the data has been corrected from the previous sector. If the data is flagged as uncorrectable, the external block count is never updated. The ECC status is not checked during a Disk write operation.

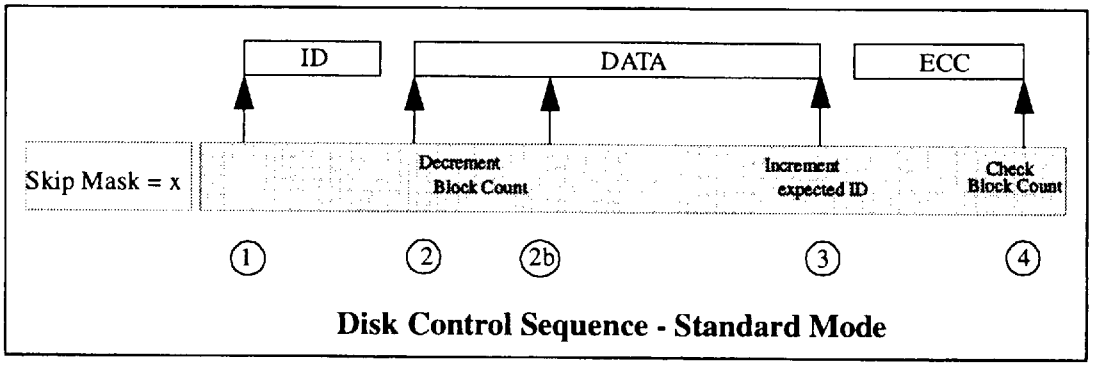

FIGURE 5-9 DISK DMA - STANDARD MODE

4. End of Data Field is reached. The expected ID is incremented at the start of the ECC field

5. End of ECC field is detected and the internal Block Count is checked. (If the block count is not zero, jump to step 1. If zero, exit to next WCS word.). The BUFF Count is incremented when the ECC for this data block is defined as "good". The internal ECC logic generates the "good" flag. In the read mode, if the data is flagged as uncorrectable, the BUFF Count and external Block Counts are not updated. In the Disk Write Mode the external Block Count and BUFF Count are updated when the true end of sector is reached.

Typically, at the end of each ECC field, the internal Block Count has been decremented and the Expected ID has been incremented. When the internal Block Count has been exhausted, the available status bytes are:

- Absolute Address points to next available address space.
- External Block Count is zero if the Data is "good."
- Expected ID points to next sector.
- BUFF Count is changed if the Data is "good."

If an ECC error has been detected and not corrected in the previous sector, the status is different. The WCS also stops at the end of the next data field read operation in the ECC on-the-fly mode. The status is as follows:

- Absolute Address points one full physical sector beyond the sector in error. In addition, the start address of the bad block is stored in the ECC Start Address Register.
- External Block Count is pointing to sector in error. (External Block Counter is updated to the microprocessor only when data transfer is considered good.

Available Buffer Status:

- Host/Disk Active Address
- Host/Disk Active Block Count
- Host/Disk Pipeline Status (IDLE, BUSY, VERY BUSY)
- Host/Disk Interrupts

5.6.10 Disk DMA Operation - Skip Mask Mode

The Disk DMA is slightly different from the host and has other features. The additional features are the Skip Mask field and the interaction with the Disk Writable Control Store. The Skip Mask defines which blocks in the Block Count have associated data transfers. For example, a block count of eight and a Skip mask field of 10101010_2 means that only four physical blocks are transferred to/from the buffer. This also means that the expected ID register is incremented eight times.

The incrementing of the expected ID register and decrementing of the Block Count are shown in the following diagram.

In a skip mask read or write operation the steps are as follows:

1. The Buffer manager examines the skip mask bit. If this bit is a one the WCS is started. The WCS reads and verifies the ID field.(If the Skip Mask is a zero, see step 4).

2. If the ID is valid, a Data field read/write begins. The Control Store contains the appropriate bit combination to induce an internal block count update (BUFF or NOXFER).

3. If an ECC error flag is pending in a Disk read operation, the external block count changes only when the data has been corrected from the previous sector. If the data is flagged as uncorrectable, the external block count is never updated. The ECC status is not checked during a Disk write operation.

4. End of Data field is reached. The expected ID is incremented at the start of the ECC field.

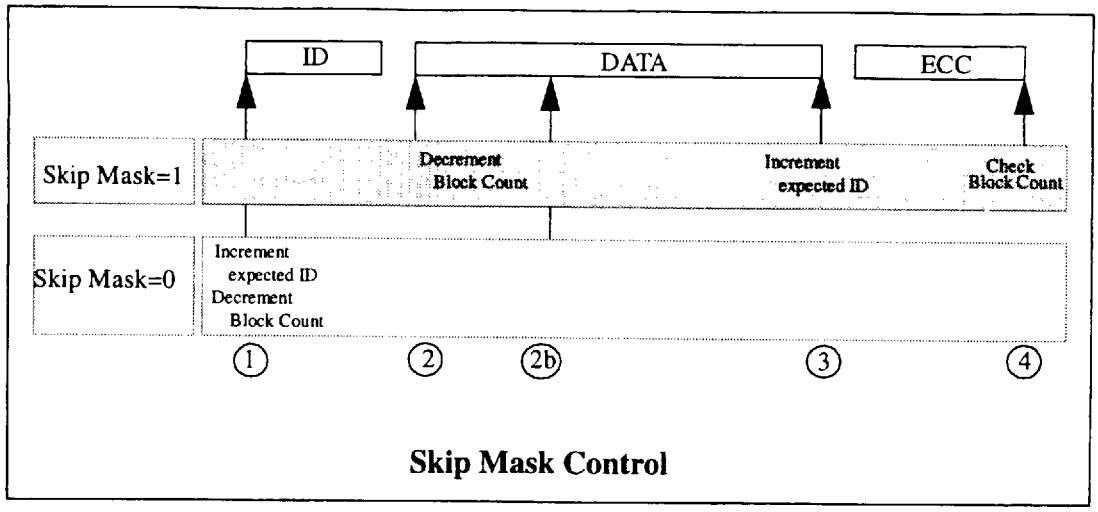

FIGURE 5-10 DISK DMA OPERATION - SKIP MASK MODE

5. End of ECC field is detected and the internal Block Count is checked. (If the block count is not zero, jump to step 1. If zero, exit to next WCS word.). The BUFF Count is incremented when the ECC for this data block is defined as "good". The internal ECC logic generates the "good" flag. In the read mode, if the data is flagged as uncorrectable, the BUFF Count and external Block Counts are not updated. In the Disk Write Mode, the external Block Count and BUFF Count are updated when the true end of sector is reached.

The Control Store is paused at the JMPEN instruction if the next skip mask is a zero. At this time the Buffer Manager logic generates a Block Count and Expected ID Change Request. The internal and external Block Count are decremented and the Expected ID is incremented. At this time the next Skip Mask bit is examined. If the bit is a zero, this step is repeated.

If the Skip Mask bit is a one in the Skip Mask field, the Buffer Manager removes the WCS Pause Request and the WCS continues at the jump address.

Typically, at the end of each ECC field, the internal Block Count has been decremented and the expected ID has been incremented. When the internal Block Count has been exhausted the available status bytes are:

- Absolute Address points to next available address space.
- External Block Count is zero if the Data is "good"
- Expected ID points to next sector
- BUFF Count is changed if the Data is "good"

If an ECC error has been detected and not corrected in the previous sector, the status is different. The WCS also stops at the end of the next data field read operation in the ECC on-the-fly mode. The status is as follows:

- Absolute Address points one full physical sector beyond the sector in error. In addition, the start address of the bad block is stored in the ECC Start Address Register.
- External Block Count is pointing to sector in error. (External Block Counter is updated to the microprocessor only when data transfer is considered good.

Available Buffer Status:

- Host/Disk Active Address
- Host/Disk Active Block Count
- Host/Disk Pipeline Status (IDLE, BUSY, VERY

BUSY)

- Host/Disk Interrupts

5.6.11 Disk DMA Operation - Write Same Mode

Enhanced Disk Mode - Write Same with Skip Mask Byte Usage

The Write Same operation is a special Disk buffer manager mode. In this mode the buffer can be set to perform repeated Disk sector write operations using the same logical block data. When the Write Same mode is selected, the Buffer Address Pointer, Block Count and Skip Mask bytes are used differently. In this mode the Buffer Address pointers are reinitialized to the starting DMA address at the end of each Logical Block boundary. The Block Count is now a Logical Block Count rather than a Physical Block Count. The Skip Mask now defines the quantity of Physical Blocks there are for one Logical Block.

Let's first make some assumptions:

Physical Block size= 512 bytes

Logical Block size= 4096 bytes

If the microprocessor receives a request for a nine logical block Write Same operation, the DMA control block is set to the following values:

Block Count= 9

Skip Mask-MSB= FFh

Skip Mask-LSB= 00h

Relative Address= 000000h

The Write Same operation is enabled when WRSAM bit in the BIFCTLD register is set.

5.6.12 Disk DMA Operation - Disk Verify Mode

There are times when the Disk sectors must be checked for valid data. In these modes the data is not transferred to the Buffer. A verify operation may require an ECC check only or an ECC check and a byte for byte comparison of the Disk data to data in the buffer. The RCMPEN (a WCS control bit in WCSCTL register), NODAT (a buffer manager control bit in BUFCTLD register), and the DDDIR (a buffer manager control bit in BUFCTLD register) define type of verification operation. In either of these modes, a standard READ control store load is used. For an example refer to section 5.3.4, Read/Write Sector without Segmentation - 10C01 Backward Compatibility Mode, on page 107. The following table defines the bit states for each respective mode.

	RCMP EN	NODA	DIR
ECC Verify Only	0	1	1
ECC and Compare	1	1	0

5.6.13 Disk Block Count, Buff Count, and ID Capture Registers (Read Operation)

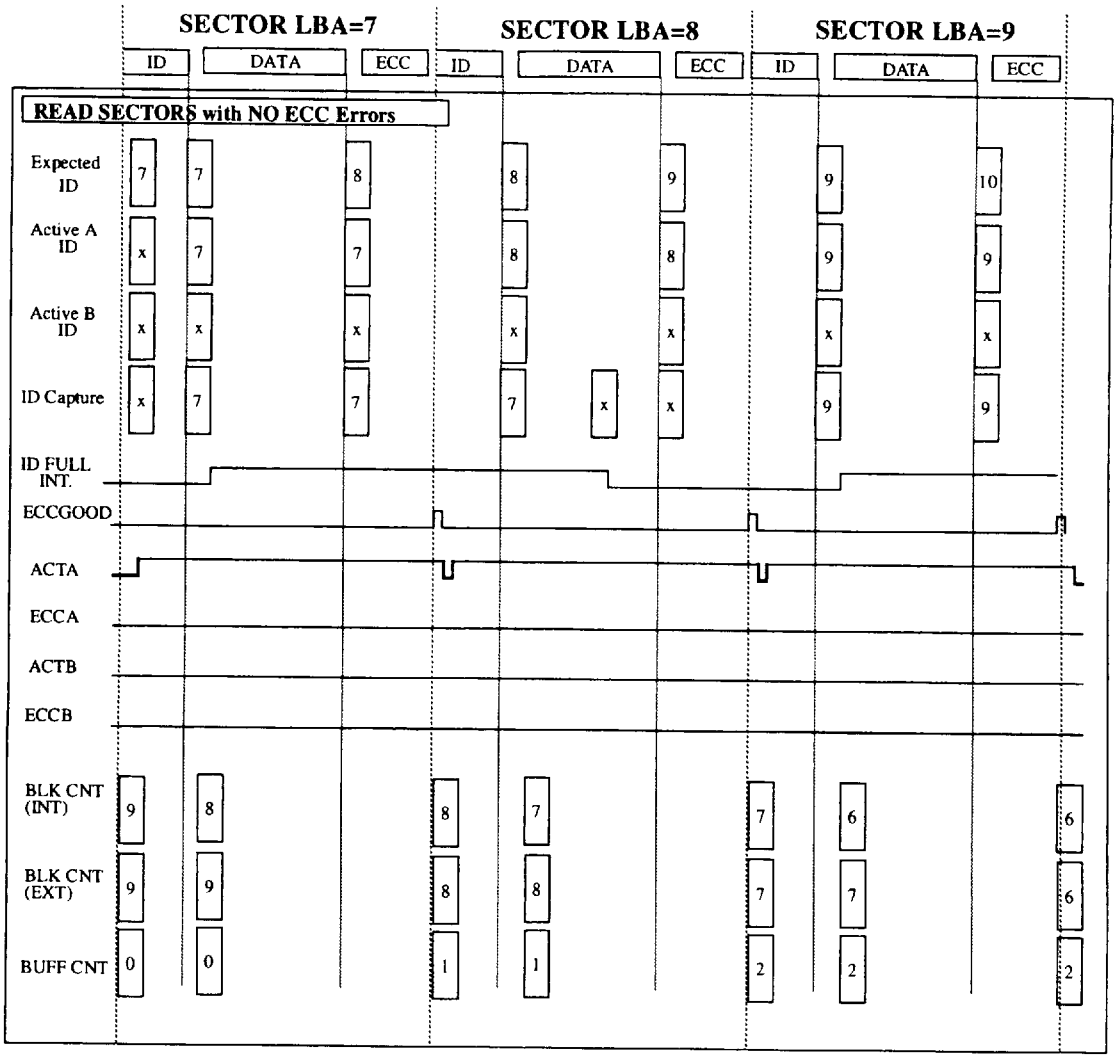

FIGURE 5-11 READ DATA WITHOUT ECC ERROR

During any Disk read/write operation, the microprocessor must be able to pinpoint the physical location of the read/write heads during error and nonerror conditions. The WD61C96A provides this data via the four following register groups:

1) Expected ID Registers

The Expected ID Registers contain the next ID to be read. The Expected ID can be in two formats. The ID can be Cylinder High, Cylinder Low, Head, and Sector or Logical Block Address. The Logical Block Address can be 3 or 4 bytes in size. The Expected ID is typically compared to the incoming Disk data during an ID read operation. If the IDs compare and the CRC is good, the expected ID is incremented at the end of the data field. See Section 4.3.20, ID/ Segment Data, on page 39.

2) Active A ID Registers

The Active A ID Register is the primary location where the ID which has just been read is stored. The Active A ID register stores as many as 8 bytes of data. If an ECC error has occurred, this register group saves the sector ID data. The next sector's ID is directed to the Active B ID register group. A flag in the Disk Status register indicates the present status of the Active A and B registers. See Section 4.3.20, ID/ Segment Data, on page 39.

3) Active B ID Registers

The Active B ID Registers are used when an ECC Error is detected. This register group now maintains the last ID data. As an example. The Active A ID register group maintains the ID of the last sector with the ECC error. A flag in the Disk Status register indicates the present status of the Active A and B registers. See Section 4.3.20, ID/ Segment Data, on page 39.

4) ID Capture Registers

The ID Capture Registers are used to locate the present position of the Disk. During an ID Read operation, the ID Capture Registers are filled. An interrupt is generated when the complete ID is stored and the ID CRC is good. The microprocessor responds by reading the ID Capture Registers and resetting the ID FULL Flag. The microprocessor can rearm the ID Capture register.

5) Block/Buff Count Capture Registers

The Block/Buff Count Capture registers store snapshots of the active conditions of the Buff Count, an up/down counter which monitors data block passing to/from the buffer, and the block count, the quantity of blocks still to be transferred. See Sections 4.5.29, Buff Count Capture Control, on page 65 and 4.5.16, Host Buff Count Capture, on page 61.

FIGURE 5-11, READ DATA WITHOUT ECC ERROR, on page 139 shows the dynamic nature of the internal Block Count, the external Block Count, and the Buff Count. The internal Block Count is the count which the Buffer Manager and WCS use to determine whether another block should be transferred. The external Block Count is the value which is captured in the microprocessor capture registers. The external Block Count is typically updated when the Buff Count is updated.

FIGURE 5-12, READ DATA WITH ECC ERRORS (NO PIPELINE CHANGE), on page 141 shows the condition of the Block and Buff Counts during a correctable ECC error condition. In this example the updating of the Block/Buff counts are delayed during LBA nine.

If the ECC is uncorrectable the external block count and the Buff Count are not updated. The result is:

The Buff Count represents only "good" data in the buffer segment

The external Block Count represents the quantity of "good" blocks in buffer in normal mode. In the Skip mode the Block Count includes the skipped blocks.

The Active A ID contains the bad sector's full ID field.

FIGURE 5-12 shows an ECC error across a pipeline boundary. In this example the Internal and External block counts are reloaded with new values at the pipeline boundary. However, the DIFF flag is set indicating that the Buff Count has a pending increment from the previous sector. Once OTF correction is completed, the Buff Count is updated and the DIFF Flag cleared. If the error is uncorrectable the Buff Count would not be incremented and the DIFF Flag would remain set. The WCS would then stop at the end of the current sector (at the FAIL instruction). Under these conditions the DIFF Flag reflects the fact that the last sector of the previous pipeline was not successfully transferred to the buffer.

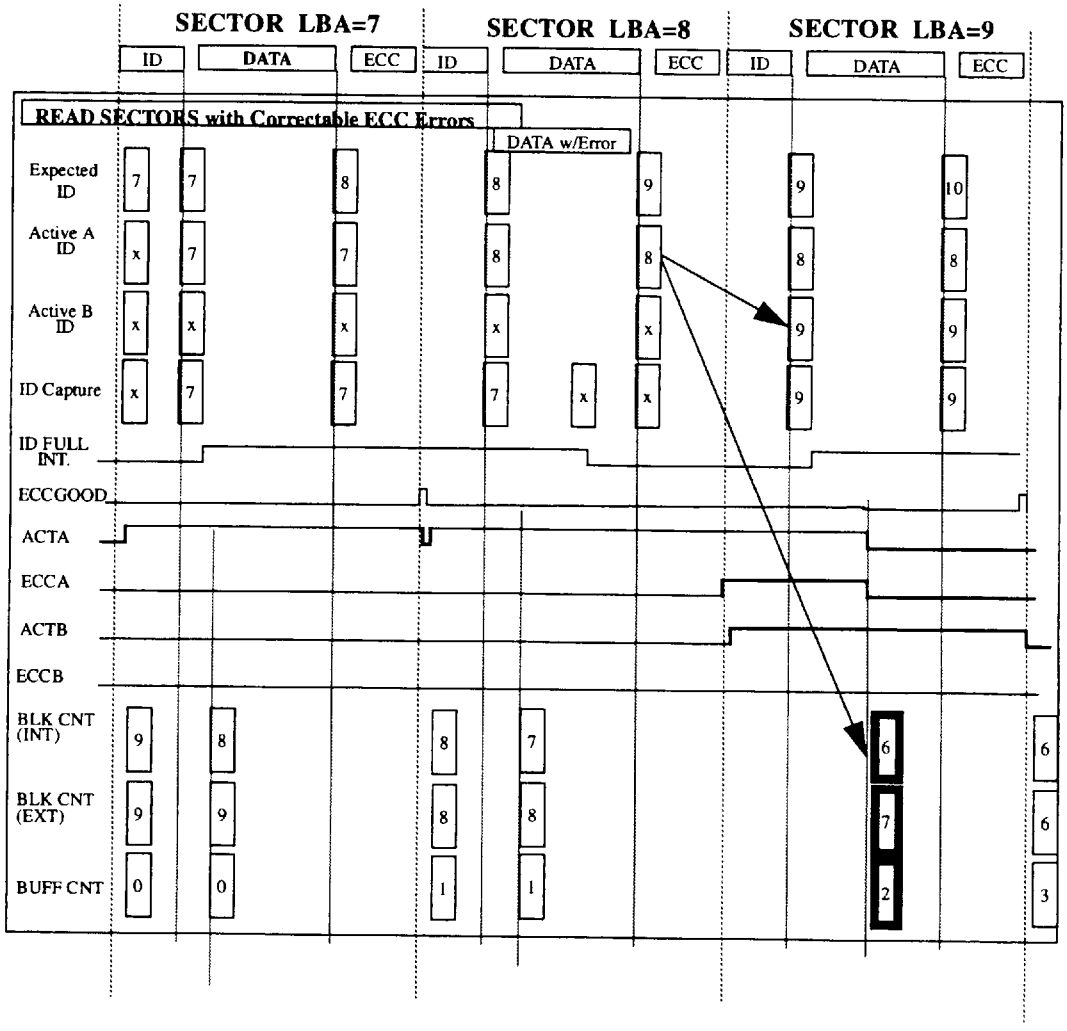

FIGURE 5-12 READ DATA WITH ECC ERRORS (NO PIPELINE CHANGE)

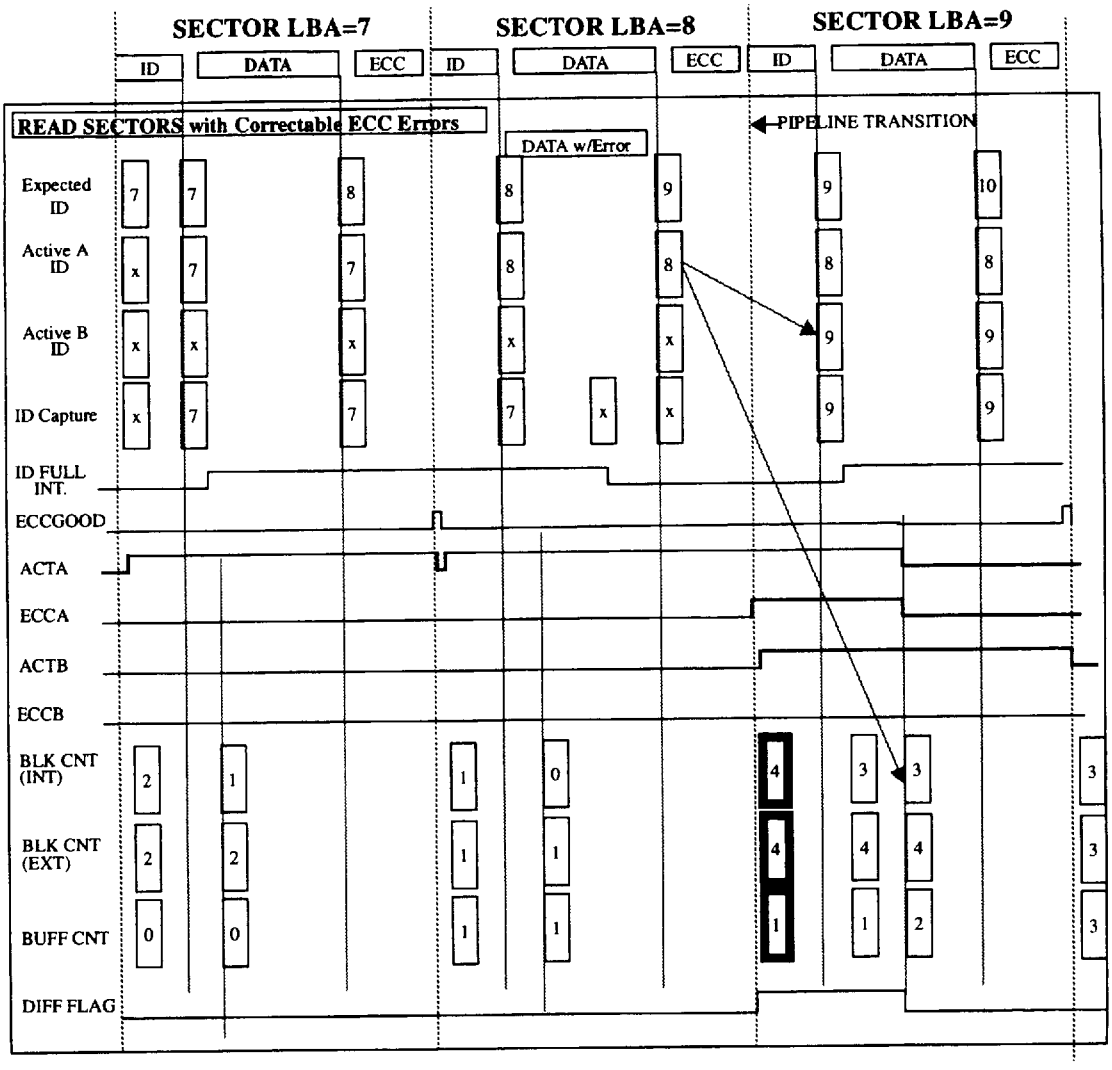

FIGURE 5-13 READ DATA WITH ECC ERRORS (PIPELINE CHANGE)

5.6.14 Disk Block Count, Buff Count, and ID Capture Registers (Skip Mask 1-No Pipe)

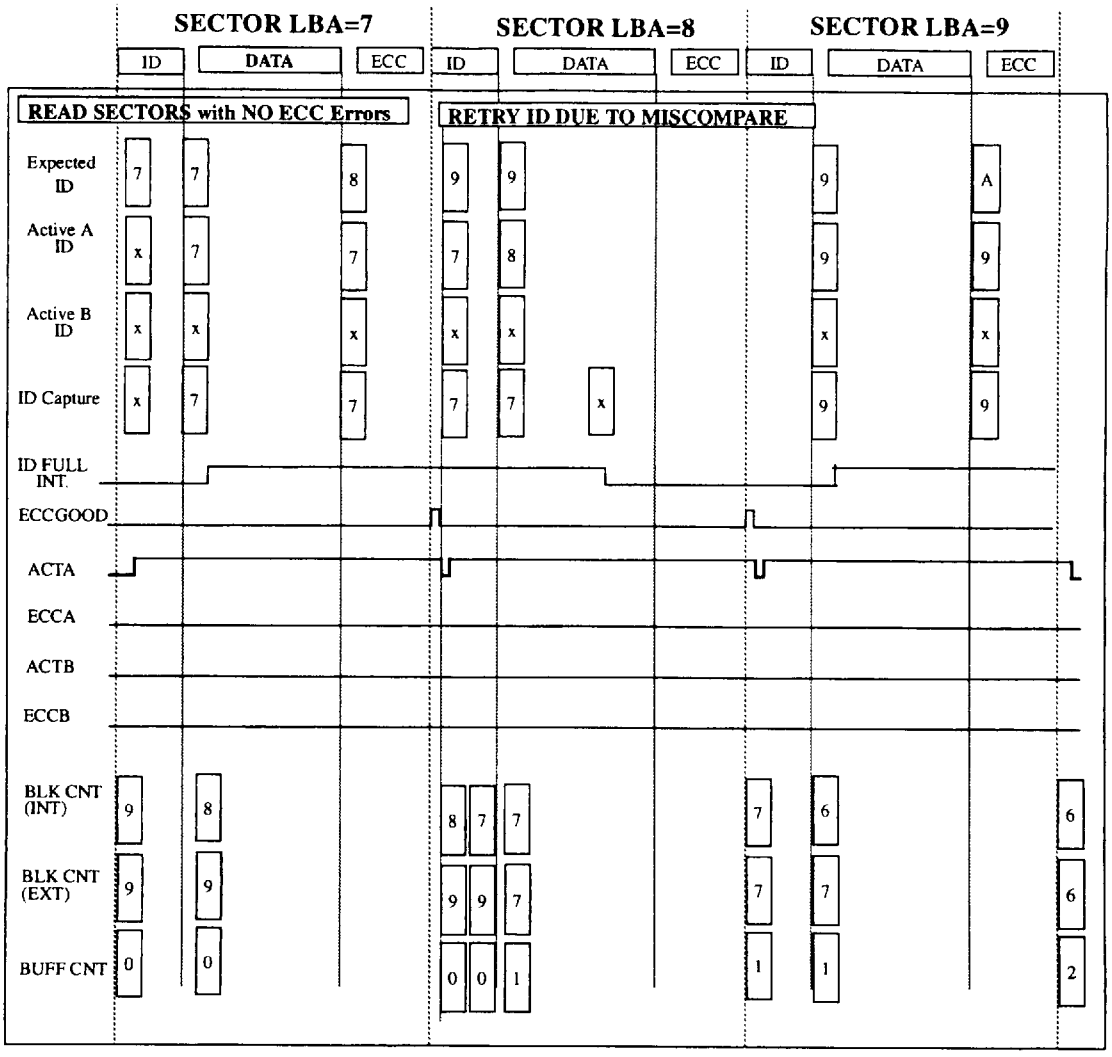

FIGURE 5-14 READ DATA W/SKIP MASK - NO ECC ERROR, NO PIPE CHANGE, SKIP MASK = 101

During any skip mask read/write operation, the microprocessor must be able to pinpoint the physical location of the read/write heads during error and nonerror conditions. The WD61C96A provides this data via the four register groups.

5.6.15 Disk Block Count, Buff Count, and ID Capture Registers (Skip Mask 2 - No Pipe)

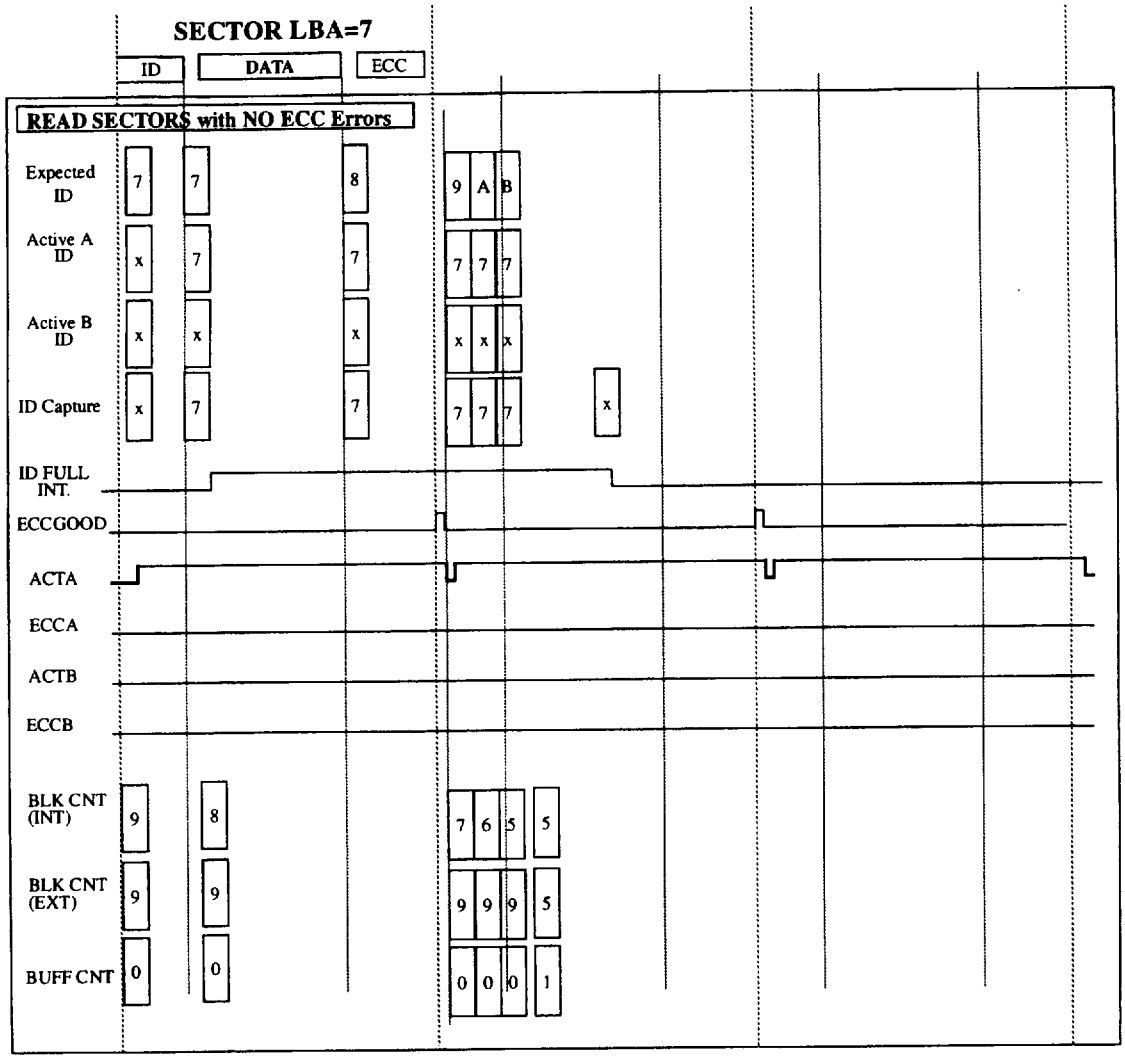

FIGURE 5-15 READ DATA W/SKIP MASK - NO ECC ERROR, NO PIPE CHANGE, SKIP MASK = 1000

During any skip mask read/write operation, the microprocessor must be able to pinpoint the physical location of the read/write heads during error and nonerror conditions. The WD61C96A provides this data via the four register groups.

5.6.16 Disk Block Count, Buff Count, and ID Capture Registers (Skip Mask 3 - Pipe)

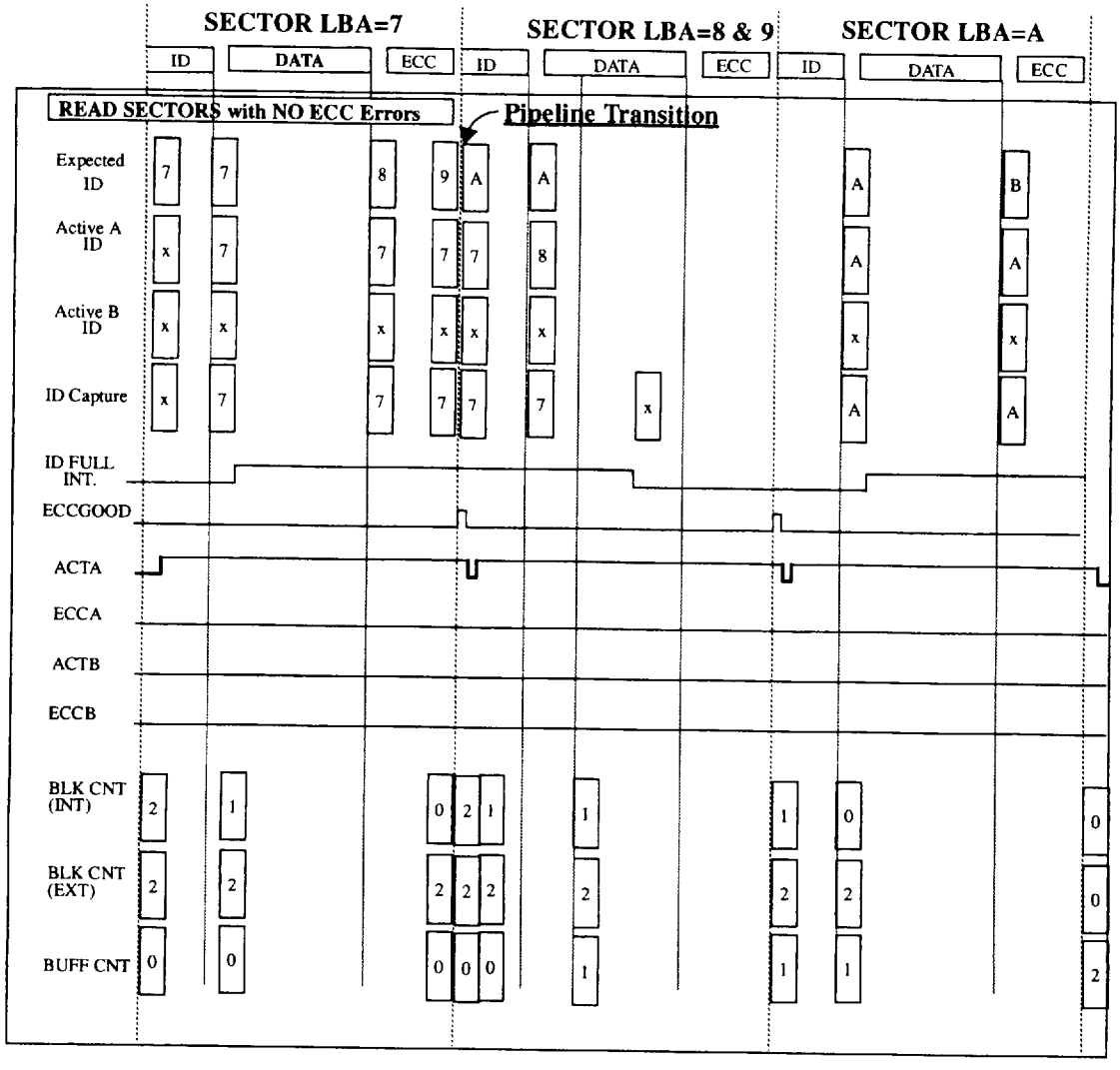

FIGURE 5-16 READ DATA W/SKIP MASK - NO ECC ERROR, PIPE CHANGE, SKIP MASK = 10 - 01

During any Skip Mask read/write operation, the microprocessor must be able to pinpoint the physical location of the read/write heads during error and nonerror conditions. The WD61C96A provides this data via the four register groups.

5.7 DATA PATH CONTROL: MICROPROCESSOR INTERFACE

5.7.1 General

The microprocessor interface supports 8-bit microprocessors with a multiplexed data/address bus. Each microprocessor access requires one cycle. For both reads and writes, the microprocessor writes the register address to the address latch by placing the address on AD[6:1] and pulsing ALE. To write data to the register, it then places the data on AD[7:0] and pulses $\overline{DWE}$. To read from the register, the microprocessor strobes $\overline{RE}$ to read the data onto AD[7:0].

The multiplexed address/data bus is suitable for most popular microprocessor-controllers such as 80196, 80186, 80188, 8051, etc.

Care should be taken when accessing the internal registers of WD61C96A, since the WD61C40 section and WD33C96 section access timings are slightly different. They are, however, compatible with commonly used processors such as 80196, 80156, 8051, etc. For more information refer to sections Section 7.1.2, PIO Read with RDYHB - CS0; Section Section 7.1.3, PIO Write with RDYB - CS0; and Section Section 7.1.4, PIO Read with RDYB - Buffer Memory Access (CS0).

For those microprocessors that do not use an ALE strobe, the indirect register mode may be used. This requires that the address register within the SCSI section must be setup correctly before any data may be accessed.

The WD61C96A also generates four potential interrupt signals (INT2:0 and RBTF) for maximum user flexibility.

5.7.2 SCSI Bus Interrupts

All SCSI interrupts have the following effect while set:

- HLR are held low.
- Writes to HLR are inhibited.
- All starts, whether due to HLR or microprocessor writes to SQADR, are inhibited.
- Microprocessor writes to SQADR will generate SREJ interrupt.

5. 7.2.1 Response to Abort / Kill (ABORTI)

If the user requires that the current operation be terminated immediately, ABORT is the most commonly used mechanism and the least destructive. FRST should only be used in conjunction with ABORT if an abort operation has failed. KILL should only be used if both ABORT and FRST have failed. ABORT and KILL set the ABORTI bit, thus, once the ABORTI bit is set, the Writable Control Store Sequencer (WCS) will not advance to the next instruction. The transfer count can be considered void only if the ABORT bit was used and successfully completed, and is not valid if either the FRST or KILL bits are used. The ABORT/FRST/KILL bits are cleared as the ABORTI interrupt is set. Whenever ABORTI is set, the High Level Response (HLR) bits are cleared, and writing to the HLR bits is inhibited. Writing to the SQADR is inhibited, and produces a Start Reject (SREJ) interrupt. ABORT and FRST does not affect BUSY and VBUSY, but KILL clears these bits, making it mandatory that the entire pipeline be reloaded.

In the event that the DMA channel is stalled, ABORT may not complete, and the use of the KILL bit may not be desirable because when the KILL bit is issued, it is possible that the SCSI synchronous offset may be non-zero. In this case, once it is determined that the ABORT operation can not complete because there is data in the FIFO that the DMA channel can not extract, the processor can issue a FRST (FIFO Reset) bit in conjunction with a second ABORT. This causes the device to end the operation only when an offset of zero is achieved. At this point the TC is not valid, but the REQ/ACK handshake remains under control. KILL should only be used after the combination of ABORT and FRST has failed to free up the device, a point that should only be reached if the SCSI bus is hung.

The following tables represent the conditions and actions associated with abortion of the SCSI section. *The italicized print represents actions appropriate to using the FRST bit. KILL operations are not known here, and are only appropriate to catastrophic failure.*

STATUS	ACTION
WCS Idle Not being (re)selected	Clear HLR; Clear ABORT; issue ABORTI
WCS idle Being selected	Clear HLR; Clear ABORT; issue ABORTI issue USEL because HLR cleared
WCS idle Being reselected	Clear HLR; Clear ABORT; issue ABORTI issue URSL, because HLR cleared
WCS executing SEL, SELA, or RSEL instruction. Arbitration not yet begun	Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI
WCS executing SEL, SELA, or RSEL instruction Arbitration in progress	If arbitration won, issue SCSIT; and start SCSI abort time out sequence; If destination responds in 200µs, the connection is completed. Halt WCS on current instruction; Clear HLR; Clear ABORT, issue ABORTI

TABLE 5-20 ABORT WHEN NOT CONNECTED TO SCSI BUS

NOTE

Neither ABORT nor KILL will complete (resulting in ABORTI) until the offset does not zero during a synchronous transfer.

STATUS	ACTION
WCS idle	Clear HLR; Clear ABORT; issue ABORTI
WCS executing non-transfer instruction	Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI

TABLE 5-21 ABORT WHEN CONNECTED ON SCSI BUS AS TARGET

STATUS	ACTION
WCS executing transfer in *Do not issue FRST unless Slave DMA stalled*	Request no more data from DMA or DPR ports; Wait for outstanding ACK pulses from SCSI port; Halt transfer after SCSI port empties FIFO; Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI
WCS executing transfer out *Issue FRST if DMA stalled*	Request no more data from SCSI port; wait for outstanding ACK pulses from SCSI port, Halt transfer after DMA port empties FIFO; Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI

TABLE 5-21 ABORT WHEN CONNECTED ON SCSI BUS AS TARGET (Continued)

STATUS	ACTION
WCS idle	Clear HLR; Clear ABORT; issue ABORTI
WCS executing non-transfer instruction	Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI
WCS executing transfer in *Issue FRST if DMA stalled*	Acknowledge last byte and hold ACK asserted; Allow DMA port to empty FIFO; Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI
WCS executing transfer out *Do not issue FRST unless Slave DMA stalled*	Request no more data from DMA or DPR ports; Allow SCSI port to empty FIFO; Acknowledge last byte/word and stop issuing ACKS; Halt WCS on current instruction; Clear HLR; Clear ABORT; issue ABORTI

TABLE 5-22 ABORT WHEN CONNECTED ON SCSI BUS AS INITIATOR

Microprocessor use of ABORT

- Microprocessor asserts ABORT.
- Microprocessor waits for ABORTI interrupt, which indicates that the WCS has halted.
- If ABORTI interrupt does not occur within a predefined time, issue ABORT and FRST.
- If still no ABORTI, issue a KILL.
- Typically, the Microprocessor programs the WCS to do one of the following:

  a. Assert ATN and then finish the transfer:

     WCS executes AATN instruction.

     WCS branches to the data-transfer instruction it was executing previously.

  b. Assert ATN and then expect another SCSI bus phase from the target:

     WCS executes AATN and NACK.

     WCS branches to instruction(s) expecting other SCSI bus phases.

  In either cases, the initiator may be forced to complete the entire transfer before the target changes phase.

5.7.2.2 Response to Parity Error (PARE)

NOTES

Any time a transfer halts, if the SCSI section is a bus-master, $\overline{DRE}$/$\overline{DWE}$ pulses stop after the FIFO is flushed. If the SCSI section is a bus-slave, DRQ is negated.

In the initiator case, the SCSI section always stops with ACK asserted so that the microprocessor can set ATN and then resume the transfer.

Whenever PARE = 1, HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited, and all writes to SQADR are inhibited.

The rising edge of PARE causes the WCS to halt, if running.

Initiator

Asynchronous transfer-in (SCSI bus parity error): FIFO or DPR transfer

1. Byte with parity error is not stored in FIFO. ACK is held asserted; PARE is set.

Asynchronous transfer-out (DMA bus parity error; FIFO transfer only):

Bus-Master

1. Byte with parity error is not stored in FIFO; $\overline{RE}$ may be asserted one more time but data will not be stored in FIFO. ACK is held asserted.
2. PARE is set.

Asynchronous transfer-out:

Bus-Slave

1. Byte with parity error is not stored in FIFO; ACK is held asserted. DRQ is negated. If another byte is written into SCSI section, it is not stored in the FIFO.
2. PARE is set.

Synchronous transfer-in (SCSI bus parity error): FIFO or DPR transfer

1. Byte with parity error is not stored in FIFO.
2. ACK is asserted and held asserted. PARE is set. Any REQ pulses received are logged to keep track of REQ/ACK offset, but any associated data is ignored.

Synchronous transfer-out (DMA bus parity error; FIFO transfer only)

Bus-Master

1. Byte with parity error is not stored in FIFO. ACK is asserted and held asserted. $\overline{RE}$ may be asserted one more time but data will not be stored in FIFO. Any REQ pulses received are logged to keep track of REQ/ACK offset.
2. PARE is set.

Bus-Slave

1. Byte with parity error is not stored in FIFO. ACK is asserted and held asserted. DRQ is negated. If another byte is written into

SCSI section, it is not stored in the FIFO. Any REQ pulses received are logged to keep track of REQ/ACK offset.

2. PARE is set.

Target

Asynchronous transfer-out (SCSI bus parity error): FIFO or DPR transfer

1. Byte with parity error is not stored in FIFO. PARE is set.

Asynchronous transfer-in (DMA bus parity error; FIFO transfer only)

Bus-Master

1. Byte with parity error is not stored in FIFO; RE may be asserted one more time but data will not be stored in FIFO.
2. PARE is set.

Bus-Slave

1. Byte with parity error is not stored in FIFO; DRQ is negated. If another byte is written into SCSI section, it is not stored in the FIFO.
2. PARE is set.

Synchronous transfer-out (SCSI bus parity error): FIFO or DPR transfer

1. byte with parity error is not stored in FIFO.
2. PARE is set. Any ACK pulses are logged to keep track of REQ/ACK offset, but data is not stored.

Synchronous transfer-in (DMA bus parity error; FIFO transfer only)

Bus-Master

1. Byte with parity error is not stored in FIFO. RE may be asserted one more time but data will not be stored in FIFO. Any ACK pulses received are logged to keep track of REQ/ACK offset.
2. PARE is set.

Bus-Slave

1. Byte with parity error is not stored in FIFO. DRQ is negated. If another byte is written into SCSI section, it is not stored in the FIFO. Any ACK pulses received are logged to keep track of REQ/ACK offset.
2. PARE is set.

5. 7.2.3 Response to ATNI (Target Mode)

Whenever ATNI = 1, HLR is cleared, writes to HLR are inhibited, HLR starts are inhibited, and all writes to SQADR are inhibited. The rising edge of ATNI causes the WCS to halt, if running, on the current instruction before the stop/jump test is performed.

WCS Idle

1. If ATN assertion edge occurs, assert ATNI.
2. If ATN is already asserted when WCS stops, take no more action (ATNI should already have been set).

Non-data-phase transfer in progress on SCSI bus

ENATN = 0 (ATNHD is ignored)

1. Ignore both ATN assertion edge and ATN level.

ENATN = 1 (ATNHD is ignored)

1. ATN is sampled at end of current instruction (after transfer has completed, before stop/jump is tested.
2. If ATN is asserted, assert ATNI.

Data-phase transfer in progress on SCSI bus

ENATN = 0 (ATNHD is ignored)

1. Ignore both ATN assertion edge and ATN level.

ENATN = 1, ATNHD = 0

1. ATN is sampled at end of current instruction (after transfer has completed, before stop/jump is tested)
2. If ATN is asserted, assert ATNI.

ENATN = 1, ATNHD = 1 (asynchronous transfer-in)

FIFO transfer (byte or block transfers)

1. ATN is sampled each time ACK negation

edge is received.

2. If ATN is asserted,
   a. request no more data from DMA bus. (microprocessor must stop writing to FIFO) --note: may halt in middle of physical/logical block.
   b. wait for FIFO to empty.
   c. assert ATNI.

DPR transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: will halt in middle.
   b. assert ATNI.

ENATN = 1, ATNHD = 1 (async. transfer-out)

FIFO transfer (byte or block transfers)

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: may halt in middle of physical/logical block
   b. wait for FIFO to empty (microprocessor must remove bytes if DMA not in use)
   c. assert ATNI.

DPR transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: will halt in middle.
   b. assert ATNI.

ENATN = 1, ATNHD = 1 (synchronous transfer-in; byte or block transfers)

FIFO transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. request no more data from DMA bus. -- note: may halt in middle of physical/ logical block/
   b. wait for FIFO to empty (send additional REQ pulses)
   c. wait for outstanding ACK pulses to be received.
   d. assert ATNI.

DPR transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: will halt in middle of transfer.
   b. wait for outstanding ACK pulses to be received.
   c. assert ATNI.

ENATN = 1, ATNHD = 1 (sync. transfer out; byte or block transfers)

FIFO transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: may halt in middle of physical/ logical block.
   b. wait for outstanding ACK pulses & data to be received.
   c. wait for FIFO to empty out DMA port.
   d. assert ATNI.

DPR transfer

1. ATN is sampled each time ACK negation edge is received.
2. If ATN is asserted,
   a. do not assert REQ -- note: will halt in middle.
   b. wait for outstanding ACK pulses and data to be received.
   c. transfer data into DPR.

d. assert ATNI.

If ATNHI is set instead of ATNHD, the transfer does not halt immediately. Instead, it continues handshaking with the initiator until it is complete or the initiator stops. The real data transfer does not take place, however. There is no need to fill / empty FIFO to continue the protocol.

5. 7.2.4 Response to STOPWCS, INTWCS, BUSYI, VBUSYI

- If INTWCS, the SQINT register is loaded with the value in the SQADR.
- The appropriate interrupt bit is set.
- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited
- All writes to SQADR are inhibited
- If STOPWCS, the WCS halts; else the WCS continues operation.

5. 7.2.5 TCOVR

- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited.
- All writes to SQADR are inhibited
- If a FIFO transfer is in progress, the transfer continues until TC = 0; the pipeline is not shifted.
- BUSY and VBUSY are cleared
- The WCS halts, if running.
- TCOVR is set.

To recover from TCOVR, the microprocessor must do a write to the CTL register with both LDTC and LDTCL set. This will flush the pipe. Then, the microprocessor can write valid transfers to the TC pipeline.

5. 7.2.6 Response to SCSIT, LRCE, TCUND, SOE, FIFOE, USEL, URSEL, UPHAS

- The appropriate interrupt bit is set.
- Transfer halts immediately, if any underway
- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited.
- All writes to SQADR are inhibited
- If SCSIT, the SCSI section tristates all SCSI bus outputs
- The WCS halts

5. 7.2.7 Response to RSTINT

- RSTINT is set
- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited
- LLR are cleared.
- INT and RSTF asserted (if not masked).
- All SCSI bus outputs are tristated.
- Transfers on the DMA port are halted (if any)
- The WCS halts (if running).

5. 7.2.8 Response to SREJ

- SREJ is set.
- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited.
- All writes to SQADR are inhibited
- WCS continues running

5. 7.2.9 Response to UDISC

- UDISC is set.
- Transfer halts immediately
- LLR are cleared
- HLR are cleared; writes to HLR are inhibited; HLR starts are inhibited
- All writes to SQADR are inhibited
- The SCSI section tristates all SCSI bus outputs
- The WCS halts, if running.

5. 7.2.10 Flow of Data through the SCSI Section

All transfers to/from the SCSI bus flow through the FIFO. DPR transfers use the FIFO as a buffer between the DPR and SCSI bus.

5.7.3 Disk Interrupt Structure

The WD61C96A has two interrupt output pins. The interrupts are organized so a user can operate in either a single or dual interrupt configuration. This allows the user to externally prioritize the interrupts to the microprocessor.

In general, all interrupts converge into the INT0 and INT1 pins through the Interrupt Summary 1 and 2 registers. When this interrupt is active, the microprocessor can read the Interrupt Summary1 or 2. The Interrupt Summary 1 or 2 defines the general source of the interrupt. These interrupts are grouped into the four categories. They are the Host Buffer, Disk Buffer, Disk Sequencer, and Disk Error. Each interrupt bit within this Interrupt Summary 1 and 2 is maskable. This means that the microprocessor can easily filter the interrupts that are considered. However, the mask bits do not clear the interrupts, but only filter the INT0 and INT1 outputs. The interrupt can only be cleared at the source of the interrupt. The microprocessor must write a one to the interrupt source register to clear the interrupt.

Note that interrupt bits are set in all interrupt registers whether they are masked or not, but only the interrupt output (INT0 and INT1) generation is masked off by the corresponding interrupt mask bits in the interrupt mask registers.

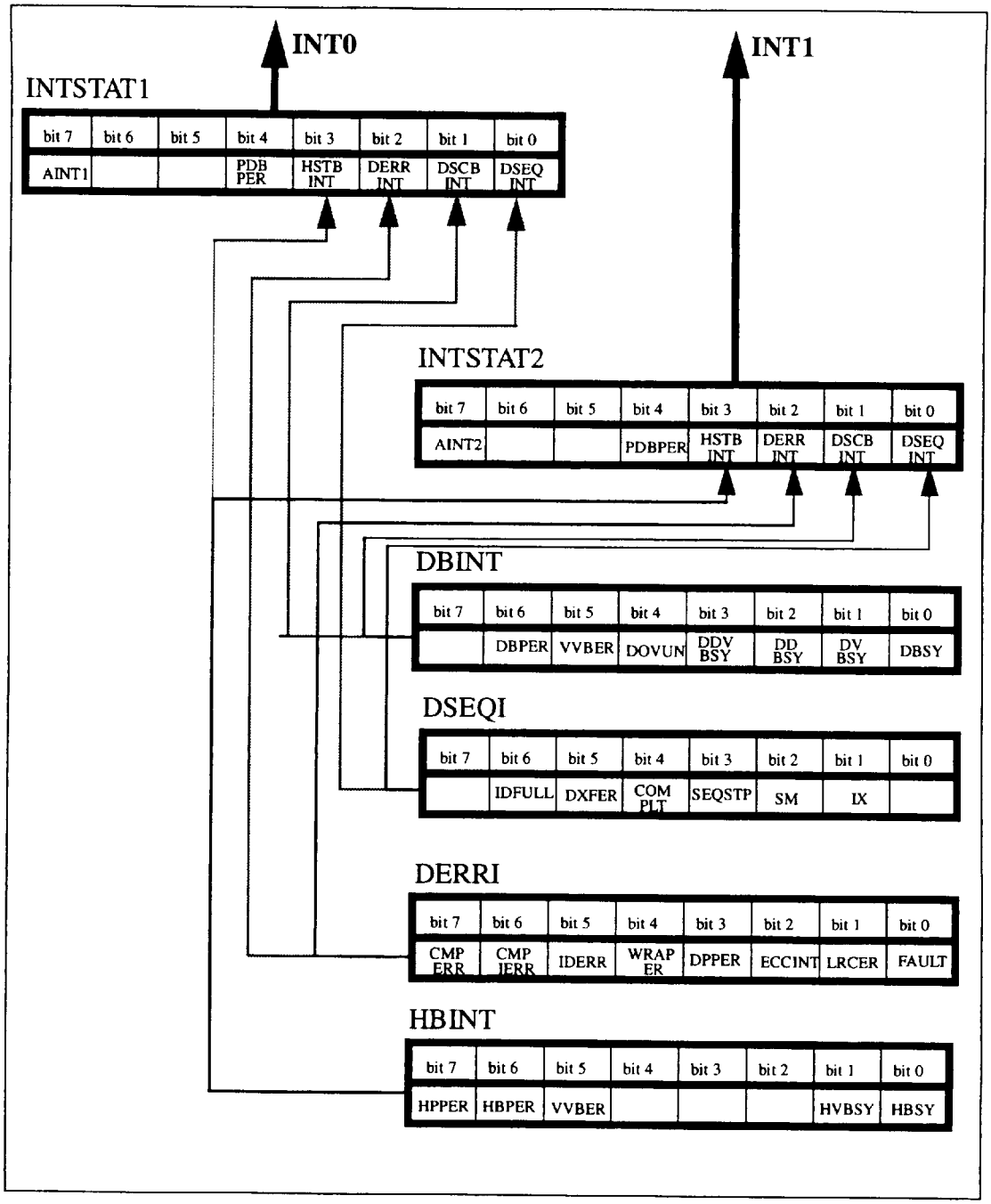

FIGURE 5-17 INTERRUPT REGISTER STRUCTURE

5. 7.3.1 Interrupt Control

The WD61C96A permits independent control of the interrupt mask and interrupt clear operation. The general interrupt structure is presented in FIGURE 5-18.

The generation of an active INT0 or INT1 output pin is accomplished by generation of the internal flag and the mask control. An Individual Interrupt Status is set whenever the right combination of conditions exists. The individual interrupt status can be read by the microprocessor. However, the microprocessor is not flagged of the event until the masks are properly set. There are two levels of masks which must be set to pass the Interrupt Status to the Interrupt output pins. First, there is the Individual Interrupt Mask Register whose bits map one-to-one with their respective interrupts. The next level of mask is the Interrupt Summary Mask. Interrupts are assigned a group by function, (For interrupt group definitions, refer to FIGURE 5-17.) and these groups are then presented to the Interrupt Summary registers. The Interrupt Summary Mask registers then filter what interrupt groups reach the Interrupt Output pins. In a single interrupt pin configuration, all masks in the Interrupt Summary 1 register, INTSTAT1 should be set. In a two interrupt pin configuration, the mask registers can be used to steer the interrupt groups to the output interrupt pins.

Once an interrupt is generated to the microprocessor, INT0 or INT1 is active. The microprocessor must clear the interrupt at the original source by writing a one to the corresponding bit in the interrupt register. This is done by writing a one to the respective individual interrupt status bit. Remember, resetting the interrupt mask, individual or group, bit does not clear the interrupt flag.

Note that interrupt bits are set in all interrupt registers whether they are masked or not, but only the interrupt output (INT0 and INT1) generation is masked off by the corresponding interrupt mask bits in the interrupt mask registers.

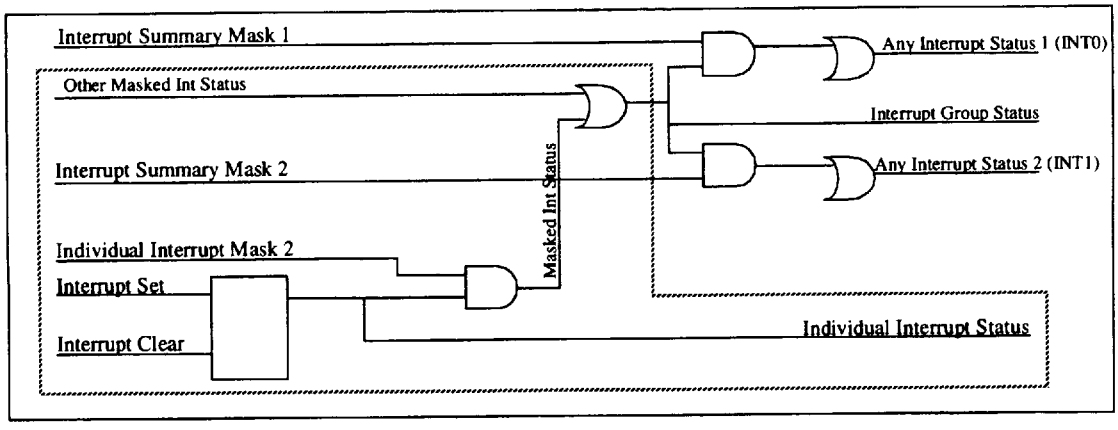

FIGURE 5-18 INTERRUPT FLAG/SUMMARY CONTROL

5. 7.3.2 Interrupt Generation

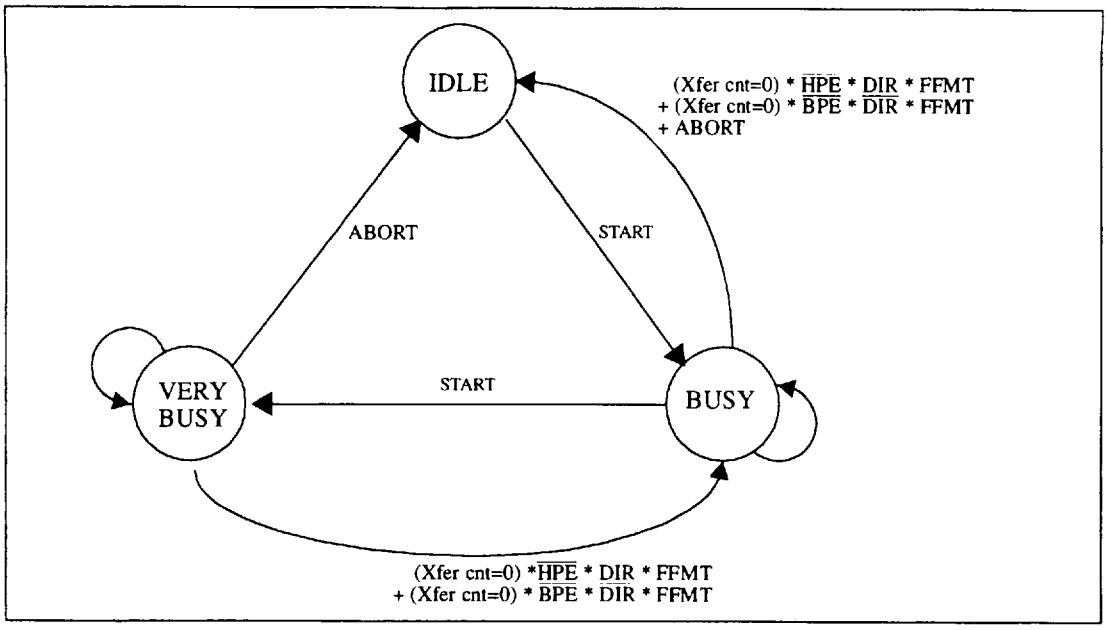

FIGURE 5-19 HOST PIPELINE CONTROL

Host Interrupts - Normal Condition

There are three possible interrupts which can be generated by the Host. Two of these interrupts are considered normal interrupts. These interrupts originate from the Host Buffer Manager control. The Host DMA pipeline consists of three possible states: Idle, Busy, and Very Busy. The IDLE state indicates no activity is expected of the pipeline. The Busy state indicates that a DMA process is active but no future process is required. A Very Busy condition exists when a DMA process is active and a future process is pending. In general, an interrupt is generated whenever the DMA pipeline control changes state and no parity errors are outstanding. The conditions for a state change are different depending upon the direction of the DMA transfer. The above figure describes these conditions and changes. These conditions are reflected in the Very Busy and Busy interrupts in the HBINT register. The definitions for the signal in the figure are as follows:

Xfer cnt = DMA transfer count which include the physical count and block count

START = Start pulse from the DMA control access register

DIR = This bit defines the DMA direction. (DIR = High; Write to Buffer)

HPE = Host Parity error

BPE = Buffer Parity Error

FFMT = FIFO empty status

ABORT = Microprocessor writes to the pipeline STOP bit

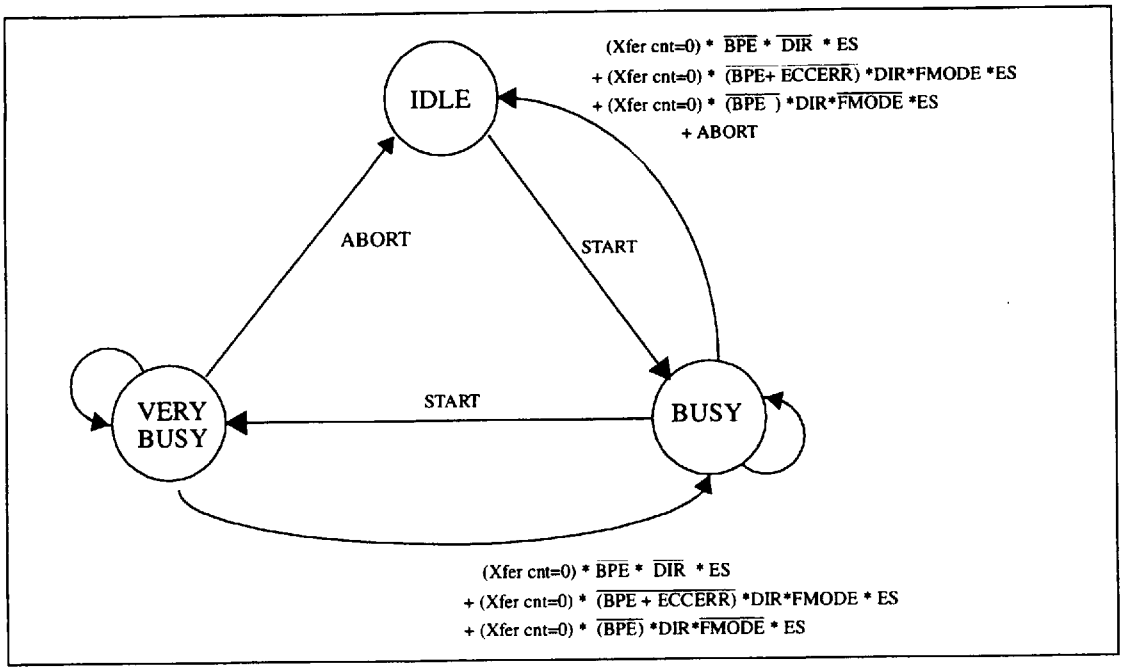

FIGURE 5-20 DISK PIPELINE CONTROL

Host Interrupts - Error Condition

The third interrupt is generated due to error conditions. This error occurs whenever a parity error is detected on the Host or Buffer buses or a Very Very Busy interrupt is generated. A Host or Buffer Parity Error interrupt is generated immediately upon detection of a parity error. A parity error causes the Host Buffer Control logic to pause. *No Very Busy or Busy interrupts are generated.*

Disk Buffer Manager Interrupts - Normal Condition

The Disk Buffer interrupts are very similar to the Host Buffer interrupts. The Disk Buffer manager control logic uses the basic three state pipeline control, Very Busy, Busy, and Idle. The difference is the Disk pipeline control has more conditions for qualifying a pipeline change. There are also delayed versions of the Very Busy and Busy interrupts which are further qualified with the ECC error. In general, the pipeline change monitors buffer parity errors, WCS End of Sector Flag, and ECC errors (when enabled by FMODE). *Note that the pipeline in FMODE mode does not change state if an ECC error flag is pending.*

There are two types of interrupts that can be generated when a pipeline change of state occurs. They are immediate interrupts or delayed interrupts. The *immediate interrupts* are generated upon immediate detection of a pipeline state change. These are flagged as Very Busy and BUSY interrupts. The second group of interrupts are the *delayed interrupts.* This interrupt is generated after a pipeline change if there is no pending ECC correction. If an ECC correction is pending, this interrupt is generated when this correction is successfully completed. In FMODE if an ECC error is uncorrectable, no Very Busy or BUSY interrupts are generated. These interrupts are called the Delayed Very Busy and Delayed Busy interrupts. FIGURE 5-20, DISK PIPELINE CONTROL describes the Disk Buffer manager control logic. Below are the signal definitions for the above figure:

Xfer cnt = DMA transfer count which include the physical count and block count

START = Start pulse from the DMA control access register

DIR = This bit defines the DMA direction. (DIR = High; Write to Buffer)

BPE = Buffer Parity Error

ECC = Any type of ECC error.

ERROR

FMODE = FMODE, when set, adds ECC status to pipeline change.

WDMODE = WD WCS data segmentation mode

ES = End of Sector Pending

ABORT = Microprocessor writes to the pipeline STOP bit

If an error is detected the Very Busy and Busy interrupts are not generated. In their place, an error interrupt is generated.

Disk Buffer Manager Interrupts - Error Conditions

As mentioned earlier, the Very Busy and Busy interrupts are not generated when any of the Disk related errors have occurred. If a Buffer bus parity error occurs, the DBPER is set in the Disk Buffer Interrupt register.

An ECCINT interrupt is generated when an uncorrectable ECC error is detected.

A Very Very Busy interrupt is generated whenever a START is requested in a Very Busy state.

Disk Port Interrupts - Normal Conditions

The Disk Port generated interrupts are independent of Buffer management logic. These interrupts are used to flag the microprocessor of the status of the Control Store or events on the Disk port. Control Store interrupts encompass the:

Sequencer Stop Interrupt

ID FULL Interrupt

Data Transfer Interrupt

The Sequencer Stop, SEQSTP, Interrupt indicates that the Control Store has reached a stop instruction. This interrupt generally occurs in the same time frame as the BUSY interrupts. This is due to the fact that the Control Store usually reaches the STOP instruction when the last data byte of the block is transferred and the block count is zero. The Disk pipeline generates an interrupt when the transfer count has expired.

The ID FULL interrupt occurs when the ID Capture register has stored a complete ID field and the CRC is valid. This interrupt occurs at the end of the ID field. The microprocessor must clear the interrupt and rearm the ID Capture logic before another interrupt is generated.

The Data Transfer, DXFER, interrupt occurs when the Control Store begins a BUFF or NOXFER instruction.

Disk port interrupts also encompass the:

COMPLT	Complete Interrupt
SM	Sector Mark Detect
IX	Index Mark Detect

These three interrupts are generated when their respective input pins are active.

Disk Port Interrupts - Error Conditions

In general, the following internal error flags are set as soon as the error is detected. However, the following interrupts are not generated until a WCS FAIL bit is detected. The Control Store examines the following errors only when the WCS FAIL bit is set in the active control store word. When the following error interrupts are generated and the Control Store aborts, the SEQSTP interrupt is also generated.

WRAPER	WRAP control errors
DPPER	Disk Port Parity Errors
LRCER	LRC Error
IDERR	ID CRC errors
CMPERR	Byte Compare Errors
CMPIERR	Compare Immediate Errors

The following interrupts are generated when the error is detected. These errors also cause the

Control store to abort at the FAIL instruction.

DOVUN = Disk FIFO Overrun/Underrun Errors

ECCINT = ECC Error

DBPER = Disk Buffer Parity Error

FAULT = Drive Fault Errors

5.8 DATA PATH CONTROL: DISK INTERFACE

The disk port supports a parallel data path and is controlled by a 32-it writable control store. Using an 8-bit disk bus plus parity, the WD61C86A can achieve a disk transfer rate of 10 Mbytes.

The integrated Reed-Solomon error correction logic and defect skipping feature maximizes disk capacity while minimizing sector reallocation.

5.9 DATA INTEGRITY: ECC

The data fields are protected using the interleaved Reed-Solomon code operating on 8-bit symbols. The WD61C96A also has the option to include a CRC to improve the miscorrection characteristic. Both the CRC Calculator and the Composite Syndrome Generator are initialized to be zeros.

The on-the-fly Corrector is part of the Disk Controller logic. The format is degree 6 with a three-way interleaved, Reed-Solomon ECC and an optional 4-byte noninterleaved CRC. The on-the-fly Corrector consists of four primary elements. (Refer to FIGURE 5-21, ECC ARCHITECTURE). They are the Reed-Solomon Encoder/Syndrome Generator, CRC Calculator/ Checker, Relative Offset/Mask Generator, and the Buffer Corrector

During write operations, the Encoder/Syndrome Generator and the Calculator monitor the outgoing data and calculates the CRC bytes and the ECC bytes which also includes the CRC. At the completion of the CRC calculation, these bytes are written to the disk. After the ECC encode is complete, the inverted ECC checkbytes are written to the disk.

During read operations, the Encoder/Syndrome Generator and Calculator monitor the incoming data. The Encoder/Syndrome Generator computes the composite syndromes while the CRC Calculator performs its calculation. The check bytes are inverted when read. If the results of the Generator and/or Calculator are non-zero then on-the-fly Corrector commences the Relative Offset/Mask Generator.

After the composite syndromes and the CRC bytes are loaded into the O/M Generator, single burst error trapping proceeds. If the single burst error is distributed such that a maximum of 1 byte per interleave is in error, a relative offset and mask is generated for each interleave. The data mask and relative offset are passed to the Buffer Corrector. The Buffer Corrector creates an absolute buffer address for the bad data. This module also interfaces with the data buffer arbiter. The arbiter sets up the proper timing on the buffer data bus to manipulate the bad data in the buffer.

FIGURE 5-22, ERROR CORRECTION TIME LINE, identifies the general sequence of ECC correction with reference to the sector format. At step 1, the initial sector buffer address is stored. This address is used when correction is necessary. At step 2a, syndrome generation begins. At step 2b, the syndrome is passes to the corrector. The correction occurs during the next ID data sector transfer. At step 3, the correction is complete

Since the ECC logic can only correct one on-the-fly burst, the microprocessor must get involved when the error exceeds this limit. (FIGURE 5-23, MICROPROCESSOR CONTROL, defines any microprocessor involvement during a read operation. Microprocessor involvement is highlighted and boxed.)

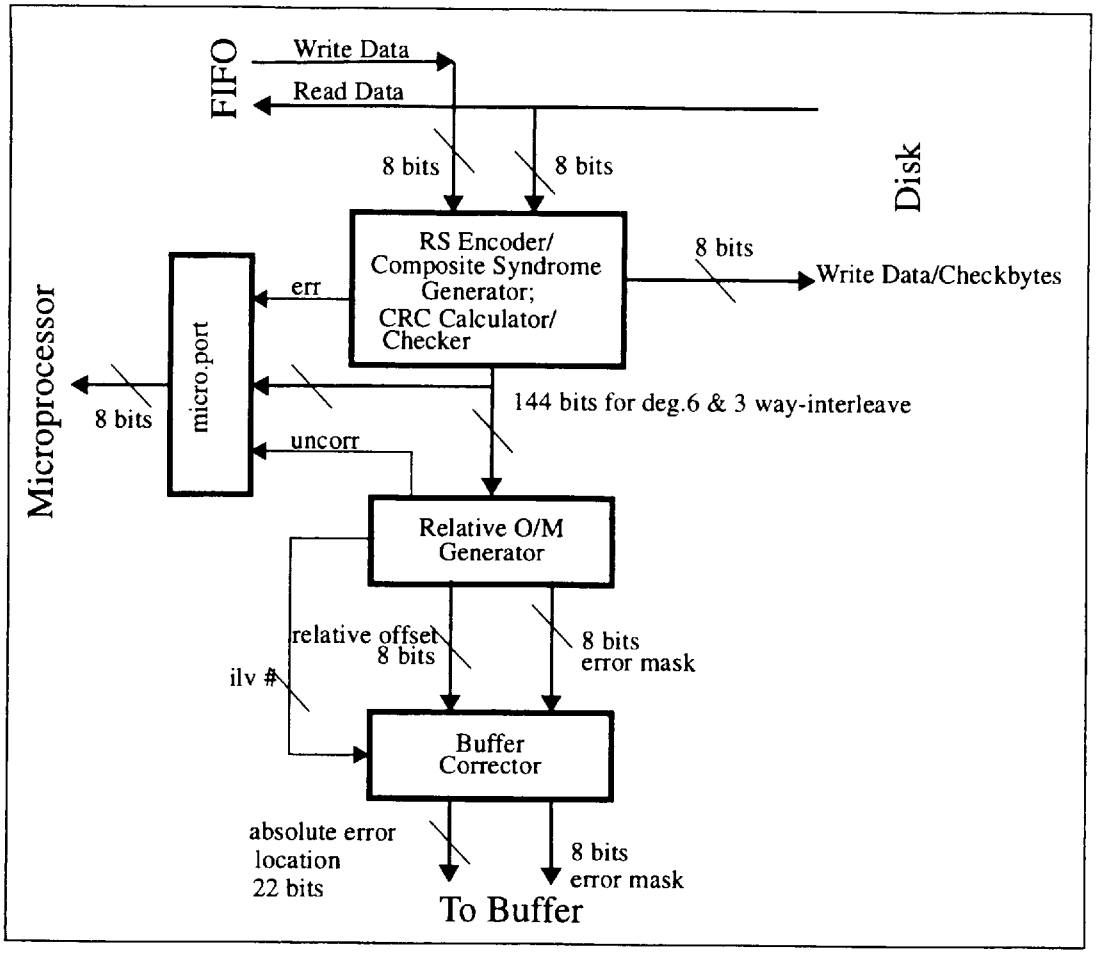

FIGURE 5-21 ECC ARCHITECTURE

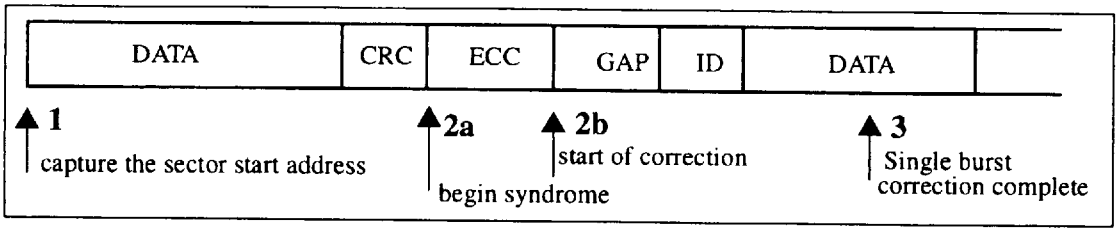

FIGURE 5-22 ERROR CORRECTION TIME LINE

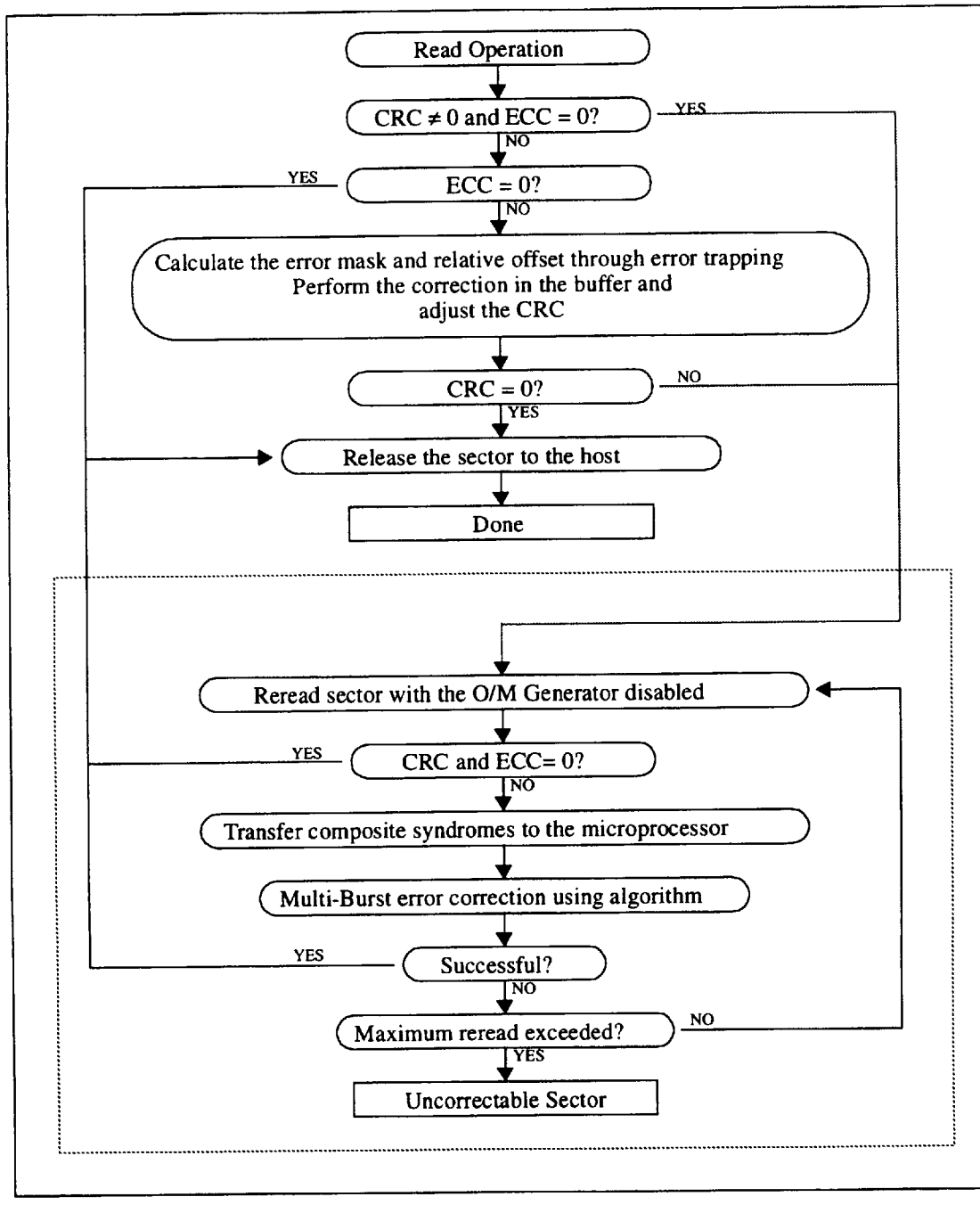

FIGURE 5-23 MICROPROCESSOR CONTROL

5.9.1 Polynomials for the On-the-Fly Corrector

The β^i represent elements of a finite field defined by a polynomial over GF(2):

$$g(x) = x^8 + x^5 + x^3 + x^2 + 1$$

The above polynomial is the same one used in the WD10C01. The elements of the finite field employed by the codes are:

$$\alpha^i = (\beta^i)^{67}$$

The Reed-Solomon generator polynomial is:

$$G(x) = (x + \alpha^{125})(x + \alpha^{126})(x + \alpha^{127})(x + \alpha^{128})$$
$$(x + \alpha^{129})(x + \alpha^{130})$$

or

$$G(x) = x^6 + \alpha^{99}x^5 + \alpha^{98}x^4 + \alpha^{155}x^3 + \alpha^{98}x^2$$
$$+ \alpha^3 x^1 + 1$$

The generator polynomial is the same one as the WD10C01. The symbol mapping, however, is not the same. The coefficients of the polynomial in decimals are:

$$\alpha^{99} = 8 \qquad \alpha^{98} = 206 \qquad \alpha^{155} = 142$$

The polynomial for the ID CRC and the optional data CRC is:

$$g(x) = (x + 1)$$
$$(x^{31} + x^{23} + x^{22} + x^{15} + x^{14} + x^7 + x^4 + x^3 + 1)$$

5.9.2 Microprocessor Correction Algorithm

The partial syndromes can be computed by dividing the composite syndromes with the factors of the generator polynomial:

$$S_i(x) = R(x) \bmod G_i(x)$$

where:

i = 0=ECC degree - 1

$S_i(x)$ = i^{th} partial syndrome

R(x) = composite syndrome

$G_i(x)$ = generator polynomial factor, $(x + \alpha^i)$

5.9.3 Valid ECC Configuration Setups

ECRST		CRCVD	RCONT	ECBEN	ECOEN	SHLD	Comments
0		1/0	0	1	1	0	1. Normal operation
0		1/0	0	0	1	0	2. Attempt OTF but no buffer access
0		1/0	0	1	1	1	3. One sector read, syndrome held
0		1/0	0	0	0	0	4. "10C01" mode, for retries
0		1/0	1	1	1	0	5. Send best data
1		1/0	1/0	1/0	1/0	1/0	6. ECC soft reset, no setup changes
0		1/0	0	0	1	1	7. NOT VALID
0		1/0	1	0	1/0	0	8. NOT VALID
0		1/0	1	1/0	0	0	9. NOT VALID
0		1/0	1	0	0	0	10. NOT VALID
0		1/0	1	1/0	1/0	1	11. NOT VALID

TABLE 5-23 VALID ECC CONFIGURATION SETUPS

1. Normal Operation

   This is the primary mode for the use of the OTF Corrector.

2. OTF Diagnostics

   Allows the OTF to attempt correction, but no buffer access is made. An ECC interrupt is issued if the OTF cannot isolate a mask and offset.

3. Syndrome Hold

   This mode is intended only for single-sector reads and not multiple-sector reads. With the SHLD bit set, the microprocessor may immediately read the syndrome bytes once an ECC interrupt is issued.

4. "10C01 Mode"

   This mode allows the syndrome to be generated and indicates if there is an error with an ECC interrupt. If the ECC interrupt is issued, the syndrome must be read before commencing further reads. Once the syndromes have been read, the microprocessor must perform the soft reset protocol. If there are no errors, an ECC interrupt will not be issued and the next sector may be read.

5. Send Best Data

   This mode is the read continuous mode. If there are correctable errors, the OTF performs the correction. If the OTF cannot correct the errors, then an ECC interrupt is issued. The buffer is not modified and data transfer continues.

6. ECC Soft Reset

   Allows the user to reset the ECC block back to initial conditions without affecting the CECTL register.

5.9.4 Control and Status Examples

ECRST	TSTCS	TSTOM	CRCVD	RCONT	ECBEN	ECOEN	SHLD	ECCBD	ECCGD	REQ	SACT	OACT	ECCER	CRCER	OMER	Comments
1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1. Reset all ECC logic
0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	2. Syndrome Generator active
0	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	3. No error
0	0	0	1	0	1	1	X	1	0	0	0	0	0	1	0	4. CRC error, no ECC error, reread
0	0	0	1	0	1	1	0	1	0	0	0	0	1	0	0	5. ECC error, continue On-the-Fly
1	0	0	1	0	1	1	0	1	0	0	0	0	1	1	0	6. ECC and CRC error, On-the-Fly
0	0	0	1	0	1	1	0	1	0	0	0	1	0	0	0	7. O/M Generator active
0	0	0	1	0	1	1	0	1	0	1	0	0	0	0	0	8. On-the-Fly correctable
0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	1	9. On-the-Fly noncorrectable
0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	10. Syndrome Generator hold
0	0	0	1	0	1	1	1	1	0	0	1	1	0	0	0	11. O/M Generator active
0	0	0	1	0	1	1	1	1	0	1	0	0	0	0	0	12. On-the-Fly correctable
0	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	13. On-the-Fly noncorrectable
0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	14. Buffer Corrector disabled
0	0	0	1	0	0	1	X	0	0	0	0	0	0	0	0	15. No error/On-the-Fly successful
0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	16. On-the-Fly noncorrectable
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	17. O/M Generator disabled
0	0	0	1	0	0	0	0	1	0	0	0	0	1/0	1/0	0	18. Error in reread case
0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	19. No error in reread

TABLE 5-24 ECC REGISTER EXAMPLES

Please note that the CECTL register must not be modified during any ECC operation with the exception of the ECRST bit. The following is a detailed explanation of TABLE 5-24, ECC REGISTER EXAMPLES.

1. The ECRST bit is used to reset all ECC logic and registers with the exception of the CECTL register contents.
2. The Composite Syndrome Generator is active.
3. This is the ECCSTAT register bit states when there are no error after a read.
4. After the Composite Syndrome Generator is complete after a read, an error has been detected by the CRC Calculator but not by the Composite Syndrome Generator. This error is not correctable by the on-the-fly Corrector thus SHLD bit value has no effect. A maskable ECC interrupt occurs and a reread should be performed with the ECOEN bit set to zero to disable the Relative Offset/Mask Generator. The Buffer Manager will reset the ECCBD bit.
5. The ECCSTAT reflects an ECC error but not CRC error. The on-the-fly Corrector attempts to correct the error. The composite syndromes are transferred to the Relative Offset/Mask Generator within 6 RRCLK cycles from the time the last byte of the ECC field is read. Since SHLD bit is zero, SACT will be zero during the O/M phase and the composite syndromes will be lost.
6. A CRC and ECC error has been detected. The same operations occur as stated in previous comment.
7. After the composite syndromes have been transferred, the Relative Offset/Mask Generator attempts to generate the relative offset and error mask bytes. Since SHLD bit is zero, SACT will be zero in this phase.
8. The on-the-fly Corrector has successfully generated the error mask(s) and relative offset value(s), i.e., OMER bit is zero. The REQ bit is one which is requesting an acknowledge from the Buffer Manager. Once an acknowledge has been received, a total of 6 offset and mask bytes are transferred to the Buffer Corrector.
9. The errors are not on-the-fly correctable. The OMER bit is one, indicating the error in the Relative Offset/Mask Generator. REQ bit remains a zero since the offset and mask bytes will not be transferred to the Buffer Corrector. A maskable ECC interrupt will occur.
10. With the SHLD bit 1, the Composite Syndrome Generator holds its contents if there is an ECC error that may be on-the-fly correctable. This means all reads must halt, i.e., program the device for one-sector blocks or have sufficient NOP commands in the Writable Control Store to allow for the FAIL bit to recognize the ECC error.
11. With the SHLD bit 1, SACT bit remains one while the Relative Offset/Mask Generator is active as indicated by the OACT bit.
12. The errors were on-the-fly correctable thus REQ bit is one. Note that SACT is zero, all composite syndromes are now lost, and normal ECC operations continue.
13. The errors were not "On-the-Fly" correctable thus REQ bit is zero. Note that SACT is still one, indicating the composite syndromes are contained in the Composite Syndrome Generator. The microprocessor must then read all 18 bytes before normal ECC operation can continue or strobe ECRST bit.
14. The Buffer Corrector is disabled.
15. There were errors that were on-the-fly correctable and REQ remains zero. The SHLD bit has no effect in this case. This example also shows the register states if there are no errors.
16. The errors were not on-the-fly correctable, OMER bit is one, and a maskable ECC interrupt occurs. This example shows that SHLD bit is zero but if the value is inverted, the composite syndrome bytes need to be read by the microprocessor.

17. The Relative Offset/Mask Generator is disabled. This must be done for reread.
18. After SACT negates, ECCER and/or CRCER bits are one, indicating errors. A maskable ECC interrupt occurs and the microprocessor is expected to read all 18 composite syndrome bytes.
19. At the completion of reread, if there are no errors, the ECCGD bit is one. The firmware then needs to release the sector.

5.9.5 ID CRC Definition

The ID CRC field, a four byte field, uses the same polynomial as the Data CRC field. This CRC checker generator is enabled through the Control Store CRCEN and CHK bits.

The polynomial for the ID CRC and optional Data CRC is:

$$g(x) = (x + 1)(x^{31} + x^{23} + x^{15} + x^{14} + x^7 + x^4 + x^3 + 1)$$

The ID CRC is seeded with ones. The Data CRC is seeded with zeroes.

5.9.6 Disk Manager Soft Reset Operations

The Disk Manager portion of the WD61C96A contains five soft reset control bits. The microprocessor is responsible for setting and resetting these bits. The primary purpose of the soft reset controls is the resetting of the internal control logic, status flags, and error conditions. Generally, the microprocessor accessible registers are not reset. All control signals, signals which cause logic to be enabled, are reset by their respective soft reset. Count and address registers, data registers, are not reset by soft resets. These bits do not execute global reset functions like the RESETB input pin. The following list describes the five soft resets and their general scope. Here are some examples.

1) Disk FIFO Enables - FFEN
   FIFO Counters
   FIFO Status Flags
   Write/Read Register File Address Pointers
2) HOST FIFO Enables - FFEN
   FIFO Counters
   FIFO Status Flags
   Write/Read Register File Address Pointers
   Host Port DMA Control
3) Host DMA - HSTRST
   Host DMA Pipeline Control Logic
   Host DMA Error Flags
   Host DMA Control Logic
4) Disk DMA and WCS -SRST
   All Disk Error Flags: CMPER, CMPIER, IDER, WRAPER,LRCER,
   All Disk Interrupt Status Bits: CMPERR, CMPIERR, IDERR, WRAPER, LRCER, BSY, VBSY, DBSY, DVBSY
   WCS/Buffer Manager Handshake flags: ES pending, ECCGOOD, ECCBAD, DIFF Flag, WCS Start Enable - STARTREQ
   Disk DMA Pipeline Control Logic
   Disk DMA Error Flags
5) ECC Soft Reset - ECRST
   Error Flags
   Uncorrectable ECC Error Flags
   OMERR, Syndrome Error
   Interrupt Status
   Uncorrectable ECC
   Internal Flags

5.9.7 Disk Register File Access

The Register File, a dual port RAM, is used quite extensively throughout the WD61C96A design. It is a very area efficient way to store same quantities of required information. The WCS Control Store, ID Capture, and ID/Segment module utilize the register file as its core. In the WD61C96A design, the register files typically look like a single register location to the microprocessor. The ID Capture and ID segment

modules read and write data through a single address space. The WCS Control Store is accessed through four address locations and addressed by another. The Disk and Host FIFOs are also based upon a register file core. The following section describes the process in which data access is performed.

5.9.8 WCS Register File Access

The WCS register file consists of five major elements. These elements are the input hold register, the WCS register file core, the output hold register, the present WCS address and the WCS Start address register. The Input Hold register temporarily holds the 32-bit word that is to be written into the WCS. The Output Hold register save the present WCS word. The Start register contains the start address for each active WCS operation or the first address for the microprocessor write operation. The Read Pointer is loaded when the Start register is written by the microprocessor. The Read pointer points to the next WCS word after reading the CSCNT register.

The WCS appears to be four unique addresses. In the WD61C96A, these four address are combined into one internal register file address. When writing to the WCS the microprocessor should follow these three steps.

1) Disable all Active WCS operations. Microprocessor access should only be performed when the Control Store is idle.

2) Initialize the beginning start address. The microprocessor loads the START address to the appropriate location.

3) Load WCS Data - CSERR, CSCTL, CSVAL, CSCNT

The microprocessor writes to the four WCS control byte register. This data is temporarily loaded into four holding registers to hold data until it is transferred to the WCS Register file. When the microprocessor writes to the CSCNT register, a flag is internally set and the data is moved to the register file. These registers can not be changed for 4 RRCLKs from the rising edge of WEB, the microprocessor write strobe. After data is written

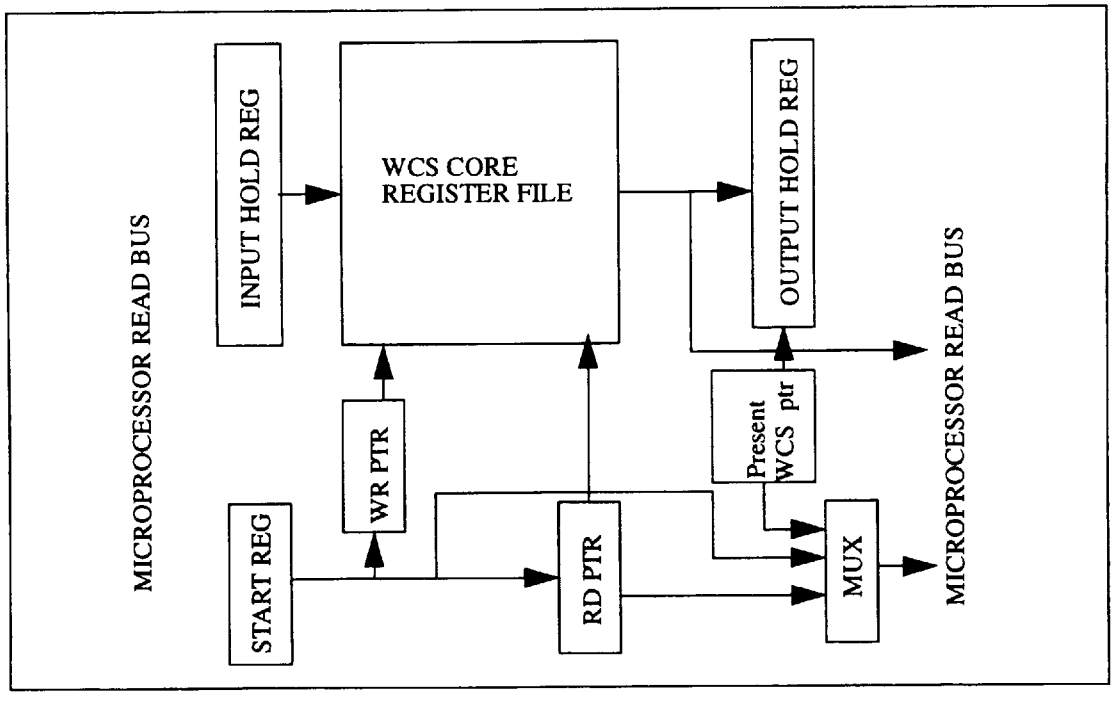

FIGURE 5-24 WCS READ/WRITE DATA PATHS

to the register file the Write Pointer address increments, and Control Store loading can proceed.

There are different WCS read modes. When the WCS is active, DIAG1 and DIAG2 are reset, the microprocessor reads the next WCS word via the CSERR, CSCTL, CSVAL, CSCNT microprocessor register location. The START address which is read is the initial START address. If DIAG1 is set, the WCS data is the same but the START address is the present WCS read address of the present (which is stored in the output hold register). If DIAG2 is set the WCS data is WCS register file data and the start address represents the present location of the register file location. In addition, the read pointer increments after each CSCNT microprocessor read access. The WCS must be idle for proper operation. (Refer to the Disk Configuration 1 register DCNF1, Section 4.3.1, for more information on DIAG1, DIAG2.)

5.9.9 ID Capture Register File Access

The ID Capture register file appears to the microprocessor as one address location. There are a maximum of eight values which the microprocessor can read. The ID capture registers are armed when the microprocessor writes an 80_{hex} to this location. The ID Capture Registers contains valid ID fields, only when the ID FULL interrupt bit is set in the DSEQI register. The ID FULL interrupt bit is set only when a complete ID field is stored and the ID CRC is good. The incoming ID from the Disk is always top justified with first ID byte always being stored in the first location (00_{hex}). An ID FULL interrupt is generated when a good ID has been stored. The microprocessor should read the IDCAP register only when this is the case. When reading the ID Capture the microprocessor should follow these two steps.

1) Initialize the address

   Writing a 00 through 07_{hex} to the IDCAP register initializes the internal pointer to the first ID byte.

2) Read and Pause

   The microprocessor reads the first ID. When the internal logic detects REB rising edge, signaling the data has been transferred, the internal read pointer increments. This pointer change takes four RRCLKs (in XA) or four X1s (in XB). The microprocessor should not expect the next valid ID byte until this read pointer increment is complete. Refer to Section 4.3.37, ID Capture Address/Data/Control, on page 51.

5.9.10 ID/Segment Register File Access

The ID/Segment register file also appears to the microprocessor as one address location. Refer to Section 4.3.20, ID/Segment Data, on page 39. There are a maximum of 32 values which the microprocessor can read. When reading the ID/Segment the microprocessor should follow these three steps.

1) Disable all Active WCS operations.

   Microprocessor access should only be performed when the Control Store is Idle.

2) Initialize the beginning write/read address.

   The microprocessor loads the address to the appropriate location along with enabling the IDEXT access bit in the IDSEGAD register. For example, writing a 0x98 enables the microprocessor to read the ID starting at the 0x18 location by initializing the read pointer to 0x18 location. Refer to Section 4.3.19, ID/Segment Address, on page 39.

3) Read/Write Data Segment

   The microprocessor reads or writes the first ID from the IDSEGDT location. The internal ID Register File pointer is incremented with every rising transition of the WEB or REB inputs from the microprocessor. This ID Register File pointer takes four RRCLKs to increment, and so the microprocessor should not expect to access the ID/Segment Data until this pointer change is complete.

5.9.11 Register File BIST (Built In Self Test)

Each of the five register files contain additional logic which performs a self diagnostic operation, if enabled. This feature is call BIST. The WCS, ID Segment, and ID Capture register files are controlled via the IDB register (refer to section 4.3.38, ID BIST Control Status, on page 51). The Host FIFO is controlled via the HCECTL register (refer to Section 4.3.38, ID BIST Control Status, on page 51). The Disk FIFO is controlled via the 4.3.29, Disk FIFO BIST Control Status, on page 46.

In general, the BIST logic is controlled through two lines, BIST (BIST test mode select) and BFC (BIST flag control). The WCS, ID Segment, and ID Capture share these same control flags (Bits 7 and 6 of the IDB register Section 4.3.38, ID BIST Control Status, on page 51. The Host and Disk FIFO have there own flags. Each register file generates its own BIST test status, BF(BIST Error Flag) and BC(BIST test complete).

The BIST sequence is as follows.

1) The BFC bit is set low.
2) The CLKSW bit is set to enable free clock. (This applies to the Host and Disk FIFOs only).
3) Enable FIFO Operation. Both the CLKSW and FIFO enable remain set until the BIST testing is complete. (This applies to the Host and Disk FIFOs only).
4) Toggle BIST Test Bit. The BIST test begins. The length of this test is based upon the size of the register file and the basic clock which is supplied to the register file.

   WCS test time = ((17 x 32) + (4 x 16) + 2) x clock period

5) Wait for the BC flag to be set. This indicates the end of the first phase of the test.
6) The BF flag is read. If this bit is high, the register file has failed the BIST test. If BF is low, the register file BIST test can continue.
7) The BFC control line is toggled. This is done so the BF flag signal is tested.
8) The BF flag is now high if functioning properly.
9) The BIST control line is now dropped. The BF and BC lines should go low.
10) BIST Testing is complete.

5.10 DATA INTEGRITY: LRC

5.10.1 DISK PORT LRC OPERATION

The WD61C96A design features longitudinal redundancy check (LRC) bytes for enhanced data integrity. The LRC field provides another layer of data error detection. LRC is simply the horizontal checksum of all data bits within a sector, i.e. the first word is XORed with the next word.

A complete data path is checked. An LRC field (2 bytes) is generated at the SCSI pins. This field enters the SCSI Manager Data FIFO and follows the data through the buffer to the disk. As the data is written to the disk, the LRC field is checked and written to the disk. When the data is read from the disk, the LRC is checked again at the SCSI pins. This operation spans the data field, typically 512 bytes for a 512 byte sector. As an option the LRC bytes can span multiple physical sectors, Physical Blocks. When these Physical Blocks are grouped together they are called Logical Blocks. The quantity of physical blocks to one logical block is the Physical To Logical Block Ratio. Typically, the LRC spans a complete Logical Block.

FIGURE 5-25, LRC EXAMPLE, shows the LRC spans a logical block. In this example, there are three physical block per one Logical Block. The LRC bytes are originally generated in an external device, typically the WD33C96. The WD61C96A checks the LRC bytes as they are being written to the Disk on each sector boundary. However, the LRC bytes are reinitialized to $AAAA_{hex}$ at the end of each Logical Block. This means that the WD61C96A internal LRC bytes are initialized preceding Data field 1 and following LRC 3.

Typically, all write operations begin at a Logical Block Boundary. This means that the WCS will reinitialize the LRC whenever the WCS begins. The WD61C96A also has the ability to begin a Disk write at any partial Logical Block boundary.

The programmer can load the LRC bytes to any value and define the physical block within the logical block start point. See Sections 4.3.35, Logical to Physical Block Ratio for LRC; 4.3.36, LRC Preset Bytes; 4.6.1.19, Physical-to-Logical Block Ratio Register; and 4.6.1.20, Physical Block Size Register for more details.

The Default value for LPR register is 00hex or one physical block per logical block. For example, a four block transfer can have the following four configurations:

LPR = 33 Calculates LRC over all 4 blocks. This is a complete transfer.

LPR = 23 Calculates LRC over last 3 blocks, then reset at logical boundary.

LPR = 13 Calculates LRC over last 2 blocks, then reset at logical boundary.

LPR = 03 Calculates LRC over last block only, then reset at logical boundary.

ALL partial transfers start with the remaining blocks in the first logical block. For example, if LPR=23, only 3 physical blocks should be read for the first logical block, followed by 4 physical blocks per logical block.

5.10.2 SCSI LRC OPERATION

When using LRC, the following conditions must be met:

- target mode only.
- physical block size must be even.
- maximum offset is 30 bytes or 15 words.
- SCSI section must be DMA master.
- cannot be used with odd-byte reconnect.
- any combination of 8-bit and 16-bit SCSI and DMA busses may be used.

5. 10.2.1 Programming The SCSI Section For LRC

The SCSI section should be programmed in the following manner to utilize LRC:

- Program the Physical Block Size register to the number of bytes in a physical block - 1, excluding the two LRC bytes.
- Program the Physical:Logical Ratio register with the number of physical blocks per logical block - 1.

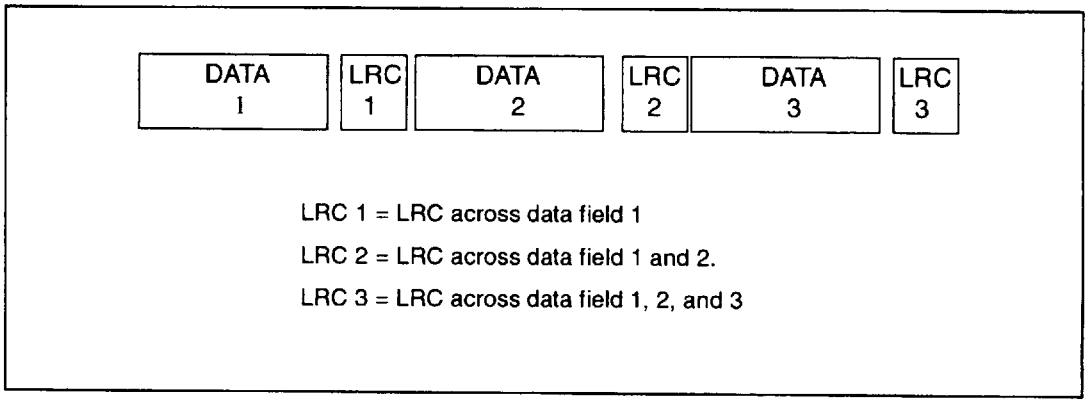

FIGURE 5-25 LRC EXAMPLE

- Program the TC to the number of logical blocks to be transferred.
- Enable LRC using the LRC field in the SCSI configuration register (CTLA).
- Set BYTEC.
- The maximum synchronous offset is limited to 15 words or 30 bytes (so that there is always room for the LRC bytes)
- If data transfer is made through non-DMA channel, e.g., DPR, the LRC logic should be disabled in order not to corrupt the LRC for subsequent transfer.
- If a possible, LRC problem due to corrupted LRC seed is suspected, proper initialization can be forced by clearing the DMA pipeline. Asserting LDTC and LDTCL bits in CTL register simultaneously will achieve this.

5. 10.2.2 LRC Generation On Data Coming In On The SCSI Bus

If LRC generation/stripping is enabled:

- at the start of each transfer, the LRC residue register is reset to AAAA, unless the microprocessor has written to the LRC residue register since the last transfer stopped.
- generate LRC for each byte/word received on the SCSI bus, before data enters the FIFO.
- at the end of each physical block received, the SCSI section performs the following:
  - write the two LRC check bytes into the FIFO.
  - if it is also the end of a logical block, the LRC residue is reset to AAAA.
- LRCCE has no effect.

5. 10.2.3 LRC Generation On Data Going Out The SCSI Bus

If LRCGS = 0, the LRC residue register will not be updated as data goes out onto the SCSI bus, and no bytes will be stripped. The value of LRCCE is ignored (no LRC checking is performed)

If LRCGS = 1:

- at the start of each transfer, the LRC residue register is reset to AAAA, unless the microprocessor has written to the LRC residue register since the last transfer stopped.
- the LRC residue register is updated as data goes out onto the SCSI bus.
- As soon as a complete physical block is transferred onto the SCSI bus, the following sequence is performed:
  - two bytes are read out of the FIFO and compared to the LRC residue register.
  - if LRCCE = 1 and the bytes do not match the LRC residue, then
  - LRCE is asserted and the transfer is halted. (see section 5. 7.2.6 on page 151), else if also at the end of a logical block, reset the LRC residue to AAAA.

If the microprocessor wishes to transfer LRC bytes (already stored in the buffer manager) onto SCSI bus, LRC should be disabled and the physical block size should be increased by two.

5.11 DISK INTERFACE WRAP CONTROL

The WRAP pin checks the complete path of the WD61C96A control lines (WRTGATE, RDGATE, and AMENA) from the IC pins to their respective destinations.

The internal WRAP logic, when enabled, checks the control lines on every RRCLK boundary. The internal WRAP logic compares the "XORing" of the internal control signals to the external "XORing" of the control signals. If there is a difference, an internal error flag is set. This flag is examined by the Control Store when the FAIL bit is active. At that time, the Control Store aborts. WRAP error and Sequencer Stop Interrupts are generated. The microprocessor resets the interrupt by writing a one to the respective interrupt bit.

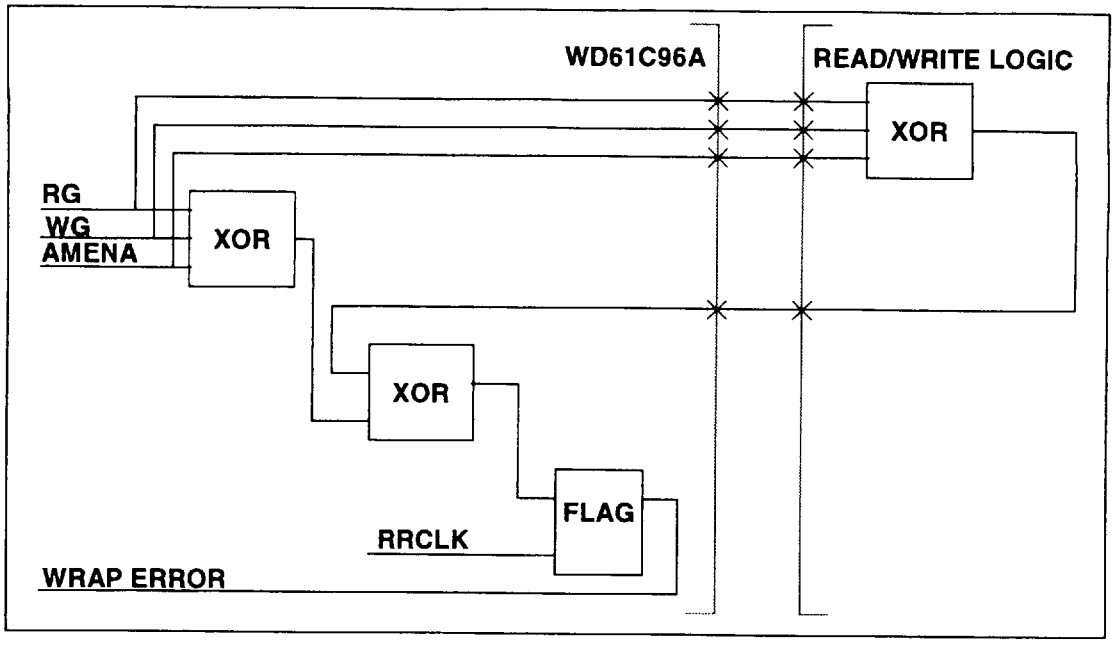

FIGURE 5-26 WRAP PATH

5.12 TEST MODES

The major test modes are invoked using the TST1B and TST2B signals, along with the state of RESETB. Other test modes are enabled via the TEST0 register. It should be noted that most of these test modes are appropriate only for device testing, and should not be invoked in a board level environment.

5.12.1 Major Test Modes

The following table shows the major test modes of the device.

RESETB	TST2B	TST1B	Description
0	0	0	Reserved
0	0	1	Reserved
0	1	0	I/O Mapping Mode (see 5.12.3 below)
0	1	1	Device Reset/ Tristate most outputs (see 3.0)
1	0	0	Enable Scan Mode (used for device test)
1	0	1	Enable Host/ DMA Bus View (used for device test)
1	1	0	Enable Test Register tests (see 5.12.2 below)
1	1	1	Normal Operation

TABLE 5-25 MAJOR TEST MODES

5.12.2 Test Register Test Modes

The TEST code bits (bits 5-3) are used to define the test. (*) indicates that the test is enabled via the Test Register Enable mode listed above. These tests are used for device testing only.

- 0 = normal mode
- 1= reserved.
- 2 = enable pulsed pullups on SCSI bus.
- 3 = CASB Hold Time Test (see section 5.12.4 on page 173). (*)
- 4 = reserved
- 5 = reserved
- 6 = force initiator mode. (*)
- 7 = force target mode (*)

5.12.3 I/O Mapping Mode

The following is a list of the signals that are testable using I/O mapping mode. When this mode is enabled, the input is directly connected to its corresponding output. This mode is intended for board level test.

INPUT	OUTPUT
ALE	INT0
REB	INT1
WEB	INT2
CS0	RDYB
CS2	AD0
DREQA	DACKA
DREQB	DACKB
DWEB	DREB
RRCLK	WRTCLK
IDXDET	RDGATE
SMDET	WRTGATE
AMDET	AD7
CMPLT	SEQOUT
DRVFLT	AD1
WRAP	AD2
DATA0	DATA4
DATA1	DATA5
DATA2	DATA6
DATA3	DATA7
DATAP	AMENA
BCLK	AD3
SCLK	AD4

TABLE 5-26 I/O MAPPING MODE

INPUT	OUTPUT
SE	AD5
DIFFSNS	AD6
RST	RSTF (normal function, not I/O map)

TABLE 5-26 I/O MAPPING MODE (Continued)

5.12.4 CASB Hold Time Test

Zero hold time measurement for CASB may be performed when the device is set up for CASB test mode. This mode is used for device test only. In this mode, the CASB signal is tristated, allowing it to be driven from outside the device. Data may then be applied to BF[15:0], BFPL, and BFPH to test the hold time of this interface.

5.12.5 Other Board Level Testing Methods

The other signals not covered by I/O mapping mode are tested as follows:

- BD[15:0], BDPH, and BDPL may be read directly via AD[7:0] through the HSTLD ports of the 61C40A core.
- GPX[7:0] may be read directly via AD[7:0] through the PRTXDAT port of the 61C40A core, when the PRTXDIR is set for input on all signals (all bits zero).
- GPY[3:0] may be read directly via AD[3:0] through the PRTYDAT port of the 61C40A core, when the PRTYDIR is set for input on all signals bits [3:0] zero).
- SCSI signals REQ, ACK, C/D, I/O, MSG, ATN, IGS, and TGS may be tested via port SC1 in setup mode. Note that the SCSIL bit in the SCNF register must be set to one.
- SCSI signals BSY, BSYIN, SEL, SELIN, RST, RSTIN, and SDP1 may be tested via port SC0 in setup mode. Note that the SCSIL bit in the SCNF register must be set to one.
- The Buffer group of signals (BF[15:0], BFPL, BFPH, BA[10:0], MEMWB, RASB, CASB) may be tested via the usual microprocessor buffer accessing.

5.12.6 Scan Mode Testing

This testing mode is used to apply automatically generated test vectors via a scan chain methodology. When the device is put into scan mode, it has the following effects:

- All I/O pins are forced to input mode only.
- The SCTL signal is used to control the shifting of signals. When SCTL is zero, scan vectors may be shifted into and out of the scan pins.
- Six pins become scan inputs; six pins become outputs as summarized below:

SCAN IN	SCAN OUT	SCAN CLOCK
DRVFLT	SEQOUT	SCLK
COMPLT	WRTGATE	BCLK
IDXDET	RDGATE	SCLK
SMDET	AMENA	RRCLK
AMDET	INT0	WEB
GPY0	GPY2	CASB

6.0 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Maximum Power Consumption:

1500mW for 176-pin package.

1500mW for 208-pin package.

6.2 DC OPERATING CHARACTERISTICS

T = 0^{O} to 70^{O} Centigrade

Vcc = 5 volts +/- 10%

6.3 AC OPERATING CHARACTERISTICS

6.3.1 Inputs*

SYMBOL	CHARACTERISTICS	MINIMUM	MAXIMUM	CONDITIONS
I_{il}	Input Leakage	10uA	+ 10uA	
V_{ih}	Input High, TTL	2.0V	5.5V	
V_{il}	Input Low, TTL	-0.2V	0.8V	
V_n	Input Hysteresis	0.3V		
V_{hys}	SCSI Pins Input Hysteresis	0.5V		V_{CL} = 5.0V
V_{CIH}	Input High, CMOS	2.4V	5.5V	
V_{CIL}	Input Low, CMOS		.4V	

TABLE 6-1 INPUTS

**All input and bidirectional input pins only.*

6.3.2 Outputs

SYMBOL	CHARACTERISTICS	MINIMUM	MAXIMUM	CONDITIONS
VOHS	Output high voltage - SCSI outputs	2.0V		IOH = -20 mA
VOH	Output high voltage - all other outputs	2.4V		IOH = -400µA
VOLRA	Output low voltage - $\overline{REQ}$ and $\overline{ACK}$ (single ended mode only)		0.4V	IOL = 60 mA
VOLS	Output low voltage - other SCSI outputs (single ended mode only)		0.4V	IOL = 48 mA
VOL6	Output low voltage - INT and RSTF		0.4V	IOL= 6 mA
VOL12	Output low voltage - AD[7:0], BF[15:0], BFPL, BFPH, RASB,CASB		0.4V	IOL = 12 mA

TABLE 6-2 OUTPUTS

SYMBOL	CHARACTERISTICS	MINIMUM	MAXIMUM	CONDITIONS
VOL	Output low voltage - all other outputs		0.4V	IOL = 2 mA

TABLE 6-2 OUTPUTS (Continued)

6.3.3 Pin External Pullups/Pulldowns

EQUIVALENT RESISTANCE	PIN TYPE	PU/PD	PIN NAME
100K	Bidirectional	PU	BD[15:0], BDPH, BDPL, DREQA, DACKA, DREQB, DACKB, DWEB, DREB, GPX[7:0]
100K	Input	PU	TST1B, TST2B, SCTL, BDP3, BDP4, BDP9, BDP10
100K	Input	PD	CMPLT
10K	Input	PU	SE, DSENSE, BSYIN, SELIN, RSTIN

TABLE 6-3 PIN INTERNAL PULLUPS

The external BD[15:0] bus is pulled down with an optional 10K resistor to ground during Power on reset. A connected pull down resistor is considered a zero in the internal Host POR latch. Only the above mentioned pins contain pullups.

7.0 TIMING CHARACTERISTICS

7.1 MICROPROCESSOR BUS TIMING

7.1.1 Microprocessor Read/Write Timings (CS0)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
T_{30a}	AD[7:0] addr setup to ALE low	10		
T_{30b}	AD[7:0] addr hold from ALE low	5		
T_{30c}	ALE pulse width	20		
T_{30d}	WEB Pulse Width	100		
T_{30e}	AD[7:0] setup to WEB high	30		
T_{30f}	AD[7:0] hold from WEB high	0		
T_{30g}	CS0 setup to WEB/REB high	10		
T_{30h}	CS0 hold from WEB/REB high	10		
T_{30j}	ALE High to CS0 Low		4.5	
T_{30k}	CS0 low to RDYB low		20	
T_{30l}	REB/WEB low to RDYB high	$3xT_{CYCB}+10$	$6xT_{CYCB}+40$	
T_{30m}	REB low to AD bus Valid		80	
T_{30n}	AD data hold from REB high	0		
T_{30p}	REB/WEB high to ALE High	4		
T_{30q}	REB pulse width	100		
T_{30r}[a]	REB low to RDYB high (Buffer)	$3xT_{CYCB}+10$	5 µs	
T_{30s}[a]	WEB low to RDYB high (Buffer)	$3xT_{CYCB}+10$	5 µs	
T_{30t}[b]	AD[7:0] setup from WEB low (Microprocessor buffer access requirements)		$4xT_{CYCB}$	

TABLE 7-1 MICROPROCESSOR INTERFACE TIMING PARAMETERS - REGISTER ACCESS

a. T30r(min) and T30s(min) time is applicable when buffer data resides within the buffer & Ready is operational; the buffer data access time is then similar to a normal register R/W access.
T30r(max) and T30s(max) time assumes a 40MHz clock, 20Mbytes/s Host port rate, CASB low of 2 clocks and micro-processor request occurring immediately after the start of the host burst operation.
Typical T30r and T30s access times are about 500ns.

b. This timing parameter applies only to writes by Waitable Microprocessors. For writes by waitable microprocessors, the data input must be valid within 4 system clocks after the falling edge of WEB, due to internal timing restrictions, for proper operation.

7.1.2 PIO Read with RDYB - CS0

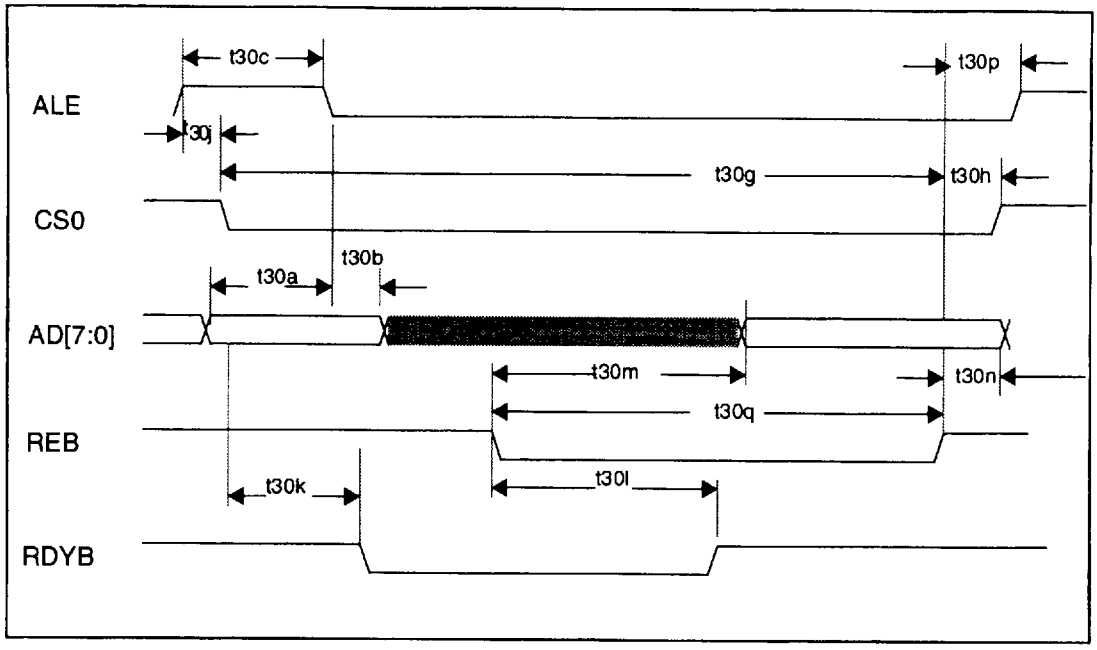

FIGURE 7-1 PIO READ WITH RDYB (CS0)

7.1.3 PIO Write with RDYB - CS0

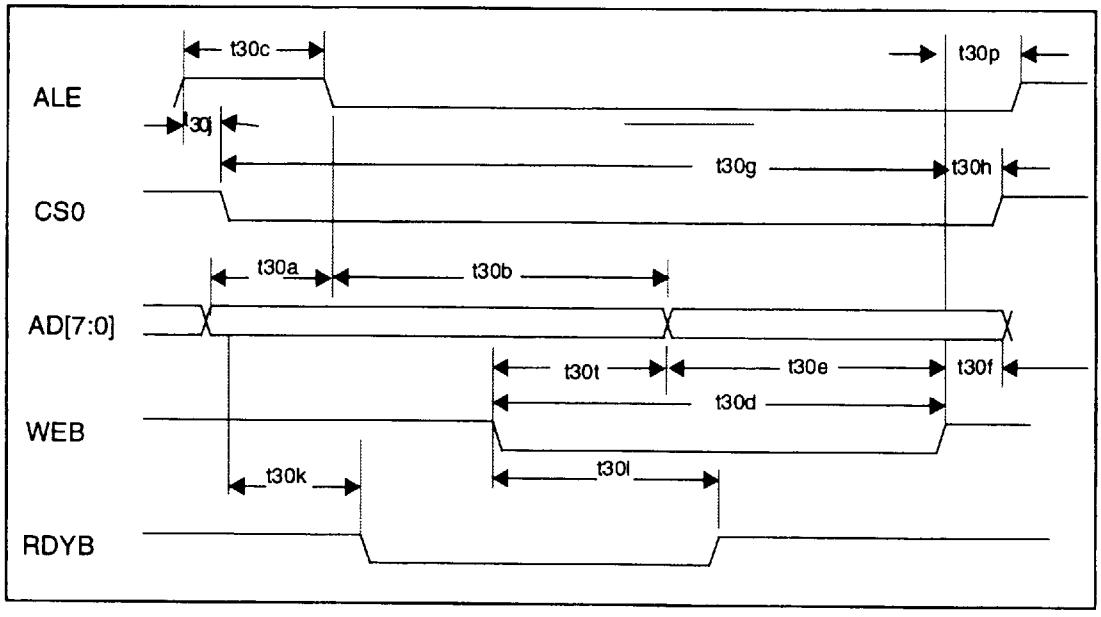

FIGURE 7-2 PIO WRITE WITH RDYB (CS0)

7.1.4 PIO Read with RDYB - Buffer Memory Access (CS0)

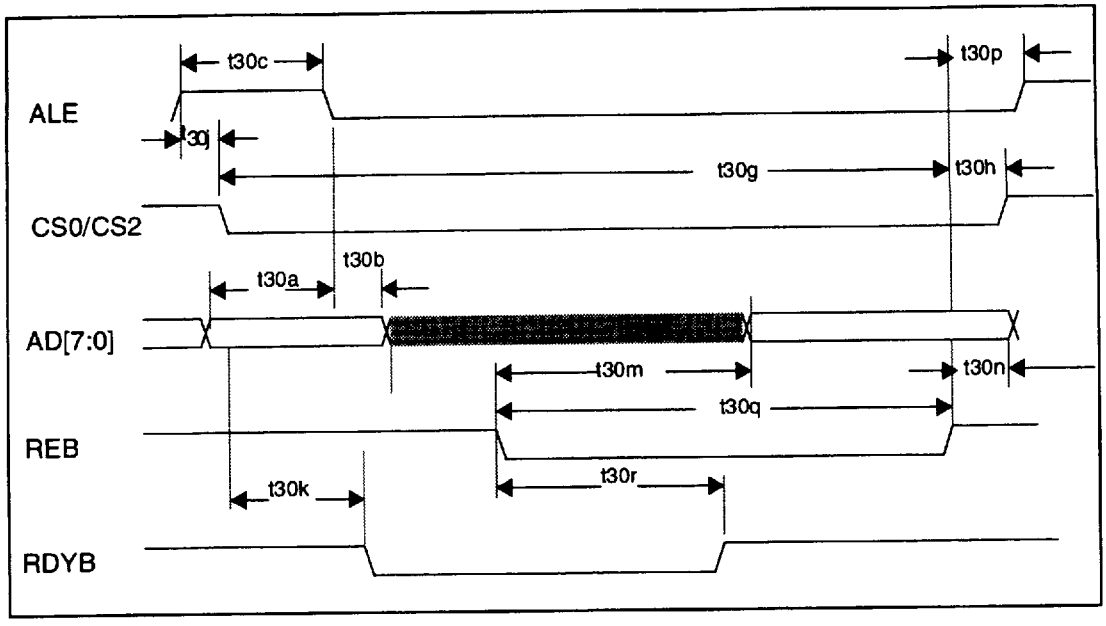

FIGURE 7-3 PIO READ WITH RDYB - BUFFER ACCESS

7.1.5 PIO Write with RDYB - Buffer Memory Access (CS0)

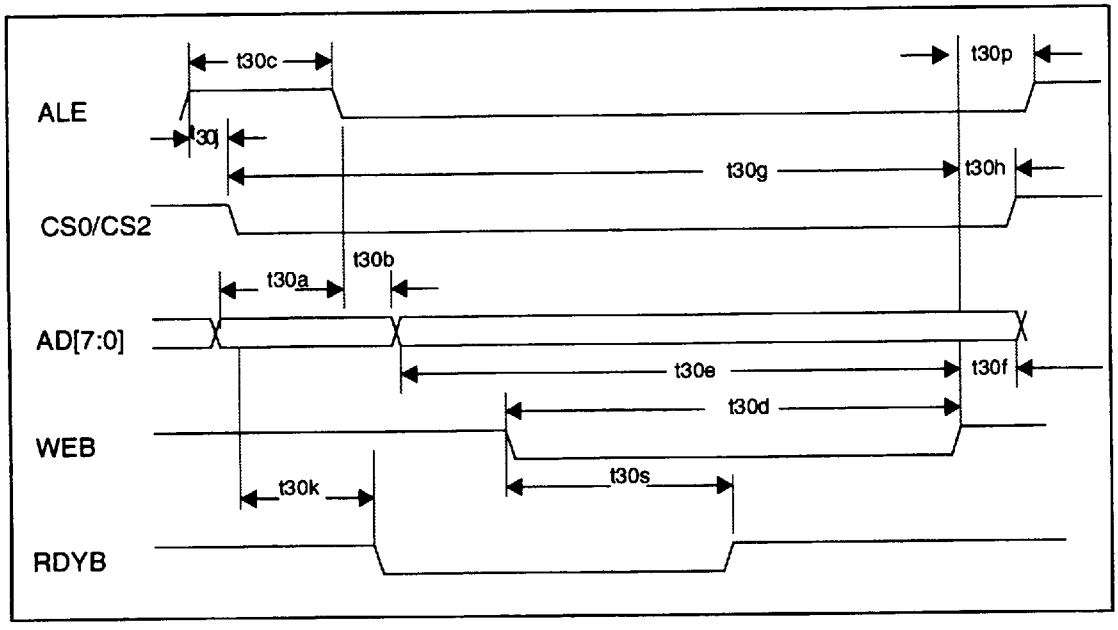

FIGURE 7-4 PIO WRITE WITH RDYB - BUFFER ACCESS

7.1.6 PIO Read/Write with RDY - CS2

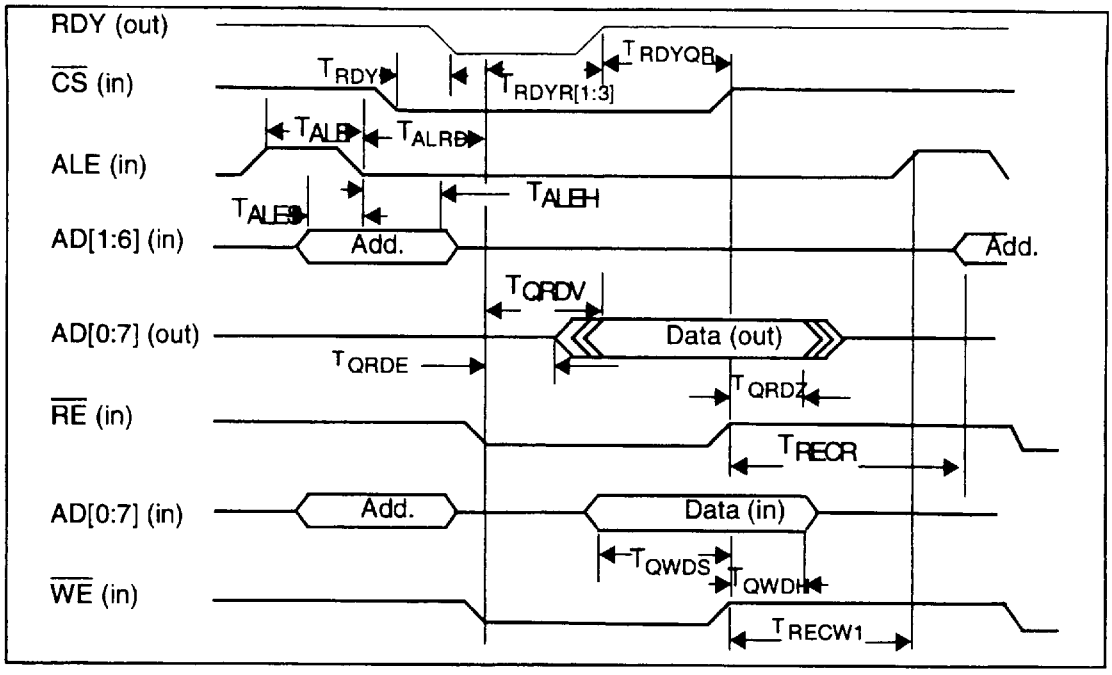

FIGURE 7-5 PIO Read Write with RDYHOST (DMA) BUS TIMING

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{ALE}	ALE high MPW	R	13		ns
T_{ALEH}	ALE fall to AD[1:6] (in) address hold	R	5		ns
T_{ALES}	AD[1:6] (in) address setup to ALE fall	R	10		ns
T_{ALRD}	ALE T.E. to QRE or QWE L.E.	R	T_{ALEH}+3		ns
T_{QRDE}	QRE L.E. to AD[0:7] outputs enabled	S	0		ns
T_{QRDV}	QRE L.E. to AD[0:7] valid	S		T_{RDYR}[1,2] (max)	ns
T_{QRDZ}	QRE T.E. to AD[0:7] Invalid / tristate	S	5	25	ns
T_{RDYQR}	RDY rise to QRE / QWE rise	R	0		ns
T_{QWDH}	AD[0:7] (in) hold after QWE T.E.	R	10		ns
T_{QWDS}	AD[0:7] (in) setup to QWE T.E.	R	25		ns
T_{RECR}	QRE T.E. to AD[0:7] (in)	R	T_{QRDZ} (max)		ns
T_{RECW1}	QWE T.E. to ALE L.E.	R	6		ns
T_{RDYF}	CS- fall to RDY fall	S		24	ns
T_{RDYR1}	QRE/QWE L.E. to RDY rise (Non-DPR)	S	$3T_{CYCS}$+14	$4T_{CYCS}$+14	ns
T_{RDYR2}	QRE L.E. to RDY rise (DPR-Read)	S	$5T_{CYCS}$+14	$9T_{CYCS}$+14	ns
T_{RDYR3}	QWE L.E. to RDY rise (DPR Write)	S	$3T_{CYCS}$+14	$7T_{CYCS}$+14	ns
T_{REC}	QWE/QRE T.E. to QWE/QRE L.E.	R	$1T_{CYCS}$+14		

TABLE 7-2 BUS SLAVE SINGLE-CYCLE DMA TIMINGS

7.2 HOST (DMA) BUS TIMING

7.2.1 Bus Master Burst DMA Timings

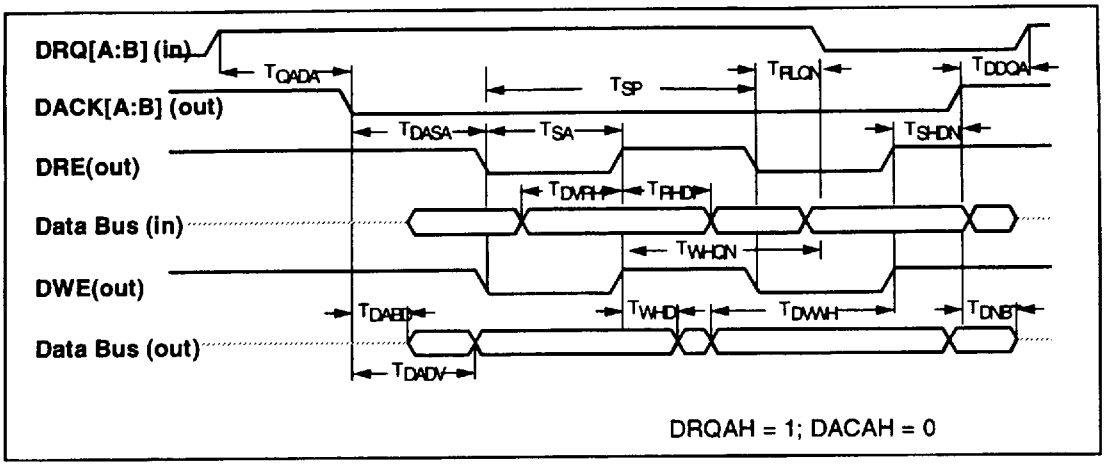

FIGURE 7-6 BUS MASTER BURST DMA TIMINGS

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{QADA}	DRQ asserted to DACK asserted	S	$2 \times T_{CYCS} + 5$		ns
T_{DASA}	DACK asserted to data strobe asserted[a]	R	$i \times T_{CYCS} - 10$	$i \times T_{CYCS} + 10$	ns
T_{DABD}	DACK asserted to data bus driving	S	$T_{CYCS} + 2$		ns
T_{DADV}	DACK asserted to data valid	S		$2 \times T_{CYCS} + 17$	ns
T_{SP}	Data strobe period[b]	S	$p \times T_{CYCS}$	$p \times T_{CYCS}$	ns
T_{SA}	Data strobe asserted width[c]	R	$a \times T_{CYCS} - 10$	$a \times T_{CYCS} + 10$	ns
T_{DVRH}	Data valid to $\overline{DRE}$ high	R	10		ns
T_{RHDI}	$\overline{DRE}$ high to data invalid	R	2		ns
T_{WHDI}	$\overline{DWE}$ high to data invalid	S	$1 \times T_{CYCS} - 9$		ns
T_{RLQN}	Read strobe low to DRQ negated[d]	R	0	$4 \times T_{CYCS} + 30$	ns
T_{WHQN}	Write Strobe high to DRQ negated[d]	R	0	$4 \times T_{CYCS} + 30$	ns
T_{DWWH}	Data valid to $\overline{DWE}$ high	S	$T_{SP} - T_{CYCS} - 15$		ns
T_{SHDN}	Data strobe high to DACK negated	S	$2 \times T_{CYCS} - 17$		ns
T_{DDQA}	DACK negated to DRQ asserted	R	0		ns
T_{DNBT}	DACK negated to data bus tristate	S		30	ns

TABLE 7-3 BUS MASTER BRST DMA TIMINGS

a. i = 2 if DSRW (DMATIM register bit 6) = 0; i = 4 if DSRW = 1.
b. $4 \leq p \leq 18$ at increment of 1, depending on DCLKL and DCLKH values in DMATIM register.
c. a = 2, 3, 4, 5, 6, 7, 8, 9, depending on DCLKL value in DMATIM register.
d. The maximum of 2 read/write cycles may occur after the cycle which causes DRQ to negate.

Note: These timing specifications are applicable for dual LUN applications only.

7.2.2 Bus Master Single-Cycle DMA Timings

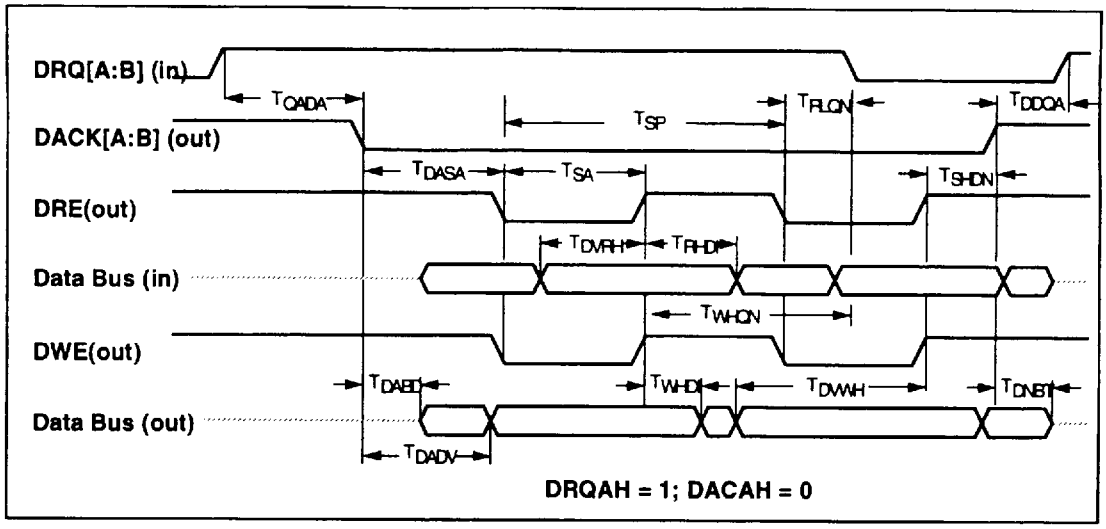

FIGURE 7-7 BUS MASTER SINGLE-CYCLE DMA TIMINGS

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{QADA}	DRQ asserted to DACK asserted	S	2T + 9		ns
T_{DAQN}	DACK asserted to DRQ negated	R	0		ns
T_{DASA}	DACK asserted to data strobe asserted[a]	S	i × C -10	i × C +10	
T_{DABD}	DACK asserted to data bus driving	S	1 × C -8		ns
T_{DADV}	DACK asserted to data valid	S	2T + 31	2 × C +31	ns
T_{SA}	Data strobe asserted width[b]	S	a × C -10	a × C +10	
T_{DVRN}	Data valid to $\overline{DRE}$ high	R	10		ns
T_{SHDN}	Data strobe high to DACK negated	S	2T -10		ns
T_{RHDI}	$\overline{DRE}$ high to data invalid	R	1		ns
T_{WHDI}	$\overline{DWE}$ high to data invalid	S	1 × C -9		ns
T_{DNQA}	DACK negated to DRQ asserted	R	0		ns
T_{SN}	Data strobe negated width[c]	S	b × C -10	b × C +10	ns
T_{DNBT}	DACK negated to data bus tristate	S		30	ns

TABLE 7-4 BUS MASTER SINGLE-CYCLE DMA TIMINGS

a. i = 2 if DSRW (DMATIM register bit 6) = 0; i = 4 if DSRW = 1.
b. a = 2, 3, 4, 5, 6, 7, 8, 9, depending on DCLKL value in DMATIM register.
c. b = 2, 3, 4, 5, 6, 6, 8, 9, depending on DCLKH value in DMATIM register.

Note that C = T_{CYCS} if '96 core is master; C = T_{CYCB} if '40 core is master.

7.3 DISK TIMING

7.3.1 Basic Disk Interface Control Timing

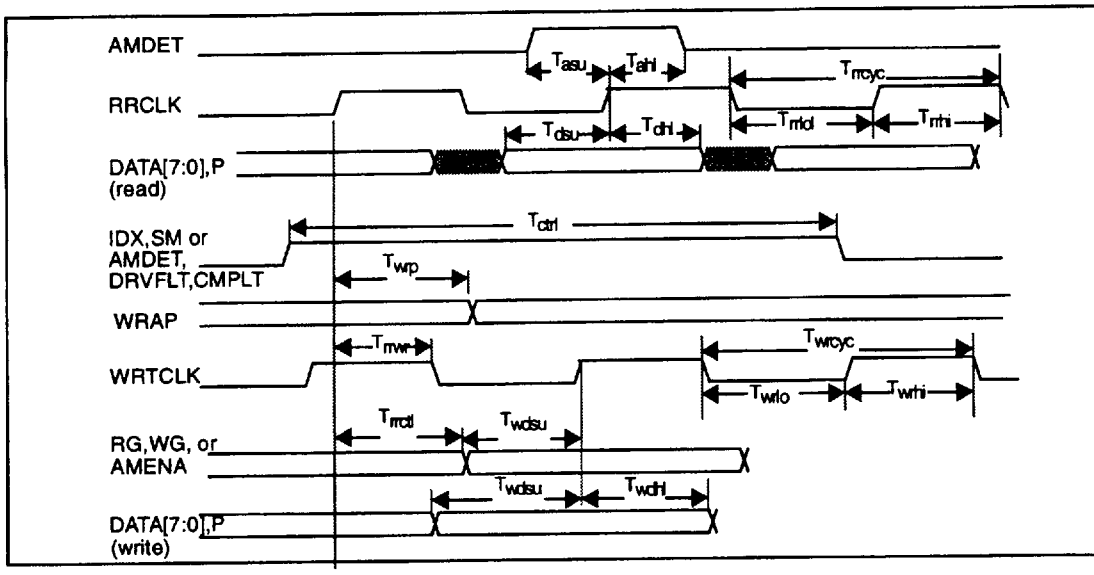

FIGURE 7-8 BASIC DISK INTERFACE CONTROL TIMING

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
T_{asu}	AMDET setup to RRCLK (Tcyc)	10		ns
T_{ahl}	AMDET hold after RRCLK	10		ns
T_{rrcyc}	RRCLK period	100		ns
T_{rrhi}	RRCLK high (Read Gate Active)	30		ns
	RRCLK high (Write Gate Active)	50		
T_{rrlo}	RRCLK low (Read Gate Active)	30		ns
	RRCLK low (Write Gate Active)	30		
T_{dsu}	DATA setup to RRCLK high	10		ns
T_{dhl}	DATA hold from RRCLK high	10		ns
T_{ctrl}	Async pulse width	2 * RRCLK		
T_{wrp}	RRCLK high to WRAP valid	0	T_{rrcyc} - 40	ns
T_{rwr}	RRCLK high to WRTCLK low		30	ns
T_{rrdl}	RRCLK high to new control output		30	ns
T_{wrcyc}	WRTCLK cycle	T_{rrcyc}		
T_{wrlo}	WRTCLK low	T_{rrlo} - 10		
T_{wrhi}	WRTCLK high	T_{rrhi} - 10		
T_{wdsu}	Write Data/Control setup to WRTCLK high	15		
T_{wdhl}	Write Data Hold from WRTCLK high	15		ns

TABLE 7-5 BASIC DISK INTERFACE CONTROL TIMINGS

7.3.2 Disk Bus Turnaround Timing

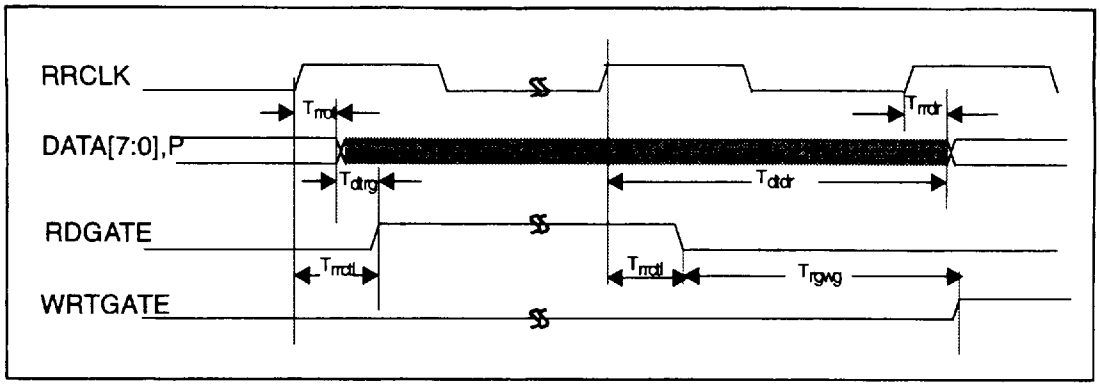

FIGURE 7-9 DISK BUS TURNAROUND TIMING

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
T_{rrdl}	RRCLK to RDGATE		30	ns
T_{rrdt}	RRCLK to Disk Data bus tristate		30	ns
T_{dtrg}	Disk Data Bus Tristate to RDGATE	0		ns
T_{dtdr}	RRCLK to Data bus driven after RDG	T_{rrcyc} -T_{rrdl}	T_{rrcyc}+T_{rrdr}	ns
T_{rgwrg}	RDGATE to next WRTGATE	T_{rrcyc}		ns
T_{rrdr}	RRCLK to Disk Data bus driven		20ns	ns

TABLE 7-6 DISK BUS TURNAROUND TIMINGS

7.4 BUFFER BUS TIMING

SYMBOL	PARAMETER	FIGURES	MINIMUM	UNITS
T_{crp}	CASB high to RAS low	9-10,9-12,9-13	5 * T_{cycb}-0	ns
T_{rcd}	RASB low to CAS low *Note1	9-10,9-12,9-13	A * T_{cycb}-10	ns
T_{csh}	CASB hold after RAS low	9-10,9-12,9-13	4 * T_{cycb}-10	ns
T_{cp}	CASB high pulse width *Note2	9-12,9-13	B * T_{cycb}-10	ns
T_{cas}	CASB low pulse width *Note3	9-10,9-12,9-13	C * T_{cycb}-10	ns
T_{rsh}	RASB hold time after CASB high	9-10,9-12,9-13	1 * T_{cycb}-10	ns
T_{wcs}	MEMWB low to CASB low	9-10, 9-12	1 * T_{cycb}-10	ns
T_{asr}	Row Address setup before RASB low	9-10,9-11, 9-12, 9-13	1 * T_{cycb}- 10	ns
T_{rah}	Row Address hold after RASB low	9-10,9-12,9-13	1 * T_{cycb}-10	ns
T_{asc}	Column Address setup to CASB low	9-10,9-12,9-13	1 * T_{cycb}-10	ns
T_{cah}	Column Address Hold after CAS low	9-10,9-12,9-13	2 * T_{cycb}-10	ns
T_{ds}	Write Data setup to CASB low	9-10,9-12	1 * T_{cycb}-10	ns
T_{dh}	Write Data hold to CASB low	9-10,9-12	2 * T_{cycb}-10	ns
T_{rras}	RAS width (refresh)	9-11	5 *T_{cycb}-10	ns
T_{rr}	RAS recovery (refresh)	9-10,9-12	4 *T_{cycb}-10	ns
T_{rrah}	Row Address hold after RAS low	9-11	4 * T_{cycb}-10	ns
T_{ww}	MEMWB width	9-10,9-12	4 *T_{cycb}-10	ns
T_{wsuc}	MEMWB setup to CASB low	9-10,9-13	1 * T_{cycb}-10	ns
T_{wch}	MEMWB hold after CASB low	9-10,9-12	3* T_{cycb}-10	ns
Tdvc	Read Data setup to CASB high	9-10,9-13	12	ns
Tdzc	Read Data hold after CASB high	9-10,9-13	0	ns
Note 1: This timing is programmable (A = 2 or 3) using RASH bit in MSPD register				
Note 2: This timing is programmable (B = 1 or 2) using CASH bit in MSPD register.				
Note 3: This timing is programmable (C = 2, 3, 4, 5) using CASL[1:0] bits in MSPD register.				

TABLE 7-7 BUFFER INTERFACE TIMING PARAMETERS

7.4.1 DMA Read/ Write RAS/CAS Cycle

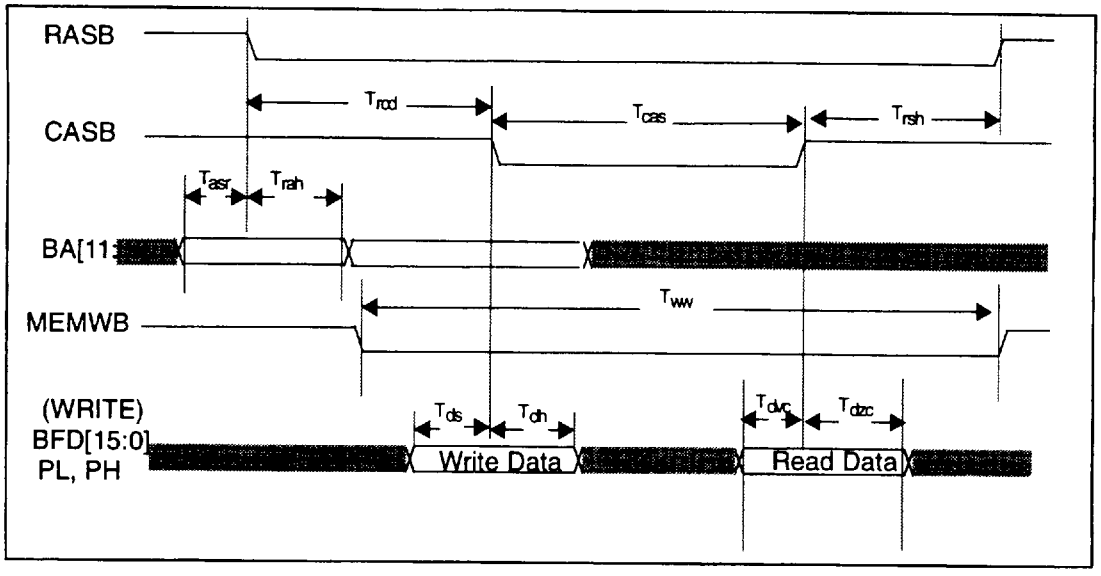

FIGURE 7-10 DMA Read/Write RAS/CAS TIMING

7.4.2 Memory Refresh Cycle

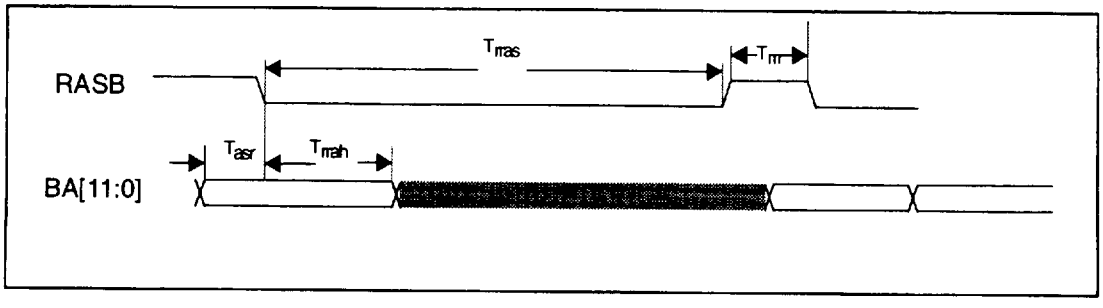

FIGURE 7-11 MEMORY REFRESH CYCLE

7.4.3 Fast Page Write Mode

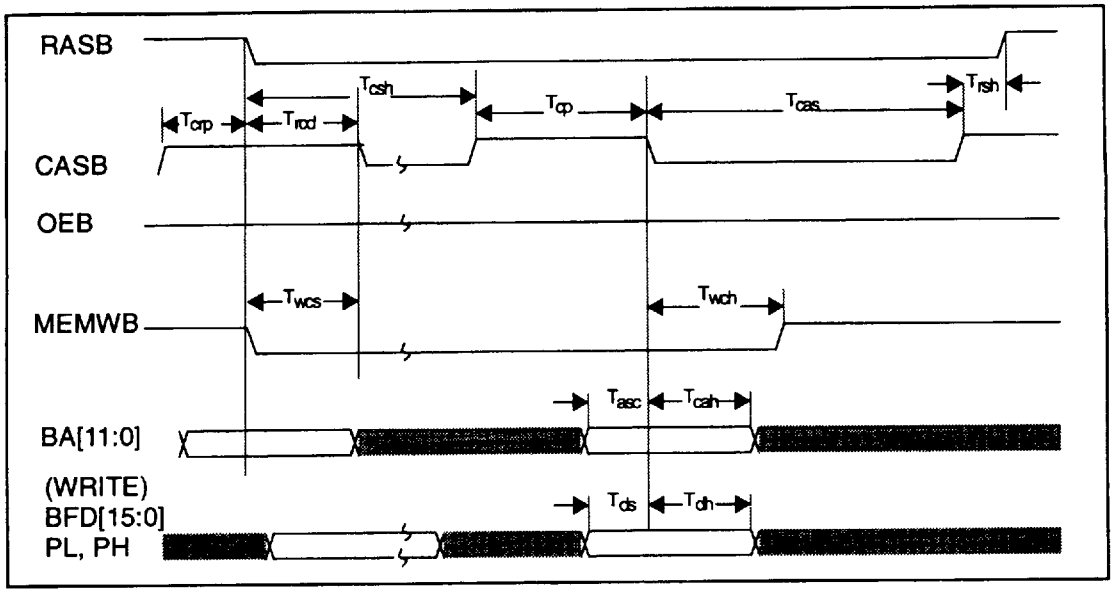

FIGURE 7-12 FAST PAGE WRITE TIMING

7.4.4 Fast Page Read Mode

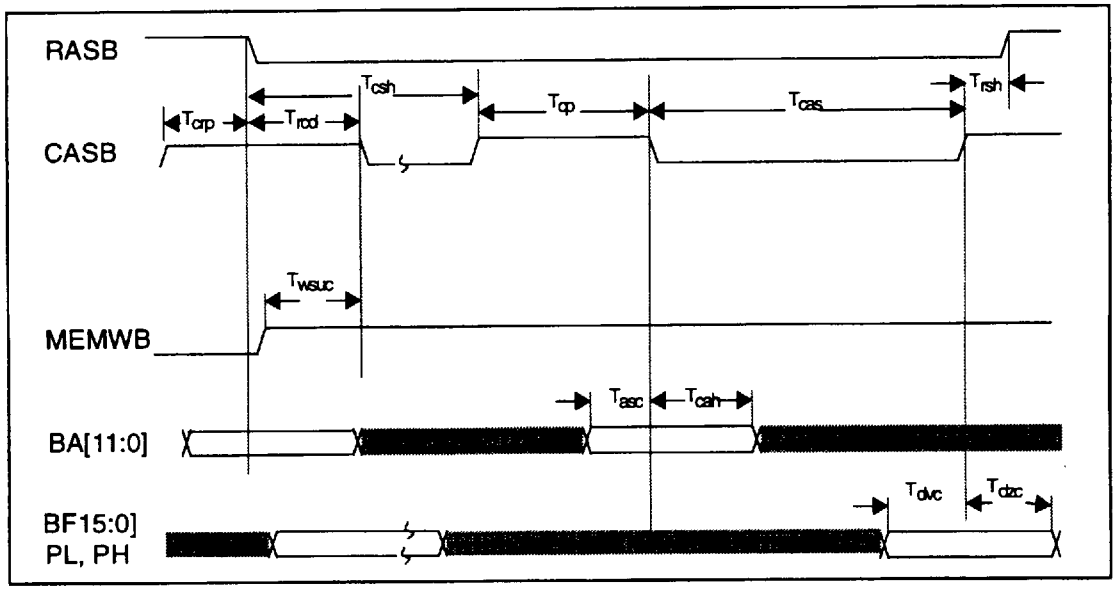

FIGURE 7-13 FAST PAGE READ TIMING

7.5 SCSI BUS TIMING

7.5.1 Initiator Asynchronous In

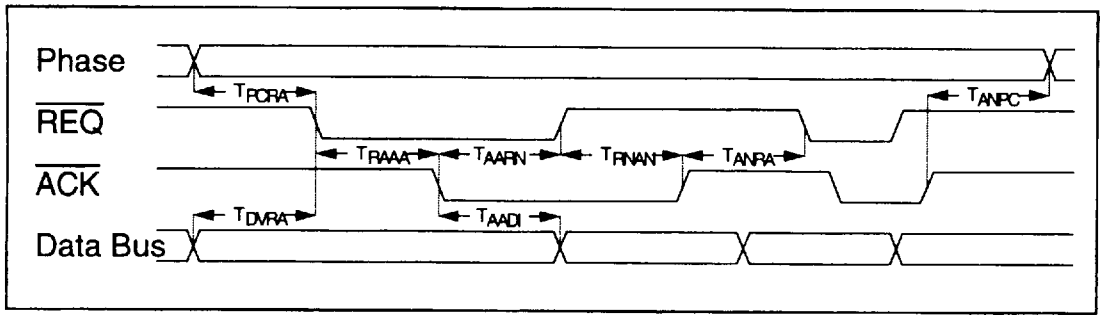

FIGURE 7-14 INITIATOR ASYNCHRONOUS IN

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNITS
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	R	20		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	R	0		ns
T_{RAAA}	$\overline{REQ}$ asserted to $\overline{ACK}$ asserted[a]	S	$3\times T_{CYCS}+4$	$4\times T_{CYC}+40$	ns
T_{AARN}	$\overline{ACK}$ asserted to $\overline{REQ}$ negated	R	0		ns
T_{RNAN}	$\overline{REQ}$ negated to $\overline{ACK}$ negated	S	$2\times T_{CYCS}+4$	$4\times T_{CYC}+40$	ns
TANRA	ACK negated to REQ asserted	R	0		ns
TDVRA	Data valid to REQ asserted	R	10		ns
TAADI	ACK asserted to data invalid	R	0		ns

FIGURE 7-15 INITIATOR ASYNCHRONOUS IN

a. Assumes FIFO not empty

7.5.2 Initiator Asynchronous Out

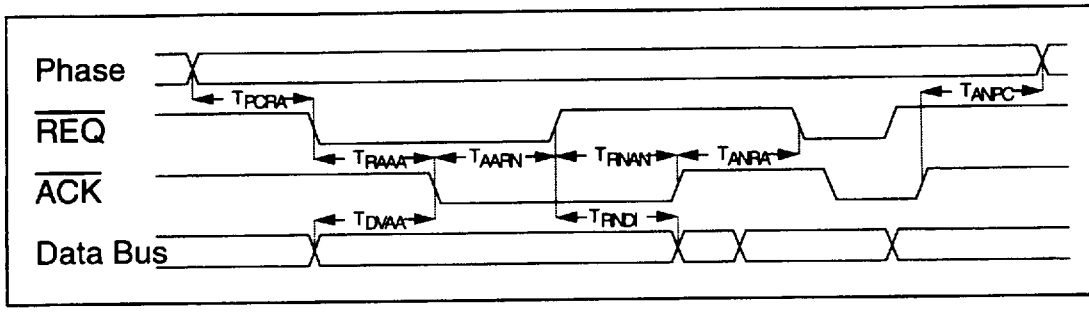

FIGURE 7-16 INITIATOR ASYNCHRONOUS OUT

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	R	20		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	R	0		ns
T_{RAAA}	$\overline{REQ}$ asserted to $\overline{ACK}$ asserted[a]	S	$3 \times T_{CYCS}+4$	$4 \times T_{CYCS}+40$	ns
T_{AARN}	$\overline{ACK}$ asserted to $\overline{REQ}$ negated	R	0		ns
T_{RNAN}	$\overline{REQ}$ negated to $\overline{ACK}$ negated	S	$3 \times T_{CYCS}+4$	$4 \times T_{CYCS}+40$	ns
T_{ANRA}	$\overline{ACK}$ negated to $\overline{REQ}$ asserted	R	0		ns
T_{DVAA}	Data valid to $\overline{ACK}$ asserted	S	T_{ST}[b]-45[c] TR_{AAA}[d]		ns
T_{RNDI}	$\overline{REQ}$ negated to data invalid	S	0		ns

FIGURE 7-17 INITIATOR ASYNCHRONOUS OUT

a. Assumes FIFO not empty
b. T_{ST} = SCLK x T_{CYC}
c. First transfer of a burst
d. Subsequent transfers of a burst

7.5.3 Initiator Synchronous In

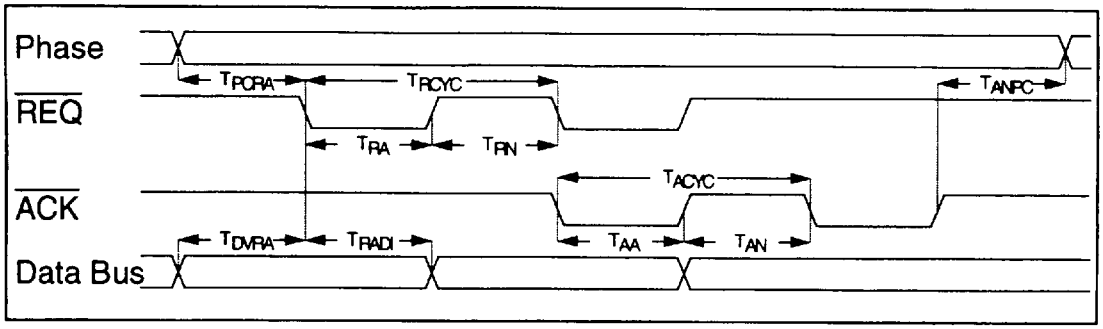

FIGURE 7-18 INITIATOR SYNCHRONOUS IN

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNITS
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	R	20		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	R	0		ns
T_{RCYC}	$\overline{REQ}$ cycle time	R	$4 \times T_{CYCS}$		ns
T_{RA}	$\overline{REQ}$ asserted width	R	30		ns
T_{RN}	$\overline{REQ}$ negated width	R	30		ns
T_{DVRA}	Data valid to $\overline{REQ}$ asserted	R	10		ns
T_{RADI}	$\overline{REQ}$ asserted to data invalid	R	15		ns
T_{ACYC}	$\overline{ACK}$ cycle time[a]	S	$a \times T_{CYCS}$	$a \times T_{CYCS}$	ns
T_{AA}	$\overline{ACK}$ asserted width[b]	S	$A \times T_{CYCS}-10$	$A \times T_{CYCS}+10$	ns
T_{AN}	$\overline{ACK}$ negated width[c]	S	$N \times T_{CYCS}-10$	$N \times T_{CYCS}+10$	ns

TABLE 7-8 INITIATOR SYNCHRONOUS IN

a. a = (SCLKA+2) + (SCLKN+2); SCLKA and SCLKN are programming parameters in SPW (SCSI Pulse Width) Register
b. A=SCLKA+2
c. N=SCLKN+2

7.5.4 Initiator Synchronous Out

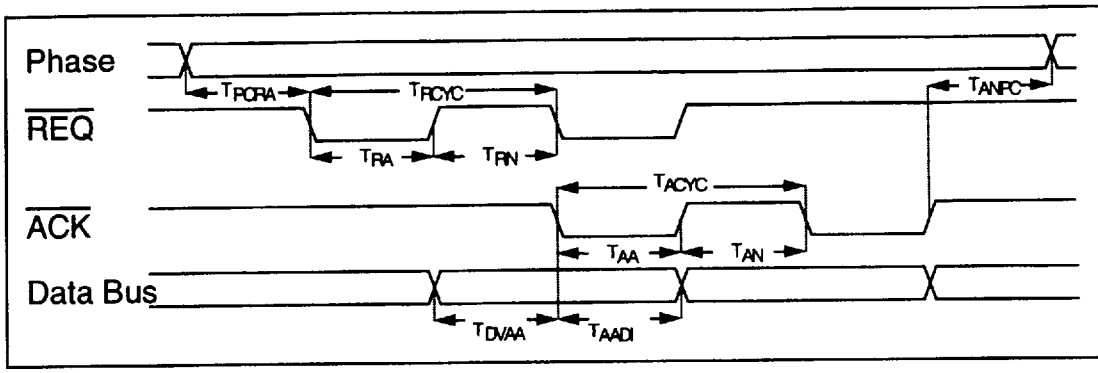

FIGURE 7-19 INITIATOR SYNCHRONOUS OUT

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	R	20		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	R	0		ns
T_{RCYC}	$\overline{REQ}$ cycle time	R	$4 \times T_{CYCS}$		ns
T_{RA}	$\overline{REQ}$ asserted width	R	30		ns
T_{RN}	$\overline{REQ}$ negated width	R	30		ns
T_{ACYC}	$\overline{ACK}$ cycle time[a]	S	$4 \times T_{CYCS}$	$18 \times T_{CYCS}$	ns
T_{AA}	$\overline{ACK}$ asserted width[b]	S	$A \times T_{CYCS}-10$	$A \times T_{CYCS}+10$	ns
T_{AN}	$\overline{ACK}$ negated width[c]	S	$N \times T_{CYCS}-10$	$N \times T_{CYCS}+10$	ns
T_{DVAA}	Data valid to $\overline{ACK}$ asserted	S	$T_{ST}-45$[d] $T_{AN}-21$[e]		ns
T_{AADI}	$\overline{ACK}$ asserted to data invalid	S	T_{AA}		ns

TABLE 7-9 INITIATOR ASYNCHRONOUS OUT

a. a = (SCLKA+2) + (SCLKN+2); SCLKA and SCLKN are programming parameters in SPW (SCSI Pulse Width) Register
b. A=SCLKA+2
c. N=SCLKN+2
d. First transfer of a burst
e. Subsequent transfers of a burst

7.5.5 Target Asynchronous In

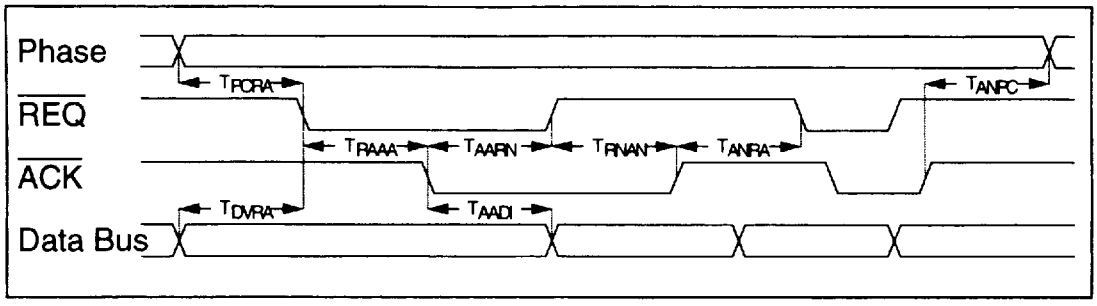

FIGURE 7-20 TARGET ASYNCHRONOUS IN

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	S	$4xT_{ST}$[a] $8xT_{ST}$[b]		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	S	0		ns
T_{RAAA}	$\overline{REQ}$ asserted to $\overline{ACK}$ asserted	R	0		ns
T_{AARN}	$\overline{ACK}$ asserted to $\overline{REQ}$ negated	S	$3xT_{CYCS}+4$	$4xT_{CYCS}$ +24	ns
T_{RNAN}	$\overline{REQ}$ negated to $\overline{ACK}$ negated	R	0		ns
T_{ANRA}	$\overline{ACK}$ negated to $\overline{REQ}$ asserted	S	$3xT_{CYCS}+4$	$4xT_{CYCS}$ +24	ns
T_{DVRA}	Data valid to $\overline{REQ}$ asserted	S	T_{ST}[c]-45[d] T_{ANRA}[e]		ns
T_{AADI}	$\overline{ACK}$ asserted to data invalid	S	0		ns

FIGURE 7-21 TARGET ASYNCHRONOUS IN

a. Preceding phase was an in phase
b. Preceding phase was an out phase
c. T_{ST} = SCLK x T_{CYCS}
d. First transfer of a burst
e. Subsequent transfers of a burst

7.5.6 Target Asynchronous Out

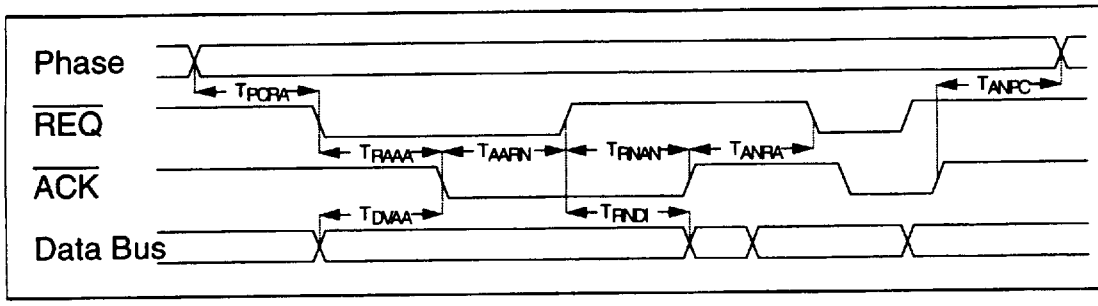

FIGURE 7-22 TARGET ASYNCHRONOUS OUT

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	S	$4 \times T_{ST}$		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	S	0		ns
T_{RAAA}	$\overline{REQ}$ asserted to $\overline{ACK}$ asserted	R	0		ns
T_{AARN}	$\overline{ACK}$ asserted to $\overline{REQ}$ negated	S	$3 \times T_{CYCS}+4$	$4 \times T_{CYCS}+24$	ns
T_{RNAN}	$\overline{REQ}$ negated to $\overline{ACK}$ negated	R	0		ns
T_{ANRA}	$\overline{ACK}$ negated to $\overline{REQ}$ asserted	S	$3 \times T_{CYCS}+4$	$4 \times T_{CYCS}+24$	ns
T_{DVAA}	Data valid to $\overline{ACK}$ asserted	R	10		ns
T_{ANDI}	$\overline{REQ}$ negated to data invalid	R	0		ns

TABLE 7-10 TARGET ASYNCHRONOUS OUT

7.5.7 Target Synchronous In

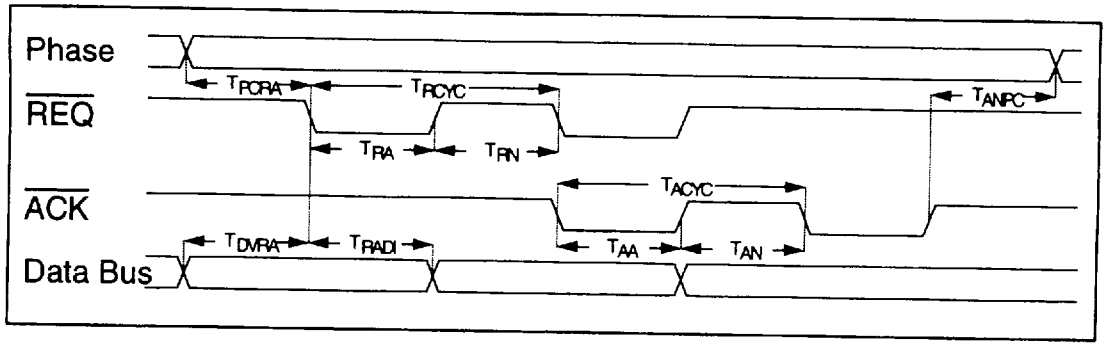

FIGURE 7-23 TARGET SYNCHRONOUS IN

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNITS
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	S	$4\times T_{ST}$[a] $8\times T_{ST}$[b]		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	S	0		ns
T_{RCYC}	$\overline{REQ}$ cycle time[c]	S	$a\times T_{CYCS}$	$a\times T_{CYCS}$	ns
T_{RA}	$\overline{REQ}$ asserted width[d]	S	$A\times T_{CYCS}$-10	$A\times T_{CYCS}$+10	ns
T_{RN}	$\overline{REQ}$ negated width[e]	S	$N\times T_{CYCS}$-10	$N\times T_{CYCS}$+10	ns
T_{DVRA}	Data valid to $\overline{REQ}$ asserted	S	T_{ST}-45[f] $N\times T_{CYCS}$-21[e]		ns
T_{RADI}	$\overline{REQ}$ asserted to data invalid	S	$A\times T_{CYCS}$+10		ns
T_{ACYC}	$\overline{ACK}$ cycle time	R	$4\times T_{CYCS}$		ns
T_{AA}	$\overline{ACK}$ asserted width	R	30		ns
T_{AN}	$\overline{ACK}$ negated width	R	30		ns

TABLE 7-11 TARGET SYNCHRONOUS IN

a. Preceding phase was an in phase
b. Preceding phase was an out phase
c. a = (SCLKA+2) + (SCLKN+2); SCLKA and SCLKN are programming parameters in SPW (SCSI Pulse Width) Register
d. First transfer of a burst - A = SCLK +2
e. N = SCLKN +2
f. First transfer of a burst

7.5.8 Target Synchronous Out

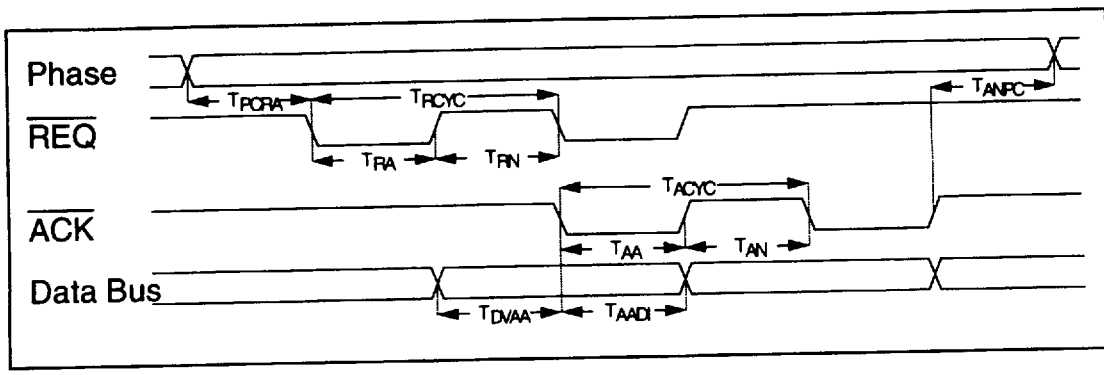

FIGURE 7-24 TARGET SYNCHRONOUS OUT

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{PCRA}	Phase change to $\overline{REQ}$ asserted	S	$4T_{ST}$		ns
T_{ANPC}	$\overline{ACK}$ negated to phase change	S	0		ns
T_{RCYC}	$\overline{REQ}$ cycle time[a]	S	$a \times T_{CYCS}$	$a \times T_{CYCS}$	ns
T_{RA}	$\overline{REQ}$ asserted width[b]	S	$A \times T_{CYCS}-10$	$A \times T_{CYCS}+10$	ns
T_{RN}	$\overline{REQ}$ negated width[c]	S	$N \times T_{CYCS}-10$	$N \times T_{CYCS}+10$	ns
T_{ACYC}	$\overline{ACK}$ cycle time	R	$4 \times T_{CYCS}$		ns
T_{AA}	$\overline{ACK}$ asserted width	R	30		ns
T_{AN}	$\overline{ACK}$ negated width	R	30		ns
T_{DVAA}	Data valid to $\overline{ACK}$ asserted	R	10		ns
T_{AADI}	$\overline{ACK}$ asserted to data invalid	R	15		ns

TABLE 7-12 TARGET SYNCHRONOUS OUT

a. a = (SCLKA+2) + (SCLKN+2); SCLKA and SCLKN are programming parameters in SPW (SCSI Pulse Width) Register
b. A=SCLKA+2
c. N=SCLKN+2

7.6 GENERAL CLOCK TIMING

7.6.1 Input Clock Timing (BCLK)

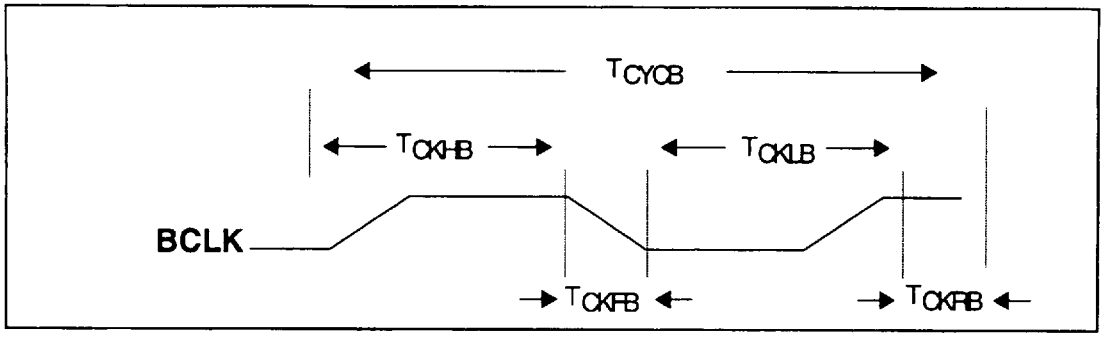

FIGURE 7-25 INPUT CLOCK TIMING (BCLK)

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{CYCB}	Input Clock Period	R	20	50	ns
T_{CKHB}	Input Clock High Pulse Width	R	5		ns
T_{CKLB}	Input Clock Low Pulse Width	R	5		ns
T_{CKRB}	Input Clock Rise Time	R		5	ns
T_{CKFB}	Input Clock Fall Time	R		5	ns

TABLE 7-13 INPUT CLOCK TIMING (BCLK)

7.6.2 Input Clock Timing (SCLK)

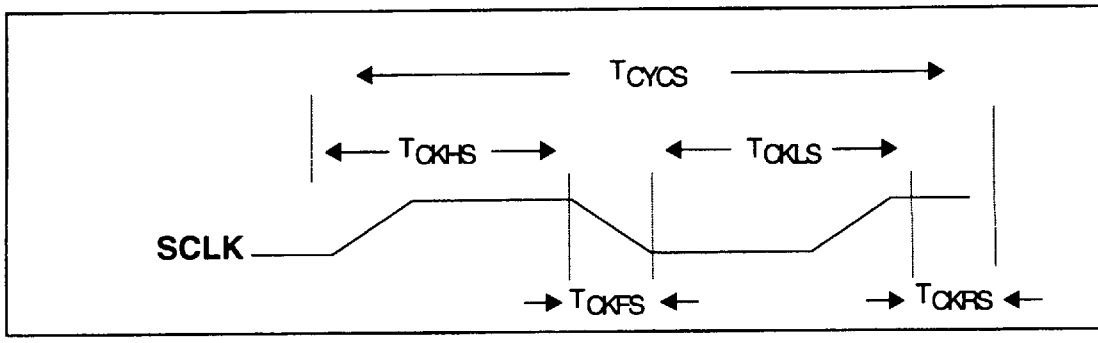

FIGURE 7-26 INPUT CLOCK TIMING (SCLK)

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{CYCS}	Input Clock Period	R	25	50	ns
T_{CKHS}	Input Clock High Duty Cycle[a]	R	40%	60%	
T_{CKLS}	Input Clock Low Duty Cycle[a]	R	40%	60%	
T_{CKRS}	Input Clock Rise Time	R		5	ns
T_{CKFS}	Input Clock Fall Time	R		5	ns

TABLE 7-14 INPUT CLOCK TIMING (SCLK)

a. Duty cycle is measured at V_{CH} min as a percent of clock period.

7.6.3 Hardware and Software Reset

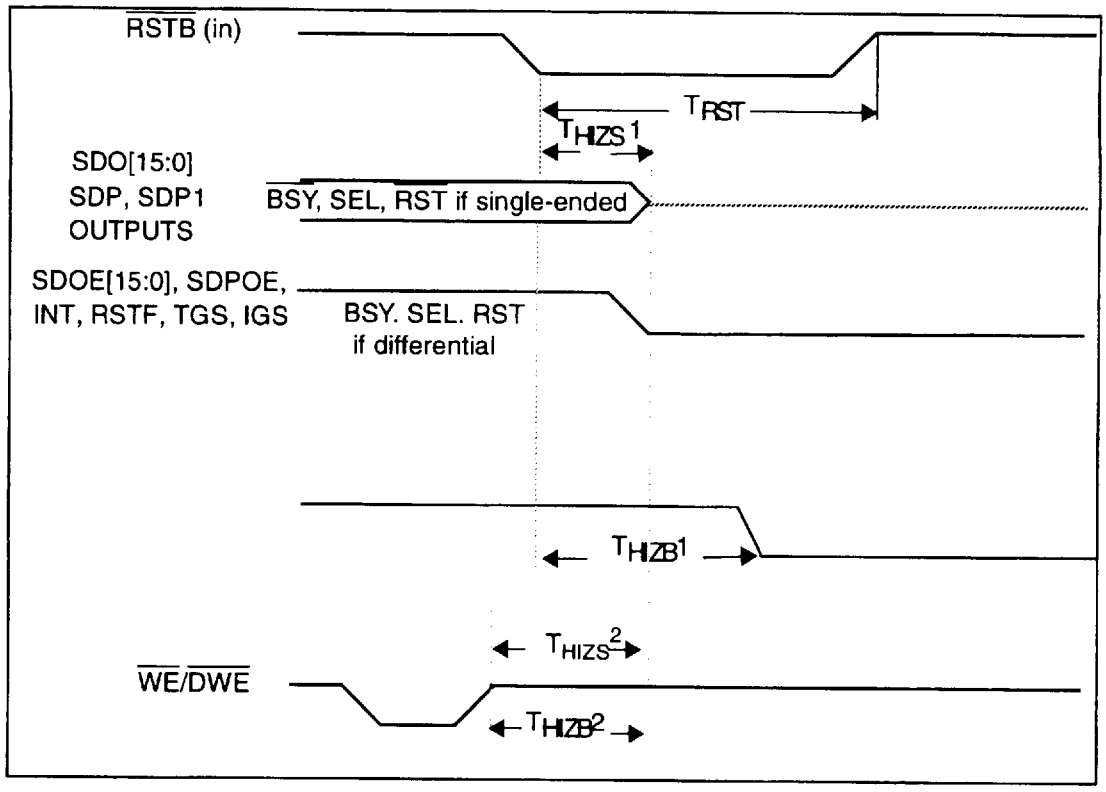

FIGURE 7-27 HARDWARE AND SOFTWARE RESET

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{RST}	Reset Pulse Width[a]	R	400		ns
T_{HZS1}	Output Inactive/High-Impedance After L.E. of RSTB on all single-ended SCSI pins	S		4 x T_{CYCS}	
T_{HZS2}	Micro write to CRST to output inactive after T.E. of WE/DWE	S		10 x T_{CYCS}	
T_{HZB1}	Output Inactive/High-Impendance after L.E. RSTB on all buffer/disk outputs			8 x T_{CYCB}	
T_{HZB2}	Microprocessor Write to CFG1 Register			8 x T_{CYCB}	

TABLE 7-15 HARDWARE AND SOFTWARE RESET

a. TheSCSI section won't recognize the reset pulse if the reset pulse width is less than 2 x T_{CYCS}.

7.6.4 SCSI Reset

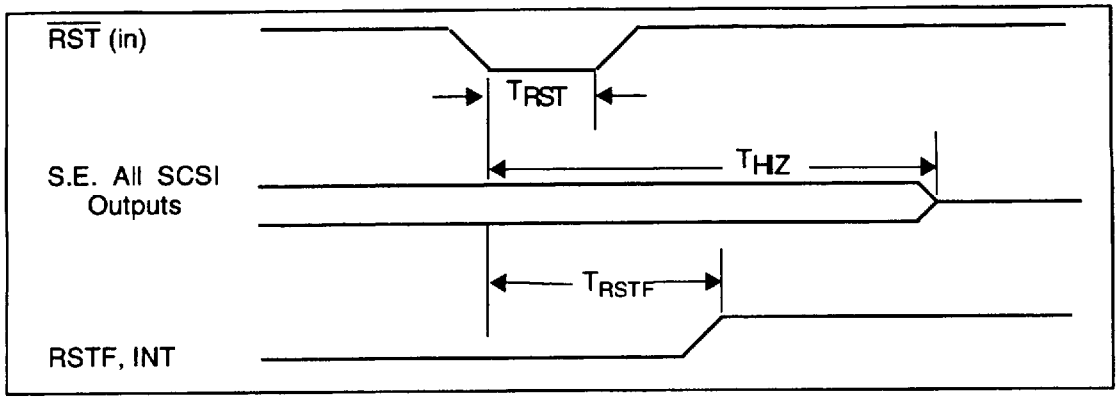

FIGURE 7-28 SCSI RESET

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{HZ}	LE of $\overline{RST}$ low to all SCSI outputs released/tristate	S		3	T_{ST}
T_{RST}	$\overline{RST}$ minimum pulse width	R	5		T_{ST}
T_{RSTF}	LE of $\overline{RST}$ low to RSTF and INT asserted	S		2	T_{ST}

TABLE 7-16 SCSI RESET

7.6.5 Interrupt and SCSI Reset Follower

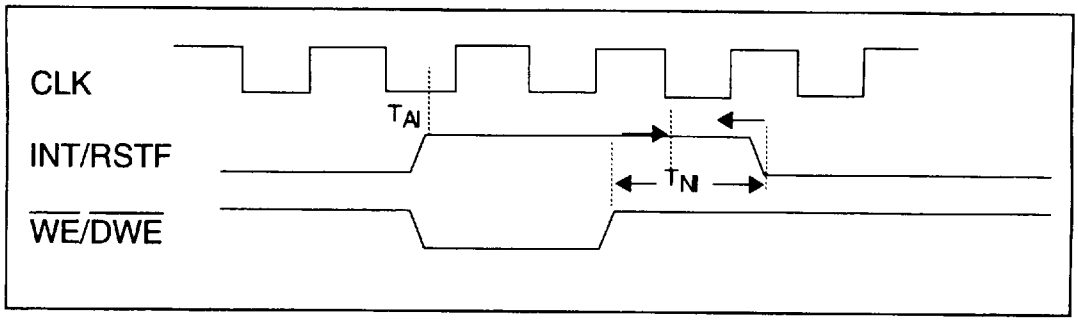

FIGURE 7-29 INTERRUPT AND SCSI RESET FOLLOWER

SYMBOL	PARAMETER	R/S	MINIMUM	MAXIMUM	UNIT
T_{AI}	$\overline{INT}$ Asserted After Rising Edge of CLK	S		100	ns
T_{NI}	$\overline{INT}$ Negated After Micro Clear	S		200	ns

TABLE 7-17 INTERRUPT AND SCSI RESET FOLLOWER

8.0 PACKAGE DIMENSION

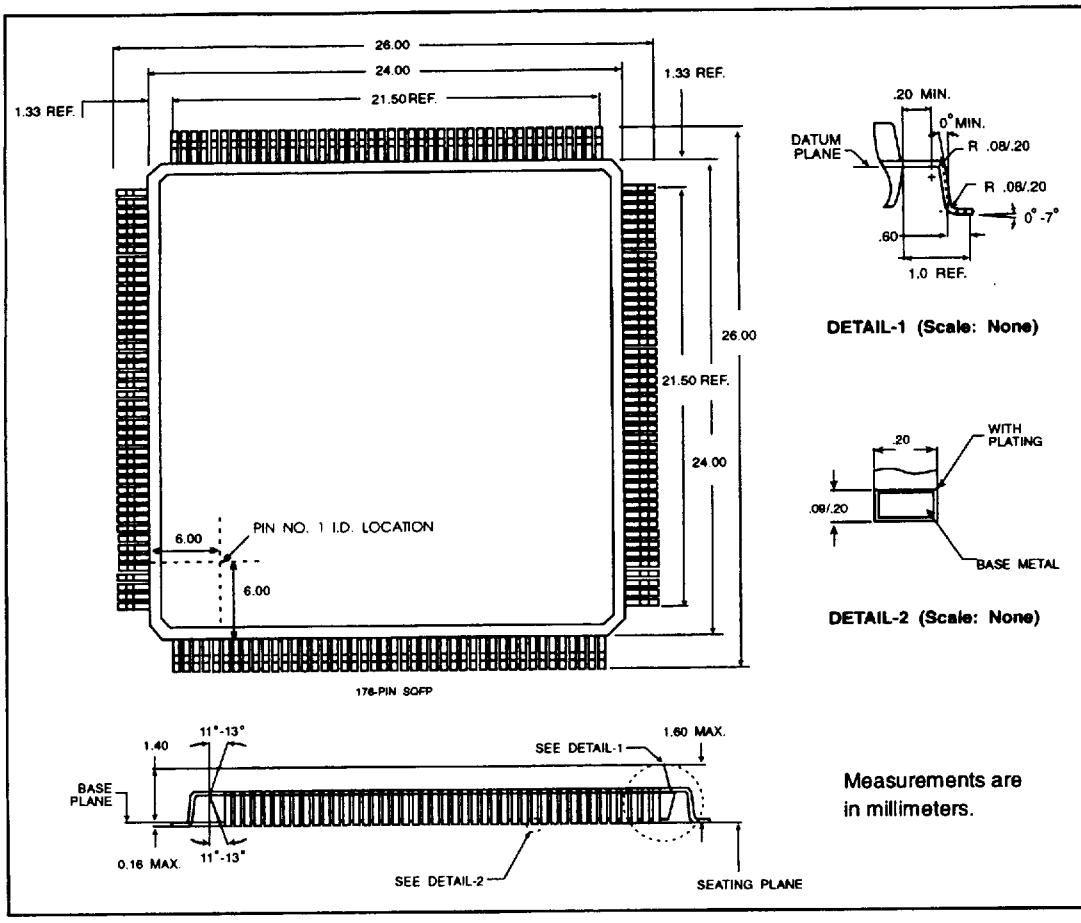

FIGURE 8-1 176-PIN SQFP

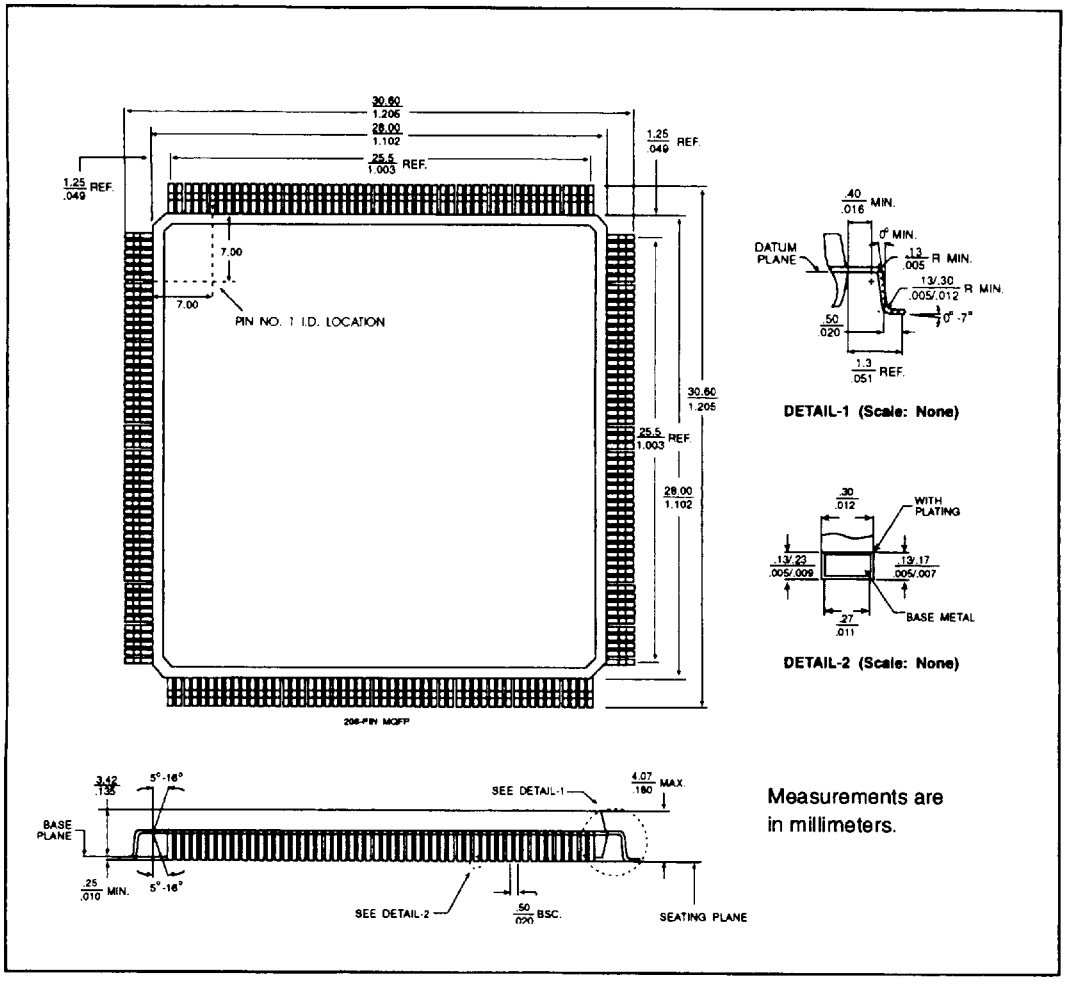

FIGURE 8-2 208-PIN MQFP