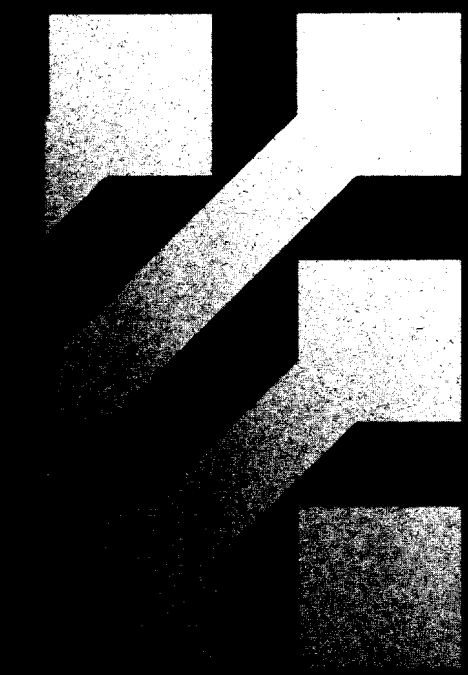
T-52-33-45

WD90C33 High Performance VGA Controller Chip for PC/AT/ISA/EISA/VESA and PS/2 Systems (Advanced Information)



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1.0 INTRODUCTION

The Western Digital® WD90C33 High Performance VGA Controller is a 0.8 micron CMOS VLSI device that provides GUI for WINDOWS. The WD90C33 supports hardware Bit Block Transfers (BITBLT), line draw, cursor, while maintaining backward compatibility with previous standards such as MDA, EGA, CGA, Hercules, and AT&T 6300. Designs that use the WD90C33 controller are able to run applications requiring VGA hardware and BIOS compatibility and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode. The WD90C33 supports high resolution graphics with 1024 by 768 dot resolution and 256 colors. The WD90C33 also supports 132-column text mode and 6-16 pixel fonts.

This data sheet provides a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package information and associated references.

1.1 FEATURES

The WD90C33 provides the following features:

- A full-function VGA controller optimized for windows.
- Built-in interface with 32-bit 386/486 local bus
- Built-in interface with VESA local bus
- Integrated bus interface for AT and Micro-Channel with minimum external component support.
- True 32-bit host-to-display memory data transfers in graphics modes
- Hardware BITBLT for 4-bit, 8-bit, and 16-bit color modes.
  - Pattern Fill
  - Raster Operations
  - Transparency
  - Color Expansion for Text Support
  - Filled Rectangles
  - 32-Bit Memory or I/O Port imaging transfer to or from host.
  - X/Y Addressing
- Hardware assisted Line Draw for 4-bit, 8-bit, and 16-bit color modes.
  - Bresenham Line Algorithm
  - Strip Line Algorithm
  - X/Y Addressing with Clipping
- Hardware assisted trapezoidal fill
- Hardware assisted rectangular clipping
- Command Buffer eight levels deep
- BITBLT pipeline 4 levels deep.
- True 24-bit color with limited BITBLT hardware support.
- Host Bit Block Transfers (HBLT) supports memory mapped 32-bit transfers through the write buffer.
- Allows the CPU to access the display memory while the drawing engine is active.
- Supports up to:
  - 1024 x 768 x 256 color
  - 640 x 480 x 64K color
  - 640 x 480 x 16 million color
  - 1280 x 1024 x 256 color interlaced
- Hardware Cursor.
  - 64 by 64 pixels or 32 by 32 pixels
  - Inversion and transparency
  - Two color and three color modes
- Provides a single chip video graphics solution for IBM AT and PS/2 compatible systems.
- Supports up to 2M bytes of display memory with two 64K by 16 DRAMs; four, eight, or sixteen 256K by 4 DRAMs; or one, two, or four 256K by 16 DRAMs
- Fully compatible with IBM's VGA and EGA with hidden register support
- Fully compatible with CGA, MDA, Hercules Graphics and AT&T Model 6300 standards
- Supports 132-column text
- Write buffer for zero wait state CPU write performance
- Provides 16-bit or 32-bit memory interface with fast page operations.
- Up to 80 MHz maximum video clock rate.
- Up to 50 MHz maximum memory clock rate.
- Up to four simultaneous displayable fonts.

- From 6 to 16 pixel-wide fonts.
- A maximum of 16 fonts can be loaded.
- Provides adapter video BIOS ROM decoding.
- Eleven-bit vertical counter to support scan resolution of up to 2048 scan lines.
- Supports 16-bit I/O register transfer to index/ data register pairs.
- Adjustable internal display FIFO and fast page memory interface.
- 208-pin MQFP (Metric Quad Flat Package)
- Integrated Feature connector interface and external RAMDAC support.
- Programmable memory mapping register to map WD90C33 into any CPU memory address space
- Separate host address and data to save external glue logic (For AT and CPU local bus.)
- True color, 24-bit hardware cursor.
- Supports 256Kx16 DRAM with four CAS strobes and one write strobe.

2.0 WD90C33 ARCHITECTURE

The WD90C33 contains the System Interface and the following six major internal modules (see Figure 2-1):

- CRT Controller
- Clock Controller
- Video Control
- Cursor Control
- DRAM Control
- Drawing Engine

An internal write buffer is used to achieve fast memory write. A zero wait state may be achieved with a 32-bit video memory interface for most memory write operations.

An internal FIFO is used to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

The CRT Controller maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware. The CRT Controller also generates a horizontal sync (HSYNC), vertical sync (VSYNC) and blanking signal for the display monitor.

The Clock Controller functions as a timing generator for the display memory cycles. It provides the character clock in the alphanumeric mode and the dot clock in the graphics mode. The Clock Controller arbitrates between video display refresh, Drawing Engine memory cycle, memory refresh, and CPU access of the video memory. This controller also provides write buffer control.

The Video Control serializes the video memory data into video data stream according to different display formats. It controls blinking, underlining, cursor, pixel panning, reverse video and background or foreground color in all display modes.

The Cursor Control reads in each line of the cursor pattern during the horizontal retrace immediately preceding the scan line on which that line of the cursor pattern is to be displayed. It then merges the cursor pattern into the video stream for the scan line.

The DRAM control provides the video memory interface for memory configurations from 256 Kbytes to 2 Mbytes. The WD90C33 supports 60 ns, 70 ns, 80 ns, and 100 ns DRAMs with a dedicated clock, and provides a choice of page mode or non-page mode operation to access fonts in text modes.

The Drawing Engine generates memory addresses, data masks, and control signals for BITBLT, Line Draw, pattern fill, and other graphics operations.The Drawing Engine also manipulates the data flow between the CPU and the video memory for both CPU write and CPU read cycles. The engine also manipulates display data by doing color compare, color expansion, and data rotation. It contains a 32-bit Arithmetic Logic Unit (ALU) for raster operations.

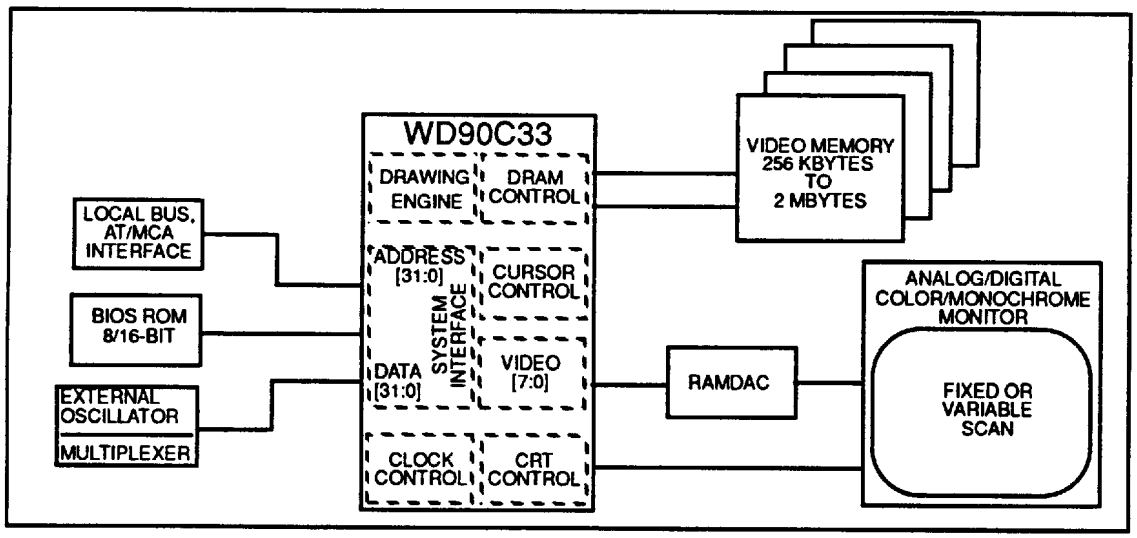


FIGURE 2-1 SYSTEM BLOCK DIAGRAM

3.0 WD90C33 INTERFACES

3.1 INTRODUCTION

This section describes the various interfaces between the WD90C33 Controller and external devices. These include system interfaces such as the CPU (Host) and BIOS ROM, DRAM, video, and clock as indicated in Figure 3-1. In addition this section contains the following figures to show connections between the WD90C33 Controller and the various external devices.

- Figure 3-2. WD90C33 Block Diagram
- Figure 3-3. AT/MicroChannel Bus Subsystem
- Figure 3-4. Local Bus Subsystem Interface
- Figure 3-5. AT Compatible Interface (16-bit) And 8-bit BIOS
- Figure 3-6. AT Compatible Interface (16-bit) And 16-bit BIOS
- Figure 3-7. MicroChannel (16-bit) Interface
- Figure 3-8. Two Or Four 64K by 16 DRAM Interface
- Figure 3-9. Four Or Eight 256K by 4 DRAM Interface
- Figure 3-10. External RAMDAC Interface
- Figure 3-11. TTL Monitor Interface
- Figure 3-12. Clock Interface

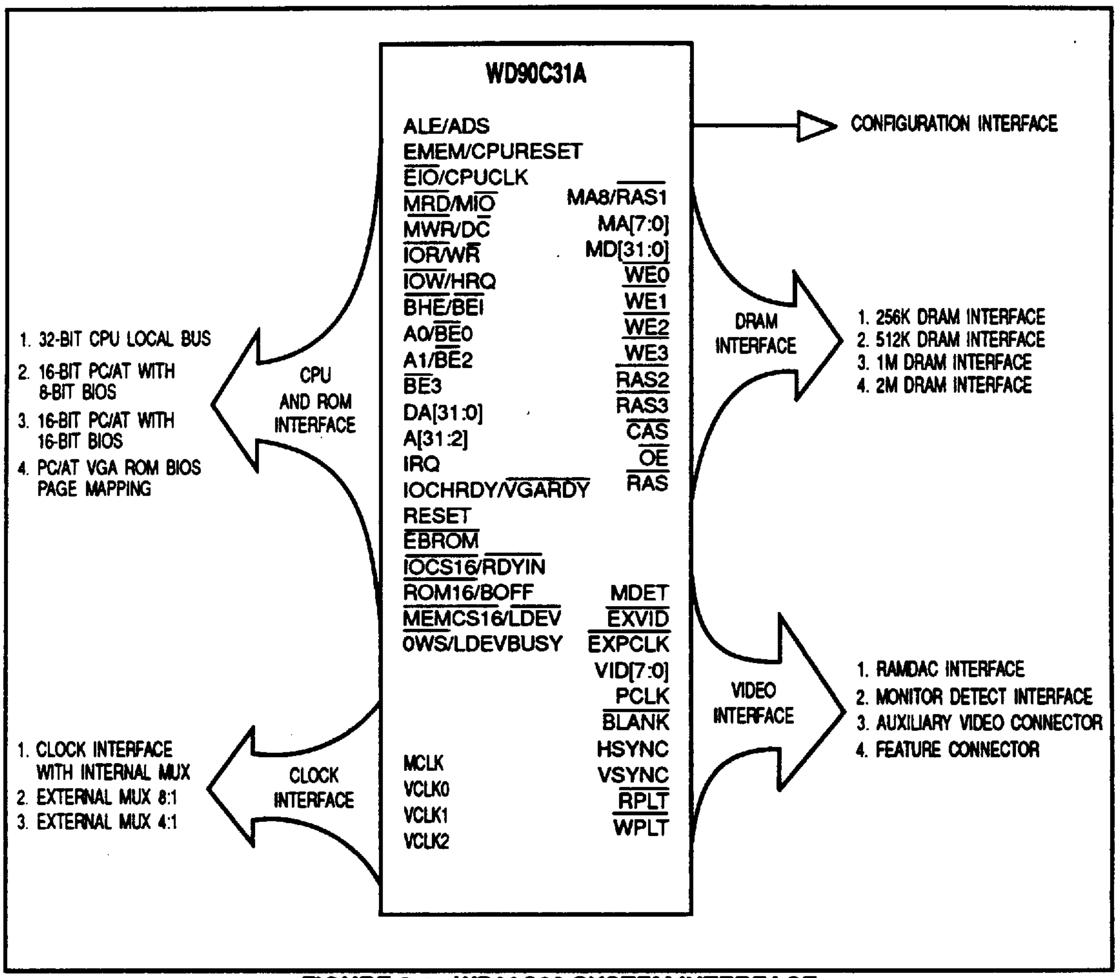


FIGURE 3-1 WD90C33 SYSTEM INTERFACE

3.2 CPU(HOST) AND BIOS ROM INTERFACE

The WD90C33 is designed to interface directly with the 386/486 CPU 32-bit local bus (see Figures 3-2 and 3-3). It also complies with the VESA local bus standard and provides the signals necessary to interface with the VESA connector. The WD90C33 also provides the interface for local bus RAMDAC, BIOS, and clock generator without using glue logic. While connected to the CPU local bus, the WD90C33 allows the user to choose whether to connect the RAMDAC to the local bus or to the system (AT) bus. The WD90C33 also supports RAMDAC write shadowing, and can interface with the video BIOS, which can be integrated with the system BIOS. Selection of the 32-bit local bus interface is determined by the state of Configuration register bit CNF(11) during power-on or system reset as described in Section 9.

The WD90C33 also operates in both the AT Bus and the PS/2 MicroChannel bus architecture configurations (see Figure 3-4). The selection of the bus architecture determines the operating mode, and is selected by the state of Configuration Register bit CNF(2) during power-on or system reset as described in Section 9.

Whether configured for Local Bus, AT, or MicroChannel operation, the WD90C33 operates functionally in a manner that is compatible with the selected interface. The signal pins, memory maps and I/O ports all operate to optimize the selected interface with a minimum of external circuits.

The WD90C33 provides all the signals and decodes all the necessary memory and I/O addresses to interface with the Local bus, AT bus, or the MicroChannel bus in 8-bit or 16-bit data path modes. It also provides the necessary decoding of the adapter video BIOS ROM. Using the provided signals, it is possible to implement designs which operate in 8-bit or 16-bit mode and control an 8-bit or 16-bit BIOS ROM (see Figures 3-5 through 3-7).

The I/O data path is programmable to be either 16-bit or 8-bit. Also, the data path between the CPU and display buffer can be eight or sixteen bits wide for all modes. $\overline{\text{ROM16}}$, $\overline{\text{IOCS16}}$, and $\overline{\text{MEMCS16}}$ signals are generated by the WD90C33 to indicate a 16-bit operation.

The WD90C33 has a display memory write buffer that holds the CPU write data until it can be transferred to the display memory, allowing the CPU to continue. This feature greatly reduces CPU wait states while writing to the video memory.

The WD90C33 provides wait states for CPU accesses to the video memory if necessary.

Special I/O ports such as 46E8h for the AT (or 03C3h for MicroChannel) for setup and 102h for VGA enable, have been implemented internally in the WD90C33.

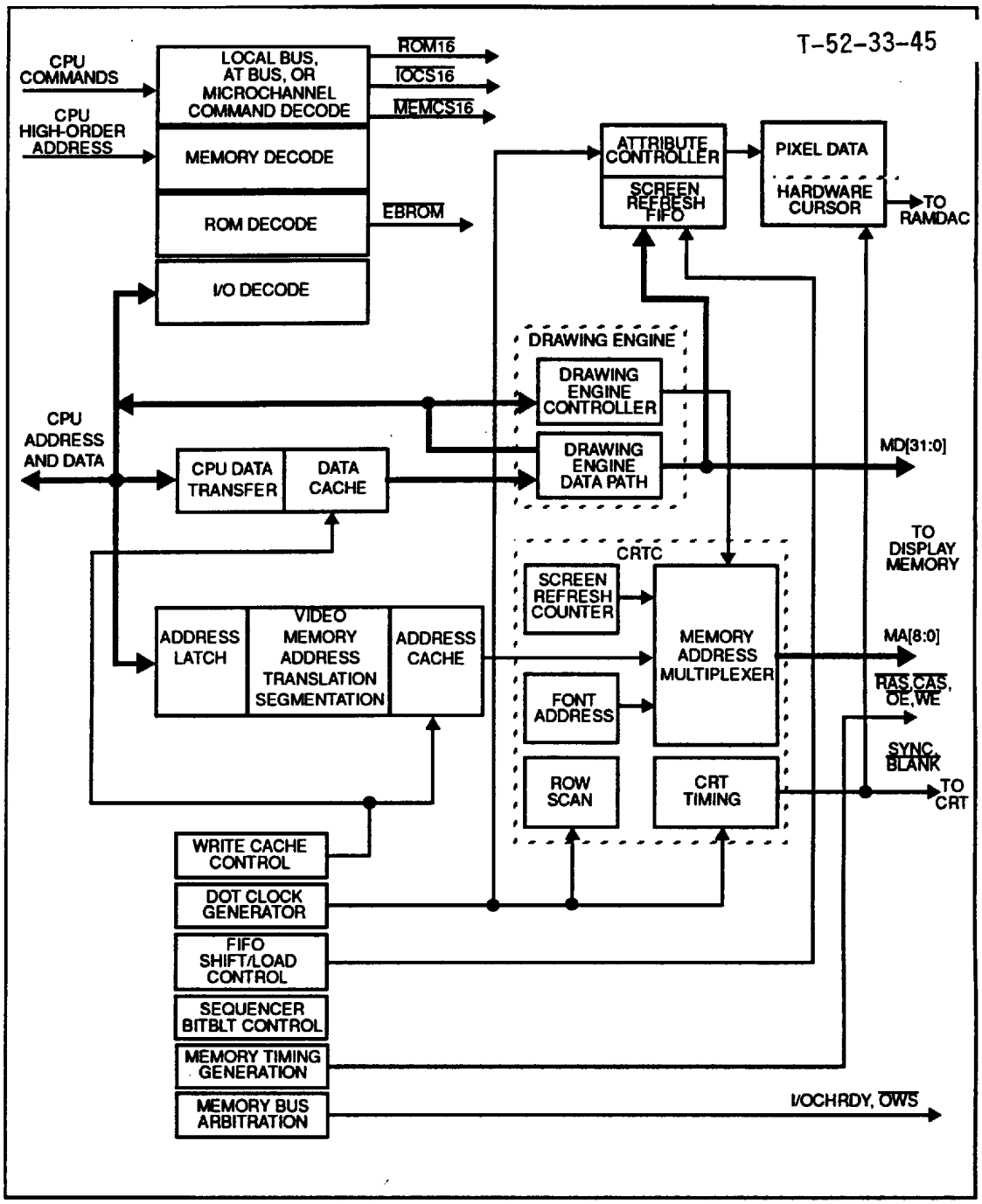
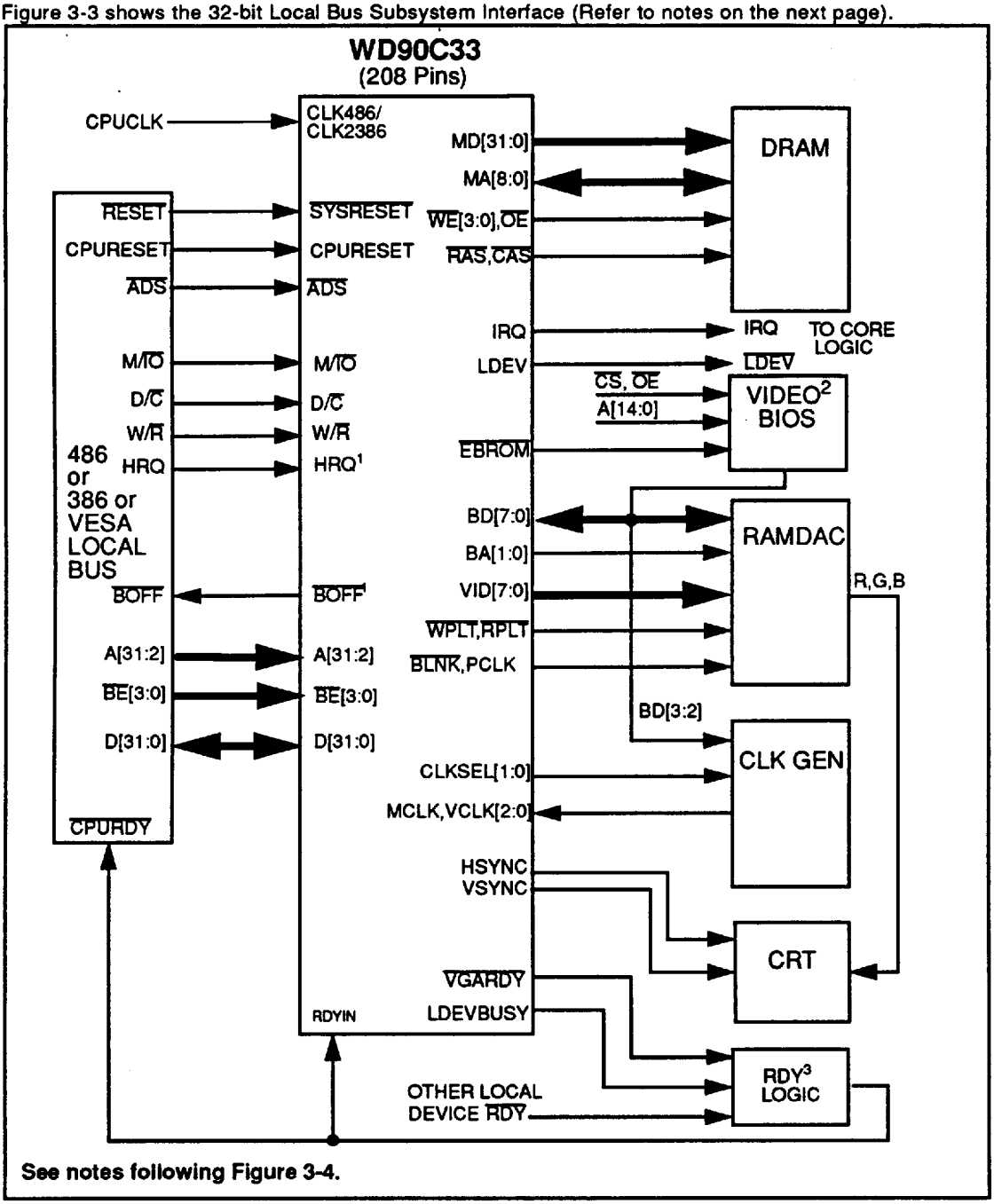


FIGURE 3-2 WD90C33 BLOCK DIAGRAM

3.3 LOCAL BUS VIDEO SUBSYSTEM INTERFACE

Figure 3-3 shows the 32-bit Local Bus Subsystem Interface (Refer to notes on the next page).



See notes following Figure 3-4.

FIGURE 3-3 LOCAL BUS SUBSYSTEM INTERFACE, 32-BIT

Figure 3-4 shows the AT/MicroChannel Bus Subsystem.

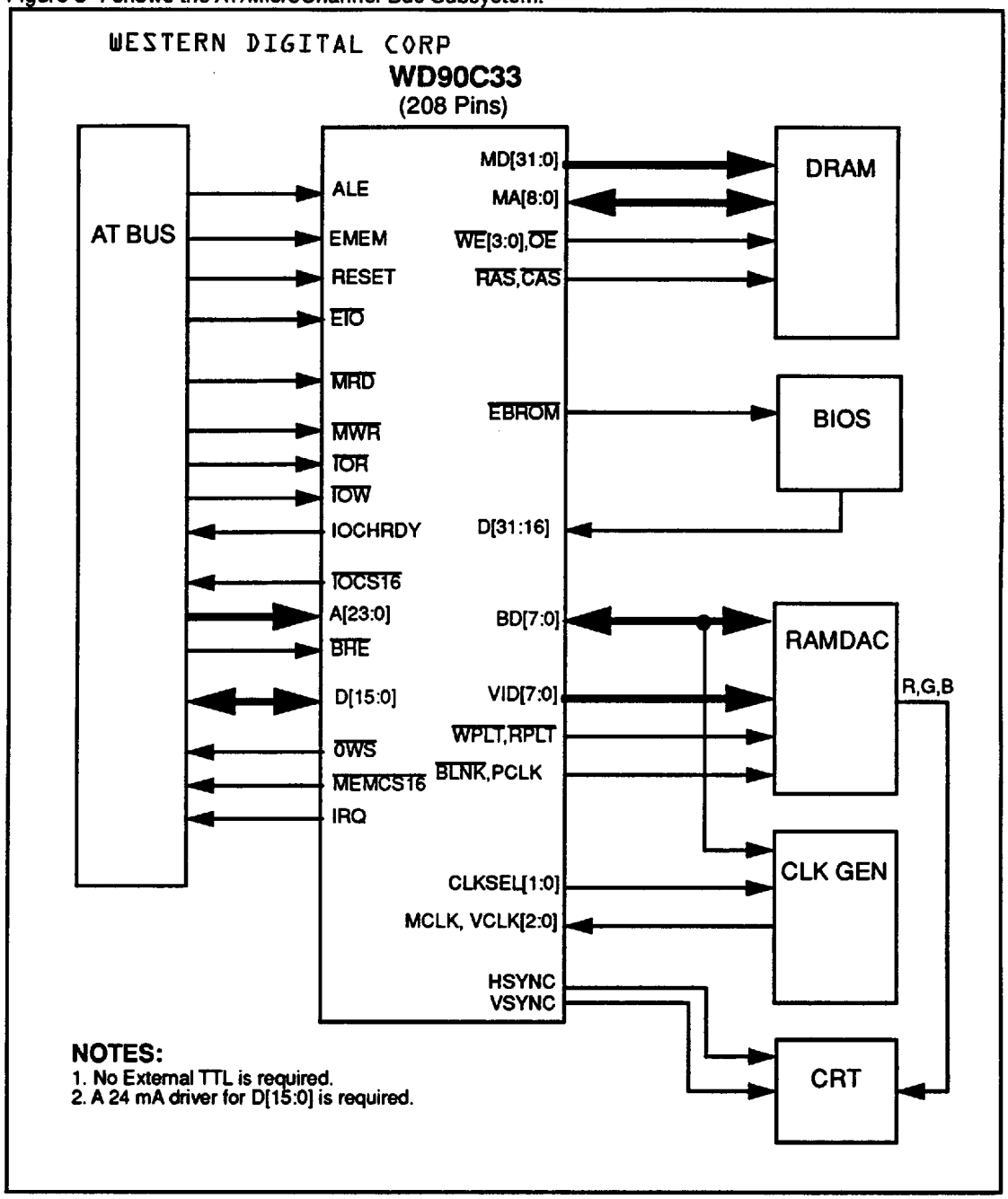


FIGURE 3-4 AT/MICROCHANNEL BUS SUBSYSTEM

NOTES FOR FIGURE 3-3

1. Use of HRQ and $\overline{BOFF}$ are optional. If the HRQ input is not used it should be tied low (inactive).
2. Typically, the video BIOS should be integrated with the system BIOS (External BIOS mode). For the Local bus mode BIOS, an 8-bit EPROM can be connected to BD[7:0]. In the mode, $\overline{EBROM}$ is decoded inside the WD90C33 and LDEV is generated to block the BIOS cycle seen by the core logic. Refer to the Local bus Interface, Section 10, for additional information.
3. Use of LDEVBUSY is also optional. Typically, $\overline{VGARDY}$ is connected to the RDY input of the core logic, which in turn generates the final $\overline{CPURDY}$. Refer to the pinout description in Section 4 for additional information.

3.5 AT COMPATIBLE INTERFACE (16-BITS) AND 8-BIT BIOS

Figure 3-5 shows the interface between a 16-bit AT compatible bus, an 8-bit BIOS, and the WD90C33 Controller. The typical use for this configuration is with 286/386 based systems.

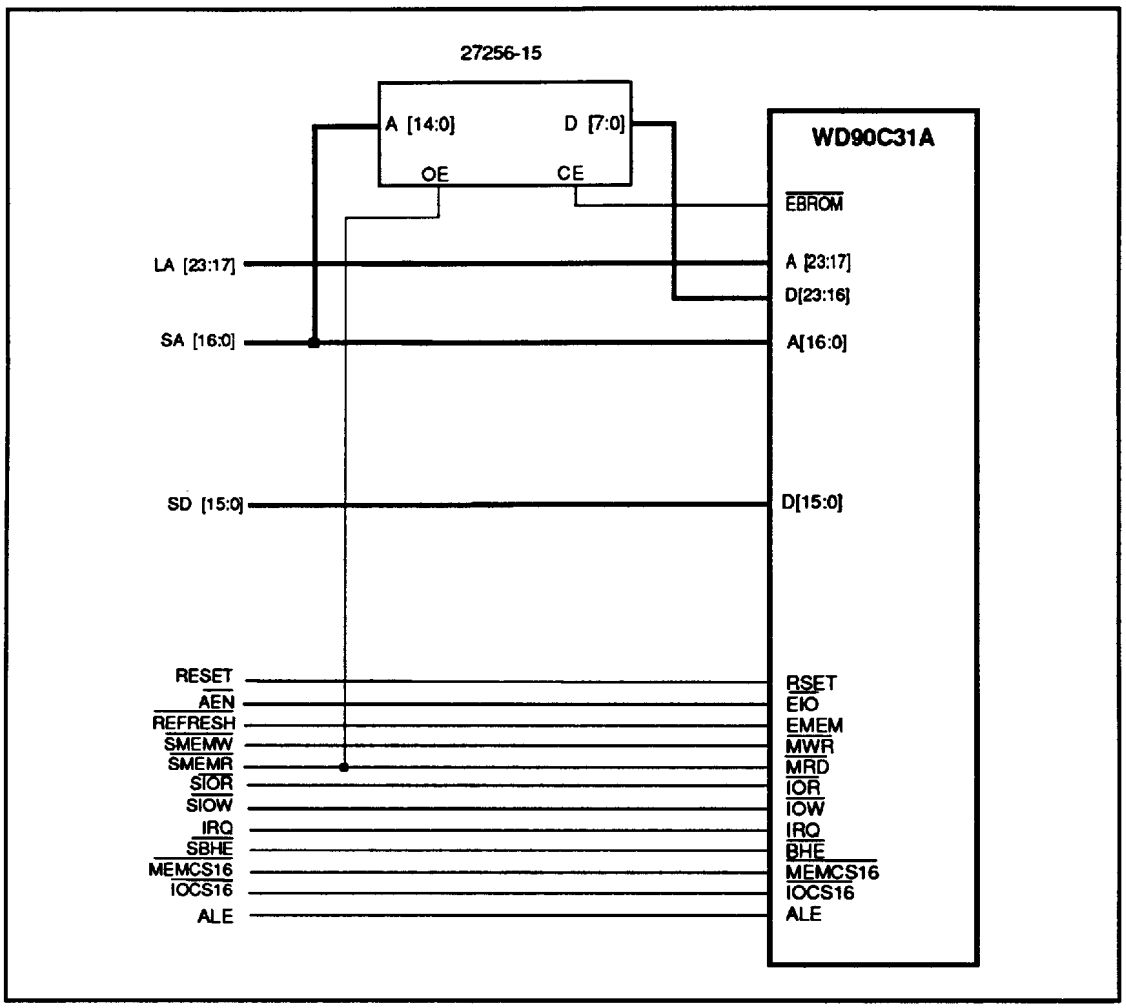


FIGURE 3-5 AT COMPATIBLE INTERFACE (16-BIT) AND 8-BIT BIOS

3.6 AT COMPATIBLE INTERFACE (16-BITS) AND 16-BIT BIOS

Figure 3-6 shows the interface between a 16-bit AT compatible bus, a 16-bit BIOS, and the WD90C33 Controller. This $\overline{\text{MEMCS16}}$ implementation is limited to slower bus speeds because address lines A16 and A15 are used for the 16-bit BIOS. The typical use for this configuration is with 386/486 based systems.

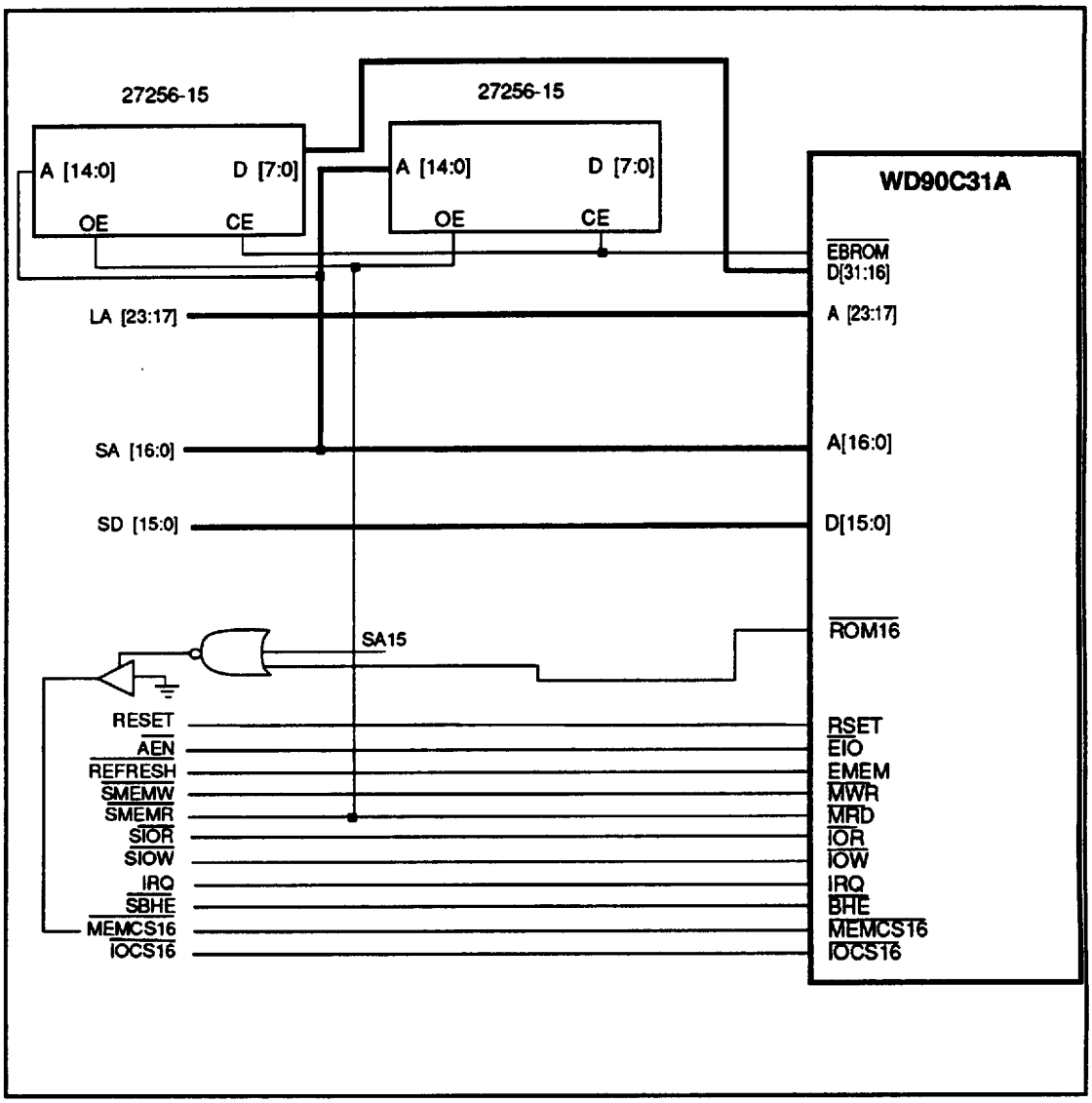


FIGURE 3-6 AT COMPATIBLE INTERFACE (16-BIT) AND 16-BIT BIOS

3.7 MICROCHANNEL (16-BIT) INTERFACE

Figure 3-7 shows the interface between a 16-bit Microchannel compatible bus and the WD90C33 Controller.The 3C3D0 signal is output from the VGA Subsystem Enable Register (3C3h, bit 0). The typical use for this configuration is with MicroChannel based systems.

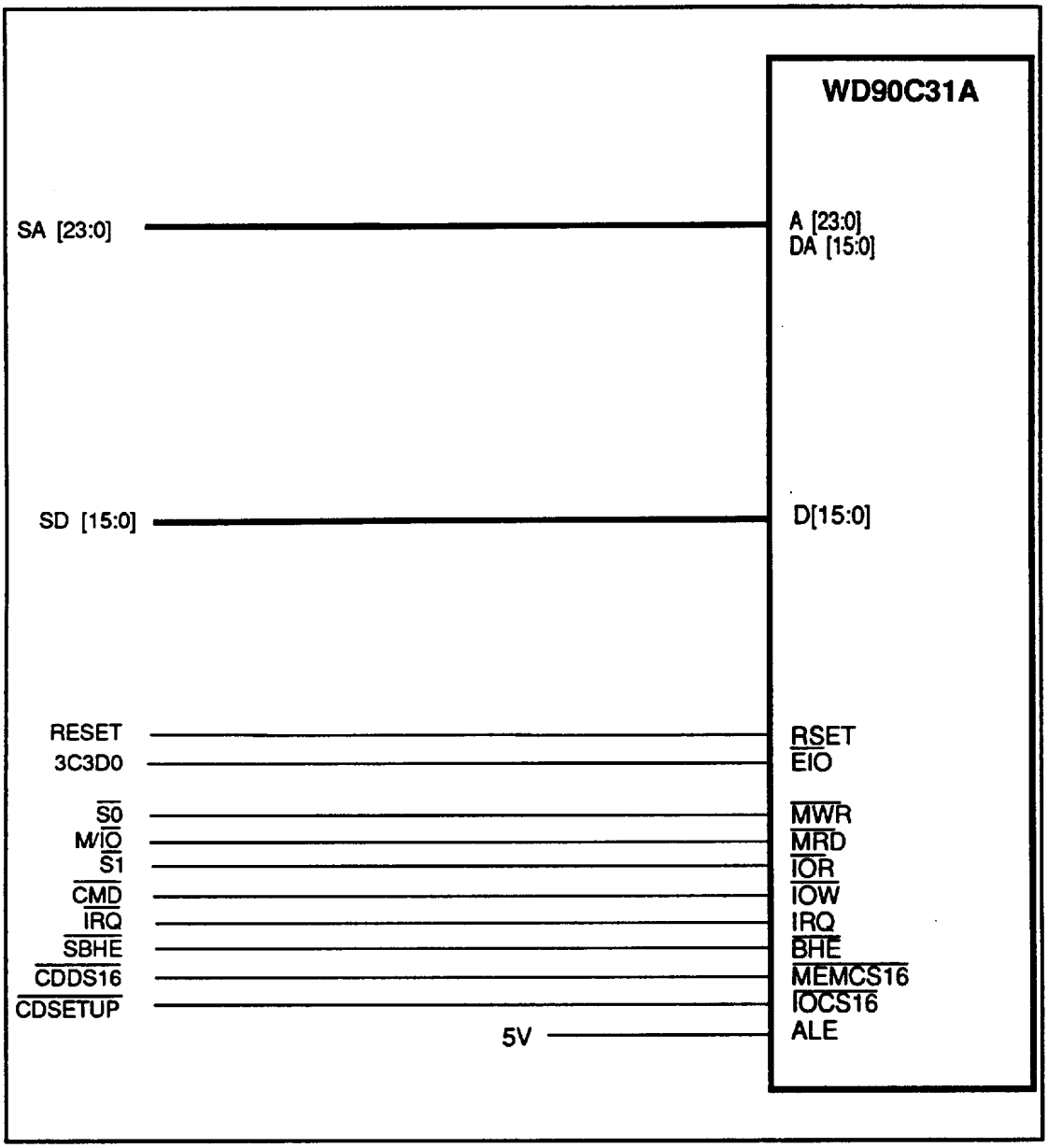


FIGURE 3-7 MICROCHANNEL (16-BIT) INTERFACE

3.8 DRAM INTERFACE

The WD90C33 has a flexible DRAM interface. It works with two or four 64K by 16 DRAMs with a 32-bit memory interface. It can also work with four 256 Kbyte by 4 DRAMs or one 256 Kbyte by 16 DRAM with a 16-bit memory interface (see Figures 3-8 and 3-9). Other possible configurations are eight or sixteen 256 Kbyte by 4 DRAMs, and two or four 256 Kbyte by 16 DRAMs with a 32-bit memory interface. In all cases the WD90C33 uses the DRAM fast page mode to optimize performance.

The WD90C33 supports all standard IBM VGA modes with only two 64K by 16 DRAMs. Because it uses a 32-bit memory interface and has an internal write buffer, the WD90C33 can update the video memory without inserting wait states to the AT bus for most standard IBM VGA modes.

When additional DRAMs are installed the WD90C33 is capable of supporting high resolution color video modes (1024 by 768 with 256 colors, non-interlaced at 72 Hz vertical refresh rate).

The WD90C33 is designed to support 60 ns, 70 ns, 80 ns and 100 ns DRAMs with the dedicated MCLK, which can operate from 32 MHz to 50 MHz maximum.

The WD90C33 generates fast page DRAM timing for all BITBLT, cursor and CPU accesses, graphics display and text display. A choice of page mode and non-page mode operation is provided to access fonts in text modes.

The WD90C33 also generates CAS before RAS DRAM refresh for the display memory.

3.9 TWO OR FOUR 64K BY 16 DRAM INTERFACE

Figure 3-8 shows the interface between two or four 64k by 16 DRAMs and the WD90C33 Controller.

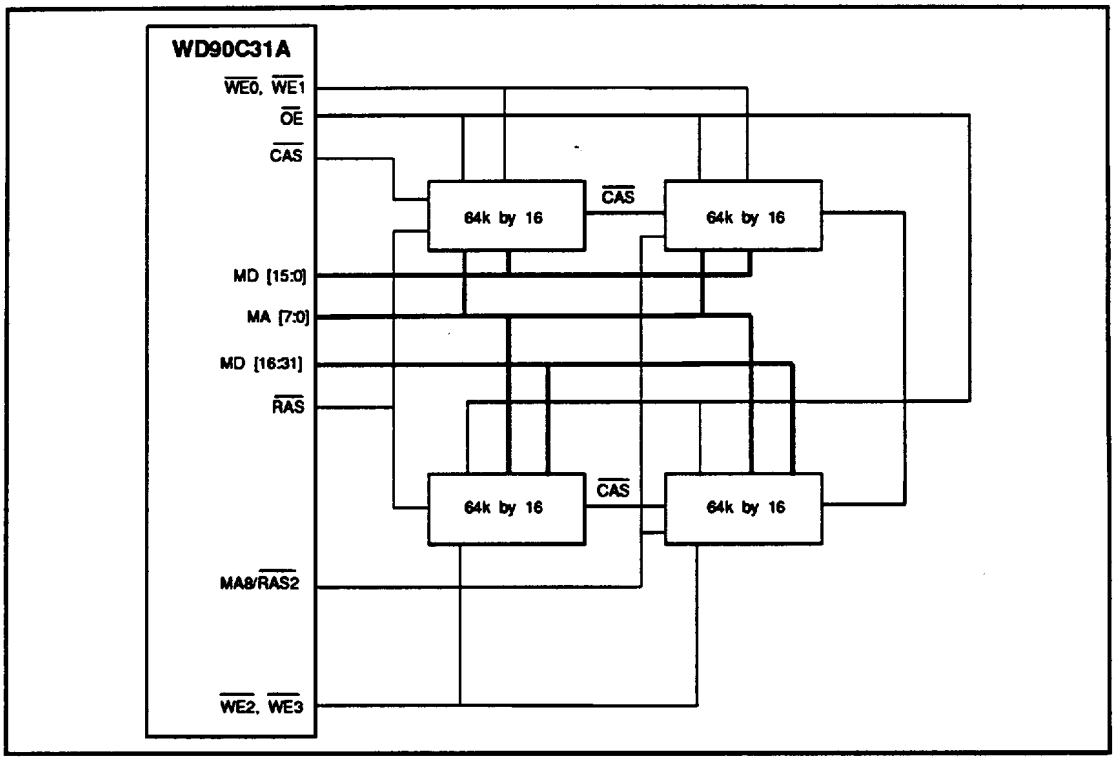


FIGURE 3-8 TWO OR FOUR 64K BY 16 DRAM INTERFACE

3.10 FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

Figure 3-9 shows the interface between four or eight 256K by 4 DRAMs and the WD90C33 Controller.

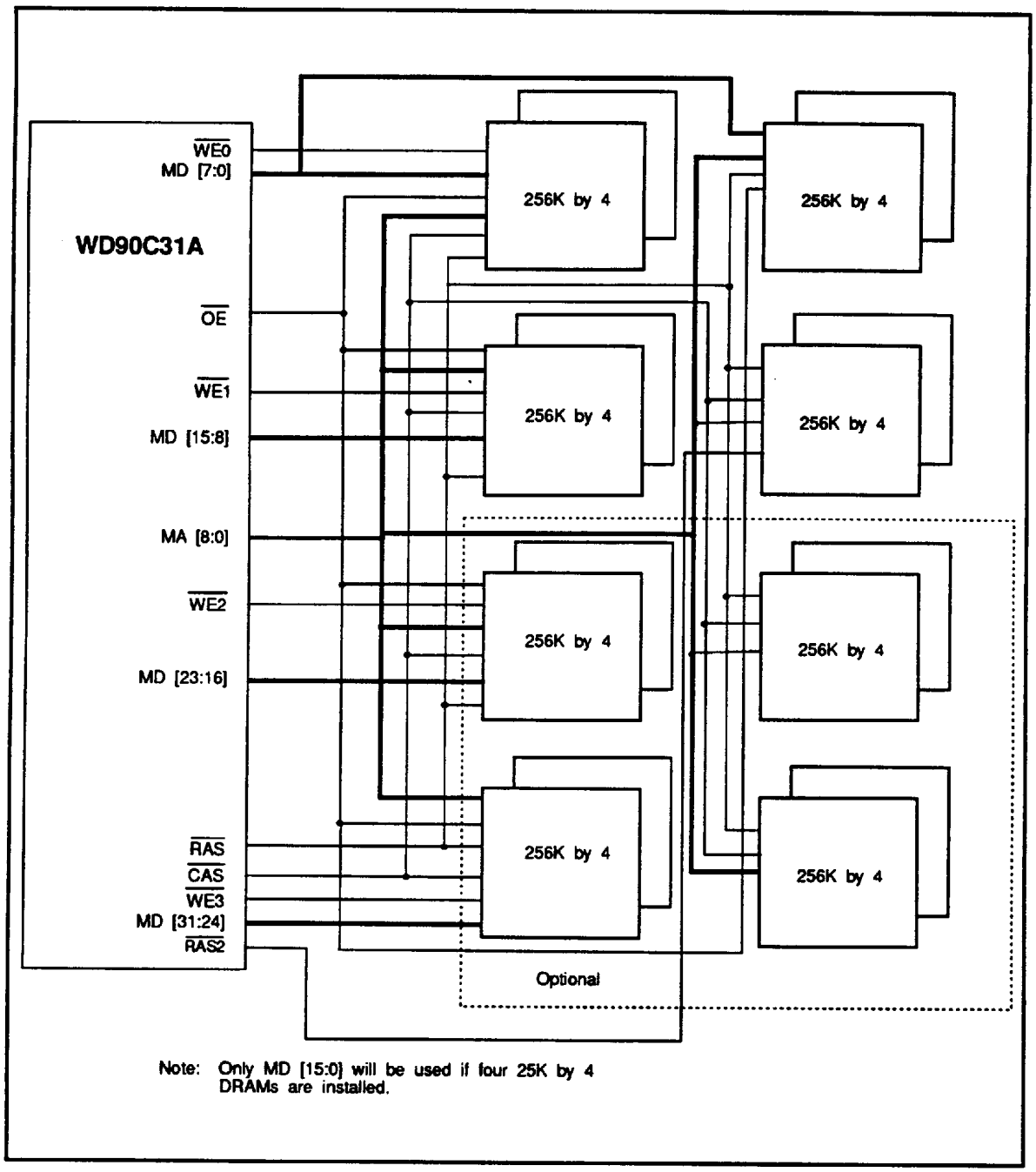


FIGURE 3-9 FOUR OR EIGHT 256K BY 4 DRAM INTERFACE

3.11 VIDEO INTERFACE T-52-33-45

The WD90C33 is optimized to connect to an analog CRT monitor through a RAMDAC but it may also be used to drive other types of displays, such as TTL monitors. In interfacing to an analog monitor through an external RAMDAC, the WD90C33 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C33 can be programmed to directly generate all the CRT signals for up to eight bits/pixel (256 color) displays.

The MicroChannel Auxiliary Video Connector and the AT Feature Connector can be connected directly to the WD90C33. The WD90C33 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.12 EXTERNAL RAMDAC INTERFACE

Figure 3-10 shows the interface between an external RAMDAC and the WD90C33 Controller.

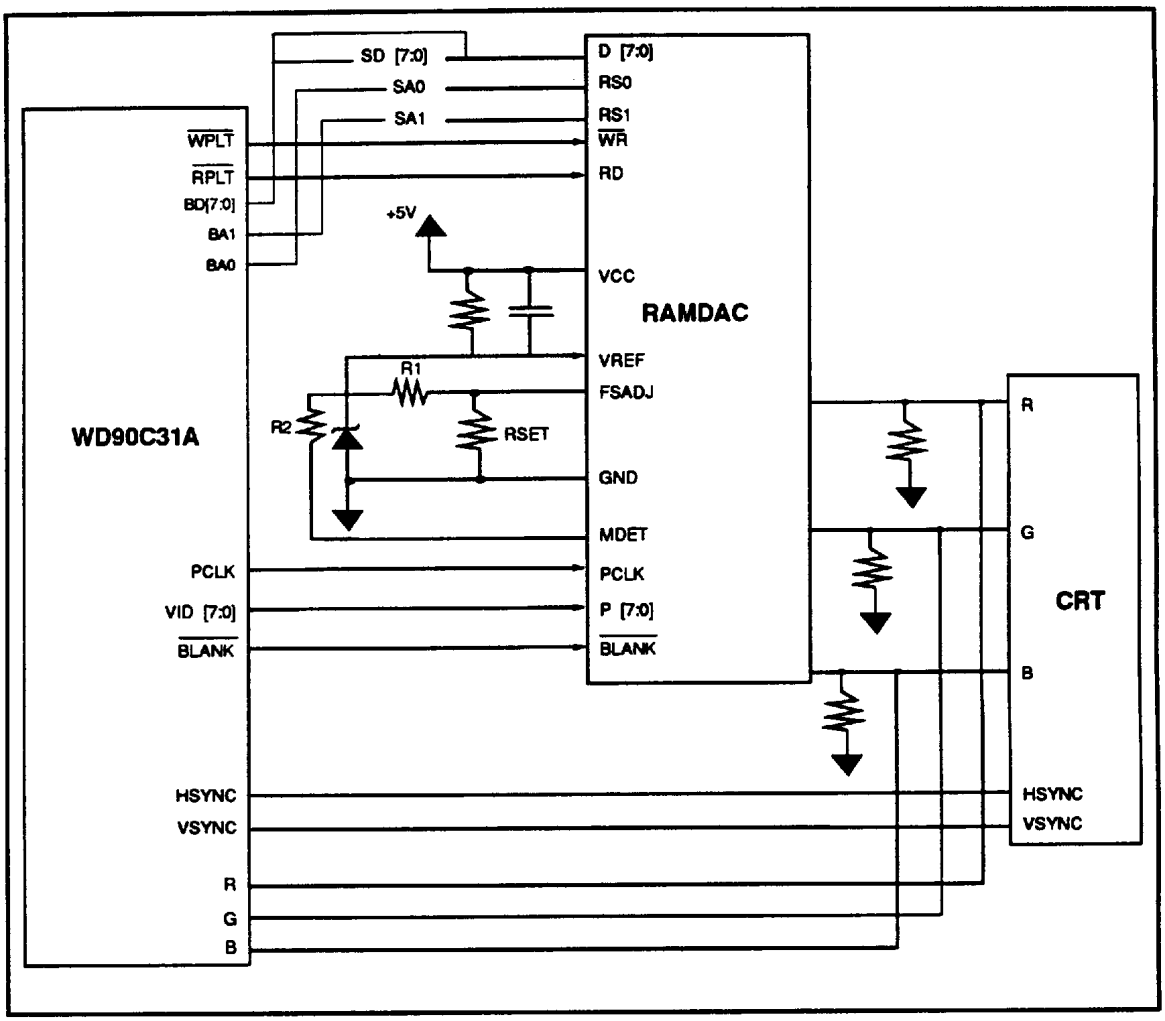


FIGURE 3-10 EXTERNAL RAMDAC INTERFACE

3.13 TTL MONITOR INTERFACE

Figure 3-11 shows the connections required to interface a TTL Monitor to the WD90C33 Controller.

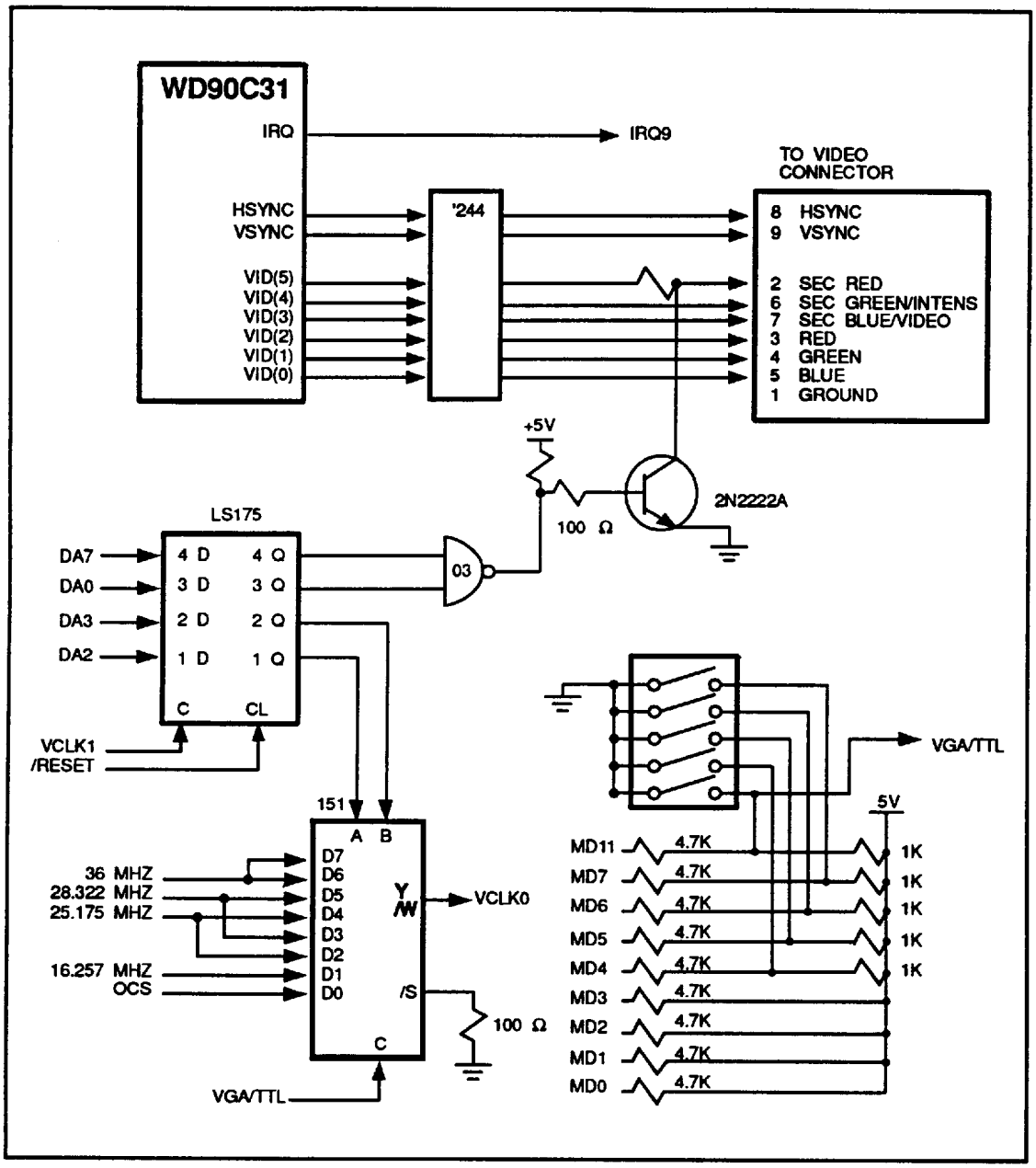


FIGURE 3-11 TTL MONITOR INTERFACE

3.14 CLOCK INTERFACE

The WD90C33 has four clock input signals, Memory Clock (MCLK), which drives the DRAM and bus interface timing, and the three Video Clocks, (VCLK0, VCLK1, and VCLK2), which drive the video timing. VCLK1 and VCLK2 can also be programmed as outputs to provide the option to externally control a multiplexer that supplies the video clock. MCLK can also be selected as a memory clock or video clock.

Figure 3-12 shows the clock interface with external oscillators configured as inputs. Clock selection is determined by register 3C2h, bits 3:2 as listed in the following table.

REGISTER 3C2h		CLOCK SELECTION
BIT 3	BIT 2	
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

NOTE T-52-33-45

Configuration bit 3 (CNF3) is pulled down to convert VCLK1 and VCLK2 to inputs. Refer to Section 9 for additional information.

3.15 SELECTING THE WD90C33 OPERATING INTERFACE CONFIGURATION

The WD90C33 uses memory data connector pins to configure an internal configuration register during power-on or system reset as described in Section 9. Configuration bit CNF(2) determines whether the WD90C33 will operate in AT or MicroChannel Architecture (MCA) implementation (AT or MicroChannel Interface Mode as shown in Figure 3-4). Configuration bit CNF(11) determines whether the WD90C33 will operate in the Local Bus or AT bus mode as shown in Figure 3-3.

Other configuration (CNF) bits configured by the WD90C33 during power-on or system reset are used as status bits or for clock source control. For more information the WD90C33 configuration register, refer to Section 9.

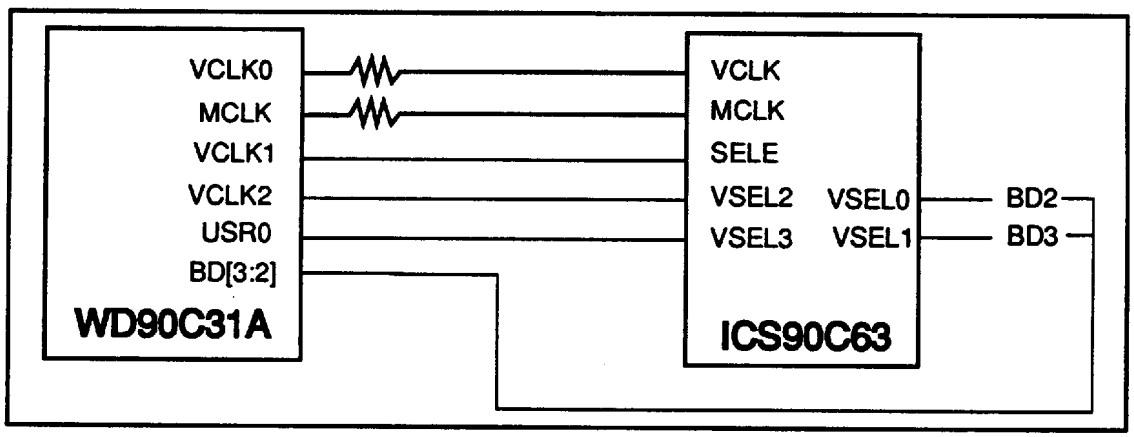


FIGURE 3-12 CLOCK INTERFACE

T-52-33-45

4.0 SIGNAL DESCRIPTIONS

This section contains detailed information concerning signals and pin outs for the WD90C33 controller 208-pin package.

4.1 INTRODUCTION

This section contains the following information:

- Signal Mnemonic to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Host Interface Pin Multiplexing

1.	$\overline{RAS2}$[1]	33.	MA1[1]	65.	A7[2]	97.	D29
2.	$\overline{WE1}$[1]/$\overline{CAS1}$[1]	34.	MA0[1]	66.	GND[3]	98.	D28
3.	MD15	35.	$\overline{OE}$[1]	67.	A8[2]	99.	GND[3]
4.	MD14	36.	GND[3]	68.	A9[2]	100.	D27
5.	MD13	37.	$\overline{OWS}$[1]/ LDEVBUSY[1]	69.	A10[2]	101.	D26
6.	MD12	38.	EMEM[2]/ CPURESET[2]	70.	A11[2]	102.	D25
7.	GND[3]	39.	$\overline{IOW}$[2]/HRQ[2]/ $\overline{CMD}$[2]	71.	A12[2]	103.	D24
8.	MD11	40.	$\overline{EBROM}$[1]	72.	A13[2]	104.	VCC[3]
9.	MD10	41.	$\overline{IOCS16}$/RDYIN/ $\overline{CDSETUP}$	73.	A14[2]	105.	D23
10.	MD9	42.	VCC[3]	74.	A15[2]	106.	D22
11.	MD8	43.	$\overline{EIO}$[2]/LCLK[2]/ 3C3D0[2]	75.	GND[3]	107.	D21
12.	$\overline{WE0}$[1]/$\overline{WE}$[1]	44.	IRQ[1]/$\overline{IRQ}$[1]	76.	A16[2]	108.	D20
13.	VCC[3]	45.	ALE[2]/$\overline{ADS}$[2]/$\overline{ALD}$[2]	77.	A17[2]	109.	VCC[3]
14.	MD7	46.	IOCHRDY[1]/ $\overline{VGARDY}$[1]	78.	A18[2]	110.	D19
15.	MD6	47.	$\overline{ROM16}$/$\overline{BOFF}$/ $\overline{CSFB}$	79.	A19[2]	111.	D18
16.	MD5	48.	GND[3]	80.	VCC[3]	112.	D17
17.	MD4	49.	$\overline{MEMCS16}$[1]/ LDEV[1]/$\overline{CDDS16}$[1]	81.	A20[2]	113.	D16
18.	GND[3]	50.	$\overline{IOR}$[2]/W/$\overline{R}$[2]/$\overline{S1}$[2]	82.	A21[2]	114.	GND[3]
19.	MD3	51.	$\overline{MRD}$[2]/M/$\overline{IO}$[2]	83.	A22[2]	115.	D15
20.	MD2	52.	$\overline{MWR}$[2]/D/$\overline{C}$[2]/$\overline{S0}$[2]	84.	A23[2]	116.	D14
21.	MD1	53.	VCC[3]	85.	GND[3]	117.	D13
22.	MD0	54.	$\overline{SYSRESET}$[2]/ RSET[2]	86.	A24[2]	118.	D12
23.	$\overline{CAS}$/$\overline{CAS0}$	55.	$\overline{BE3}$[2]	87.	A25[2]	119.	VCC[3]
24.	VCC[3]	56.	A1[2]/$\overline{BE2}$[2]	88.	A26[2]	120.	D11
25.	MA8[1]	57.	$\overline{BHE}$[2]/$\overline{BE1}$[2]	89.	A27[2]	121.	D10
26.	MA7[1]	58.	A0[2]/$\overline{BE0}$[2]/$\overline{BLE}$[2]	90.	A28[2]	122.	D9
27.	MA6[1]	59.	GND[3]	91.	A29[2]	123.	D8
28.	MA5[1]	60.	A2[2]	92.	A30[2]	124.	GND[3]
29.	MA4[1]	61.	A3[2]	93.	A31[2]	125.	D7
30.	GND[3]	62.	A4[2]	94.	GND[3]	126.	D6
31.	MA3[1]	63.	A5[2]	95.	D31	127.	D5
32.	MA2[1]	64.	A6[2]	96.	D30	128.	D4

NOTE: Refer to notes at the end of this table.

TABLE 4-1 SIGNAL TO PIN LOCATION

129. VCC[3]	149. $\overline{WPLT}$[1]	169. VID5[1]	189. MD29
130. D3	150. $\overline{RPLT}$[1]	170. VID6[1]	190. MD28
131. D2	151. MDET[2]	171. VID7[1]	191. GND[3]
132. D1	152. $\overline{EXVID}$[2]	172. GND[3]	192. MD27
133. D0	153. No Connection	173. No Connection	193. MD26
134. GND[3]	154. No Connection	174. No Connection	194. MD25
135. VSYNC[1]	155. No Connection	175. No Connection	195. MD24
136. HSYNC[1]	156. No Connection	176. MCLK[2]	196. $\overline{WE2}$[1]/$\overline{CAS2}$[1]
137. BD0	157. No Connection.	177. GND[3]	197. VCC[3]
138. BD1	158. No Connection	178. VCLK0[2]	198. MD23
139. BD2	159. No Connection	179. VCLK1	199. MD22
140. BD3	160. GND[3]	180. VCLK2	200. MD21
141. VCC[3]	161. PCLK[1]	181. VCC[3]	201. MD20
142. BD4	162. $\overline{BLNK}$[1]	182. $\overline{EXPCLK}$[2]	202. GND[3]
143. BD5	163. VID0[1]	183. USR1[2]	203. MD19
144. BD6	164. VID1[1]	184. USR0[2]	204. MD18
145. BD7	165. VID2[1]	185. VCC[3]	205. MD17
146. GND[3]	166. VID3[1]	186. $\overline{WE3}$[1]/$\overline{CAS3}$[1]	206. MD16
147. BA1[1]	167. VCC[3]	187. MD31	207. $\overline{RAS}$[1]
148. BA0[1]	168. VID4[1]	188. MD30	208. VCC[3]

NOTES:

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates power distribution pins.

Signal names not otherwise indicated are input/output.

The direction of signal flow is relative to the WD90C33 controller.

TABLE 4-1 SIGNAL TO PIN LOCATION

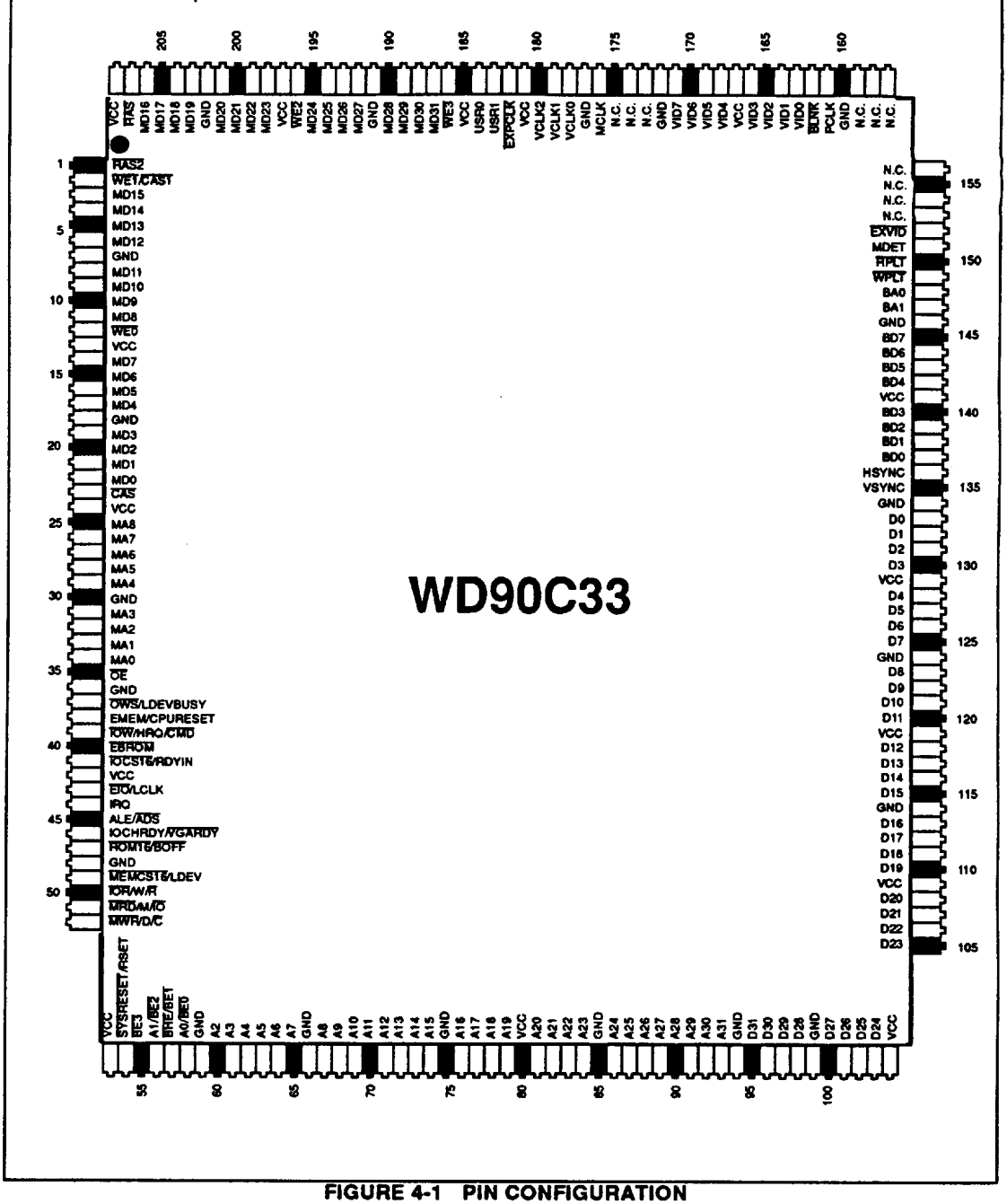


FIGURE 4-1 PIN CONFIGURATION

4.3 DETAILED SIGNAL DESCRIPTIONS

The following tables provide detailed signal descriptions for the WD90C33 controller 208-pin package. The signal descriptions are listed by the pin number and mnemonic given in Table 4-1. The definitions are listed in functional groups. The functional groups are listed below:

- Display Memory Interface
- RAMDAC Interface
- Clock Selection
- User Program
- Feature Connector
- CRT Control
- Host CPU Bus Interface
- Power Distribution
- Unused Connections

Where more than one signal name is indicated on the same pin, the signal names are separated by a virgule (/) in Table 4-1. The pin usage, as described in Table 4-2, changes for each signal name depending upon which bus interface is used as follows:

1. The letters AT in the bus column indicate an Industry Standard Architecture (ISA) bus compatible signal. The terms AT bus and ISA bus are used interchangeably unless otherwise indicated.
2. The letters MC in the bus column indicate an IBM MicroChannel bus compatible signal.
3. The letters LOC in the bus column indicate a local bus compatible signal.
4. Where no specific bus is indicated, the signals are used in all bus modes.

Table 4-2 lists and provides descriptions for the WD90C33 connector pins. T-52-33-45

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
Display Memory Interface (49 Pins)				
207	$\overline{RAS}$	---	Active Low Output	**ROW ADDRESS STROBE** Strobe for the first 1 Mbyte of DRAM
1	$\overline{RAS2}$	---	Active Low Output	**ROW ADDRESS STROBE 2** Strobe for the second 1 Mbyte of DRAM, only if 2M of DRAM memory are used.
186	$\overline{WE3}$ or $\overline{CAS3}$	---	Active Low Output	**WRITE ENABLE 3 or COLUMN ADDRESS STROBE 3** If CNF17 = 1, $\overline{WE3}$ is the write enable signal for MD[31:24] If CNF17 = 0, $\overline{CAS3}$ is the column address strobe for MD[31:24]
196	$\overline{WE2}$ or $\overline{CAS2}$	---	Active Low Output	**WRITE ENABLE 2 or COLUMN ADDRESS STROBE 2** If CNF17 = 1, $\overline{WE2}$ is the write enable signal for MD[23:16] If CNF17 = 0, $\overline{CAS2}$ is the column address strobe for MD[23:16]
2	$\overline{WE1}$ or $\overline{CAS1}$	---	Active Low Output	**WRITE ENABLE 1 or COLUMN ADDRESS STROBE 1** If CNF17 = 1, $\overline{WE1}$ is the write enable signal for MD[15:8] If CNF17 = 0, $\overline{CAS1}$ is the column address strobe for MD[15:8]
12	$\overline{WE0}$ or $\overline{WE}$	---	Active Low Output	**WRITE ENABLE 0 or WRITE ENABLE** If CNF17 = 1, $\overline{WE0}$ is the write enable signal for MD[7:0] If CNF17 = 0, $\overline{WE}$ is the write enable signal for MD[31:0]
23	$\overline{CAS}$ or $\overline{CAS0}$	---	Active Low Output	**COLUMN ADDRESS STROBE or COLUMN ADDRESS STROBE 0** If CNF17 = 1, $\overline{CAS}$ is the column address strobe for one, two, four, eight, and sixteen DRAM configurations If CNF17 = 0, $\overline{CAS0}$ is the column address strobe for MD[7:0]
35	$\overline{OE}$	---	Active Low Output	**OUTPUT ENABLE** Output enable signal
25 26 27 28 29 31 32 33 34	MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	---	Active High Output	**MEMORY ADDRESS** Display memory DRAM address. For testing, these pins can be tristated by setting PR4 register bit 4 to 1.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
187 188 189 190 192 193 194 195 198 199 200 201 203 204 205 206 3 4 5 6 8 9 10 11 14 15 16 17 19 20 21 22	MD31 MD30 MD29 MD28 MD27 MD26 MD25 MD24 MD23 MD22 MD21 MD20 MD19 MD18 MD17 MD16 MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	---	Active High Input/ Output	**DISPLAY MEMORY DATA** These lines are the data bus for the video display DRAMs. These data lines are pulled up by internal 50 Kohm resistors, but may be pulled down by external 4.7 Kohm resistors to provide configuration information during power-on and system reset as follows: **MD — FUNCTION — CONFIGURATION[BIT]** [31:30] $\overline{\text{VIOR}}$/$\overline{\text{VIOW}}$ High/Low Duration — CNF[31:30]+ [29:28] $\overline{\text{VMWR}}$/$\overline{\text{VMRD}}$ High Duration — CNF[29:28]+ [27:26] $\overline{\text{VMWR}}$/$\overline{\text{VMRD}}$ Low Duration — CNF[27:26]+ 25 Set BIOS In Local Bus Mode — CNF[25]+ 24 Connect RAMDAC In Local Bus Mode — CNF[24]+ 23 Enable Local Bus Interface — CNF[23]+ 22 Select Pulse Width High/Low Duration for RAMAC, IOR, and IOW; also Duration of $\overline{\text{EBROM}}$ MRD — CNF[22]+ 21 Select 386/486 Local Bus Interface — CNF[21]+ 20 Terminated Local Bus VGA Cycle — CNF[20]+ 19 Reserved — CNF[19]+ 18 Enable ROM16 as $\overline{\text{EXBLANK}}$ — CNF[18]+ 17 Memory Write Control ($\overline{\text{CAS}}$ or $\overline{\text{WE}}$) — CNF[17]+ 16 64K by 16 or 256K by 4 DRAM Select — CNF[16]+ 15 EGA SW4/General Purpose, PR11[7] — CNF[15]+ 14 EGA SW3/General Purpose, PR11[6] — CNF[14]+ 13 EGA SW2/General Purpose, PR11[5] — CNF[13]+ 12 EGA SW1/General Purpose, PR11[4] — CNF[12]+ 11 Select AT/Local Bus Mode — CNF[11]+ 10 Set 16-bit ROM, PR1[1] — CNF[10]* 9 Wakeup I/O Port 3C3h or 46E8h — CNF[9]+ 8 Analog/TTL Display, PR5[3] — CNF[8]* 7 General Purpose, PR5[7] — CNF[7]* 6 General Purpose, PR5[6] — CNF[6]* 5 General Purpose, PR5[5] — CNF[5]* 4 General Purpose, PR5[4] — CNF[4]* 3 VCLK1, VCLK2 I/O — CNF[3]+ 2 Select AT/ MicroChannel Mode — CNF[2]+ 1 Select 1 ROM or 2 ROMs — CNF[1]* 0 BIOS ROM Mapping, PR1[0] — CNF[0]* **NOTES:** * = Pulldown resistor sets these bits to 1. += Pulldown resistor sets these bits to 0. CNF[30:20] have no effect unless Local bus mode is selected. For addition information, refer to the Configuration Register descriptions in Section 9.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION T-52-33-45
RAMDAC Interface (22 Pins)				
148 147	BA0 BA1	---	Active High Output	**RAMDAC ADDRESS BUS** A 2-bit wide address bus to read/write the RAMDAC.
145 144 143 142 140 139 138 137	BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0	---	Active High Input/ Output	**RAMDAC DATA BUS** An 8-bit wide data bus to read/ write the RAMDAC. **NOTE:** In Local Bus mode configuration, the BIOS EPROM data lines can be connected to this bus.
171 170 169 168 166 165 164 163	VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0	---	Active High Output	**VIDEO** Pixel video data output to DAC and to Feature Connector. These lines can drive an up to 8 mA load.
150	$\overline{\text{RPLT}}$	---	Active Low Output	**READ PALETTE** Video DAC register and color palette read signal for an external RAMDAC. Active low during I/O read of addresses 3C6h, 3C8h, and 3C9h.
149	$\overline{\text{WPLT}}$	--	Active Low Output	**WRITE PALETTE** Video DAC register and color palette write signal for an external RAMDAC. Active low during I/O write of addresses 3C6h through 3C9h.
161	PCLK	---	Active High Output	**PIXEL CLOCK** Video pixel clock used by the DAC to latch video signals VID7 through VID0. Its source is one of the video clock inputs (VCLK0, VCLK1, or VCLK2) as selected by the Miscellaneous Output Register.
162	$\overline{\text{BLNK}}$	---	Active Low Output	**BLANK** Active low display monitor blanking pulse to external RAMDAC.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
			Clock Selection (4 Pins)	
176	MCLK	---	Active High Input	**MEMORY CLOCK** Provides VGA DRAM and system interface control timing. Should be 37.5 MHz minimum for 80 ns DRAMs.
178	VCLK0	---	Active High Input	**VIDEO CLOCK 0** Provides video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. VCLK0 is selected as the clock when VCLK1 and VCLK2 are used as inputs and Miscellaneous Output register bits 2 and 3 are both set to 0.
179	VCLK1	---	Active High Input/ Output	**VIDEO CLOCK 1** Provides a second video clock input or an output to an external clock selection module. The direction is determined at Reset by a pull-up or pull-down resistor on MD3. Typically, VCLK1 is 28.322 MHz to display 720 pixels per horizontal display line. As an output, VCLK1 is an active low pulse during I/O writes to port 3C2h, or reflects the contents of 3C2h (Miscellaneous Output Register, bit 2). For addition information, refer to the Configuration Register and PR15 register bit 5 descriptions.
180	VCLK2	---	Active High Input/ Output	**VIDEO CLOCK 2** Provides a third video clock input or an output to an external clock selection module. The direction is programmed simultaneously with VCLK1. VCLK2 performs as a user-defined external clock input, an output reflecting the state of PR2 register bit 1, or reflects the contents of port 3C2h (Miscellaneous Output Register, bit 2). For addition information, refer to the Configuration Register and PR15 register bit 5 descriptions.
			User Program (2 Pins)	
183 184	USR1 USR0	---	Active High Output	**USER PROGRAMMABLE OUTPUTS** Either or both outputs may be used to control a system feature of special device.
			Feature Connector (2 Pins)	
152	$\overline{\text{EXVID}}$	---	Active Low Input	**ENABLE EXTERNAL VIDEO DATA** A feature connector input. A low tristates video data lines VID7:0. An internal pullup resistor is provided.
182	$\overline{\text{EXPCLK}}$	---	Active Low Input	**ENABLE EXTERNAL PIXEL CLOCK** A feature connector input. A low tristates the PLCK output. An internal pullup resistor is provided.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
				CRT Control (3 Pins) T-52-33-45
136	HSYNC	---	Active High Input/ Output	**HORIZONTAL SYNC** Display monitor horizontal synchronization pulse. Active high or low depending upon the Miscellaneous Output Register programming.
135	VSYNC	---	Active High Input/ Output	**VERTICAL SYNC** Display monitor vertical synchronization pulse. Active high or low depending upon the Miscellaneous Output Register programming.
151	MDET	---	Active High Input	**MONITOR DETECT** When the RAMDAC is external, MDET is used to determine the monitor type. MDET can be read at port 3C2h, bit 4.
				Host CPU Bus Interface (80 Pins)
93 92 91 90 89 88 87 86	A31 A30 A29 A28 A27 A26 A25 A24	LOC	Active High Input	**SYSTEM ADDRESS BUS BIT 31 THROUGH 24** Address Bus bits 31 through 24 for the 32-bit Local bus interface. These pins are not connected for either AT or MicroChannel bus compatible systems.
84 83 82 81 79 78 77	A23 A22 A21 A20 A19 A18 A17	LOC	Active High Input	**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** Address Bus bits 23 through 17 for the 32-bit Local bus interface.
		AT		**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** For the AT bus, A17 through A23 are connected to LA23 through LA17 to provide a 24-bit AT address bus.
		MC		**SYSTEM ADDRESS BUS BITS 23 THROUGH 17** For the MicroChannel bus, A17 through A23 are connected to SA23 through SA17 to provide a 24-bit MicroChannel address bus.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
76 74 73 72 71 70 69 68 67 65 64 63 62 61 60	A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2	---	Active High Input	**SYSTEM ADDRESS BUS BITS 16 THROUGH 2** Address Bus bits 16 through 2 for all bus operating modes.
56	A1	AT, MC	Active High Input	**SYSTEM ADDRESS BUS BIT 1** For AT and MicroChannel bus mode operation, A1 provides Address Bus bit 1.
	$\overline{BE2}$	LOC	Active Low Input	**BYTE ENABLE 2** In Local bus mode, $\overline{BE2}$ provides Byte Enable for data bits D23 through D16.
58	A0	AT, MC	Active High Input	**SYSTEM ADDRESS BUS BIT 0** For AT bus mode operation, A0 provides Address Bus bit 0.
	$\overline{BLE}$	LOC	Active Low Input	**BYTE LOW ENABLE** In Local bus mode for 386SX only, this line is connected to the $\overline{BLE}$ line from the CPU to enable the low byte for data transfers.
	$\overline{BE0}$	LOC	Active Low Input	**BYTE ENABLE 0** In normal Local bus mode, $\overline{BE0}$ provides Byte Enable for data bits D7 through D0.
57	$\overline{BE1}$	LOC	Active Low Input	**BYTE ENABLE 1** In Local bus mode, $\overline{BE1}$ provides Byte Enable for data bits D15 through 8.
	$\overline{BHE}$	AT, MC		**BYTE HIGH ENABLE** For AT and MicroChannel bus mode operation, this line is connected to the $\overline{BHE}$ line from the CPU to enable the high byte for data transfers.
55	$\overline{BE3}$	LOC	Active Low Input	**BYTE ENABLE 3** In Local bus mode, $\overline{BE2}$ provides Byte Enable for data bits D31 through D24. Not used in AT or MicroChannel modes.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
45	$\overline{ADS}$	LOC	Active High Input	**ADDRESS DATA STROBE** Local bus address data strobe connected to the ADS pin on the CPU.
	ALE	AT	Active High Input	**ADDRESS LATCH ENABLE** In AT mode, A23 through A17 (LA23:LA17) are latched internally at the falling edge of ALE.
	$\overline{ALD}$	MC	Active High Input	**ADDRESS LATCH** In MicroChannel mode, this signal is not used and should be tied high.
51	M/$\overline{IO}$	LOC, MC	Active High Input	**MEMORY or I/O CYCLE** Indicator for memory or I/O cycle. Low indicates I/O cycle; high indicates memory cycle. In MicroChannel mode, indicator for memory or I/O cycle. Low indicates I/O cycle; high indicates memory cycle.
	$\overline{MRD}$	AT	Active Low Input	**MEMORY READ** In AT mode, $\overline{MRD}$ is the memory read strobe.
52	D$\overline{C}$	LOC	Active High or Low Input	**DATA or COMMAND CYCLE** Data or command cycle indicator. Low indicates command cycle; high indicates a data cycle.
	$\overline{MWR}$	AT	Active Low Input	**MEMORY WRITE** In AT mode, $\overline{MWR}$ is the memory write strobe.
	$\overline{S0}$	MC	Active Low Input	**STATUS 0** In MicroChannel mode, $\overline{S0}$ is a channel status signal that indicates the start and type of a channel cycle. The $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals are decoded to interpret I/O and memory commands.
50	W/$\overline{R}$	LOC	Active High or Low Input	**WRITE or READ CYCLE** Write or read cycle indicator. Low indicates a read cycle; high indicates a write cycle.
	$\overline{IOR}$	AT	Active Low Input	**I/O READ** In AT mode, $\overline{IOR}$ provides an I/O read strobe.
	$\overline{S1}$	MC	Active Low Input	**STATUS 1** In MicroChannel mode, $\overline{S1}$ is a channel status signal that indicates the start and type of a channel cycle. The $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ signals are decoded to interpret I/O and memory commands.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
39	HRQ	LOC	Active High Input	**HOLD REQUEST** Indicates that a system bus request was received via a REFRESH, DMA, or MASTER signal. The processor responds by asserting a HOLD ACKNOWLEDGE after relinquishing the bus.
	$\overline{IOW}$	AT	Active Low Input	**I/O WRITE** In AT mode, $\overline{IOW}$ provides an I/O write strobe.
	$\overline{CMD}$	MC	Active Low Input	**COMMAND** In MicroChannel mode, $\overline{CMD}$ is the bus data strobe. $\overline{CMD}$ low indicates address bus validity and the rising edge of $\overline{CMD}$ indicate the end of a MicroChannel bus cycle.
43	LCLK	LOC	Active High Input	**PROCESSOR CLOCK** Normal clock input from 80486; for 80386, this is CPU-CLK2, which the WD90C33 divides internally to drive other logic.
	$\overline{EIO}$	AT	Active Low Input	**ENABLE I/O** In AT mode, $\overline{EIO}$ enables address decoding and is connected to AEN (address Enable).
	3C3D0	MC	Active High Input	**PORT 3C3h** In MicroChannel mode, when I/O port 3C3h bit 0 is set to 1, it enables video subsystem memory and I/O address decoding.
54	SYSRESET	LOC	Active High Input	**SYSTEM RESET** For local bus, MCLK and VCLK0 must be connected to initialize the WD90C33 during power-on and reset. Western Digital configuration bits are initialized at power-on and reset, based on the logic levels of display memory data bits MD31 through MD0 bus, as determined by pullup and pulldown resistors. The reset pulse width should be at least 10 MCLK clock periods.
	RSET	AT, MC	Active High Input	**SYSTEM RESET** For AT and MicroChannel bus operation, MCLK and VCLK0 must be connected to initialize the WD90C33 during power-on and reset. Western Digital configuration bits are initialized at power-on and reset, based on the logic levels of display memory data bits MD19 through MD0 bus, as determined by pullup and pulldown resistors. The reset pulse width should be at least 10 MCLK clock periods.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
95 96 97 98 100 101 102 103 105 106 107 108 110 111 112 113	D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D119 D18 D17 D16	LOC, AT	Active High Input/ Output	**DATA BUS BITS 31 THROUGH 16** System data lines connect to host CPU data bus D[31:16]. In AT mode, the BIOS EPROM can be connected to this bus. Then, the BIOS data will be sent to the host via D[15:0] D[31:16} are not used for MicroChannel bus operations.
115 116 117 118 120 121 122 123 125 126 127 128 130 131 132 133	D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	---	Active High Input/ Output	**DATA BUS BITS 15 THROUGH 0** System data lines connect to the host CPU or system data bus D[15:0].
49	$\overline{\text{LDEV}}$	LOC	Active Low Output	**LOCAL BUS VGA CYCLE** Indicates a local bus VGA cycle. System controllers should not respond to this cycle.
	$\overline{\text{MEMCS16}}$	AT	Active Low Output	**MEMORY CHIP SELECT, 16 BITS** In AT mode, $\overline{\text{MEMCS16}}$ indicates to the host that the WD90C33 is ready to perform a requested 16-bit video memory data transfer.
	$\overline{\text{CDDS16}}$	MC	Active Low Input	**CHANNEL SELECT, 16 BITS** In MicroChannel mode, $\overline{\text{CDDS16}}$ indicates a 16-bit video memory or I/O access.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
47	$\overline{\text{BOFF}}$	LOC	Active Low Output	**BOFF** Connects to the 80486 BOFF# pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus. Its operation is similar to a read cycle for the VGA when the write buffers are full.
	$\overline{\text{ROM16}}$	AT	Active Low Output	**BIOS ROM SELECT, 16 BITS** In AT mode, $\overline{\text{ROM16}}$ decodes ROM address (LA23-LA17) for space 0C0000h through 0DFFFFh. Also, it can be combined externally with A16 and A15 to control $\overline{\text{MEMCS16}}$ for address space C0000h through C7FFFh. If CNF(17) is set to at power-up/reset, the $\overline{\text{ROM16}}$ address decoding is disabled. Then, $\overline{\text{ROM16}}$ reflects the status of PR1 register bit 16.
	$\overline{\text{CSFB}}$	MC	Active Low Input	**CARD SELECT FEEDBACK** In Microchannel mode, $\overline{\text{CSFB}}$ acknowledges that the WD90C33 is present at the specified host address.
38	CPURESET	LOC	Active High Input	**CPU RESET** Provides a synchronous reset to the CPU, and is used to generate an internal CLK to maintain phase of CLK2 in sync with 80386dx and 80386sx CPUs.
	EMEM	AT, MC		**ENABLE MEMORY** In AT and MicroChannel mode, EMEM enables memory decoding. Normally it is connected to REFRESH.
37	LDEVBUSY	LOC	Active High Output	**VIDEO LOCAL BUS BUSY** When an external RAMDAC exists on the AT bus, or a monochrome interface card in installed on the AT bus, the writing cycle for these devices is passed to the AT bus. Then, the AT controller is expected to terminate the cycle. The write cycle is also sent to the local bus VGA, where LDEVBUSY is asserted until the write data are captured.
	$\overline{\text{0WS}}$	AT, MC	Active Low Output	**ZERO WAIT STATE** In AT and MicroChannel mode, $\overline{\text{0WS}}$ is asserted to generate a zero wait state. It is controlled by PR33 register bits 7 and 6. Refer to the PR33 description for additional information.

TABLE 4-2 SIGNAL DESCRIPTIONS

T-52-33-45

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
46	VGARDY	LOC	Active Low Output	**VGA READY** Ready signal to host CPU. This signal can be connected directly to the ready input of the CPU or connected in combination with other local bus slaves. When not active, this signal is tristated.
	IOCHRDY	AT, MC	Active High Output	**I/O CHANNEL READY** In AT and MicroChannel mode, IOCHRDY indicates to the host processor that the requested memory or I/O access is complete. When IOCHRDY is low, the video controller is not able to immediately complete a requested memory or I/O access and that causes the host processor to wait.
41	RDYIN	LOC	Active High Output	**READY INPUT** For Local bus mode, RDYIN provides the final CPURDY feedback to the WD90C33 to terminate its local bus cycle. The use of RDYIN is optional depending on the setting of Configuration register bit CNF20 as follows: If CNF20 = 0, a Local bus cycle is terminated when VGARDY is active, regardless of the state of RDYIN. If CNF20 = 1, a Local bus cycle is terminated when RDYIN provides the final CPURDY feedback.
	IOCS16	AT	Active Low Output	**I/O CHIP SELECT, 16 BITS** In AT mode, IOCS16 indicates to the host that the WD90C33 is ready to perform a requested 16-bit I/O accesses.
	CDSETUP	MC	Active Low Input	**CHANNEL SETUP** In MicroChannel Mode, CDSETUP is driven by the host to individually select channel connector slots during system configuration.
40	EBROM	---	Active Low Output	**ENABLE BIOS ROM** Active low to enable BIOS ROM (C0000h through C7FFFh) if enabled by PR1 register, bit 0. A write to WD90C33 internal I/O port 46E8h causes EBROM to be used as a write strobe for an external register used in BIOS ROM page mapping.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
44	IRQ	LOC, AT	Active High Output	**INTERRUPT REQUEST** For Local and AT bus modes, IRQ provides a programmable interrupt request to the host CPU. The interrupt request is enable by Vertical Retrace End Register, bit 5. When the end of vertical display occurs, this signal is active, requesting an interrupt, and it stays active until cleared by CRTC11 register bit 4.
	$\overline{IRQ}$	MC	Active Low Output	**INTERRUPT REQUEST** For MicroChannel bus mode, operation is the same as is Local and AT bus modes except that an active low IRQ is used.
Power Distribution				
13 24 42 53 80 104 109 119 129 141 167 181 185 197 208	VCC	---	---	**+5 VDC** Power supply pins.

TABLE 4-2 SIGNAL DESCRIPTIONS

PIN NO.	MNEMONIC	BUS	INPUT/ OUTPUT	DESCRIPTION
7 18 30 36 48 59 66 75 85 94 99 114 124 134 146 160 172 177 191 202	GND	---	---	**GROUND** Power return pins.
Unused Connections (10 Pins)				
153 154 155 156 157 158 159 173 174 175	No Connection	---	---	These pins are not connected to internal circuits of the WD90C33 controller.

TABLE 4-2 SIGNAL DESCRIPTIONS

4.4 HOST INTERFACE PIN MULTIPLEXING

Table 4-3 lists the WD90C33 connector pins that have more than one signal mnemonic depending on the host system bus structure where the video controller is used.

PIN NO.	SIGNAL MNEMONICS		
	LOCAL BUS INTERFACE	AT BUS	MICROCHANNEL BUS
37	LDEVBUSY	$\overline{0WS}$	$\overline{0WS}$
38	CPURESET	EMEM	EMEM
39	HRQ	$\overline{IOW}$	$\overline{CMD}$
40	$\overline{EBROM}$,	$\overline{EBROM}$	$\overline{EBROM}$
41	RDYIN	$\overline{IOCS16}$	$\overline{CDSETUP}$
43	LCLK	$\overline{EIO}$	3C3D0
44	IRQ	IRQ	$\overline{IRQ}$
45	$\overline{ADS}$	ALE	$\overline{ALD}$
46	$\overline{VGARDY}$	IOCHRDY	IOCHRDY
47	$\overline{BOFF}$	$\overline{ROM16}$	$\overline{CSFB}$
49	$\overline{LDEV}$	$\overline{MEMCS16}$	$\overline{CDDS16}$
50	W/$\overline{R}$	$\overline{IOR}$	$\overline{ST}$
51	M/$\overline{IO}$	$\overline{MRD}$	M/$\overline{IO}$
52	D/$\overline{C}$	$\overline{MWR}$	$\overline{S0}$
54	SYSRESET	RSET	RSET
55	$\overline{BE3}$	Not Used	Not Used
56	$\overline{BE2}$	A[1]	A[1]
57	$\overline{BE1}$	$\overline{BHE}$	$\overline{BHE}$
58	$\overline{BE0}$ or $\overline{BLE}$*	A[0]	A[0]
93-86	A[31:24]	Not Used	Not Used
84-81, 79-76, 74-67, 65-60	A[23:2]	A[23:2]	A[23:2]
95-98, 100-103, 105-108, 110-113	D[31:16]	D[31:16]	Not Used
115-118, 120-123, 125-128, 130-133	D[15:0]	D[15:0]	D[15:0]

* The signal on pin 58 is $\overline{BLE}$ for 386SX and $\overline{BE0}$ for all others.

TABLE 4-3 HOST INTERFACE PIN MULTIPLEXING

5.0 VGA/EGA REGISTERS

All the standard IBM registers incorporated inside the WD90C33 are functionally equivalent to the VGA implementation, while additional Western Digital registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA and CGA standards, which were previously defined for the 6845 CRT Controller. This section describes the VGA/EGA registers.

5.1 EGA MODE ENTRY

A brief description of the procedure for entering EGA mode of operation is provided here. The actual software implementation details are not covered in this procedure.

- Load Configuration Register Bit 8. Select logic 0 for a VGA-compatible PS/2 display or logic 1 for an EGA-compatible TTL monitor by using the appropriate pull-up or pull-down resistor on MD11. A pull-up resistor on MD11 causes CNF(8) to be latched with logic 0 for analog PS/2 compatible displays. This status information signifies the type of monitor attached to the system and is available to the BIOS or application.
- Unlock all the PR registers.
- Program PR2(6) to 0 for EGA mode.
- Set PR4 Bit 1 to logic 1 for EGA compatibility.
- Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on Pins MD(15:12). (A pull-up resistor causes logic 1 to be latched after power-on-reset.)
- The EGA switch setting may then be read from PR11(7:4) at I/O Port 3C2h Bit 4.
- If EGA mode is to be emulated on an IBM PS/2 analog display, follow the suggested steps listed below:
  - Initialize all the registers.
  - Lock CRT controller registers.
  - Force clock control rate of the CRT controller.
- Set EGA emulation mode by programming:
  - PR11(3) = 1; Set EGA emulation on PS/2 type display
  - PR14(6) = 1; Vertical double scan
  - PR11(2) = 1; Lock clock select
  - PR11(0) = 1; Lock 8/9 dot timing
  - PR14(7) = 1; Enable IRQ (optional).
  - Lock the PR registers PRO through PR5 and PR10 through PR17.
  - Read protect PR registers.
- When EGA is required on a TTL monitor, the suggested steps are:
  - Initialize all the registers.
  - Set EGA TTL mode by programming:
    - PR11(3) = 0; EGA TTL
    - PR14(7) = 1; Enable IRQ
    - PR15(6) = 1; Set Low Clock
    - PR14(7) = 1; Enable IRQ
    - Lock PR registers PRO through PR5 and PR10 through PR17.
    - Read protect PR registers.

Tables 5-1 and 5-2 summarize the VGA and EGA mode registers, respectively. For information about the PR registers, refer to Section 7.

5.2 VGA REGISTER SUMMARY

Table 5-1 lists the VGA registers.

REGISTERS[1]	RW[2]	MONO	COLOR	INDEX
GENERAL REGISTERS				
Miscellaneous Output Register	W	3C2	3C2	
	R	3CC	3CC	
Input Status Register 0	RO	3C2	3C2	
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	W	3BA	3DA	
	R	3CA	3CA	
Video Subsystem Enable Register[3]	RW	3C3	3C3	
SEQUENCER REGISTERS				
Sequencer Index Register	RW	3C4	3C4	
Sequencer Data Register	RW	3C5	3C5	00h:04h
CRT CONTROLLER REGISTERS				
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5	3D5	00h:18h
GRAPHICS CONTROLLER REGISTERS				
Index Register	RW	3CE	3CE	
Other Graphics Registers	RW	3CF	3CF	00h:08h
ATTRIBUTE CONTROLLER REGISTERS				
Index Register	RW	3C0	3C0	
Attribute Controller Data Register	W	3C0	3C0	00h:14h
	R	3C1	3C1	
VIDEO DAC PALLETTTE REGISTERS[4]				
Write Address	RW	3C8	3C8	
Read Address	W	3C7	3C7	
DAC State	R	3C7	3C7	
Data	RW	3C9	3C9	
Pel Mask	RW	3C6	3C6	
DRAWING ENGINE REGISTERS				
Index Control	RW	23C0/23C1	23C0/23C1	Refer to Sections 12 and 13.
Register Access Port	RW	23C2/23C3	23C2/23C3	
Host Bit Block Transfer (HBLT) Blocks 1 and 2	RW	23C4/23C7	23C4/23C7	
Command Buffer and Interrupt Control	RW	23CE/23CF	23CE/23CF	

NOTES:

1. All Register addresses are in hexadecimal.
2. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
3. I/O Port 3C3h can be used to replace 46E8h [if CNF(9) = 0] for setup in AT mode. In Micro-Channel mode, writes to 3C3h, Bit 0 = 1 enables memory and I/O address decoding.
4. PR16(0) = 1 locks these registers.

TABLE 5-1 VGA REGISTERS SUMMARY

Table 5-2 lists the EGA registers.

REGISTERS[1]	RW[2]	MONO	COLOR	INDEX
GENERAL REGISTERS				
Miscellaneous Output Register	WO	3C2	3C2	
Input Status Register 0	RO	3C2	3C2	
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	WO	3BA	3DA	
SEQUENCER REGISTERS				
Sequencer Index Register	WO	3C4	3C4	
Sequencer Data Register	RW	3C5	3C5	01h, 03h, 04h
CRT CONTROLLER REGISTERS				
Index Register	RW	3B4	3D4	
CRT Controller Data Register	RW	3B5[3]	3D5[3]	00h, 03h, 05h:07h, 09h:0Bh, 10h, 11h, 14h, 16h, 17h
GRAPHICS CONTROLLER REGISTERS				
Index Register	RW	3CE	3CE	
Other Graphics Registers	RW	3CF	3CF	04h:05h
ATTRIBUTE CONTROLLER REGISTERS				
Index Register	RW	3C0	3C0	
Attribute Controller Data Register	W	3C0	3C0	00h:13h
	R	3C1	3C1	

NOTES:

1. All Register addresses are in hexadecimal.
2. RO = Read-Only, WO = Write Only, RW = Read/Write, W = Write, and R = Read.
3. Miscellaneous Output Register bit 0 = 0, "B" in Monochrome modes
   Miscellaneous Output Register bit 0 = 1, "D" in Color modes
4. This table lists the registers that differ from VGA mode. The registers not listed are the same in VGA and EGA modes.

TABLE 5-2 EGA REGISTERS SUMMARY

5.4 GENERAL REGISTERS

REGISTER NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES

1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as follows:
   0 = B in Monochrome Modes
   1 = D in Color Modes
3. Unless specifically identified, the descriptions apply to both VGA and EGA.

5.4.1 Miscellaneous Output Register, VGA - Read Port = 3CCh, VGA/EGA - Write Port = 3C2h

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3:2	Video Clock Select
1	Enable Video RAM
0	I/O Address Select

Bit 7 - Vertical Sync Polarity Selection.

This bit is locked if PR3(7) = 1

0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 - Horizontal Sync Polarity Selection.

This bit is locked if PR3(6) = 1

0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

The vertical and horizontal sync polarity bits (bits 7:6) should be set to conform with the vertical size of the frame used by the monitor.

VERTICAL FRAME SIZE

00 = Reserved

01 = 400 lines/scan

10 = 350 lines/scan

11 = 480 lines/scan

Bit 5 - Odd or Even Memory Page Select.

When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.

0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved.

Bits (3:2) - Video Clock Select.

These bits are locked if PR11(2) = 1 or if PR2(1) = 1 and CNF(3) = 0.

00 = Selects VCLK0 for VGA/EGA applications. For VGA, can be connected to allow 640 dots/line (25.175 MHz). For EGA, 14.318 MHz is selected.
01 = Selects VCLK1 for VGA/EGA applications if Configuration Register Bit 3 = 0. For VGA, can be connected to allow 720 dots/line (28.322 MHz). For EGA, 16.257 MHz clock is selected.
10 = Selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.
11 = Reserved. Also selects VCLK2 (external user defined input) if Configuration Register Bit 3 = 0.

Bit 1 - VGA - System Processor Video RAM Access Enable.

0 = CPU access disabled.
1 = CPU access enabled.

EGA - Reserved.

Bit 0 - CRT Controller I/O Address Range Selection

Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

5.4.2 Input Status Register 0, Read Only Port = 3C2h

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7 - CRT Vertical Retrace Interrupt Pending or Cleared.

0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bits (6:5)

Reserved.

Bit 4 - VGA Mode - Monitor Detection.

MDET monitor status is sampled and can be read from this bit.

0 = Monochrome.
1 = Color.

EGA Mode - Configuration Switches SW4-SW1

The information stored in the four configuration switches in PR11 can be read at this bit if the EGA compatibility bit PR4(1) has been set to 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2h as follows.

WRITE 3C2h		READ 3C2h Bit 4
Bit 3	Bit 2	
0	0	PR11(7) = EGA SW4
0	1	PR11(6) = EGA SW3
1	0	PR11(5) = EGA SW2
1	1	PR11(4) = EGA SW1

These bits may be used as general purpose scratch bits.

Bits (3:0)

Reserved. In EGA mode they must be set to 1.

5.4.3 Input Status Register 1, Read Only Port = 3?Ah

BIT	FUNCTION
7:6	Reserved
5:4	Diagnostic
3	Vertical Retrace
2:1	Reserved
0	Display Enable

Bits (7:6)

Reserved. In EGA mode, bit 6 must be set to 1.

Bits (5:4) - Color Plane Diagnostics.

These bits return two of the eight video outputs VID7 through VID0, as selected by Color Plane Enable Register Bits 5 and 4 (refer to Section 5.6.6.)

Bit 3 - Vertical Retrace Status.

0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bits (2:1)

Reserved. In EGA mode bit 2 must be set to 1.

Bit 0 - Display Enable Status.

0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.4.4 Feature Control Register, VGA - Read Port = 3CAh, VGA/EGA - Write Port = 3?Ah

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits (7:4)

Reserved

Bit 3 - VGA - Vertical Sync Control.

0 = VSYNC output enabled.
1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

EGA - Reserved

Bits (2:0)

Reserved

5.5 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4h	-----	Sequencer Index
3C5h	00	Reset
3C5h	01	Clocking Mode
3C5h	02	Map Mask
3C5h	03	Character Map Select
3C5h	04	Memory Mode

NOTE

Reserved bits should be set to zero.

5.5.1 Sequencer Index Register, Read/Write Port = 3C4h - VGA/EGA

BIT	FUNCTION
7:5	Reserved
4:0	Sequencer Address/Index Bits

Bits (7:5)

Reserved.

Bits (4:0) - Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00h-04h) of the Sequencer Register to be accessed. Sequencer extension registers are also indexed by this register.

5.5.2 Reset Register, Read/Write Port = 3C5h, Index = 00h - VGA/EGA

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits (7:2)

Reserved.

Bit 1 - Synchronous Reset.

0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0 - Asynchronous Reset.

0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

NOTE

Both bits 1 and 0 must be set to 1 for Operational mode.

5.5.3 Clocking Mode Register, Read/Write Port = 3C5h, Index = 01h

Bits 5:2 are locked if PR11(1) = 1. They appear unlocked during reads.

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits (7:6)

Reserved.

Bit 5 - VGA - Screen Off.

0 = Normal screen operation.

1 = Screen is turned off but SYNC signals remain active. This bit may be used to provide maximum display memory bandwidth for quick full screen updates.

EGA - Reserved

Bit 4 - VGA - Video Serial Shift Register Loading.

0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.

1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

EGA - Reserved

Bit 3 - Dot Clock Selection.

0 = Normal dot clock selected by VCLK input frequency.

1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2 - Shift Load. Effective Only If Bit 4 = 0.

0 = Video serializers are loaded every character clock.

1 = Video serializers are loaded every other character clock.

Bit 1

Reserved. In EGA mode bit 1 must be set to 0.

Bit 0 - 8/9 Dot Clock.

Commands Sequencer to generate an eight or nine dot wide character clock.

This bit is locked if PR11(0) = 1

0 = Nine dot wide character clock.

1 = Eight dot wide character clock.

5.5.4 Map Mask Register, Read/Write Port = 3C5h, Index = 02h - VGA/EGA

BIT	FUNCTION
7:4	Reserved
3:0	Map 3:0 Enable

Bits (7:4)

Reserved.

Bits (3:0) - Enables Writing to Memory Maps 3 Through 0, Respectively.

0 = Writing to respective Memory Map disabled.

1 = Writing to respective Memory Map enabled.

5.5.5 Character Map Select Register, Read/Write Port = 3C5h, Index = 03h

Bits 5:0 are locked if PR11(1) = 1. They appear unlocked during reads.

BIT	FUNCTION
7:6	Reserved
5, 3, 2	Character Map Select A Bits 2:0
4,1, 0	Character Map Select B Bits 2:0

If Sequencer Register 4, Bit 1 = 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. A "0" selects Character Map B. A "1" selects Character Map A. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and Bit 4 of the attribute code.

Bits (7:6)

Reserved. VGA

Bits (7:4)

Reserved. EGA

Bits 5, 3, 2 - VGA - Character Map A Select.

These bits select the location of Character Map A as shown below.

BITS			MAP	FONT/PLANE 2 OR 3 LOCATION
5	3	2		
0	0	0	0	1st 8 KByte Block
0	0	1	1	3rd 8 KByte Block
0	1	0	2	5th 8 KByte Block
0	1	1	3	7th 8 KByte Block
1	0	0	4	2nd 8 KByte Block
1	0	1	5	4th 8 KByte Block
1	1	0	6	6th 8 KByte Block
1	1	1	7	8th 8 KByte Block

Bits (3:2) - EGA - Character Map A Select.

These bits select the location of Character Map A as shown below.

BITS		MAP	FONT/PLANE 2 LOCATION
3	2		
0	0	0	1st 8 KByte Block
0	1	1	2nd 8 KByte Block
1	0	2	3rd 8 KByte Block
1	1	3	4th 8 KByte Block

Bits 4, 1, 0 - VGA - Character Map B Select.

These bits select the location of Character Map B as shown below.

BITS			MAP	FONT/PLANE 2 OR 3 LOCATION
4	1	0		
0	0	0	0	1st 8 KByte Block
0	0	1	1	3rd 8 KByte Block
0	1	0	2	5th 8 KByte Block
0	1	1	3	7th 8 KByte Block
1	0	0	4	2nd 8 KByte Block
1	0	1	5	4th 8 KByte Block
1	1	0	6	6th 8 KByte Block
1	1	1	7	8th 8 KByte Block

Bits (1:0) - EGA - Character Map B Select.

These bits select the location of Character Map B as shown below.

BITS		MAP	FONT/PLANE 2 LOCATION
1	0		
0	0	0	1st 8 KByte Block
0	1	1	2nd 8 KByte Block
1	0	2	3rd 8 KByte Block
1	1	3	4th 8 KByte Block

NOTE

Character Map selection from Plane 2 is determined by bit 3 of the attribute code.

5.5.6 Memory Mode Register, Read/Writ Port = 3C5h, Index = 04h

BIT	FUNCTION
7:4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bits (7:4)

Reserved.

Bit 3 - VGA - Chains Four Maps.

0 = Processor sequentially accesses data using Map Mask Register.

1 = Directs the two lower order video Memory Address pins (MA1, MA0) to select the map to be addressed. The map selection is given in the following list:

MA1	MA0	MAP
0	0	0
0	1	1
1	0	2
1	1	3

- EGA - Reserved

Bit 2 - VGA/EGA - Odd/Even Map Selection.

0 = Even processor addresses to access Maps 0 and 2. Odd processor addresses to access Maps 1 and 3.

1 = Sequential processor access as defined by Map Mask Register.

Bit 1 - VGA/EGA - Extended Video Memory.

0 = 64 KB of video memory.

1 = Greater than 64 KB of memory for VGA/ EGA modes.

Bit 0 - VGA - Reserved
EGA - Alpha Mode

0 = Disables Alpha modes and enables non-Alpha modes.

1 = Alpha mode is active and character map selection is enabled.

5.6 CRT CONTROLLER REGISTERS

Table 5-3 lists the CRT Controller registers and their equivalent 6845 registers, if applicable.

PORT[1]	INDEX	VGA/EGA REGISTER NAME	6845[2] REGISTER NAME
3?4	---	CRT Controller Address Register	CRTC Address Register
3?5	00[3]	Horizontal Total	Horizontal Total
3?5	01	Horizontal Display Enable End	Horizontal Display
3?5	02	Start Horizontal Blanking	See note 4.
3?5	03[3]	End Horizontal Blanking	See note 4.
3?5	04	Start Horizontal Retrace	See note 4.
3?5	05[3]	End Horizontal Retrace	See note 4.
3?5	06[3]	Vertical Total	+ Vertical Display
3?5	07[3]	Overflow	See note 4.
3?5	08	Preset Row Scan	See note 4.
3?5	09[3]	Maximum Scan Line	Maximum Scan Line Address
3?5	0A[3]	Block Cursor Start	Cursor Start
3?5	0B[3]	Block Cursor End	Cursor End
3?5	0C	Start Address High	Start Address High
3?5	0D	Start Address Low	Start Address Low
3?5	0E	Block Cursor Location High	Cursor Location High
3?5	0F	Block Cursor Location Low	Cursor Location Low
3?5	10[3]	Vertical Retrace Start	Light Pen High Read
3?5	11[3]	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	See note 4.
3?5	13	Offset	See note 4.
3?5	14[3]	Underline Location	See note 4.
3?5	15	Start Vertical Blank	See note 4.
3?5	16[3]	End Vertical Blank	See note 4.
3?5	17[3]	CRTC Mode Control	See note 4.
3?5	18	Line Compare	See note 4.
3?5	23	Horizontal Counter Test	See note 4.

NOTES:

1. The value of ? is controlled by Miscellaneous Output Register, bit 0. Bit 0 is programmed as follows:
   When bit 0 is set to 0, ? = B and is used in Monochrome modes.
   When bit 0 is set to 1, ? = C and is used in Color modes.
2. For detailed descriptions of the 6845 Mode Registers refer to the literature listed following the table of contents.
3. Parameters for these registers vary depending on whether they are used in VGA or EGA mode.
4. This register can be programmed in VGA/EGA mode only. It is not applicable in 6845 mode.
5. Reserved bits should be set to zero.

TABLE 5-3 CRT CONTROLLER REGISTERS

5.6.1 CRT Register Index, Read/Write Port = 3?4h

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bits (7:5)

Reserved.

Bits (4:0) - CRT Register Index Bits.

These bits specify the CRT Controller register to be addressed. Its value is programmed in hexadecimal.

5.6.2 Horizontal Total Register, Read/Write Port = 3?5h, Index = 00h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Horizontal Total Period

Bits (7:0)- VGA - Count Plus Retrace Less Five
EGA - Count Plus Retrace Less Two.

The total character count is the total number of characters including retrace time per horizontal scan line, less 5 in VGA mode, less 2 in EGA mode.

5.6.3 Horizontal Display Enable End Register, Read/Write Port = 3?5h, Index 01h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Displayed Characters per Scan Line

Bits (7:0) - Number Of Displayed Characters Less One

This register contains the total number of displayed characters less one.

5.6.4 Start Horizontal Blanking Register, Read/Write Port = 3?5h, Index = 02h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the value written in this register.

5.6.5 End Horizontal Blanking, Read/Write Port = 3?5h, Index = 03h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

Bit 7

Reserved

Bits (6:5) - Display Enable Signal Skew Control
These bits define the display enable signal skew time in relation to horizontal synchronization pulses.

BITS		CHARACTER CLOCK SKEW
6	5	
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0) - End Horizontal Blanking.
- VGA Mode

These five bits, along with bit 7 of the End Horizontal Retrace Register (Index 05h), determine when horizontal blanking is to end. Bits 4:0 are the least significant bits, bit 7 is the most significant bit.

When the least significant six bits of the Horizontal Character Counter matches these six bits, the horizontal blanking ends.

EGA Mode

These five bits, determine when horizontal blanking is to end. When the least significant five bits of the Horizontal Character Counter matches these five bits, the horizontal blanking ends.

5.6.6 Start Horizontal Retrace Pulse Register, Read/Write Port = 3?5h, Index = 04h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits (7:0) - Start Horizontal Retrace Character Count

The character count at which the horizontal retrace output is to become active is programmed in this register as a hexadecimal value.

5.6.7 End Horizontal Retrace Register, Read/Write Port = 3?5h, Index = 05h

This register is locked if register PR3(5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7	End Horizontal Blank Bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

Bit 7 - VGA - End Horizontal Blank Bit 6.

This is the sixth bit (Bit 5) of the End Horizontal Blanking Value programmed in bits 4:0 of the End Horizontal Blanking Register at Port 3?5h, Index 03h.

- EGA - CRT Counter Memory Address.

This bit defines whether the CRT counter memory address starts at an even or odd address following the horizontal retrace.

0 = Even Address
1 = Odd Address

Bits (6:5) - Horizontal Retrace Delay.

These bits define the horizontal retrace signal delay.

BITS		CHARACTER CLOCK DELAY
6	7	
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0) - End Horizontal Retrace

The least significant five bits are programmed in this register. When the least significant bits of the Horizontal Character Counter match these five bits, the Horizontal Retrace signal is turned off.

5.6.8 Vertical Total Register, Read/Write Port = 3?5h, Index = 06h

This register is locked if register PR3(0) = 1, or the Vertical Retrace End Register Bit 7 = 1.

BIT	FUNCTION
7:0	Raster Scan Line Total Less 2

Bits (7:0) - VGA - Raster Scan Line Total Less 2

This register contains the least significant eight bits of an eleven bit count of raster scan lines for a display frame. The programmed value includes the total number of vertical scan lines, minus two. Time for vertical retrace and vertical sync are also included. Bit 10 of this count is in register PR18 at Port 3?5h, Index 3Eh, Bit 0. Bits 9 and 8 of this count are loaded into the Vertical Overflow Register at Port 3?5h, Index 07h, Bit 5 and Bit 0, respectively.

In 6845 mode, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09h Bits 4 through 0).

- EGA - CRT Vertical Frame Time.

This register contains the least significant eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

5.6.9 Overflow Vertical Register, Read/Write Port = 3?5h, Index = 07h

BIT	FUNCTION
7, 2	Start Vertical Retrace Bits 9:8
6, 1	End Vertical Display Enable Bits 9:8
5, 0	Vertical Total Bits 9:8
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8

Bits (7:5) - EGA

Reserved

Bits 7, 2 - VGA

Start Vertical Retrace - Bits 9:8. (Bits 7:0 are at Index 10h.)

This register is locked if Register PR3(0) = 1 **or** the End Vertical Retrace Register Bit 7 = 1.

Bits 6, 1 - VGA

End Vertical Display Enable - Bits 9:8. (Bits 7:0 are at Index 12h.

This register is locked if Register PR3(1) = 0 **and** the End Vertical Retrace Register Bit 7 = 1.

Bits 5, 0 - VGA

Vertical Total - Bits 9:8. (Bits 7:0 are at Index 06h.)

This register is locked if Register PR3(0) = 1 **or** the End Vertical Retrace Register Bit 7 = 1.

Bit 4 - VGA/EGA

Line Compare - Bit 8. (Bit 9 is at Bit 6 of index 09h, Bits 7:0 are at Index = 18h.)

Bit 3 - VGA/EGA

Start Vertical Blank - Bit 8. (Bit 9 is at Bit 5 of index 09h, Bits 7:0 are at Index =15h.)

This register is locked if Register PR3(0) = 1 **or** the End Vertical Retrace Register Bit 7 = 1.

Bits 2 - EGA

Start Vertical Retrace - Bit 8. (Bits 7:0 are at Index 10h.)

This register is locked if Register PR3(0) = 1 **or** the End Vertical Retrace Register Bit 7 = 1.

Bits 1 - EGA

End Vertical Display Enable - Bit 8. (Bits 7:0 are at Index 12h.).

This register is locked if Register PR3(1) = 0 **and** the End Vertical Retrace Register Bit 7 = 1.

Bits 0 - EGA

Vertical Total - Bit 8. (Bits 7:0 are at Index 06h.).

This register is locked if Register PR3(0) = 1 **or** the End Vertical Retrace Register Bit 7 = 1.

5.6.10 Preset Row Scan Register, Read/Write Port = 3?5h, Index = 08h

BIT	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits (6:5) - Byte Panning Control.

These bits allow up to three bytes to be panned in modes programmed as multiple shift modes.

OPERATION

0 0 = Normal
0 1 = 1 Byte Left Shift
1 0 = 2 Bytes Left Shift
1 1 = 3 Bytes Left Shift

Bits (4:0) - Preset Row Scan Count

These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period until the maximum row scan count is reached. When the maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

5.6.11 Maximum Scan Line Register, Read/Write Port = 3?5h, Index = 09h

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

In 6845 mode, Bits 7 through 5 are reserved,

Bits (7:5) - EGA

Reserved

Bit 7 - VGA - 200 to 400 Line Conversion

0 = Normal operation.

1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines. Each line is double scanned.

Bit 6 - VGA - Line Compare

This is Bit 9 of the Line Compare Register at Port 3?5h, Index 18h.

Bit 5 - VGA - Start Vertical Blank

This is Bit 9 of the Start Vertical Blank Register at Port 3?5h, Index 15h. The Vertical Blank Register is locked if register PR3(0) = 1. or the Vertical Retrace End Register Bit 7 = 1.

Bits (4:0) - VGA/EGA - Maximum Scan Line

These bits are the maximum number of scanned lines for each row of characters. The value programmed is one less than the maximum number of scanned rows per character.

In 6845 mode, the value programmed is one less than the maximum scan line count for non-interlace mode. Interlaced mode is not supported.

5.6.12 Block Cursor Start Register, Read/Write Port = 3?5h, Index = 0Ah

BIT	FUNCTION
7:6	Reserved
5	Block Cursor Control
4:0	Block Cursor Start Scan Line

Bits (7:6)

Reserved.

Bit 5 - VGA - Block Cursor Control

0 = Block Cursor on.

1 = Block Cursor off.

- EGA - Reserved

Bits (4:0) - VGA/EGA - Block Cursor Start Scan Line

These bits specify the value of the row scan counter within the cursor's starting character box. These bits are programmed with one less than the value of the character row. If these bits are programmed with a value greater than the Block Cursor End Register at Port 3?5h, Index 0Bh, no cursor is generated.

For 6845 modes, Bits 7 and 6 are reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value.

5.6.13 Block Cursor End Register, Read/Write Port = 3?5h, Index = 0Bh

BIT	FUNCTION
7	Reserved
6:5	Block Cursor Skew
4:0	Block Cursor End Scan Line

In 6845 mode, Bits 7 through 5 are reserved.

Bit 7

Reserved.

Bits (6:5) - Block Cursor Skew Bits

Moves the displayed cursor to the right by the skew value in character clocks, e.g., one character clock skew moves the cursor right by one position on the screen.

SKEW

0 0 = 0 Character Clocks
0 1 = 1 Character Clocks
1 0 = 2 Character Clocks
1 1 = 3 Character Clocks

Bits (4:0) - VGA - Block Cursor End Scanline.

These bits specify the value of the last row scan counter within the character box in which the cursor is active. If this value is less than the cursor start value, no cursor is displayed.

In 6845 mode, Bits 4 through 0 contain the row value of the cursor end.

NOTE

There are three types of cursors generated, depending upon the mode, i.e, VGA, EGA or 6845 (non-VGA). The above description refers to the VGA cursor only.

- EGA - Block Cursor End Scanline.

These bits specify the Cursor End value of the last row scan address counter. The programmed value is equal to N+1 where N is the last row of the cursor to be displayed.

5.6.14 Start Address High Register, Read/Write Port = 3?5h, Index = 0Ch

BIT	FUNCTION
7:0	Start Address High Byte

Bits (7:0) - Display Screen Start Address Upper Byte Bits.

These are the high order eight bits of the 16-bit video memory address, used for screen refresh. The low order 8-bit register is at Port 3?5h Index 0Dh. Register PR3 Bits 4 and 3 extend this video memory start register to 18 bits.

In 6845 mode, Bits 7 and 6 are forced to 0 regardless of this register's contents. The lower order eight bits are at Port 3?5h Index 0Dh.

5.6.15 Start Address Low Register, Read/ Write Port = 3?5h, Index = 0Dh

BIT	FUNCTION
7:0	Start Address Low Byte

Bits (7:0) - Start Address Low Byte.

These are the low order eight bits of the 16-bit video memory address in VGA/EGA or 6845 modes.

5.6.16 Block Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7:0	Block Cursor Location High Byte

Bits (7:0) - Block Cursor Address Upper Byte Bits.

In VGA mode, these are the eight high order bits of the 16-bit cursor location. For the low order eight bits, see the Block Cursor Location Low Register at Port 3?5h, Index 0Fh. Register PR3 Bits 4 and 3 extend the cursor location High Register to 18 bits.

In 6845 mode, Bits 7 and 6 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

5.6.17 Block Cursor Location Low Register, Read/Write Port = 3?5h, Index = 0Fh

BIT	FUNCTION
7:0	Block Cursor Location Low Byte

Bits (7:0) - Block Cursor Address Low Byte Bits

These are the low order eight bits of the 16-bit video memory address in VGA/EGA or 6845 mode.

5.6.18 Vertical Retrace Start Register, Read/Write Port = 3?5h, Index = 10h

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Vertical Retrace Start (Lower eight bits)

Bits (7:0) - Vertical Retrace Start Pulse Lower Eight Bits

In VGA mode, these are the lower eight bits of the 11-bit Vertical Retrace Start Register. Bit 10 is located in 3?5h, Index 3Eh, Bit 2. Bits 9 and 8 are located in the Overflow Register at Port 3?5h, Index 07h.

In 6845 mode, Bits 7 and 6 are reserved. Bits 5 through 0 are read back as the high order six bits of the Light Pen Value. The lower order eight bits of the Light Pen Value are read back at Index 11h.

In EGA mode, this register is read back as the low order eight bits of the Light Pen Value.

5.6.19 Vertical Retrace End Register, Read/Write Port = 3?5h, Index = 11h

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End.

In 6845 mode, this register reads back the value of the lower eight bits of Light Pen Register.

Bit 7 - VGA - CRTC Registers Write Protect

0 = Enables writing to CRT index registers 00h-07h.

1 = Write protects CRT Controller index registers in the range of index 00h-07h. Line Compare Bit 4 in the Overflow Register (07h) is not protected.

- EGA - Reserved

Bit 6 - VGA - DRAM Refresh/Horizontal Scan Line T-52-33-45

This bit selects DRAM refresh cycles per horizontal scan line.

0 = Generates three refresh cycles for each horizontal scan line for normal VGA operation.

1 = Generates five DRAM refresh cycles per horizontal scan line.

- EGA - Reserved

Bit 5 - VGA - Enable Vertical Retrace Interrupt

0 = Enable vertical retrace interrupt.

1 = Disable vertical retrace interrupt.

- EGA - IRQ Output Buffer

0 = The IRQ output buffer control is enabled. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal.

1 =The IRQ output buffer is switched to a high impedance state.

Bit 4 - VGA - Clear Vertical Retrace Interrupt

0 = Clears the vertical retrace interrupt by writing a 0 to (resetting) an internal flip flop.

1 = Vertical retrace interrupt. This allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

- EGA - IRQ Latch

0 = The IRQ latch is reset if bit 5 = 0.

1 = The IRQ latch is set at the end of the vertical display.

Bits (3:0) - VGA/EGA - Vertical Retrace End

These bits specify the scan count at which vertical sync becomes inactive. When these four bits match the four low-order bits of the vertical counter, vertical sync becomes inactive.

Bits (3:0) are locked if register PR3(0) = 1.

5.6.20 Vertical Display Enable End Register, Read/Write Port = 3?5h, Index = 12h

BIT	FUNCTION
7:0	Vertical Display Enable End (Lower eight bits)

Bits (7:0) - Vertical Display Enable End Lower Eight Bits.

These bits define where the active display frame ends and are the lower eight bits of an 11-bit register. The programmed count is in scan lines minus one. Bit 10 is in Port 3?5h, Index 3Eh, Bit 10. Bits 9 and 8 are in the Overflow Register at Port 3?5h, Index 07h, Bits 6 and 1, respectively.

5.6.21 Offset Register, Read/Write Port = 3?5h, Index = 13h

BIT	FUNCTION
7:0	Logical Line Screen Width

Bits (7:0) - Logical Line Screen Width

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address equals the Current Row Scan Start Address, plus the product of the Offset Register multiplied by either 2 in the byte mode or 4 in word mode.

5.6.22 Underline Location Register, Read/Write Port = 3?5h, Index = 14h

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7 - VGA/EGA

Reserved.

Bit 6 - VGA - Doubleword Mode.

0 = Display memory addressed for byte or word access.

1 = Display memory addressed for doubleword access. This overrides the state of Port 3?5h, Index 17h, Bit 6 (refer to bit 6 in Section 5.4.25).

- EGA - Reserved

Bit 5 - VGA - Count by Four for Doubleword Access.

0 = Memory address counter clocked for byte or word access.

1 = Memory address counter is clocked at the character clock rate divided by four.

- EGA - Reserved

Bits (4:0) - VGA/EGA - Underline Location.

These bits specify the row scan counter value within a character matrix where underline is to be displayed. The value programmed should be one less than the desired scan line number.

5.6.23 Start Vertical Blank Register, Read/Write Port = 3?5h, Index =15h

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	Start Vertical Blank (Lower eight bits)

Bits (7:0) - Start Vertical Blank Lower Eight Bits.

These are the lower eight bits of the 11-bit Start Vertical Blank Register. Bit 10 is in register PR18 at Port 3?5h, Index 3Eh, Bit 3. Bit 9 is in the Maximum Scan Line Register at Port 3?5h, Index 09h. Bit 8 is in the Overflow Register at Port 3?5h, Index 07h.

The eleventh bit value is reduced by one from the desired scan line count where the vertical blanking signal starts.

5.6.24 End Vertical Blank Register, Read/Write Port = 3?5h, Index = 16h

This register is locked if register PR3(0) = 1.

BIT	FUNCTION
7:0	End Vertical Blank

Bits (7:0) - VGA - Vertical Blank Inactive Count

End Vertical Blank is an eight-bit value calculated as follows:

Eight-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

Bits (7:5) - EGA

Reserved

Bits (4:0) - EGA

End Vertical Blank is a five-bit value calculated as follows:

Five-bit End Vertical Blank value = (value of Start Vertical Blank minus one) + (value of Vertical Blank signal width in scan lines).

5.6.25 CRT Mode Control Register, Read/Write Port = 3?5h, Index = 17h

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select.
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7 - VGA/EGA - Hardware Reset

0 = Horizontal and vertical retrace outputs inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6 - VGA/EGA - Word or Byte Mode

The state of this bit is ignored and Doubleword mode selected when Port 3?5h, Index 14h, Bit 6 is set to 1 (refer to Section 5.4.22, Bit 6).

0 = Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB.
1 = Byte address mode.

CRT14h BIT 6	CRT17h BIT 6	ADDRESS MODE
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 - VGA/EGA - Address Wrap

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MA0.
1 = Select MA15 for odd/even mode when 256 Kbytes of video memory are used on the system board.

Bit 4 - VGA/EGA

Reserved.

Bit 3 - VGA/EGA - Count by 2

0 = Character clock increments memory address counter.
1 = Character clock divided by two increments the address counter.

Bit 2 - VGA/EGA - Horizontal Retrace Clock Rate Select for Vertical Timing Counter

This bit is locked if register PR3(5) = 1.

0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by two.

Bit 1 - VGA/EGA - Select Row Scan Counter

0 = Row Scan Counter Bit 1 replaces CRTC when MA14 is selected to drive an address pin.
1 = CRTC drives MA14 when MA14 is selected to drive an address pin.

Bit 0 - 6845 CRT Controller Compatibility Mode Support for CGA Operation

0 = Row Scan Counter Bit 1 replaces CRTC when MA13 is selected to drive an address pin.

1 = CRTC drives MA13 when MA13 is selected to drive an address pin.

5.6.26 Line Compare Register, Read/Write Port = 3?5h, Index = 18h

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bits (7:0) - Line Compare Lower Eight Bits

These are the lower eight bits of the ten-bit Scan Line Compare Register. Bit 9 is in the Maximum Scan Line Register at Port 3?5h, Index 09h. Bit 8 is in the Overflow Register at Port 3?5h, Index 07h. When the vertical counter reaches the value programmed in the Scan Line Compare Register, the internal start of the line counter is cleared.

5.6.27 Horizontal Counter Test Register 23, Read/Write Port = 3?5h, Index = 23h

BIT	FUNCTION
7:0	Horizontal Counter Test Register (One Additional Bit)

Bits (7:0) - Horizontal Counter Test Register

(To be supplied.)

5.7 GRAPHICS CONTROLLER REGISTERS

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PORT (HEX)	INDEX (HEX)	NAME
3CE	--	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

TABLE 5-4 GRAPHICS CONTROLLER REGISTERS

NOTE

Reserved bits should be set to zero.

5.7.1 Graphics Index Register, Read/Write Port = 3CEh

BIT	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits (7:4)

Reserved.

Bits (3:0) - Graphics Controller Register Index Pointer Bits

NOTE

Some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.7.2 Set/Reset Register, Read/Write Port = 3CFh, Index = 00h

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Set/Reset Map

When the CPU executes display memory write with Write Mode 0* selected, and the Enable Set/Reset Register at Port 3CFh Index 01h activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight-bit fill operation.

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE

*The selection of Write Mode 0 is determined by the Graphics Mode Register (Index = 05h) Bit 1 and Bit 0.

5.7.3 Enable Set/Reset Register, Read/Write Port = 3CFh, Index = 01h

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Enable Set/Reset Register Maps 3 through 0, respectively (Index 00h)

0 = In Write Mode 0, each bit (3:0) when set to 0, disables its corresponding Set/Reset Register (Index = 00h) bit and the corresponding memory map is written with the rotated 8-bit data from the system microprocessor, as defined by the Data Rotate Register.

1 = In Write Mode 0, each bit (3:0) when set to 1, enables memory map access defined by the corresponding Set/Reset Register (Index = 00h) bit and the respective memory map is written with the Set/Reset Register value.

5.7.4 Color Compare Register, Read/Write Port = 3CFh, Index = 02h

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Color Compare

The Color Compare bits contain the value to which all eight bits of the corresponding memory map are compared. This comparison also occurs across all four maps and a 1 is returned for the map positions when the bits of all four maps equal the Color Compare Register. If a system read is done with Bit 3 = 0 for the Graphics Mode Register at Port 3CFh, Index 05h, data is returned without comparison. Color compare map coding is shown in the following table.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.7.5 Data Rotate Register, Read/Write Port = 3CFh, Index = 03h

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits (7:5)

Reserved.

Bits (4:3) - Function Select

This is the Function Select for any of the write mode operations defined in the Graphics Mode Register at Port 3CFh, Index 05h as defined below.

00 = Video memory data unmodified.
01 = Video memory data ANDed with system data in the latches.
10 = Video memory data ORed with system data in the latches.
11 = Video memory data XORed with system data in the latches.

NOTE

"Data" refers to CPU data that has gone through data rotation. The latches contain the data from the last memory read operation.

Bits (2:0) - Rotate Count

These bits specify the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register at Port 3CFh, Index 05h.

5.7.6 Read Map Select Register, Read/Write Port = 3CFh, Index = 04h

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BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits (7:3) - VGA/EGA

Reserved.

Bit 2 - VGA

Reserved.

Bits (2:0) - EGA - Map Select

These bits select the memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value is defined below.

BITS			FUNCTION
2	1	0	
0	0	0	Map 0 selected
0	0	1	Map 1 selected
0	1	0	Map 2 selected
0	1	1	Map 3 selected

Bits (1:0) - VGA - Map Select

These bits select the memory map in memory read operations. It has no effect on color compare read mode. In odd/even modes, the value is defined below.

BITS		FUNCTION
1	0	
0	0	Map 0 selected
0	1	Map 1 selected
1	0	Map 2 selected
1	1	Map 3 selected

5.7.7 Graphics Mode Register, Read/Write Port = 3CFh, Index = 05h

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7 - VGA/EGA -

Reserved.

Bit 6 - EGA

Reserved

Bit 6 - VGA - 256 Color Mode

This bit is locked if PR11(1) = 1. It appears unlocked during reads.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four-bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID7, VID6) are determined by Bits 3 and 2 of the Color Select Register located at Port 3C1h/3C0h, Index 14h within the Attribute Controller.

1 = Load Video Shift Registers to support 256-color mode

Bit 5 - VGA/EGA - Shift Register

Shift Register Load controls the way in which memory data is formatted in the four Video Shift Registers. MSB is shifted out in all cases.

This bit is locked if PR11(1) = 1. It appears unlocked during reads.

0 = Map 3 through Map 0 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 - VGA/EGA - Odd/Even Mode

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the Sequencer Memory Mode Register at Port 3CFh, Index 04h. Even system addresses access Maps 2 or 0 and odd system addresses access Maps 3 or 1.

Bit 3 - VGA/EGA - Read Mode

0 = System reads data from memory maps selected by Read Map Select Register at Port 3CFh, Index 04h. This setting has no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2 - VGA/EGA

Reserved.

Bits (1:0) - VGA/EGA - Write Mode

Table 5-5 defines the four write modes.

BIT 1	BIT 0	WRITE MODE	DESCRIPTION
0	0	0	If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data, which is rotated right by the number of bits defined in the Data Rotate Register. This results in the previous LSB becoming the current MSB.
0	1	1	This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	2	Memory maps 3:0 are filled with the eight-bit value of the corresponding CPU data bits 3:0. The 32-bit output from the four memory maps is then operated on by the Bit Mask register and the resulting data are written to the four memory maps.
1	1	3	Eight bits of the value contained in the Set/Reset Register (index = 00h) are written into the corresponding map, regardless of the Enable Set/Reset Register (index 01h) value. The right rotated CPU data (refer to Write Mode 0) are ANDed with Bit Map Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in write modes 0 and 2. In EGA mode, Write Mode 3 is not valid and if selected will default to Write Mode 1.

TABLE 5-5 WRITE MODES

5.7.8 Miscellaneous Register, Read/Write Port = 3CFh, Index = 06h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits (7:4)

Reserved.

Bits (3:2) - Memory Map 1, 0

Display memory map control into the CPU address space is shown below:

BITS			
3	2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0h-BFFF:Fh	128KB
0	1	A000:0h-AFFF:Fh	64KB
1	0	B000:0h-B7FF:Fh	32KB
1	1	B800:0h-BFFF:Fh	32KB

Bit 1 - Odd/Even Mode

0 = CPU address Bit A0 is the memory address Bit MA0.

1 = CPU address Bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects Map 2 or 0, while A0 = 1 selects Map 3 or 1.

Bit 0 - Graphics/Alphanumeric Mode

This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register at Port 3C1h/ 3C0h, Index 10h.

0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.7.9 Color Don't Care Register, Read/Write Port = 3CFh, Index = 07h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits (7:4)

Reserved.

Bits (3:0) - Memory Map Color Compare Operation

0 = Disable color compare operation.
1 = Enable color compare operation.

5.7.10 Bit Mask Register, Read/Write Port = 3CFh, Index = 08h

BIT	FUNCTION
7:0	Bit Mask

Bits (7:0) - Bit Mask

Bit Mask operation applies simultaneously to all four maps. In Write Modes 2 and 0, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.8 ATTRIBUTE CONTROLLER REGISTERS

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PORT (HEX)	INDEX (HEX)	NAME
3C0	---	Index Register
3C0	00-0F	VGA - Palette Pixel Colors EGA - Dynamic Color Selection
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

TABLE 5-6 ATTRIBUTE CONTROLLER REGISTERS

NOTES

1. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the Address and Data Registers. Reading the Input Status Register 1 (Port 3?Ah) clears the flip-flop and selects the Address Register, which is read at address 3C1h and written at address 3C0h. Once the Address Register has been loaded with an index, the next write operation to 3C0h loads the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0h but does not toggle for reads from address 3C1h.
2. Attribute Register data is written at 3C0h and register data is read from address 3C1h.
3. Reserved bits should be set to zero.

5.8.1 Attribute Index Register, Read/Write Port = 3C0h

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits (7:6)

Reserved.

Bit 5 - Palette Address Source

0 = Disable internal color palette outputs and video outputs to allow CPU access to Color Palette Registers Port 3C0h, Index 00 - 0Fh.

1 = Enable internal color palette and normal video translation.

Bits (4:0) - Attribute Controller Index Register Address Bits

5.8.2 VGA - Palette Registers, Read Port = 3C1h, Write Port = 3C0h, Index 00-0Fh

These registers are locked if PR4(2) = 1.

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:6)

Reserved.

Bits (5:0) - Palette Pixel Colors

Bits 5 through 0 control VID5 through VID0 respectfully.

They are defined as follows:

0 = Current pixel color deselected.

1 = Enables the corresponding pixel color.

5.8.3 EGA - Dynamic Color Registers, Read Port = 3C1h, Write Port = 3C0h, Index 00-0Fh

These registers are locked if PR4(2) = 1.

Bits (7:6)

Reserved.

Bits (5:0) - Dynamic Color Selection

Bits 5 through 0 are defined as follows:

0 = Color deselected.

1 = Color selected.

Bit	Color	Pixel
5	Secondary Red	VID5
4	Secondary Green/Intensity	VID4
3	Secondary Blue/Mono	VID3
2	Red	VID2
1	Green	VID1
0	Blue	VID0

5.8.4 Attribute Mode Control Register, Read Port = 3C1h, Write Port = 3C0h, Index = 10h

BIT	FUNCTION
7	VID5 and VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Character Map Enable
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bits (7:4) - EGA -

Reserved.

Bit 7 - VGA - VID5, VID4 Select

0 = VID5 and VID4 palette register outputs are selected.

1 = Color Select Register Port 3C1h/3C0h, Index 14h, Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 - VGA - Pixel Width

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.

1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5 - VGA - PEL Panning Compatibility

Line Compare in the CRT Controller.

0 = A Line compare will have no effect on the PEL Panning Register.

1 = Allows a successful line compare to disable the PEL Panning Register and Bits 6 and 5 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4 - VGA - Character Map Enable

Bit 4 of this register is used with bits 5 and 2 of Video Select Register PR2 to select the Character Map from plane 2 or 3. Refer to Section 7.

Bit 3 - VGA/EGA - Background Intensity/Blink Selection

0 = Selects background intensity from the MSB of the attribute byte.

1 = Selects blink attribute.

Bit 2 - VGA/EGA - Enable Line Graphics Character Code

This bit should be set to zero for character fonts that do not utilize line graphics character codes.

0 = Forces the ninth dot to be the same color as the background in line graphics character codes.

1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 - VGA/EGA - Mono/Color Emulation

0 = Color display attributes.

1 = MDA attributes.

Bit 0 - VGA/EGA - Graphics/Alphanumeric Mode Enable

0 = Alphanumeric mode.

1 = Graphics mode.

5.8.5 Overscan Color Register, Read Port = 3C1h, Write Port = 3C0h, Index = 11h

This register is locked if PR4(2) = 1.

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BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bits (7:0) - VGA - Overscan/Border Color

These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

Bits (7:6) - EGA

Reserved.

Bits (5:0) - EGA - Overscan/Border Color

For a monochrome display, Bits 5:0 = 0.

For the border color, refer to Bits (5:0) in the Dynamic Color Selection in Section 5.6.3.

5.8.6 Color Plane Enable Register, Read Port = 3C1h, Write Port = 3C0h, Index = 12h

BIT	FUNCTION
7:6	Reserved
5:4	Video Status Multiplexer
3:0	Color Plane Enable

Bits (7:6) - VGA/EGA -

Reserved.

Bits (5:4) - VGA - Video Status Multiplexer

These bits select two out of eight color outputs which can be read by the Input Status Register 1 at Port 3?Ah, Bits 5 and 4. Refer to Section 5.2.3.

COLOR PLANE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bits (5:4) - EGA - Video Status Multiplexer

These bits select two out of six color outputs which can be read by the Input Status Register 1 at Port 3?Ah, Bits 5 and 4. Refer to Section 5.2.3.

COLOR PLANE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2 Red	VID0 Blue
0	1	VID5 SRed	VID4 SGreen
1	0	VID3 SBlue	VID1 Green
1	1	VID5 SRed	VID4 SGreen

Bits (3:0) - VGA/EGA - Color Plane Enable.

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.

1 = Enables the respective display memory color plane.

5.8.7 Horizontal Pel Panning Register, Read Port = 3C1h, Write Port = 3C0h, Index = 13h

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits (7:4) - VGA/EGA -

Reserved.

Bits (3:0) - Horizontal Pel Panning.

- VGA -

Horizontal Pel Panning is available in text or graphics modes. These bits select pixel shift to the left. For nine dots/character modes, up to eight pixels can be shifted. Likewise, for eight dots/character modes, up to seven pixels can be shifted. For 256 color, up to three position pixel shifts can occur. The following table defines the shift for different modes.

- EGA -

These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alphanumeric modes, (nine dots/ character) image can be shifted by nine pixels. For all other graphics or alphanumeric modes, a maximum left shift of eight pixels is permitted.

Register Value	9 Dots/ Character	8 Dots/ Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

TABLE 5-7 LEFT SHIFT PIXEL VALUE

5.8.8 Color Select Register, Read Port = 3C1h, Write Port = 3Ch, Index = 14h

BIT	FUNCTION
7:4	Reserved
3	S Color 7
2	S Color 6
1	S Color 5
0	S Color 4

Bits (7:4)

Reserved.

Bits (3:2) - Color Value MSB.

These are the two most significant bits of the eight-digit color value for the video DAC. They are normally used in all modes except 526 color graphics.

BITS		FUNCTION
3	2	
X	1	Set color bit VID6
1	X	Set color bit VID7

Bits (1:0) - Substituted Color Value Bits.

These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight-bit color value. They are selected by the Attribute Controller Mode Control Register at Port 3C0h, Index 10h.

5.9 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C33. However, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals required by the RAMDAC are provided by the WD90C33. Setting PR16 Bit 0 to 1 de-asserts $\overline{\text{WPLT}}$ disabling I/O writes to the RAMDAC. Normally, the $\overline{\text{WPLT}}$ and $\overline{\text{RPLT}}$ signals to the RAMDAC are generated when selected I/O ports are written to or read from as listed in Table 5-8.

DAC		FUNCTION
ADDRESS	OPERATION	
3C8	PEL Address Port (Write)	Read/Write Port
3C7	PEL Address Port (Read)	Read Only Port
3C7[1]	DAC State (Read Only)	If bits 1:0 are set to 1, DAC is in a read operation. If bits 1:0 are set to 0, DAC is in a write operation. Bits 7:2 are reserved.
3C6	PEL Mask (Read/Write)	Refer to **CAUTION.**
3C9	PEL Data Register (Read/Write)	Three successive read/write bytes

NOTE:

1. This port is internal to the WD90C33.

CAUTION

Do not write to this address with any application code. To do so changes the color look-up table.

TABLE 5-8 VIDEO RAMDAC PORTS

6.0 COMPATIBILITY REGISTERS

6.1 INTRODUCTION

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting register PR2(6) = 1.
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting register PR2(7) = 1.
3. The value indicated by "?" is controlled by Bit 0 of the Miscellaneous Output Register at Port 3CCh/3C2h and is programmed as shown below:
   0 = B in Monochrome Modes
   1 = D in Color Modes

REGISTERS	R/W	ADDRESS			
		MDA	CGA	AT&T	HERCULES
Mode Control	WO	3B8	3D8	3D8	3B8
Color Select	WO	---	3D9	3D9	---
Status	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	---
Clear Light Pen Latch	WO	3BB	3DB	3DB	---
AT&T/M24	WO	---	---	3DE	---
Hercules	WO	---	---	---	3BF
CRTC (6845 Mode)	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. Addresses are given in hexadecimal notation.
2. WO indicates Write Only, RO indicates Read Only, and RW indicates Read and Write.

TABLE 6-1 COMPATIBILITY REGISTER SUMMARY

6.2 HERCULES/MDA MODE CONTROL REGISTER, MDA OPERATION

WRITE ONLY PORT = 3B8h

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFh Enable
0	High Resolution Mode

Bit 7 - Select Display Memory Page Address In Hercules Mode

Reserved in MDA mode.

In Hercules Graphics mode, this bit selects the Display Memory Page if Bit 1 of this register is1 and Bit 0 in Port 3BFh is 0.

0 = Display memory page address starts at B000:0h.
1 = Display memory page address starts at B800:0h.

Bit 6

Reserved.

Bit 5 - Enable Blink

0 = Disable Blinking.
1 = Enable Blinking.

Bit 4

Reserved.

Bit 3 - Video Enable

0 = Video Disabled.
1 = Video Activated.

Bit 2

Reserved.

Bit 1 - Port 3BFh Enabled

0 = Prevents setting of Port 3BFh Bits 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh Bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0 - High Resolution Mode

Should be set to "1".

0 = High resolution disabled.
1 = High resolution is enabled.

6.3 HERCULES REGISTERS

The Hercules Mode Register is a two-bit write only register located at I/O port address 3BFh. It affects the device operation only in the 6845 mode. The Enable Mode Register located at address 3B8h overrides the write port 3BFh functions defined by its Bits 1 and 0.

6.3.1 Enable Mode Register, Port 3B8h

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7 - Select Display Memory Page Address In Graphics Mode

0 = Display memory page address starts at B000:0h.
1 = Display memory page address starts at B800:0h.

Bits (6:2, 0)

Not applicable in Hercules Mode.

Bit 1 - Port 3BFh, Bit 0 Override

0 = Prevents setting of Port 3BFh, Bit 0, thereby forcing the Alpha Mode operation.
1 = Allows the Port 3BFh, Bit 0 to switch for the Alpha or Graphics Mode selection.

6.3.2 Hercules Compatibility Register, Write Only Port = 3BFh

This register is locked if PR17(1) = 1

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1 - Upper Memory Page Address

In graphics mode, Bit 7 of the Enable Mode Control Register at Port 3B8h selects the displayed memory page address. When that bit is reset, bit 1 of this register prevents access to the second memory page, located at B800:0h for the 32 Kbyte memory space.

0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0 - Enable Graphics.

Bit 1 of Enable Mode Register at Port 3B8h may prevent setting this bit, thereby selecting Alpha Mode display.

0 = Alpha mode display.
1 = Graphics modes may be displayed.

6.4 CGA REGISTERS

6.4.1 Color CGA Operation Register, Write Only Port = 3D8h

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	(40 by 25) or (80 by 25) Alpha Mode

Bits (7:6)

Reserved.

Bit 5 - Enable Blink Function.

0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4 - B/W Graphics Mode Enable.

0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3 - Enable Video Signal.

0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2 - B/W or Color Display Mode.

0 = Color mode selected.
1 = B/W mode selected.

Bit 1 - Graphics or Alpha Mode Selection.

0 = Alpha mode selected.
1 = Graphics mode (320 by 200) selected.

Bit 0 - Alpha Mode Selection, (40 by 25) or (80 by 25)

0 = 40 by 25 alpha mode selected.
1 = 80 by 25 alpha mode selected.

6.4.2 CGA Color Select Register, Write Only Port = 3D9h

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	High Intensity Component
2	Red Component
1	Green Component
0	Blue Component

Bits (7:6)

Reserved.

Bit 5 - 320 by 200 Color Set Select for the CGA (two bits per pixel).

0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4 - Alternate Color Set Enable.

0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3 - High Intensity Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.

0 = No selection.
1 = Selects intensified border color.

320 by 200 Graphics Mode.

0 = No selection.
1 = Selects intensified background and border color.

640 by 200 Graphics Mode.

0 = No selection.
1 = Selects red foreground color.

Bit 2 - Red Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.
1 = Red component added to border color.

320 by 200 Graphics Mode.

0 = No component added.
1 = Red component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.
1 = Red component added to foreground color.

Bit 1 - Green Component.

Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.
1 = Green component added to border color.

320 by 200 Graphics Mode.

0 = No component added.
1 = Green component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.
1 = Green component added to foreground color.

Bit 0 - Blue Component.

Border color select in text modes and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.

0 = No component added.
1 = Blue component added to border color.

320 by 200 Graphics Mode.

0 = No component added.
1 = Blue component added to background and border color.

640 by 200 Graphics Mode.

0 = No component added.
1 = Blue component added to foreground color.

6.4.3 CRT Status Register, MDA Operation, Read Only Port = 3BAh

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7 - Vertical Retrace.

0 = Indicates that the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bits (6:4)

Reserved.

Bit 3 - B/W Video Status.

0 = B/W Video disabled.
1 = B/W Video enabled.

Bits (2:1)

Reserved.

Bit 0 - Display Enable.

0 = Display Enable is active.
1 = Indicates that the screen border or blanking is active, Display Enable is inactive.

6.4.4 CRT Status Register, CGA Operation, Read Only Port = 3DAh

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits (7:4)

Reserved.

Bit 3 - Vertical Retrace.

0 = Indicates that vertical retrace is inactive.
1 = Indicates that the raster is in vertical retrace mode.

Bit 2 - Light Pen Switch Status.

0 = Light pen switch closed.
1 = Light pen switch open

Bit 1 - Light Pen Latch.

0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0 - Display Enable.

0 = Display Enable is active.
1 = Indicates that the screen border or blanking is active, Display Enable is inactive.

6.4.5 AT&T/M24 Register, Write Only Port = 3DEh

This is a write only, eight-bit register located at address 3DEh. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting Bit 7 in register PR2

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5:4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bits (7, 5, 4, 1)

Reserved.

Bit 6 - White/Blue Underline.

Defines underline attribute according to the MDA display requirements.

0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit 3 - Page Select.

Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.

0 = Display memory address starts at B800:0h (16 Kbyte length).
1 = Display memory address starts at BC00:0h (16 Kbyte length).

Bit 2 - Character Set Select.

Selects between two character font planes.

0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 0 - M24 or Non-IBM Graphics Mode, 400-line mode.

A 400-line monitor is required for this mode.

0 = 200-line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400-line graphics.

7.0 PARADISE REGISTERS

7.1 INTRODUCTION

The WD90C33 has additional features that enhance the performance and functions of the basic VGA subsystem. To accomplish this, the WD90C33 architecture is optimized with additional I/O registers called Paradise registers.

The Paradise (PR) registers are located at I/O addresses that are not used in IBM compatible computers. All PR registers are read/write, and are set to 0 during power-on and reset unless otherwise noted.

NOTES

1. The designation 3?5h means that the register is mapped into either 3B5h in monochrome mode or 3D5h in color modes.
2. PR Register notation - XXX.YY where XXX is the data port address and YY is the register index. For example, address 3CF.0Fh indicates that the register base address is 3CFh, and 0Fh is the base register index.
3. Registers PR0 through PR4 and PR11 through PR1A are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101. A register remains unlocked until another value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17, load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFh. Setting PR4 Bit 1 to 1 does not read protect registers PR10 through PR17. PR21-PR23 and PR30-PR35 are R/W protected by PR20. PR20 must be loaded with 48h to make it possible to read or write to PR21-PR23 and PR30-PR35.

PARADISE REGISTERS		READ/ WRITE	ADDRESS	
NO.	NAME		MONO	COLOR
PR0(A)	Address Offset A	R/W	3CF.09	3CF.09
PR0(B)	Address Offset B (Alternate)	R/W	3CF.0A	3CF.0A
PR1	Memory Size	R/W	3CF.0B	3CF.0B
PR2	Video Select	R/W	3CF.0C	3CF.0C
PR3	CRT Control	R/W	3CF.0D	3CF.0D
PR4	Video Control	R/W	3CF.0E	3CF.0E
PR5	Unlock (PR0 through PR4) Status	R/W	3CF.0F	3CF.0F
PR10	Unlock (PR11 through PR17)	R/W	3B5.29	3B5.29
PR11	EGA Switches	R/W	3B5.2A	3B5.2A
PR12	Scratch Pad	R/W	3B5.2B	3B5.2B
PR13	Interlace H/2 Start	R/W	3B5.2C	3B5.2C
PR14	Interlace H/2 End	R/W	3B5.2D	3B5.2D
PR15	Miscellaneous Control 1	R/W	3B5.2E	3B5.2E
PR16	Miscellaneous Control 2	R/W	3B5.2F	3B5.2F
PR17	Miscellaneous Control 3	R/W	3B5.30	3B5.30
PR18	CRTC Vertical Timing Overflow	R/W	3B5.3E	3B5.3E
PR19	Signature Analyzer Control	R/W	3B5.3F	3B5.3F
---	Reserved 3X5.31h through 3X5.3Ch	R/W	3B5.31-3B5.3C	3B5.31-3B5.3C
PR20	Unlock Sequencer Extended Registers	W	3C5.06	3C5.06
PR21	Display Configuration and Scratch Pad	R/W	3C5.07	3C5.07
PR22	Scratch Pad	R/W	3C5.08	3C5.08
PR23	Scratch Pad	R/W	3C5.09	3C5.09
PR30	Memory Interface Write Buffer and FIFO Control	R/W	3C5.10	3C5.10
PR31	System Interface Control	R/W	3C5.11	3C5.11
PR32	Miscellaneous Control 4	R/W	3C5.12	3C5.12
PR33	DRAM Timing and Zero Wait State Control	R/W	3C5.13	3C5.13
PR34	Video Memory Mapping	R/W	3C5.14	3C5.14
PR35	Reserved	R/W	3C5.15	3C5.15

NOTES:

1. All PR register can be read/write protected. Refer to the particular PR register description for additional information.
2. A register description from locations such as 3CF.09h is the value read from, or written to, the location 3CFh, after a value of 09h has been written to the corresponding Index register 3CEh.

TABLE 7-1 PARADISE (PR) REGISTER SUMMARY

7.2 ADDRESS OFFSET REGISTERS PR0(A) AND PR0(B)

7.2.1 PR0(A) - Address Offset Register A, Read/Write Port = 3CFh, Index = 09h

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:0	Primary Address Offset Bits

7.2.2 PR0(B) - Address Offset Register B, Read/Write Port = 3CFh, Index = 0Ah

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C33 can control up to 1 Mbyte of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000h and ends at BFFFFh. To help VGA reach the memory beyond this range, the WD90C33 has two CPU address offset registers, PR0(A) and PR0(B) which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PR0(A) (Bits 7:0) or PR0(B) (Bits 7:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture. PR0(A) and PR0(B) will then provide 4 Kbyte segmentation of the display memory. (Increment PR0(A) or PR0(B) by one of its equivalents to jump from one 4 Kbyte segment to another 4 Kbyte segment of the display memory.).

PR0(A) and PR0(B) are all set to zero at power-on-reset. There are two ways to control whether PR0(A) or PR0(B) get added into CPU address.

- **Sequencer Extension Register 3C5h, Index = 11h, Bit 7 = 0**

When PR1-3 = 0, PR0(A) is always selected as the CPU address offset register.

When PR1-3 = 1 and the display memory is mapped into A000 - BFFFF (128 Kbytes), PR0(A) offset CPU address range is B0000 - BFFFF, the PR0(B) offset CPU address range is A0000 - AFFFF. (If CPU address bit A16 = 1, select PR0(A). Otherwise PR0(B) is selected.)

When PR1-3 = 1 and the display memory is mapped into A0000 - AFFFF (64 Kbytes) or B0000 - B7FFF or B800 - BFFFF (32 Kbytes), then PR0(B) offset CPU address range is A0000 - A7FFF or B0000 - B7FFF. PR0(A) offset CPU address range is A8000 - AFFFF or B8000 - BFFFF. (If CPU address bit A15 = 1, select PR0(A). Otherwise PR0(B) is selected.)

- **Sequencer Extension Register 3C5h, Index = 11h, Bit 7 = 1**

Both PR0(A) and PR0(B) are enabled. A CPU memory write selects PR0(B) as the offset register. Otherwise, PR0(A) is selected as the offset register.

7.3 PARADISE (PR) REGISTER DESCRIPTIONS

7.3.1 PR1 - Memory Size, Read/write Port = 3CFh, Index = 0Bh

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate Address Offset Register PR0(B)
2	16-Bit System Interface
1	16-bit BIOS ROM
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1(1:0) are latched internally at power on reset from the corresponding memory data bus pins MD10, MD0, using either pull-up or pull-down external resistors. Pull-up resistors on MD10, MD0 cause PR1(1:0) bits to be latched low.

Bits(7:6) - Memory Size

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits, in conjunction with PR0(A), PR0(B), PR16(1), select the way memory is mapped into the CPU address space. IF PR16(1) is set to 1, the memory mapping will be set identical to the IBM VGA, regardless of PR1(7), PR1(6).

Tables 7-2 through 7-5 list the applicable settings of PR1 bits 7 and 6 for different memory organizations.

Refer to notes following Table 7-5.

PR1(7) = 0, PR1(6) = 0						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA[5]	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)	MA(1)
A(0)	CA(0)	A(14) or[3] XRN(5)	CA(15) or[4] CA(13)	A(14)	CA(12)	MA(0)

TABLE 7-2 IBM COMPATIBLE VGA MEMORY ORGANIZATION, 256K BYTES TOTAL

Refer to notes following Table 7-5.

PR1(7) = 0, PR1(6) = 1						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA[5]	PA	PA	PA	PA	PA	MA(17)
0	0	0	0	0	0	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or[3] XRN(5)	CA(15)	A(14)	CA(12)	MA(0)

TABLE 7-3 IWD90C33 MEMORY ORGANIZATION, 256K BYTES

Refer to notes following Table 7-5.

PR1(7) = 1, PR1(6) = 0						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA[5]	PA	PA	PA	PA	PA	MA(17)
A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	MA(1)
A(0)	CA(0)	A(16) or[3] XRN(5)	CA(15)	A(16)	CA(14)	MA(0)

TABLE 7-4 IWD90C33 MEMORY ORGANIZATION, 512K BYTES, 128K BYTES PER PLANE

Refer to notes following Table 7-5.

PR1(7) = 1, PR1(6) = 1						
ADDRESS FROM CPU OR CRTC						ADDRESS TO VIDEO MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)	MA(17)
A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)	MA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	MA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	MA(14)
A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)	MA(13)
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	MA(2)
A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)	MA(1)
A(0)	CA(0)	A(16) or[3] XRN(5)	CA(15)	A(18)	CA(16)	MA(0)

TABLE 7-5 IWD90C33 MEMORY ORGANIZATION, 1M BYTES, 256K BYTES PER PLANE

NOTES FOR TABLES 7-2 THROUGH 7-5

1. A(19:0) are WD90C33 internally modified system addresses (CPU address plus offset address).
2. CA(17:0) are either CRT Character Address Counter bits or BITBLT generated counter bits
3. XRN(5) represents the inverted bit 5 or the Miscellaneous Output Register (3C2h). XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. For IBM compatible memory mapping,3C5.4, bit 1 = 1 selects XRN(5) to replace CPU address bits. In other memory mapping schemes, PR1(7,6) are not set to 00., 3C5.4, bit 1 = 1 and PR16 (2) = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as MA(0) if CRTC Mode Register 17, bit 5 = 1 1 in word addressing modes.
5. PA is the memory plane select bit when the DRAM interface is set for 16 bits.

   PA = 0 selects Plane 1, 0

   PA = 1 selects Plane 3, 2
6. MA(17:0) are divided into $\overline{RAS}$ and $\overline{CAS}$ addresses as follows:

MEMORY CONFIGURATION	MEMORY ADDRESS BITS	$\overline{RAS}$ OR $\overline{CAS}$ BITS
256K X 4 DRAM	MA(16)-MA(8)	$\overline{RAS}$(8)-$\overline{RAS}$(0)
	MA(17), MA(7)-MA(0)	$\overline{CAS}$(8)-$\overline{CAS}$(0)
256K X 16 DRAM	MA(16)-MA(8)	$\overline{RAS}$(8)-$\overline{RAS}$(0)
	MA(17), MA(7)-MA(0)	$\overline{CAS}$(8)-$\overline{CAS}$(0)
64K X 16 DRAM	MA(15)-MA(8)	$\overline{RAS}$(7)-$\overline{RAS}$(0)
	MA(7)-MA(0)	$\overline{CAS}$(7)-$\overline{CAS}$(0)
MA(17,16)=00 MA(17,16)=01 MA(17,16)=10 MA(17,16)=11	Select first 64K bank Select second 64K bank Select third 64K bank Select forth 64K bank	

Bits (5:4) - PR1(5,4) Memory Map Select.

BITS		FUNCTION
5	4	
0	0	IBM VGA mapping. CPU addresses are decoded from 0A0000h - 0BFFFFh from the lowest 1 Mbyte CPU address space (depending on 3CF.06 bits 2 and 3).
0	1	First 256 Kbyte in any 1 Mbyte CPU addressing space (X00000h - X3FFFFh)
1	0	First 512 Kbyte in any 1 Mbyte CPU addressing space (X00000h - X7FFFFh)
1	1	In any 1Mbyte CPU address space (X00000h - XFFFFFh)
NOTE: PR34(3C5.14) Bits (3:0) control which 1 Mbyte of CPU address space the WD90C33 maps (refer to Section 7.3.26).		

Bit 3 - Enable Alternate Address Offset Register PR0(B).

Bit 2 - Enable 16 bit system interface bus.

0 = System interface is 8 bits.
1 = System interface is 16 bits.

Bit 1 - 16-bit BIOS ROM.

0 = BIOS ROM access is 8 bits.
1 = BIOS ROM access is 16 bits.

A pull-down resistor on MD10 sets this bit to 1 after power-on reset.

Bit 0 - BIOS ROM Map Out.

0 = The BIOS ROM is available.
1 = The BIOS ROM is mapped out.

A pull-down resistor on MD0 sets this bit to 1 at power-on-reset.

7.3.2 PR2 - Video Select Register, Read/write Port = 3CFh, Index = 0Ch

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7 - Enable AT&T/M24 Register and Mode.

0 = Disable.
1 = Enable.

Bit 6 - 6845 Compatibility.

0 = VGA or EGA mode.
1 = Non-VGA (6845) mode.

Bit 5 - Character Map Select.

Bits 5 and 2 of this register, and Bit 4 of the Attribute byte, enables character maps from Planes 2 or 3 to be selected as shown in the following list:

PR15 (2)	3DE (2)	PR2 (5)	PR2 (2)	ATT (4)	PLANE SELECT
0	0	0	X	X	2
0	0	1	0	X	3
0	0	1	1	0	2
0	0	1	1	1	3

The above functions are overridden by setting PR15(2) or 3DE(2) to 1 (refer to Section 7.3.12).

Bits (4:3) - Character clock period control.

BITS		FUNCTION
4	3	
0	0	IBM VGA character clock (8 or 9 dots).
0	1	7 dots (used for 132-character text mode only).
1	0	9 dots.
1	1	6 dots if PR17(5) = 0 1 0 dots if PR17(5) = 1.1
NOTE: The character clock period control functions have no effect in graphics modes (Graphics Mode always uses eight dots).		

Bit 2 - Underline and character map select.

Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., programming 1 gives blue underline. It overrides the background color function of the Attribute Code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. Refer to the PR2, bit 5 description for additional information.

Bit 1 - Third Clock Select Line.

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) = 1. When CNF(3) = 0, it locks the internal video clock select multiplexer.

Bit 0 - Force VCLK.

This bit forces horizontal sync timing clock of the CRT Control Register to VCLK.

Uses VCLK when Sequencer Register 1, Bit 3, is set for VCLK/2. This is for compatibility modes that require locking the CRT Control Register timing parameters.

7.3.3 PR3 - CRT Lock Control Register, Read/write Port = 3CFh, Index= 0Dh

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7 - Lock VSYNC Polarity.

This bit locks VSYNC polarity as programmed at Port 3C2h, Bit 7.

Bit 6 - Lock HSYNC Polarity.

This bit locks HSYNC polarity as programmed at Port 3C2h, Bit 6.

Bit 5 - Lock Horizontal Timing.

This bit locks CRT Control Registers of Groups 4 and 0. It prevents applications software from unlocking Group 0 registers by setting 3?5.11 Bit 7 = 0.

Bit 4 - Bit 9 Control.

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(17).

Bit 3 - Bit 8 Control.

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA(16).

Bit 2 - Cursor Control.

Cursor Start, Stop, Preset Row Scan and Maximum Scan Line Address registers value multiplied by two.

Bit 1 - Lock Prevention.

When set to 1, this bit prevents attempts by applications software to lock registers of Group 1 by setting 3?5.11, Bit 7 = 1.

Bit 0 - Lock vertical timing.

When set to 1, this bit locks CRTC registers of Groups 2 and 3 and overrides attempts by applications software to unlock Group 2 registers by setting 3?5.11, Bit 7 = 0.

7.3.4 CRT Controller Register Locking

Register locking is controlled by four bits. They are PR3(5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register Bit 7 controlled by Index register 11). When 3?5.11 Bit 7 = 1, CRT controller registers (R0:7) are write-protected per VGA definition. For more information on the five groups and their locking schemes, refer to the following sections.

- **Group 0**

These registers are locked if PR3(5) = 1 **OR** 3?5.11(7) = 1.

ADDRESS 3?5h		
INDEX	BIT(S)	NAME
00	7:0	Horizontal Total Characters per Scan
01	7:0	Horizontal Display Enable End
02	7:0	Start Horizontal Blanking
03	7:0	End Horizontal Blanking
04	7:0	Start Horizontal Retrace
05	7:0	End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1) = 0 **AND** 3?5.11(7) = 1.

ADDRESS 3?5h		
INDEX	BIT(S)	NAME
07	6	Vertical Display Enable End Bit 9
7	1	Vertical Display Enable End Bit 8
3E	1	Vertical Display Enable End Bit 10

- **Group 2**

These registers are locked if PR3(0) = 1 **OR** 3?5.11(7) = 1.

ADDRESS 3?5h		
INDEX	BIT(S)	NAME
06	7:0	Vertical Total
07	7	Vertical Retrace Start Bit 9
07	5	Vertical Total Bit 9
07	3	Start Vertical Blank Bit 8
07	2	Vertical Retrace Start Bit 8
07	0	Vertical Total Bit 8
09	5	Start Vertical Blank Bit 9
3E	0	Vertical Total Bit 10
3E	2	Vertical Retrace Start Bit 10
3E	3	Start Vertical Blank Bit 10

- **Group 3**

These registers are locked if PR3(0) = 1.

ADDRESS 3?5h		
INDEX	BIT(S)	NAME
10	7:0	Vertical Retrace Start
11	3:0	Vertical Retrace End
15	7:0	Start Vertical Blanking
16	7:0	End Vertical Blanking

- **Group 4**

This register is locked if PR3(5) = 1.

CRTC Mode Control Register 17 (Bit 2) - Selects divide-by-two vertical timing.

7.3.5 PR4 - Video Control Register, Read/write Port = 3CFh, Index = 0Eh

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs, as well as video data for the RAMDAC and memory control outputs.

This register is locked if PR5(2:0) = 5.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$/Display Enable
6	PCLK = VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256-color Shift Register Control

Bit 7 - $\overline{\text{BLANK}}$/Display Enable.

This bit controls the output signal $\overline{\text{BLANK}}$. Normally in the VGA mode, $\overline{\text{BLANK}}$ is used by the external video DAC to generate blanking.

With this bit set to 1, the $\overline{\text{BLANK}}$ output supplies a display enable signal. A choice of two types of display enable timing can be selected and is determined by PR15(1).

Bit 6 - Select PCLK equal to VCLK.

0 = PCLK is either the inverted internal video dot clock or half the dot clock frequency, depending upon the video mode.

1 = PCLK is always the non-inverted VCLK input clock.

Bit 5 - Tristate Video Outputs.

With this bit set to 1, the video outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLANK}}$ are tristated.

Bit 4 - Tristate Memory Control Outputs.

With this bit set to 1, the memory address bus, MA(8:0), and all ten DRAM control signals are tristated.

Bit 3 - Override CGA Enable Video Bit.

Overrides the CGA Enable Video Bit 3 of mode register 3D8h, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2 - Lock Internal Palette and Overscan Registers.

With this bit set to 1, the internal palette and overscan registers are locked.

Bit 1 - EGA compatibility.

Setting the bit to 1 selects the EGA Compatible Mode. Reads are disabled to all registers that are write-only registers in the IBM EGA mode. Also, registers at 3COh/3C1h change to write-only mode. Reading of PR5 through PR0 is disabled. In VGA mode [PR(4) Bit 1 = 0], 3C0h register is read/write while 3C1h register is read only, per the Attribute Controller Register definitions.

Bit 0 - Extended Shift Register Control.

With this bit set to 1, the extended 256-color mode is selected (IBM Mode 13 is not included).

7.3.6 PR5 - General Purpose Status Bits, Read/write Port = 3CFh, Index = 0Fh

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR4-PR0 Unlock
1	PR4-PR0 Unlock
0	PR4-PR0 Unlock

Bits (7:3) - CNF Status

Bits (7:3) provide a means of reading the read only Configuration Register (CNF), Status Bits (8:4). CNF(8:4) are described in Section 9.

BIT	FUNCTION
7	CNF(7) General Purpose Status
6	CNF(6) General Purpose Status
5	CNF(5) General Purpose Status
4	CNF(4) General Purpose Status
3	CNF(8) Analog/TTL Display Status

Bits (2:0) - PR4-PR0.

These are read/write bits and are cleared by reset. They provide lock and unlock capability for PR registers PR4 through PR0. The PR4 through PR0 registers are unlocked when "X5h" is written to PR5. They remain unlocked until any other value is written to PR5.

Setting PR4 Bit 1 to 1, read protects registers PR5 through PR0.

PR5			PR4-PR0 STATUS
2	1	0	
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write enabled

7.3.7 PR10 - Unlock PR1A, PR(17:11) Read/write Port = 3?5h, Index = 29h

PR10 is a read/write register and is cleared by reset. PR10 controls access to registers PR1A and PR17 through PR11.

BIT	FUNCTION
7	PR1A and PR17 through PR11 Read Enable Bit 1
6:4	Reserved. Must be set to 0
3	PR1A and PR17 through PR11 Read Enable Bit 0
2:0	PR1A and PR17 through PR11 Write Enable

Bits 7, 3 - PR1A, PR(17:11) Read Enable.

Bits (7, 3) enable read operations for PR1A and PR17 through PR11.

BIT7	BIT3	PR1A and PR17 - PR11
0 X	X 1	Read protected. Read back data FFh
1	0	Read Enabled

Bits 6:4 - Reserved

Bits (6:4) are reserved, and must be set to 0.

Bits 2:0 - PR1A, PR(17:11) Write Enable.

Bits (2:0) enable write operations for PR1A and PR17 through PR11.

PR10			PR1A and PR17 - PR11
2	1	0	
0	X	X	Write protected
X	1	X	
X	X	0	
1	0	1	Write enabled

7.3.8 PR11 - EGA Switches, Read/write Port = 3?5h, Index = 2Ah

The EGA switch configuration details are stored in register PR11.

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7	EGASW4/General Purpose
6	EGASW3/General Purpose
5	EGASW2/General Purpose
4	EGASW1/General Purpose
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4) - EGA Configuration Switches W4 through SW1.

These read/write bits from corresponding memory data bus pins MD(15:12) are latched internally at power-on-reset with either pull-up or pull-down external resistors. Pulling-up MD(15:12) causes PR11(7:4) to be latched high. These bits can be read from Bit 4 of the Input Status Register at Port 3C2h if the EGA compatibility bit PR4(1) = 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register at Port 3C2h, as follows.

WRITE 3C2h		READ 3C2h
Bit 3	Bit 2	Bit 4
0	0	PR11(7) = EGA SW4
0	1	PR11(6) = EGA SW3
1	0	PR11(5) = EGA SW2
1	1	PR11(4) = EGA SW1

These bits may be used as general purpose scratch bits.

Bit 3 - Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

This is a read/write bit and is set to zero at power-on-reset.

Bit 2 - Lock Clock Select.

This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

This is a read/write bit and is set to zero at power-on-reset.

Bit 1 - Lock Graphics Controller/Sequencer Screen Control.

Setting this bit to 1 prevents modification of the following bits in the Graphics Controller as well as the Sequencer:

Graphics Controller3CF.05 bits (6:5) Sequencer 3C5.01 bits (5:2) Sequencer3C5.03 bits (5:0)

Although the internal functions selected by the graphics controller and sequencer bits are locked by setting PR11 Bit 1 to 1, they appear unlocked to the system processor during read operation.

This is a read/write bit and is set to zero at power-on-reset.

Bit 0 - Lock 8/9 Dots.

Setting this bit to 1 prevents modification of the Clocking Mode Sequencer Register 3C5.01, Bit 0.

With this bit set to 1, eight and nine dot wide character timing is locked. Register 3C5h.01 Bit 0 still appears unlocked to the system processor during read operations.

This is a read/write bit and is set to zero at power-on-reset.

7.3.9 PR12 - Scratch Pad, Read/write Port = 3?5h, Index = 2Bh

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

7.3.10 PR13 - Interlace H/2 Start, Read/write Port = 3?5h, Index = 2Ch

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up.

In interlaced operations, this register defines the starting horizontal character count at which vertical timing is clocked on alternate fields. Interlaced operation is enabled by setting PR14(5) to 1.

All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE

In the preceding expression, HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

7.3.11 PR14 - Interlace H/2 End, Read/write Port = 3?5h, Index = 2Dh

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bits 7 through 5 are set to 0 by reset.

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up.

Bit 7 - Enable IRQ.

This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used and this bit should be set to 0. This bit should not be set to 1 in MicroChannel operation.

0 = IRQ disabled. Used in VGA operations with an AT bus and MicroChannel operations.
1 = IRQ enabled.

Bit 6 - Vertical Double Scan.

This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTCs Vertical Displayed Line Counter and Row Scan Counter to be clocked by divide-by-two horizontal timing, if vertical sync polarity (3C2h Bit 7 = 0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: N=2(n+1).

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5 - Interlaced Mode.

The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000. Line compare and double scan are not supported.

0 = Interlaced Mode not enabled.
1 = Interlaced Mode is enabled.

Bits (4:0) - Interlaced H/2 End Bits (4:0).

Add the contents of the Interlaced H/2 Start Register PR13 to the horizontal sync width (same as defined by 3X5.04,05). Program the five LSBs of the sum into these bit locations.

7.3.12 PR15 - Miscellaneous Control 1, Read/write Port = 3?5h, Index = 2Eh

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7	Read 46E8h Enable
6	High VCLK
5	VCLK1 and VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7- Enable Reading Port 46E8h.

This bit is functional only if AT BUS architecture [CNF(2)=1] is selected.

With this bit set to 1, I/O Port 46E8h may be read, regardless of the state of its own Bits 4 and 3 and of Port 102h, Bit 0 (sleep bit). Only Bits(4:0) of Port 46E8h are readable, Bits (7:5) are 0.

Bit 6 - High VCLK.

This bit should be set to 1 when (MCLK in MHz / VCLK in MHz) equals 1.5, or in an extended 256-color mode.

With this bit set to 1, memory timing is adjusted to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency.

Bit 5 - Latched VCLK1 and VCLK2.

This bit is used only if CNF(3) = 1, which configures the VCLK1 and VCLK2 pins as outputs.

With this bit set to 1, outputs VCLK2 and VCLK1 are equal to Bits 3 and 2 of I/O write register (Miscellaneous Output Register) at Port 3C2h, respectively.

Bit 4 - Select MCLK as Video Clock.

With this bit set to 1, MCLK input is selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3 - Interlaced Compatibility.

This bit should be set to 1 only if interlaced mode is selected (see PR14) and exact timing emulation of the IBM 8514/A's interlaced video timing is required.

With this bit set to 1, vertical sync is generated from the trailing edge of non-skewed horizontal sync instead of the leading edge, as generated for VGA timing. Also, two VCLK delays are removed from the default VGA video dot path delay chain.

Bit 2 - Select Page Mode Addressing.

Graphics Modes automatically use Page Mode addressing.

Alpha modes require this bit to be set to 1 for screen refresh memory read cycles to use Page Mode addressing. Setting this bit to 1 in any Alpha Mode overrides the character map select functions of PR2(2) and PR2(5).

Page Mode addressing requires less time than $\overline{\text{RAS}}$-$\overline{\text{CAS}}$ addressing, therefore, selecting Page Mode addressing increases the bandwidth for the CPU to access video memory by 30-40%.

PR15(2) should be set to 1 if 132 Character Mode timing is selected (see description of PR2).

When PR15(2) is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight 8K memory segments containing a pair of maps in Plane 3 or Plane 2 is addressed by Bits(2:0) of this register while the map selection is determined by Bits(4:3). A pair of adjacent 8K character maps in Planes 3 and 2, (adjacent in the sense that they have the same addressing) may be selected by Bit 3 of the Attribute Code.

The Character Attribute Bit 3 (refer to Section 5.6.4), in conjunction with Bits 4 and 3 of the Character Map Select Register (3C5.03), determine a character map from either Plane 3 or Plane 2 as shown by the following table.

The following Character Map Select functions override the functions of PR2(5) and PR2(2).

PR15 (2)	3C5.03 (4)	3C5.03 (3)	ATT (3)	PLANE SELECT
1	0	0	X	2
1	0	1	0	3
1	0	1	1	2
1	1	0	0	2
1	1	0	1	3
1	1	1	X	3

PR15, bit 2 must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1, internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1 - Display Enable Timing Select.

This bit is used to select between two types of display enable timings available at output pin $\overline{\text{BLANK}}$ if PR4(7) = 1. If PR4(7) = 0, this bit has no effect.

0 = $\overline{\text{BLANK}}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{\text{BLANK}}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0 - Disable Border.

Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

7.3.13 PR16 - Miscellaneous Control 2, Read/write Port = 3?5h, Index = 2Fh

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7	External Register 46E8h Lock
6	CRT Control Address Count Width Bit 1
5	CRT Control Address Count Width Bit 0
4	CRT Control Address Counter Offset Bit 1
3	CRT Control Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7 - Lock External 46E8h Register.

Setting this bit to 1 causes EBROM output to be forced high (Inactive) during I/O writes to Port 46E8h.

Bits (6:5) - CRT Control Address Counter Width.

Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT Controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory, in which CRT Controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations.

BITS		COUNTER WIDTH
6	5	
0	0	256KBytes
0	1	128K Bytes
1	X	64K Bytes

Bits (4:3) - CRT Control Address Counter Offset.

Bits 4 and 3 are summed with the CRT Controller's Address Counter Bits CA(17) and CA(16), respectively, and the two-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2 - Enable Page Bit for Odd/Even.

This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the Page Bit for Odd/Even [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size Bits PR1(7:6).

Bit 1 - VGA Memory Mapping.

Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size Bits PR1(7:6).

Bit 0 - Lock RAMDAC Write Strobe (3C6h - 3C9h).

0 = Normal operation.

1 = Output $\overline{\text{WPLT}}$ to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C33, is also protected from the modification but may still be read at the Port 3C7h.

7.3.14 PR17 - Miscellaneous Control 3, Read/write Port = 3?5h, Index = 30h

This register is locked if PR10(2:0) is not set to 5.

BIT	FUNCTION
7:6	Reserved
5	Character Clock Period Select
4	PCLK = VCLK/2
3	Map Out 4K Of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map Out 2K Of BIOS ROM

Bits (7:6)

Reserved.

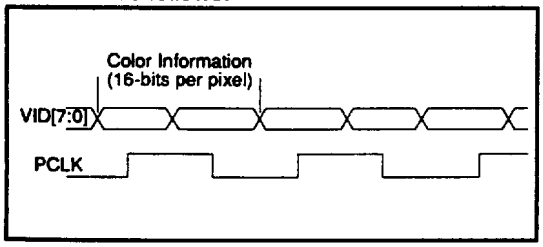
Bit 5: - Character Clock Period Select.

To enable PR17 Bit 5, PR2 (3CF.0C) Bits 4:3 must equal 11. When Bit 5 is not enabled, it has no effect.

0 = Six-dot font is selected.
1 = Ten-dot font is selected.

Bit 4 - PCLK = VCLK/$_2$.

With this bit set to 1 it forces PCLK = VCLK/$_2$. This control is useful for interface with high color RAMDAC as follows:



Bit (3) - Map Out 4K of BIOS ROM.

With this bit set to 1, it disables access of the BIOS ROM in the system address range C600:0h through C6FF:Fh. Power-on-reset sets this bit to 0.

Bit 2 - Enable 64K BIOS ROM.

With this bit set to 1, it enables access of the BIOS ROM in the system address range C000:0h through CFFF:Fh. Power-on-reset sets this bit to 0.

Bit 1 - Hercules Compatibility.

With this bit set to 1, it locks Hercules compatibility register (I/O Port 3BFh). Power-on-reset sets this bit to 0.

Bit 0 - Map Out 2K of BIOS ROM.

With this bit set to 1, it disables access of the BIOS ROM in the system address range C600:0h through C67F:Fh. Power-on-reset sets this bit to 0.

7.3.15 PR18 - CRTC Vertical Timing Overflow, Read/write Port = 3?5h, Index = 3Eh

These register bits are combined with other vertical timing overflow bits in CRT Control, constitutes an 11-bit vertical timing control. These bits are set to zero at power-on-reset.

BIT	FUNCTION
7	Enable 2 Mbyte Memory for 1280x1024 mode, 256 colors
6	CRTC Start Memory Address High, Bit 10 (3?5.0Ch)
5	Horizontal Total Bit 8 (Supports 24-bit color mode)
4	Line Compare Bit 10
3[1]	Start Vertical Blank Bit 10
2[1]	Start Vertical Retrace Bit 10
1[2]	Vertical Display Enable End Bit 10
0	Vertical Total Bit 10

NOTES:

1. This bit is locked if PR3(0) = 1 OR the 3?5 Index 11 Bit 7 = 1.
2. This bit is locked if PR3(1) = 0 AND the 3?5 Index 11 Bit 7 = 1.

Bits 7 - Enable 2 Mbyte Memory

This bit must be set to 1 for support of 1280x1024x256 color interlaced mode.

0 = Disable 2 Mbyte DRAM interface
1 = Enable 2 Mbyte DRAM interface

Bit 6 - CRTC Start Memory Address High, Bit 10

This bit corresponds to character address CA8. CRTC Start Memory Address High bits 9:8 are contained in PR3 (3CF.0Dh) register, bits 3 and 4, respectively. Bits 7:0 are located at address 3?5.0Ch

Bit 5 - Horizontal Total Bit 8

This bit provides bit 8 of the Horizontal Total Register located at 3?5.00h.

7.3.16 PR19 - Video Signature Analyzer Control, Read/write Port = 3?5h, Index = 3Fh

BIT	FUNCTION
7:4	Reserved
3	Signature Read Enable
2	Enable Video Input
1	Preload Control
0	Enable/Status Bits

Bits 7:4

Reserved

Bit 3 - Signature Read Enable.

When this bit is set to 1, signature analyzer results can be read from 3?5h, Index 20 and 21.

Bit 2 - Enable Video Input.

This bit is used for self-test.

0 = Enable video input for signature analyzer.
1 = Self-testing. The video input to the signature analyzer is disabled.

Bit 1 - Preload Control.

0 = The Signature Analyzer Result Register (3?5, Index 20 and 21) is preloaded with 0001h.
1 = Normal operation.

Bit 0 - Enable/Status Bits.

Writing to this bit:

Setting this bit to 1 enables the signature analyzer to collect signature on video input.

Reading this bit:

Indicates the status of the signature analyzer collecting the signature on video input.

0 = Finished (or not enabled).
1 = Busy.

7.3.17 PR1A - Shadow Register Control, Read/write Port = 3?5h, Index = 3Dh

This register is locked if PR10(2:0) is not set to 5.

Bits (7:4)

Reserved.

Bits 3 - I/O Read Select.

0 = Select actual CRT Control registers for read.
1 = Select shadow CRT Control registers for read.

Bits (2:0) - Shadow Lock.

When bits 2:0 are set to 101, all the shadowed register bits are locked. This lock overrides any other locks. Refer to the Shadow Register description for details.

7.3.18 PR20 - Unlock Sequencer Extended Registers, Read/write Port 3C5h, Index = 6h

This register is locked at power-on or reset.

A value of X1X01XXX must be written to this register to allow Read or Write operations of the Sequencer Extended Registers. When the extended registers are locked, the Sequencer Index is read as three bits. When unlocked, the Sequencer Index reads as six bits.

7.3.19 PR21 - Display Configuration Status And Scratch Pad Bits Register, Read Only Port 3C5h, Index = 07h

This register is locked at power-on or reset.

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

This register provides a convenient location for determining the current state of the VGA configuration. This information is required for many BIOS calls.

BIT	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2 Bit 0, Read/Write Bit
2	Status of PR2 Bit 6, Read/Write Bit
1	Status of PR4 Bit 1, Read/Write Bit
0	Status of PR5 Bit 3, Read/Write Bit

Bits (7:4) - Scratch Pad Bits.

These read/write bits serve as a scratch pad for any BIOS status data that may need to be saved. These bits are preset to 1111 at reset.

Bit 3 - Status of 3C2h Bit 0.

This read only bit represents the setting of the I/O address select bit in the Miscellaneous Output Register.

0 = MDA (3Bx) addresses have been selected.
1 = CGA (3Dx) addresses have been selected.

Bit 2 - Status of PR2 Bit 6.

This read only bit represents the setting of the VGA/6845 select bit in PR2 (3CFh Index Ch).

0 = VGA or EGA compatibility has been selected.
1 = 6845 compatibility has been selected.

Bit 1 - Status of PR4 Bit 1.

This read only bit represents the setting of the VGA/EGA select bit in PR4 (3CFh Index Eh).

0 = VGA was selected.
1 = EGA compatibility has been selected.

Bit 0 - Status of PR5 Bit 3.

This read only bit represents the setting of the Analog/TTL status bit in PR5 (3CFh Index Fh).

0 = An analog monitor was selected.
1 = A TTL-type monitor was selected.

7.3.20 PR22 - Scratch Pad Register, Read/write Port = 3C5h, Index = 8h

Bits (7:0)

Scratch pad bits.

7.3.21 PR23 - Scratch Pad Register, Read/write Port = 3C5h, Index = 9h

Bits (7:0)

Scratch pad bits.

7.3.22 PR30 - Memory Interface, Write Buffer And FIFO Control Register, Read/write Port = 3C5h, Index 10h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

This register controls display memory data width and its bandwidth. All bits are reset to zero at power-on-reset.

BIT	FUNCTION
7:6	Write Buffer Control
5	32-bit or 16-bit Memory Data Path
4	Disable 16-bit CPU Interface for Unchain Mode
3	Twelve-level FIFO
2	Four or Eight-level FIFO
1:0	Display FIFO control

Bits (7:6) - Write Buffer Control.

Bits 7 and 6 determine the depth of the write buffer.

PR31 Bit 2 must be set to 1 for these two bits to have any effect.

BITS		WRITE BUFFER LEVEL
7	6	
0	0	One level deep.
0	1	Two levels deep.
1	0	Three levels deep.
1	1	Four levels deep.

Bit 5 - Memory Data Path.

0 = The display memory data path is 32-bits wide.
1 = The display memory data path is 16-bits wide.

Bit 4 - Disable Unchained Mode.

0 = Normal conditions.
1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3 - Twelve-Level FIFO.

0 = The FIFO is four or eight levels deep, depending on Bit 2 of this register.
1 = The FIFO is 12 levels deep, regardless of Bit 2.

Bit 2 - Four or Eight-Level FIFO.

0 = FIFO set to eight levels deep.
1 = FIFO set to four levels deep.

Bits (1:0) - Display FIFO Control.

These two bits determine when the display FIFO will make a memory bus request. The bits can be used to reduce DRAM page breaks and to optimize memory bus arbitration. When the display FIFO makes a memory bus request, the memory controller stops its current operation and starts to serve the display FIFOs request. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

Depending on whether the FIFO level is two, four, or 12 levels deep (refer to bits 3:2), the display FIFO requests a memory cycle according to how bits 1:0 are set.

BITS		FIFO IS 2 OR 4 LEVELS DEEP	FIFO IS 12 LEVELS DEEP
1	0		
0	0	One level empty	Two levels empty
0	1	Two levels empty	Four levels empty
1	0	Three levels empty	Six levels empty
1	1	Four levels empty	Eight levels empty

7.3.23 PR31 - System Interface Control, Read/write Port = 3C5h, Index = 11h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

At power-on or reset this register is set to 00.

This register provides the control bits for the system interface. This register should be set during the post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 is used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Reserved
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable Write Buffer
1	Enable 16-bit I/O Attribute Controller
0	Enable 16-bit I/O Operation on CRTC, Sequencer and Graphics Controller

Bit 7 - Read/Write Offset Enable.

0 = Normal (Refer to PR0A and PR0B definitions).
1 = During read cycles, the offset register PR0-A, is added to the CPU address. During write cycles PR0-B is added to the CPU address.

Bit 6 - Turbo Mode for Blanked Lines.

0 = Normal.
1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.

Bit 5 - Reserved

Reserved

Bits (4:3) - CPU Read IOCHRDY Release Controls 1,0.

These two bits select the IOCHRDY timing for CPU reads. To improve performance of systems with a slower bus clock, IOCHRDY may be asserted earlier. Data will be ready following IOCHRDY no sooner than the time selected by bits (4:3).

BITS		FUNCTION
4	3	
0	0	40 ns. (Default after Power-on-reset)
0	1	40 ns. plus 1 MCLK.
1	0	40 ns. plus 2 MCLKs.
1	1	40 ns. minus 1 MCLK.

NOTE:

For 10 MHz or slower systems, the 01 setting is recommended.

For 12 MHz or faster systems, the 11 setting is recommended.

Bit 2 - Enable Write Buffer.

0 = Write buffer disabled.

1 =Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.

Bit 1 - Enable 16-bit I/O Attribute Controller.

If Bit 1 and Bit 0 are both set to 1, the Attribute Controller (3C0h/3C1h) is configured for 16-bit access. The index is at 3C0h while the data is at 3C1h and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for eight-bit cycles. $\overline{IOCS16}$ is asserted for all cycles to 3C0h or 3C1h.

Bit 0 - Enable 16-bit I/O Operations.

0 = The VGA I/O is eight-bits.

1 = Enables 16-bit access to the CRTC (3?4h/3?5h), Sequencer (3C4h/3C5h) and Graphics Controller (3CEh/3CFh). The output $\overline{IOCS16}$ will be active for any I/O read or write to these addresses.

7.3.24 PR32 - Miscellaneous Control 4, Read/write Port = 3C5h, Index = 12h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

At power-on or reset this register is set to 00.

This register provides control for several different features. Some of these features help to support Genlock of the WD90C33 to another display controller for overlay.

BIT	FUNCTION
7	Enable External Sync Mode
6	Disable Cursor Blink
5	USR1 Function Select
4	USR1 Control
3	USR0 Function Select
2	USR0 Control
1	Allow Read Back in Backward compatible Modes
0	Force Standard CPU Addressing in 132-column Mode

Bit 7 - Enable External Sync Mode.

0 = Normal operation mode.

1 = $\overline{EXVID}$ is configured to input external Horizontal Sync and $\overline{EXPCLK}$ inputs external Vertical Sync. The external $\overline{HSYNC}$ signal also synchronizes the character clock timing. In this configuration, $\overline{EXVID}$ and $\overline{EXPCLK}$ do not control the VID7:0 and PCLK output buffers, but they are used to genlock the WD90C33 to another display controller.

Bit 6 - Disable Cursor Blink.

0 = Blink enabled.

1 = The text cursor blink is disabled and the cursor remains on. This option can be used when cursor blink is not desired.

Bit 5 - USR1 Function Select.

0 = The USR1 output represents the state of Bit 4. This can be used to control new features added by the system board designer.

1 = Reserved.

Bit 4 - USR1 Control.

Controls the USR1 output when selected by Bit 5.

Bit 3 - USR0 Function Select.

0 = The USR0 output represents the state of Bit 2. This can be used to control new features added by the system board designer.

1 = Reserved.

Bit 2 - USR0 Control.

Controls the USR0 output when selected by Bit 3.

Bit 1 - Read in Backward Compatible Modes.

0 = Registers that are not normally readable in backward compatibility modes may not be read.

1 = Registers that are not normally readable in backward compatibility modes may be read.

This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0 - 132-Column Mode.

When this bit is set to 1, the special CPU address mapping for page mode font access in 132-column text is set for standard mapping without disturbing the display. This is used only for special virtual VGA applications.

7.3.25 PR33 - DRAM Timing And Zero Wait State Control, Read/write Port = 3C5h, Index = 13h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

BITS	FUNCTION
7:6	$\overline{0WS}$ Control
5	Memory Refresh Cycle
4	Memory Read/Write Cycle
3:0	Defined for WD90C31

Bits (7:6) - $\overline{0WS}$ Control.

These two bits control the operation of the $\overline{0WS}$ output pin. In non-Local bus mode, $\overline{0WS}$ is disabled if PR31 bit 2 = 0 (Write Buffer is off).

BITS		FUNCTION
7	6	
0	0	$\overline{0WS}$ = 0 if the internal write buffer is ready.
0	1	$\overline{0WS}$ = 0 if the internal write buffer is ready and the memory address is decoded.
1	0	$\overline{0WS}$ = 0 if the internal write buffer is ready and the memory address is decoded and MWR = 0.
1	1	$\overline{0WS}$ = 0 if write buffer is ready, memory address is decoded, and $\overline{MWR}$ is set to 0, OR MRD is set to 0, the HBLT destination is the host, and the BITBLT data path FIFO is not empty.

Bit 5 - Memory Refresh Cycle T-52-33-45

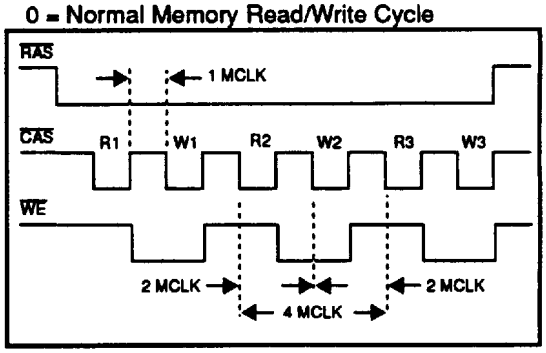
0 = Normal Memory Refresh

1 = Suppress RAS strobe during memory refresh

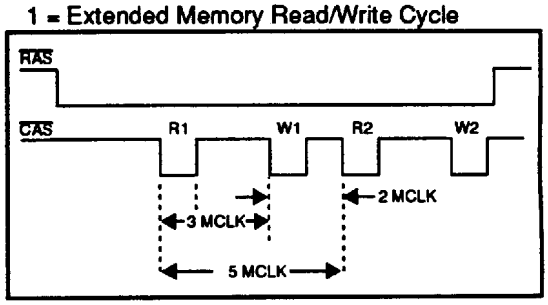
Bits 4 - Memory Read/Write Cycle Control

This bit controls $\overline{CAS}$ cycle duration for read/write cycle.

0 = Normal Memory Read/Write Cycle



1 = Extended Memory Read/Write Cycle



Bit 3 - $\overline{CAS}$ Timing

0 = $\overline{CAS}$ cycle is 2 MCLKs
$\overline{CAS}$ low is 1 MCLK + (1.5 ~ 3.0 ns)
$\overline{CAS}$ high is 1 MCLK - (1.5 ~ 3.0 ns)

1 = $\overline{CAS}$ cycle is 2 MCLKs
$\overline{CAS}$ low is 1 MCLK + (8 ~ 14 ns)
$\overline{CAS}$ high is 1 MCLK - (8 ~ 4 ns)

Bit 2 - $\overline{CAS}$ After $\overline{RAS}$ Timing

0 = $\overline{CAS}$ cycle starts 2.5 MCLKs after $\overline{RAS}$ low.

1 = $\overline{CAS}$ cycle starts 1.5 MCLKs after $\overline{RAS}$ low.

Bits (1:0) - $\overline{RAS}$ Precharge.

These two bits control $\overline{RAS}$ precharge. Refer to DRAM timing adjustments in Section18.

BITS		FUNCTION
1	0	
0	0	$\overline{RAS}$ high is 2-1/2 MCLKs plus a 4:7 ns delay.
0	1	$\overline{RAS}$ high is 3 MCLKs wide.
1	0	$\overline{RAS}$ high is 2 MCLKs wide.
1	1	$\overline{RAS}$ high is 2-1/2 MCLKs.

7.3.26 PR34 - Video Memory Mapping, Read/write Port = 3C5h, Index = 14h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

Bits (7:4)

Bits 7:6 are reserved, and bits 5:4 are reserved for driver usage.

Bits (3:0) - Video Memory Mapping.

These four bits are compared with the CPU address A(23:20) as part of the video memory address decoding. This allows the VGA to be mapped into any 1 Mbyte CPU memory space.

This register does not affect the $\overline{EBROM}$ and $\overline{ROM16}$ decoding. $\overline{EBROM}$ and $\overline{ROM16}$ are still decoded at A(23:20) = 0h. Used with the correct setting of PR1, Bits 5 and 4, this register supports virtual VGA applications.

These four bits are set to 0 at power-on-reset.

7.3.27 PR35 - Reserved, Read/write Port = 3C5h, Index = 15h

This register is locked if PR20 bits 6, 4, 3 are not set to 101b.

Bits (7:0)

Reserved.

8.0 INTERNAL I/O PORTS

8.1 INTRODUCTION

The following registers function as internal I/O ports.

8.1.1 AT Mode Setup, Enable, Write Only Port 46E8h (Also At Ports 56E8h, 66E8h, 76E8h)

BIT	FUNCTION
7:5	Reserved
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bits (7:5)

Unused.

Bit 4 - Setup.

This bit puts the WD90C33 into Setup mode where only I/O Port 102h is accessible.

Bit 3 - Enable I/O and Memory Accesses.

This bit enables I/O and memory accesses.

Bits (2:0) - BIOS ROM Page Select.

On I/O accesses to Port 46E8h, EBROM becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits and define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM therefore, appears to consist of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using these bits (D2:D0). The WD90C33 also provides Port 3C3h as an alternative to Port 46E8h. If a pull-down resistor is connected to MD9 during power-on-reset [CNF(9) = 0], Port 3C3h is decoded instead of Port 46E8h to support the same functions as described above. Otherwise, Port 46E8h is selected and decoded.

8.1.2 Setup Mode Video Enable (AT and MicroChannel Modes) Read/write Port = 102h (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7:1	Reserved
0	Wakeup VGA

Bits (7:1)

Unused.

Bit 0 - Wakeup VGA.

Wakeup VGA for I/O and Memory Accesses. Only the lower three address bits are decoded for this port and the WD90C33 must be in Setup mode. VGA Enable Sleep bit or Programmable Option Select (POS) Register 102h Bit 0 is used to awaken the WD90C33 after power on in the MCA and AT mode. To enter the Setup mode in AT bus applications, Bit 4 of the partially decoded internal I/O Port 46E8h is set to 1 before accessing the I/O Port 102h. In MCA mode, the WD90C33 is in Setup mode and Port 102h can be accessed when the VGA setup ($\overline{EIO}$) signal pin is active low.

9.0 CONFIGURATION REGISTER BITS CNF(31:0)

9.1 INTRODUCTION

Memory Data Lines MD[31:0] are used to set Configuration Registers CNF[31:0] during power-on and Reset (RST) operations. The Configuration Registers are set by means of pullup or pulldown resistors. The resistors cause bits to be set in internal registers, which then establish the operating configuration during power-on and Reset. Some configuration bits are contained in non-writable registers while others can be modified after start up. The non-writable bits set features such as "bus type" that are not modified after start up. Configuration bits CNF[15:12], CNF10, and CNF0 can be changed by software after start up. The MD[18:0] lines are all internally pulled up by 50 Kohm resistors.

Configuration Register bits [31:20] are used for Local bus mode operation only and have no effect unless Local bus mode is selected.

Table 9-1 lists the Configuration Register (CNF) bits and their functions, and also provides a typical value (TYP column) that each bit may be set to for normal operation.

CNF	TYP	FUNCTION
[31:30]	11	Setup Local Bus Interface Control Register 2DF1h[5:4] for Power-on and Reset
[29:28]	11	Setup Local Bus Interface Control Register 2DF1h[3:2] for Power-on and Reset
[27:26]	11	Setup Local Bus Interface Control Register 2DF1h[1:0] for Power-on and Reset
[25:22]	1111	Setup Local Bus Interface Control Register 2DF0h[7:4] for Power-on and Reset
21	1	Select 386/486 CPU Bus Interface
20	1	Local Bus VGA Cycle Termination Control
19	1	Reserved
18	1	Enable ROM16 as EXBLANK Input
17	1	Select 4 $\overline{CAS}$, 1 $\overline{WE}$ for Memory Interface
16	1	64K by 16 or 256K by 4 DRAM Select
15:12	0001	EGA Switches
11	1	Select Local Bus Interface Mode
10	0	Disable $\overline{ROM16}$ Address Decode
9	1	46E8h/3C3h Select
8	0	Display Status
7:4	0000	General Purpose Status
3	1	Video Clock Source Control
2	1	AT/MCA Bus Select
1	0	ROM Configuration
0	0	BIOS ROM Mapping

NOTE: The TYP column lists typical values as follows:

A 0 indicates that an external pulldown resister sets the bit to 0 during power-on and reset.

A 1 indicates that an external pullup resister sets the bit to 1 during power-on and reset.

TABLE 9-1 CONFIGURATION REGISTER BITS

NOTE

Configuration Register bits [31:20] have no effect unless Local bus mode is selected.

CNF[31:19] - Local Bus Interface Registers

Refer to Section 10 for additional information on the Local Bus.

CNF18 - ROM16 As EXBLANK input.

0 = A 4.7K pull-down resistor on Pin MD18. $\overline{ROM16}$ is configured as $\overline{EXBLANK}$ input.

1 = No pull-down resistor, the internal pull-up sets CNF18 to 1. Normal $\overline{ROM16}$ operation. $\overline{ROM16}$ is an output.

CNF17 - Select CAS and WE for Memory Interface

0 = $\overline{CAS}$ becomes $\overline{CAS0}$
$\overline{WE1}$ becomes $\overline{CAS1}$
$\overline{WE2}$ becomes $\overline{CAS2}$
$\overline{WE3}$ becomes $\overline{CAS3}$
$\overline{WE0}$ becomes $\overline{WE}$

1 = Use $\overline{CAS}$ and $\overline{WE}$[3:0]

CNF16 - 64K By 16 Or 256K By 4 DRAM Select.

0 = A 4.7K pull-down resistor on pin MD16 sets the WD90C33 to interface with a 64K by 16 DRAM.

1 = No pull-down resistor. The internal pull-up sets WD90C33 to interface with a 256K by 4 or 256K by 16 DRAM.

CNF[15:12] - EGA Configuration Switches SW4-SW1.

No external pull-down resistors on MD(15:12) causes PR11(7:4) to be latched high. Pulling down MD(15:12) causes these bits to be latched low.

PR11(7:4) are writable bits. These bits can be read as Bit 4 of Port 3C2h (as on a standard EGA) if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of which bit to read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2h, as follows.

WRITE 3C2h		READ 3C2h
Bit 3	Bit 2	Bit 4
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

CNF11 - Select Local Bus Interface Mode

0 = Selects Local Bus Host Interface Mode if CNF2 is set to 1.

1 = AT or MicroChannel Bus Interface Mode if CNF2 is set to 1.

In the default state, CNF11 is set to 1. To set CNF11 to 0, MD11 must have a pulldown resister.

CNF10 - Disable ROM16 Address Decode.

0 = The internal pull-up sets CNF(10) = PR1(1) = 0. To enable the 16-bit BIOS, PR1(1) must be set to 1 by writing to Port 3CFh, Index 0Bh Bit 1 and, at the same time, CNF(1) must be 1.

1 = A 4.7K pull-down on Pin MD10 sets CNF10 = PR1(1) = 1. Upon power-up, the pin $\overline{\text{ROM16}}$ is enabled for 16-bit BIOS ROM decoding.

This bit is read/write at PR1(1).

CNF9 - 46E8h/3C3h Select.

This bit has no effect in MicroChannel applications.

0 = A 4.7K pull-down on Pin MD9. Port 03C3h is selected as the VGA setup and enable register instead of Port 46E8h in the AT interface.

1 = No pull-down resistor. The internal pull-up sets CNF9 = 1. Port 46E8h is selected as VGA setup and enable register.

CNF8 - Analog/TTL Display Status Bit.

Whether provided with either a pull-up or pull-down external resistor, CNF8 is latched internally at power-on-reset from memory data bus Pin MD8.

Pulling up MD11 causes CNF8 to be latched Low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F). Suggested implementation is:

0 = Analog (VGA - compatible) display is attached.

1 = TTL (EGA-compatible) display is attached.

CNF[7:4] - General Purpose Status Bits.

Bits CNF[7:4] are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pull-up or pull-down external resistors.

Pulling down MD(7:4) causes CNF(7:4) to be latched high.

These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F).

CNF3 - Video Clock Source Control.

This bit cannot be written or read as I/O port.

Pulling up MD3 causes CNF3 to be latched high. It configures WD90C33 pins VCLK1 and VCLK2 as inputs or outputs.

0 = Inputs.

1 = Outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer.

When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to Port 3C2h. This load pulse may be inhibited by setting PR11(2) = 1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK2 and VCLK1 outputs are equal to Bits 3 and 2 of the Miscellaneous Output Register at 3C2h when PR15 Bit 5 = 1.

CNF 2 - AT/MCA Bus Architecture Select.

This bit cannot be written or read as I/O. Pulling down MD2 causes CNF2 to be latched low.

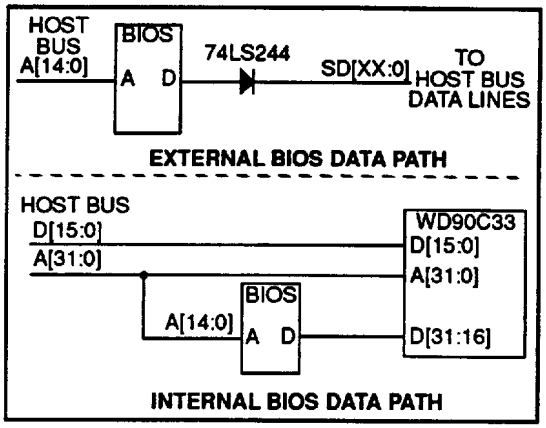
0 = MicroChannel architecture.
1 = AT BUS architecture.

Selecting CNF2 changes the pinout definition between AT BUS and MicroChannel bus. (See Signal Description.)

PC-AT BUS		MICROCHANNEL	
NAME	I/O	NAME	I/O
MEMCS16	OUT	CDDS16	OUT
ROM16	OUT	CSFB	OUT
EIO	IN	3C3D0	IN
MRD	IN	M/IO	IN
MWR	IN	S0	IN
IOR	IN	S1	IN
IOW	IN	CMD	IN
IRQ	OUT	IRQ	OUT
IOCS16	OUT	CDSETUP	OUT

CNF1 - ROM Configuration for AT or MicroChannel Mode.

0 = Selects External BIOS Data Path. The BIOS EPROM data can go through D[321:16] to D[15:0], which saves two external data buffers.
1 = Selects Internal BIOS Data Path. The BIOS EPROM data does not go through the WD90C33. An external buffer is required to connect the BIOS EPROM to the system bus.



CNF 0 - BIOS ROM Mapping.

This bit may read or written at PR1(0).

0 = No pull-down resistor on MD0. The internal pullup resistor sets this bit to 0 at power-on-reset.
1 = The BIOS ROM is mapped out. An external 4.7 Kohm pull-down resistor sets CNF(0) = 1 on power-on-reset.

10.0 LOCAL BUS INTERFACE REGISTERS

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The local bus interface registers (2DF2h through 2DF0h) are summarized in the following table.

I/O PORT	BITS	LOGIC	POWER-ON SETUP BY:	DESCRIPTION
2DF2	7:0	00	BIOS	Compared with A[31:24] to decode video memory. The default value is 00.
2DF1	7:6	---	BIOS	Reserved
	5:4	---	CNF[31:30]	$\overline{VIOR}$ and $\overline{VIOW}$ High/Low Duration
		00		2 Clocks
		01		3 Clocks
		10		4 Clocks
		11		5 Clocks (**Default**)
	3:2	---	CNF[29:28]	$\overline{VMWR}$ or $\overline{VMRD}$ High Duration
		00		2 Clocks
		01		3 Clocks
		10		4 Clocks
		11		5 Clocks (**Default**)
	1:0		CNF[27:26]	$\overline{VMWR}$ or $\overline{VMRD}$ Low Duration
		00		2 Clocks
		01		3 Clocks
		10		4 Clocks
		11		5 Clocks (**Default**)
2DF0	7	---	CNF25	Select BIOS (Refer to following paragraph.)
		0		External BIOS
		1		Local Bus BIOS (**Default**)
	6	---	CNF24	Select RAMDAC (Refer to following paragraph.)
		0		External RAMDAC
		1		Local Bus RAMDAC (**Default**)
	5	---	CNF23	Local Bus Interface Enable
		0		Disable Local Bus Interface
		1		Enable Local Bus Interface (**Default**)
	4	---	CNF22	Select Pulse Width High/Low Duration for RAMDAC, IOR, and IOW; also duration of $\overline{EBROM}$ MRD.
		0		9 Clocks
		1		18 Clocks (**Default**)
	3	---	DRIVER	Select VGA Data Path
		0		16-bit Data Path (**Default**)
		1		32-bit Data Path

TABLE 10-1 SUMMARY OF WD90C33 LOCAL BUS INTERFACE REGISTERS

I/O PORT	BITS	LOGIC	POWER-ON SETUP BY:	DESCRIPTION
2DF0	Continued			
	2		BIOS	Assert $\overline{BOFF}$
		0		$\overline{BOFF}$ Asserted (**Default**)
		1		$\overline{BOFF}$ Not Asserted
	1:0		BIOS	Select CGA or MDA Display (Refer to Section10.3)
		00		CGA Disabled/MDA Disabled (**Default**)
		01		CGA Disabled/MDA Disabled
		10		CGA Disabled/MDA Enabled
		11		CGA Enabled/MDA Disabled
None			CNF21	Select 386/486 Local Bus Interface
		0		Local Bus Mode for 386 is selected
		1		Local Bus Mode for 486 is selected
None			CNF20	Local Bus VGA Cycle Termination Control
		0		Terminate cycle when $\overline{VGARDY}$ is generated
		1		Terminate cycle by sampling $\overline{RDYIN}$ signal

NOTES

1. For CNF[31:20], the default value is 1 at power-on and /reset.
2. VLBI terminates its cycle when $\overline{VLBIRDY}$ is active or when the feedback $\overline{CPURDY}$ is active.
3. I/O Ports for Indexed Registers are 23C0h through 23CFh.

TABLE 10-1 SUMMARY OF WD90C33 LOCAL BUS INTERFACE REGISTERS

CNF[31:30] - $\overline{\text{VIOR/VIOD}}$ High/Low Duration

Provides setup of Local Bus Interface Control Register 2DF1h[5:4] for Power-on and Reset as follows:

00 = Two Clocks Per Bus Cycle
01 = Three Clocks Per Bus Cycle
10 = Four Clocks Per Bus Cycle
11 = Five Clocks Per Bus Cycle (Default)

CNF[28:29] - $\overline{\text{VMWR/VMRD}}$ High Duration

Provides setup of Local Bus Interface Control Register 2DF1h[3:2] for Power-on and Reset as follows:

00 = Two Clocks Per Bus Cycle
01 = Three Clocks Per Bus Cycle
10 = Four Clocks Per Bus Cycle
11 = Five Clocks Per Bus Cycle (Default)

CNF[27:26] - $\overline{\text{VMWR/VMRD}}$ Low Duration

Provides setup of Local Bus Interface Control Register 2DF1h[1:0] for Power-on and Reset as follows:

00 = Two Clocks Per Bus Cycle
01 = Three Clocks Per Bus Cycle
10 = Four Clocks Per Bus Cycle
11 = Five Clocks Per Bus Cycle (Default)

CNF25 - Set BIOS in Local Bus Mode

Provides setup of Local Bus Interface Control Register 2DF0h[7] for Power-on and Reset. Refer to Section 10.1.

0 = BIOS is External
1 = BIOS is set in Local Bus Mode (Default)

CNF24 - Connect RAMDAC in Local Bus Mode

Provides setup of Local Bus Interface Control Register 2DF0h[6] for Power-on and Reset. Refer to Section10.2.

0 = RAMDAC is External
1 = RAMDAC is Connected Local Bus Mode (Default)

CNF23 - Enable Local Bus Interface

Provides setup of Local Bus Interface Control Register 2DF0h[5] for Power-on and Reset as follows:

0 = Local Bus Interface is Not Enabled
1 = Local Bus Interface is Enabled (Default)

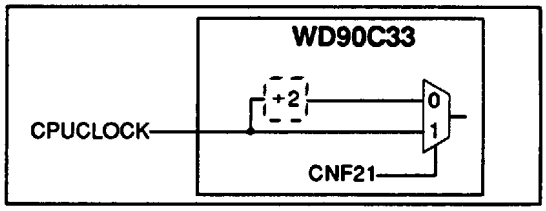
CNF22 - Select Pulse Width (High and Low) Duration for RAMDAC, IOR, AND IOW; also Duration of $\overline{\text{EBROM}}$ MRD Access

Provides setup of Local Bus Interface Control Register 2DF0h[4] for Power-on and Reset as follows:

	NUMBER OF CPUCLOCKS	
CNF22	RAMDAC, IOR, IOW DURATION	EPROM MRD ACCESS
0	9	4
1	18	8

CNF21 - Select 386/486 Local Bus Interface

0 = Local Bus Mode for 386 is selected. The CPU clock is internally divided by 2 and synchronized by the CPURESET signal.
1 = Local Bus Mode for 486 is selected. The CPU clock is not divided or affected by CPURESET.



CNF20 - Local Bus VGA Cycle Termination Control

0 = Local Bus VGA Cycle is terminated by WD90C33 internal ready ($\overline{\text{VLBIRDY}}$).
1 = Local Bus VGA Cycle is terminated by host (RDYIN), which is the default case.

CNF19 - Reserved

Reserved bits should be set to 1.

10.1 SELECT LOCAL BUS OR EXTERNAL BIOS, REGISTER 2DF0, Bit 7 (CNF25)

The Local Bus BIOS or an External BIOS is selected via Local Bus Interface Register 2DF0h, bit 7.

10.1.1 Local Bus BIOS (Bit 7=1)

When the Local Bus BIOS is selected (Bit 7=1), VLBI generates $\overline{\text{VLBICS}}$, and the core logic will not see the video BIOS cycle. VBLI also generates $\overline{\text{MRD}}$ to VGA.

The pulse width of $\overline{\text{MRD}}$ low is determined by 2DF0h, bit 4. If bit 4 is set to 0, $\overline{\text{MRD}}$ is low for four clocks during the BIOS cycle. When bit 4 is set to 1, $\overline{\text{MRD}}$ is low for eight clocks during the BIOS cycle. The pulse width for $\overline{\text{MRD}}$ high is not a concern for the BIOS cycle.

Also, with 2DF0h, bit 7 set to 1, $\overline{\text{EBROM}}$ is generated by VGA. $\overline{\text{EBROM}}$ is always decoded with A[31:20] set to 0.

Finally, VLBI terminates the BIOS cycle since $\overline{\text{VLBUSY}}$ is not generated.

10.1.2 External BIOS (Bit 7=0)

When an External BIOS is selected (Bit 7=0), VLBI generates $\overline{\text{EBROM}}$ by decoding the row CPU address. $\overline{\text{EBROM}}$ is decoded for addresses 000C0000h through 000C7FFFh if register 3?5h, bit 2 is set to 0 (PR17, bit 2). $\overline{\text{EBROM}}$ is decoded for addresses 000C0000h through 000CFFFFh if register 3?5h, bit 2 is set to 1.

With bit 7 set to 0, VLBI does not generate $\overline{\text{VLBICS}}$ or $\overline{\text{VLBUSY}}$.

10.2 SELECT RAMDAC, REGISTER 2DF0, BIT 6 (CNF24)

The Local Bus RAMDAC or an External RAMDAC is selected via Local Bus Interface Register 2DF0h, bit 6.

10.2.1 Local Bus RAMDAC (Bit 6=1)

When the Local Bus RAMDAC is selected (Bit 6=1), VLBI generates $\overline{\text{VLBICS}}$, and the core logic will not see the RAMDAC cycle. VLBI also generates $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ for the RAMDAC cycle to VGA.

VLBI will not generate $\overline{\text{VLBUSY}}$, and will terminate the RAMDAC cycle by counting either 9 or 18 clocks for IOR or IOW high or low (refer to register 2DF0h, bit 4).

10.2.2 External RAMDAC (Bit 6=0)

When an External RAMDAC is selected (Bit 6=0), VLBI does not generates $\overline{\text{VLBICS}}$, and the core logic does see the RAMDAC cycle during both read and write operations.

VLBI still generates $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ for the RAMDAC cycle to VGA. However, core logic terminates RAMDAC cycles to the VGA.

VLBI will generate a RDY (ready) signal to the CPU, and also generate $\overline{\text{VLBUSY}}$ to intercept the core logic RDY signal for RAMDAC write cycles.

10.3 SELECT CGA OR MDA DISPLAY, REGISTER (2DF0, BITS 1:0

An MDA display or a CGA display is selected via Local Bus Interface Register 2DF0h, bits 1:0 as listed in Table 10-1.

The MDA display is selected when bits 1:0 are set to 10, and the CGA display is selected when bits 1:0 are set to 11.

For selecting dual displays, follow the table on page 5 of the WD90C56 Data Sheet.

***

Is the above reference to the WD90C56 Data Sheet correct, or should that information be put in this data sheet?

11.0 HARDWARE CURSOR

The Hardware Cursor supports a user-defined pattern of up to 64 by 64 pixels, defined at 2 bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all packed and planar VGA graphics modes, as well as VGA text modes.

The Hardware Cursor is accessed at Port 23C2h/ 23C3h when the register block pointer at Port 23C0h has been set to 02h. For additional information on accessing indexed registers, refer to Section 13.

INDEX	BITS	NAME
0*	11:0	Cursor Control
1	11:0	Cursor Pattern Address Low
2	11:0	Cursor Pattern Address High
3	11:0	Cursor Primary Color, Byte 0
4	11:0	Cursor Primary Color, Byte 1 (For 16-bit Color)
5	11:0	Cursor Primary Color, Byte 2 (For 24-bit Color)
6	11:0	Cursor Secondary Color, Byte 0
7	11:0	Cursor Secondary Color, Byte 1 (For 16-bit Color)
8	11:0	Cursor Secondary Color, Byte 2 (For 24-bit Color)
9	11:0	Cursor Auxiliary Color, Byte 0
A	11:0	Cursor Auxiliary Color, Byte 1 (For 16-bit Color)
B	11:0	Cursor Auxiliary Color, Byte 2 (For 24-bit Color)
C	11:0	Cursor Origin
D	11:0	Cursor Display Position X
E	11:0	Cursor Display Position Y
F	11:0	Register Block/Index (New)

TABLE 11-1 HARDWARE CURSOR INDEXED REGISTERS

11.0.1 Cursor Control Register, Index 0

The Cursor Control register controls operation of the hardware cursor.

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BIT	FUNCTION
15:12	0000 (Index)
11	Cursor Enable
10:9	Cursor Pattern Type
8	Cursor Plane Protection
7:5	Cursor Color Mode
4	Enhanced Hardware Cursor (24 bits per pixel)
3:0	Reserved

NOTE

A write to either the Cursor Enable or the Cursor Pattern Type fields does not take effect until the beginning of a video frame following the next write to the Cursor Control Register. (In interlaced mode, it's the next video field.)

Bits (15:12) - Index 0.

Bit 11 - Cursor enable.

0 = Cursor is not displayed.
1 = Cursor is displayed.

Bits (10:9) - Cursor Pattern Type

00 = Cursor is 2 bits per pixel, 32x32 pixels.
01 = Cursor is 2 bits per pixel, 64x64 pixels.
10 = Reserved.
11 = Reserved.

Bit 8 - Cursor Plane Protection

0 = Cursor plane protection disabled.
1 = Cursor plane protection enabled.

Bits (7:5) - Cursor Color Mode

BITS			FUNCTION
7	6	5	
0	0	0	Software Compatible Cursor.
0	0	1	Two-color Cursor with Inversion.
0	1	0	Two-color Cursor with Special Inversion.
0	1	1	Three-color Cursor.
1	0	0	Reserved.
1	0	1	Reserved.
1	1	0	Reserved.
1	1	1	Reserved.

Bit 4 - Enhanced Hardware Cursor (24 bits per pixel)

0 = Disable enhanced hardware cursor
1 = Enable enhanced hardware cursor (24 bits per pixel).

NOTE

The standard hardware cursor (16 bits per pixel) is enabled by Control Register 2 (Register Block 1, Index 1, bits 11:10 = 10). Refer to Section 12 for additional information.

Bits (3:0)

Reserved.

11.1 CURSOR PATTERN ADDRESS

The two Cursor Pattern Address registers form a 21-bit address, specifying the location in the display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin. The cursor pattern may be stored anywhere in the display memory but is generally stored in a non-visible location.

Generally, this address represents the CPU address at which the pattern begins, minus the CPU address of the top-left corner of the screen, in whichever current VGA mode is in use. Not all addresses are valid in all modes. Refer to the Section 11.6.1 on Cursor Address Mapping.

NOTE

A write to either of the Cursor Pattern Address Registers or the Cursor Origin Register does not take effect until the beginning of a video frame following the next write to the Cursor Control Register. (In interlaced mode, it's the next video field.)

11.1.1 Cursor Pattern Address Low, Index 1

BIT	FUNCTION
15:12	0001 (Index)
11:0	Cursor Pattern Address Bits 11:0. Bits 1 and 0 must be set to 0.

11.1.2 Cursor Pattern Address High, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:9	Reserved
8:0	Cursor Pattern Address Bits 20:12

11.2 CURSOR COLOR REGISTERS

The cursor color registers control the display of 2-bit per pixel cursor patterns.

The Cursor Primary Color, Cursor Secondary Color and Cursor Auxiliary Color registers specify eight-bit, 16-bit, or 24-bit colors to be displayed for different parts of the cursor pattern.

NOTE

Even in planar mode, in which pixels are four bits each, these colors are eight bits per pixel.

11.2.1 Cursor Primary Color, Byte 0, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:8	Reserved
7:0	Cursor Primary Color, Byte 0

11.2.2 Cursor Primary Color, Byte 1, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:8	Reserved
7:0	Cursor Primary Color, Byte 1 (For 16-bit color.)

11.2.3 Cursor Primary Color, Byte 2, Index 5

BIT	FUNCTION
15:12	0101 (Index)
11:8	Reserved
7:0	Cursor Primary Color, Byte 2 (For 24-bit color.)

11.2.4 Cursor Secondary Color, Byte 0, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11:8	Reserved
7:0	Cursor Secondary Color, Byte 0

11.2.5 Cursor Secondary Color, Byte 1, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:8	Reserved
7:0	Cursor Secondary Color, Byte 1 (For 16-bit color.)

11.2.6 Cursor Secondary Color, Byte 2, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Reserved
7:0	Cursor Secondary Color, Byte 2 (For 24-bit color.)

11.2.7 Cursor Auxiliary Color, Byte 0, Index 9

BIT	FUNCTION
15:12	1001 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color, Byte 0

11.2.8 Cursor Auxiliary Color, Byte 1, Index A

BIT	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color, Byte 1 (For 16-bit color.)

11.2.9 Cursor Auxiliary Color, Byte 2, Index B

BIT	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color, Byte 2 (For 24-bit color.)

11.3 CURSOR ORIGIN, INDEX C

The Cursor Origin register specifies the offset in pixels from the top-left corner of the pattern which will be displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

For 32 by 32 cursor patterns each field is restricted to the values 31:0.

BIT	FUNCTION
15:12	1100 (Index)
11:6	Cursor Origin Y (63-0)
5:0	Cursor Origin X (63-0)

11.4 CURSOR DISPLAY POSITION

The Cursor Display Position X and Y registers specify the location on the screen at which the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels not characters. The cursor can be displayed at any position on the screen, including between characters.

NOTE

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. (In interlaced mode, it's the next video field.)

11.4.1 Cursor Display Position X, Index D

BIT	FUNCTION
15:12	1101 (Index)
11	Reserved
10:0	Cursor Display Position X

11.4.2 Cursor Display Position Y, Index E

BIT	FUNCTION
15:12	1110 (Index)
11:10	Reserved
9:0	Cursor Display Position Y

11.5 REGISTER BLOCK INDEX, INDEX F

Information to be supplied.

BIT	FUNCTION
15:12	1111 (Index)
11:0	Register Block Index

11.6 CURSOR REGISTER UPDATES

When a new cursor pattern is selected, up to four different registers must be updated. If a new video frame were to begin before all registers were updated, a single frame could be displayed with incorrect cursor data. While the display would recover within one video frame, the results would be visually annoying. Therefore, the WD90C33 holds off use of updated register data until all of the associated registers have been updated.

Writing to either the Cursor Pattern Address register or the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the Cursor Control register. Therefore, the Cursor Control register must be written to after updating either of these registers, even if the data in the Cursor Control register is to remain unchanged. However, reading any of these registers always returns the data last written to the register, whether or not such data has already taken effect.

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. In interlaced mode, updates occur at the beginning of the next video field.

11.6.1 Cursor Address Mapping

Cursor patterns are always stored in contiguous locations in display memory, usually in a non-visible portion, and always across all four maps. The definition of contiguous locations differs slightly by mode, as defined in Tables 11-2, 3 and 4.

Each mode has restrictions on where a cursor pattern may begin and how such a pattern must be stored. The location where the currently required cursor pattern is stored in display memory is loaded by the host into the Cursor Pattern Address registers, as defined in Tables 11-2, 3, and 4.

The Cursor Pattern Address registers point to the doubleword starting region of the cursor pattern. They are not byte addresses and consecutive register values generally do not point to consecutive memory bytes. However, the cursor pattern must use all of the consecutive memory bytes (1K or 256 bytes) assigned to it starting from the byte pointed to.

CPU ADDRESS	CURSOR PATTERN ADDRESS
Bank 0	
A0000[1]	
Map 0	0 If pattern starts here...
Map 1	[2] then the next byte is here...
Map 2	[2] then here...
Map 3	[2] then here...
A0001	
Map 0	[1] and the fifth byte is here
⇓	
AFFFF	
Map 0	FFFF
Bank 1	
A0000	
Map 0	10000
⇓	
AFFFF[3]	
⇓	
Map 3	1FFFF (Theoretical maximum for 1K X 1K display memory.)
Refer to the following notes.	

TABLE 11-2 PLANAR MODES

NOTES FOR TABLES 11-2 THROUGH 11-4

1. These locations are usually visible. In practice, cursor pattern is usually stored in non-visible memory.
2. Cursor pattern must start in map 0 but pattern is stored on all maps.
3. Some modes and/or boards may not support CPU addresses up to this level. Since up to 1K consecutive locations are required for the pattern, the pattern cannot actually start at the highest locations.
4. In mode 7, CPU addresses are B0000-B7FFE.

CPU ADDRESS	CURSOR PATTERN ADDRESS
Bank 0	
A0000[1]	0 If pattern starts here. . .
A0001	[2] then next byte is here. . .
A0002	[2] then here. . .
A0003	[2] then here. . .
A0004	[1] and the fifth byte is here
⇓	
AFFFC	3FFF
Bank 1	
A0000	4000
⇓	
Bank 0F	
⇓	
AFFFC[3]	3FFFF (Theoretical maximum for 1K X 1K display memory.)
Refer to the previous notes.	

TABLE 11-3 PACKED MODES

CPU ADDRESS	CURSOR PATTERN ADDRESS
Maps 0:1	
B8000[1]	0 If pattern starts here. . .
B8001	[2] then next byte is here. . .
Maps 2:3	
B8000	[2] then here. . .
B8001	[2] then here. . .
Maps 0:1	
B8002	[1] and the fifth byte is here
B8003	
⇓	
BFFFE	3FFF
BFFFF	
Refer to the previous notes.	

TABLE 11-4 TEXT MODES,

11.6.2 Two-Bit Cursor Pattern Format

The cursor pattern pointed to by the Cursor Pattern Address registers for two-bit cursor patterns is stored in either 1K or 256 consecutive memory byte locations. The cursor pattern data is stored for 64 by 64 and 32 by 32 cursors as follows:

11. 6.2.1 Cursor Pattern - 2-Bit, 64 x 64 Cursors

OFFSET[1]	MAP[2]	CURSOR PATTERN[3,4]
0	0	AND plane, row 0, col 0-7
	1	XOR plane, row 0, col 0-7
	2	AND plane, row 0, col 8-15
	3	XOR plane, row 0, col 8-15
1	0	AND plane, row 0, col 16-23
	1	XOR plane, row 0, col 16-23
	2	AND plane, row 0, col 24-31
	3	XOR plane, row 0, col 24-31
2	0	AND plane, row 0, col 32-39
	1	XOR plane, row 0, col 32-39
	2	AND plane, row 0, col 40-47
	3	XOR plane, row 0, col 40-47
3	0	AND plane, row 0, col 48-55
	1	XOR plane, row 0, col 48-55
	2	AND plane, row 0, col 56-63
	3	XOR plane, row 0, col 56-53
4	0	AND plane, row 1, col 0-7
	1	XOR plane, row 1, col 0-7
	2	AND plane, row 1, col 8-15
	3	XOR plane, row 1, col 8-15
⇓		
255	0	AND plane, row 63, col 48-55
	1	XOR plane, row 63, col 48-55
	2	AND plane, row 63, col 56-63
	3	XOR plane, row 63, col 56-63
Refer to the following notes.		

NOTES

1. Offset is relative to the value in the Cursor Pattern Address register.
2. In packed mode, Map is selected by the two low-order CPU address bits.
3. Cursor pattern must start in map 0 but pattern is stored on all maps.
4. Within each byte, the high-order bit represents the left most column.

11. 6.2.2 Cursor Pattern - 2-Bit, 32 x 32 Cursors

OFFSET[1]	MAP[2]	CURSOR PATTERN[3,4]
0	0	AND plane, row 0, col 0-7
	1	XOR plane, row 0, col 0-7
	2	AND plane, row 0, col 8-15
	3	XOR plane, row 0, col 8-15
1	0	AND plane, row 0, col 16-23
	1	XOR plane, row 0, col 16-23
	2	AND plane, row 0, col 24-31
	3	XOR plane, row 0, col 24-31
2	0	AND plane, row 1, col 0-7
	1	XOR plane, row 1, col 0-7
	2	AND plane, row 1, col 8-15
	3	XOR plane, row 1, col 8-15
3	0	AND plane, row 1, col 16-23
	1	XOR plane, row 1, col 16-23
	2	AND plane, row 1, col 24-31
	3	XOR plane, row 1, col 24-31
⇓		
63	0	AND plane, row 31, col 16-23
	1	XOR plane, row 31, col 16-23
	2	AND plane, row 31, col 24-31
	3	XOR plane, row 31, col 24-31
Refer to the previous notes.		

11.6.3 Loading The Cursor Pattern

Loading a cursor pattern requires writing the pattern to a non-visible portion of display memory, then pointing to the pattern with the Cursor Pattern Address registers (Index 1, 2). A cursor pattern already in display memory can be selected simply by loading these registers.

In some VGA modes, certain maps are not defined but the physical RAM connected to those maps appears at higher memory locations in the maps that are defined. For instance, the first byte of map 2 may appear as the 64th Kbyte in map 0. Therefore a cursor pattern that occupies contiguous locations in one mode may appear fragmented in other modes. It is the responsibility of the software to track these fragments and assure that no part of the pattern will be accidentally overwritten.

11.6.4 Cursor Color Modes

T-52-33-45

A cursor may be displayed using any of four color modes selected by the Cursor Color Mode field of the Cursor Control Register (Index 0). Depending on the color mode selected, each 2-bit pixel of the cursor pattern will be displayed against the background as described in Table 11-5.

The "special" color generates the exclusive-NOR (XNOR) of the background and the Auxiliary Color Register (Index 9, A, or B). This retains the "different from background" color property of inversion while adding the ability to specify one preferred "special inversion" from a background color to any desired color.

To use this feature, the Cursor Color Mode field must be set to "special", and the Cursor Auxiliary Color should be loaded with the exclusive NOR (XNOR) of the background color to be translated and the desired color to be displayed. When set in this manner, any screen pixel of the former color covered by an inverting cursor pattern pixel will be "inverted" into the auxiliary color.

CURSOR PATTERN[1]	COLOR MODE 0	COLOR MODE 1	COLOR MODE 2	COLOR MODE 3
00	All 0s	Secondary	Secondary	Secondary
01	All 1s	Primary	Primary	Primary
10	Transparent	Transparent	Transparent	Transparent
11	Inverted	Inverted	Special[2]	Auxiliary

NOTES:

1. The high-order bit of each 2-bit pattern is the AND mask, and the low-order bit is the XOR mask.
2. The result is Background XNORd with the auxiliary color.

TABLE 11-5 CURSOR COLOR MODES

11.6.5 Compatibility Differences Between Hardware And Software Cursor

Some cursor colors may display differently using the hardware cursor than when using a software cursor. This can happen in Planar Modes, because a software cursor modifies memory data that is then passed through the Attribute Controller's Palette registers, while the hardware cursor operates on data at the output of the Attribute Controller's Palette registers. The following section on Cursor Plane Protection explains how to minimize these incompatibilities.

11.6.6 Cursor Plane Protection

In 256-color modes, a background pixel covered by the cursor is either replaced by a specified 8-bit color or is inverted. For other modes, cursor plane protection is available.

When the Cursor Plane Protection bit of the Cursor Control register is set, some bits of the background are handled differently. In these cases the two or four high-order bits of the background are replaced with the corresponding bits of the Cursor Auxiliary Color register (Index 9, A, or B).

When bit 7 of the VGA Attribute Mode Control register (Port 3C0h/3C1h, Index 10h) is reset, cursor plane protection applies to the two high-order bits of the background. When this bit is set, protection applies to the four high-order bits.

This feature is designed to provide as much flexibility and compatibility with a software cursor as possible, due to the processing done by the VGA attribute controller.

12.0 DRAWING ENGINE

The Drawing Engine (DE) supports accelerated data transfers between regions of display memory. A full complement of raster operations are available. Color expansion and transparency, useful for accelerating text modes as well as plane masking, are supported.

This same hardware can be used to accelerate 8 by 8 pattern filled rectangles, solid rectangles, line drawing, and trapezoid fill using trapezoid fill strip.

The Drawing Engine hardware supports text modes and monochrome, 4-bit and 8-bit color modes, as well as the 16-bit color mode.

The Drawing Engine hardware uses two sets of indexed registers, which are listed in Tables 12-1 and 12-2. The registers are accessed at I/O Port 23C2h. For additional information on accessing indexed registers, refer to Section 13.

In the following tables, the REF column refers to the Section containing additional information.

INDEX	BITS	NAME	REF
0	11:0	Control Register 1	12.1
1	11:0	Control Register 2	12.1
2	11:0	Source X	12.2
3	11:0	Source Y	12.2
4	11:0	Destination X	12.2
5	11:0	Destination Y	12.2
6	11:0	Dimension X	12.3
7	11:0	Dimension Y	12.3
8	11:8	Raster Operation	12.8
9	11:0	Left Clip (X Position for Clipping)	12.4
A	11:0	Right Clip (X Position for Clipping)	12.4
B	11:0	Top Clip (Y Position for Clipping)	12.4
C	11:0	Bottom Clip (Y Position for Clipping)	12.4
D	11:0	Reserved	---
E	11:0	Reserved	---
F	11:0	Register Block Index	12.16

TABLE 12-1 DRAWING ENGINE REGISTERS, I/O PORT 23C2h, (BLOCK 1 OF 2)

INDEX	BITS	NAME	REF
0	8:0	Map Base Address (Linear Address Offset)	12.5
1	11:0	Row Pitch	12.3
2	7:0	Foreground Color Byte 0	12.6
3	7:0	Foreground Color Byte 1 (For 16-bit Color)	12.6
4	7:0	Background Color Byte 0	12.6
5	7:0	Background Color Byte 1 (For 16-bit Color)	12.6
6	7:0	Transparency Color Byte 0	12.12
7	7:0	Transparency Color Byte 1	12.12
8	7:0	Transparency Mask Byte 0	12.12
9	7:0	Transparency Mask Byte 1 (For 16-bit Color)	12.12
A	7:0	Mask Byte 0	12.7
B	7:0	Mask Byte 1 (For 16-bit Color)	12.7
C	11:0	Reserved	--
D	11:0	Reserved	---
E	11:0	Reserved	---
F	11:0	Register Block Index	12.16

TABLE 12-2 DRAWING ENGINE REGISTERS, I/O PORT 23C2h, (BLOCK 2 OF 2)

12.1 DRAWING ENGINE CONTROL

The Drawing Engine control uses two 16-bit registers. Control Register 1 is located at Index 0, and Control Register 2 is located at Index 1. Refer to Table 12-1.

12.1.1 Drawing Engine Control Register 1, Index 0

The functions of Control Register 1 are listed in Table 12-3. Writing to Control Register 1 with any drawing mode other than a "No Operation" will start the Drawing Engine with the specified drawing mode active.

For the functions of Control Register 2, Refer to Table 12-4.

BITS	LOGIC	FUNCTION
15:12	0000	Index 0
11:9	---	Drawing Modes (Section 12.17)
	000	No Operation
	001	BITBLT
	010	Line Strip
	011	Trapezoidal Fill Strip
	100	Bresenham Line
	101	Reserved
	110	Reserved
	111	Reserved
8	---	X Direction
	0	Positive
	1	Negative
7	---	Y Direction
	0	Positive
	1	Negative
6	---	Major
	0	X Major
	1	Y Major
5	---	Source Select
	0	Screen Memory
	1	Host I/O or Memory
4:3	---	Source Format
	00	Color
	01	Monochrome from Color Comparators
	10	Fixed Color (Rectangle Fill, Line, Line Strip, and Trapezoidal Fill)
	11	Monochrome from Host
2	---	Pattern Enable
	0	Pattern Not Used
	1	Pattern Used As Source
1	---	Destination Select
	0	Screen Memory
	1	Host I/O or Memory
0	---	Last Pixel Off*
	0	Last Pixel ON
	1	Last Pixel OFF
* For Bresenham Line		

TABLE 12-3 DRAWING ENGINE CONTROL REGISTER 1

Bits 15:12 - Index 0.

Bits11:9 - Drawing Mode

These bits control the Drawing Engine drawing mode as listed in Table 12-3. For descriptions of the drawing modes refer to Section 12.16.

Bits 8:6 - Direction

Bits 8 and 7 control the direction of movement in the X and Y direction, respectively. Bit 6 controls whether the major movement is in the X or Y direction. Bit 6 is not used for BITBLT operations. Refer to Table 12-3.

Bit 5 - Source Select

This bit selects the source as either the screen memory or the host CPU memory, which can be either the host I/O or system memory. Refer to Table 12-3. This bit is used only for BITBLT operations.

Bits 4:3 - Source Format

Bits 4 and 3 specify the format of the BITBLT source. The four choices are listed in Table 12-3.

Bit 2 - Pattern Enable

Bit 2 controls pattern enable. With this bit set to 1, pattern is used as the BITBLT source. Refer to Table 12-3. This bit is used only for BITBLT operations.

Bit 1 - Destination Select

This bit selects the destination as either the screen memory or the host CPU memory, which can be either the host I/O or system memory. Refer to Table 12-3. This bit is used only for BITBLT operations.

Bit 0 - Last Pixel Off

This bit is used to control the last pixel for Bresenham lines.

12.1.2 Drawing Engine Control Register 2, Index 1

The functions of Control Register 2 are listed in Table 12-4.

For the functions of Control Register 1, Refer to Table 12-3.

BITS	LOGIC	FUNCTION
15:12	0001	Index 1
11:10	---	Pixel Depth
	00	4-Bits/Pixel (Planar)
	01	8-Bits/Pixel (Packed)
	10	16-Bits/Pixel (Packed)
	11	Reserved
9	---	Transparency Enable
	0	Not Enabled
	1	Enabled
8	---	Transparency Polarity
	0	Negative
	1	Positive
7	---	Monochrome Transparency
	0	OFF
	1	ON
6:5	---	Reserved
	11	Reserved bits should be set to 1
4	---	Data Path FIFO Depth
	0	4-Levels Deep
	1	2-Levels Deep
3	---	HBLT thru Memory Port
	0	Data thru I/O Port
	1	Data thru Memory/not I/O
2:0	---	HBLT Color Expand Data Bits/Host Write*
	000	Not Defined
	001	Reserved
	010	2 Bits/CPU Write (16 Bits/Pixel only)
	011	4 Bits/CPU Write (8 or 16 Bits/Pixel only)
	100	8 Bits/CPU Write (4, 8, or 16 Bits/Pixel)
	101	16 Bits/CPU Write (4, 8, or 16 Bits/Pixel)
	110	Reserved
	111	Not Defined
* High density not available for some MCLK Frequencies		

TABLE 12-4 DRAWING ENGINE CONTROL REGISTER 2

Bits 15:12 - Index 1.

Bits 11:10 - Pixel Depth

These bits select the pixel depth. The available addressing modes are 4-bits per pixel in Planar mode, and 8- or 16-bits per pixel in Packed mode. Refer to Table 12-4.

Bits 9:7 - Transparency

These bits are used to control the transparency features. Bit 9 is used to enable transparency, bit 8 controls the transparency polarity, and bit 7 controls transparency for monochrome mode operation. Refer to Table 12-4

Bit 6:5 - Reserved

Reserved bits should be set to 1.

Bit 4 - Data Path FIFO Depth

This bit selects the Data Path FIFO depth as either 4-levels deep or 2-levels deep. Refer to Table 12-4.

Bit 3 - Host BITBLT (HBLT) through Memory Port

This bit controls which memory port is used by the host BITBLT. The data can be transferred through memory (not I/O) or through the I/O. Refer to Table 12-4.

Bits 2:0 - HBLT Color Expanded Data Bits/CPU Write

These bits control the number of bits used to expand HBLT color for CPU writes. Refer to Table 12-4.

NOTE

High density is not available for some MCLK frequencies.

12.2 SOURCE AND DESTINATION

The Source X and Source Y registers specify the source address for BITBLT operations. The Destination X and Destination Y registers specify the destination address. The X and Y fields of each register pair are pointing to a screen memory location. Refer to Table 12-1.

For BITBLT operations, the starting corner for source and destination can be any of the four corners as specified with the X Direction and Y Direction bits of the Drawing Engine Control Register 1 as follows:

X DIRECTION	Y DIRECTION	STARTING CORNER
0	0	Top Left
0	1	Bottom Left
1	0	Top Right
1	1	Bottom Right

When the source and destination areas do not overlap, a BITBLT operation can be started in any corner. When these areas overlap, the corner and direction must be selected to prevent parts of the source area from being overwritten by the destination array before they are copied.

For pattern fill (BITBLT operation with pattern enable bit set), Source X and Source Y are used to point to the starting location of the pattern. Destination X and Destination Y are always updated after the operation is complete.

Source X, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:0	Source X Position Bits 11:0

Source Y, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:0	Source Y Position Bits 11:0

Destination X, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:0	Destination X Position Bits 11:0

Destination Y, Index 5

BIT	FUNCTION
15:12	0101 (Index)
11:0	Destination Y Position Bits 11:0

12.3 DIMENSIONS AND ROW PITCH

12.3.1 Dimension X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11:0	Dimension X *
* legal range is 1 to 4K - 1	

The Dimension X register is programmed with the desired value minus one as follows:

- For BITBLT operations, this register specifies the width of the rectangular region to be copied.
- For line strip and trapezoidal fill strip operations, this register specifies the length of the strip.
- For Bresenham lines, this register specifies the number of pixels to be drawn
- In Graphic Modes, this register value is expressed in pixels.
- In Text Modes, this register value is expressed in the number of characters multiplied by eight (even though each character is stored using only two bytes).

12.3.2 Dimension Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:0	Dimension Y *
* legal range is 1 to 4K - 1	

The Dimension Y register is programmed with the desired value minus one as follows:

- For BITBLT operations, this register specifies the height of the rectangular region to be copied.
- For line strip operations, this register is programmed with the number of line strips with the same length.
- In Graphic Modes, this register value is the height of the region in pixels.
- In Text Modes, this register value is the height of the region in character rows.
- The Dimension Y register is not used for Bresenham line Trapezoid Fill Strip operations.

12.3.3 Row Pitch, Index 1

BIT	FUNCTION
15:12	1000 (Index)
11:0	Row Pitch *
* In Packed Mode the two low order bits of this field must be zero. In Planar Mode the three low order bits must be zero.	

The Row Pitch register specifies the number of pixels offset from any location in a given row to the same location in the next row. This offset is in the same units as the source and destination fields to which it applies.

12.4 CLIPPING

A rectangle clipping function is supported (refer to Table 12-1). The four clipping registers (left, right. top, and bottom) define a rectangular area. Any pixel inside and on the boundary of the rectangular area can be updated during a drawing operation.

Left Clip, Index 9

BIT	FUNCTION
15:12	1001 (Index)
11:0	Left Clip (X position for clipping)

Right Clip, Index A

BIT	FUNCTION
15:12	1010 (Index)
11:0	Right Clip (X position for clipping)

Top Clip, Index B

BIT	FUNCTION
15:12	1011 (Index)
11:0	Top Clip (Y position for clipping)

Bottom Clip, Index C

BIT	FUNCTION
15:12	1100 (Index)
11:0	Bottom Clip (Y position for clipping)

12.5 ADDRESS MAPPING

The Source X and Y and the Destination X and Y (refer to Table 12-1) are converted internally to linear addresses that point to pixel locations. The linear address (LA) is defined as:

LA = (Y * ROWPITCH + X) * S + MAP BASE ADDRESS * 4K

Where: S = 1/2 for 4 bits per pixel
1 for 8 bits per pixel
2 for 16 bits per pixel

12.5.1 Map Base Address, Index 0

The Map base Address provides a linear address offset from the start of display memory Each increment of offset corresponds to a 4 Kbyte increment in display memory. Refer to Table 12-2.

BIT	FUNCTION
15:12	0000 (Index)
8:0	Map Base Address

12.5.2 Monochrome and Planar Mode

CPU ADDRESS	LINEAR ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Location 0, bit 7 (left most pixel)
	1	Location 0, bit 6
	⇩	
	7	Location 0, bit 0 (right most pixel)
A0001	8	Location 1, bit 7
	⇩	
AFFFF[2]	2M-1	Location 512K-1, bit 0[1]

NOTES:
1. Last location in a 1 MB system. Smaller memory configurations have fewer display memory locations.
2. Not in the same memory page as A0001 above.

CPU ADDRESS	LINEAR (18-BIT/ PIXEL) ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Map 0, Location 0 (left most pixel)
A0001	1	Map 1, Location 0
A0002	2	Map 2, Location 0
A0003	3	Map 3, Location 0 (right most pixel)
A0004	4	Map 0, Location1 (left most pixel)
	⇩	
A0007	7	Map 3, Location 1 (right most pixel)
	⇩	
AFFFF[2]	2M-1	Map 3, Location 512K-1[1]

NOTES:
1. Last location in a 1 MB system. Smaller memory configurations have fewer display memory locations.
2. Not in the same memory page as A0007 above.

12.5.3 Packed Modes

The locations referred to in Sections 12.5.2 and 12.5.3 are the CPU address offset in bytes from the top of the display memory for any given mode. For example, where display memory starts at CPU address A0000h, location 123h would correspond to CPU address A0123h. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64 Kbytes, location 10123h would correspond to CPU address A0123h in the second page of the display memory.

When the source or destination of a BITBLT operation is not a display memory location, the corresponding pair of position registers are unused and may contain any value, except that up to three of the low-order bits are still used to specify source alignment of the data.

12.6 FOREGROUND AND BACKGROUND COLORS

The Foreground and Background Color registers specify 4-bit, 8-bit, or 16-bit digital colors to be used when expanding monochrome source areas. The foreground color can also be specified as the source of a BITBLT to produce a filled rectangle. Refer to Table 12-2.

Foreground Color, Byte 0, Index 2

BIT	FUNCTION
15:12	0010 (Index)
11:8	Reserved
7:0	Foreground Color*
*In Planar modes only bits 3:0 are used to specify a color.	

Foreground Color, Byte 1, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:8	Reserved
7:0	Foreground Color*
*For 16-bit color.	

Background Color, Byte 0, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:8	Reserved
7:0	Background Color *
*In Planar modes only bits 3:0 are used to specify a color.	

Background Color, Byte 1, Index 5

BIT	FUNCTION
15:12	1001 (Index)
11:8	Reserved
7:0	Background Color *
*For 16-bit color.	

12.7 MAP AND PLANE MASK

The Mask registers control both Map and Plane Masks used in drawing operations. Refer to Table 12-2.

The Mask Byte 0 specifies a 4-bit mask that prevents data in the specified registers from being updated. This mask is needed for BITBLT operations in all text modes to prevent font data from being overwritten in a character-attribute move and vice versa, and VGA mode F. It can also be used in VGA modes 4, 5 and 6 for partial hardware support. Additionally, it can be used in VGA modes D, E, 10, 11 and 12 and extended Planar modes as a Plane Mask if desired.

The Mask Byte 0 and Byte 1 together specify an 8-bit or 16-bit mask that prevents data in the specified planes from being updated. This is useful in VGA Mode 13 and extended Packed modes when Plane Masking is desired.

Mask Byte 0, Index A

BIT	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	Map/Plane Mask*
* In Planar Modes only bits 3:0 are used.	

Mask Byte 1, Index B

BIT	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	Plane Mask*
* For 16-bit color.	

Plane Mask, Packed Modes for 8-bit and 16-bit Color

BYTE 0 BITS 7:0	PLANE MASK
XXXX XXX0	Plane 0 Disabled
XXXX XXX1	Plane 0 Enabled
⇓	⇓
0XXX XXXX	Plane 7 Disabled
1XXX XXXX	Plane 7 Enabled

BYTE 1 BITS 7:0	PLANE MASK
XXXX XXX0	Plane 8 Disabled
XXXX XXX1	Plane 8 Enabled
⇓	⇓
0XXX XXXX	Plane 16 Disabled
1XXX XXXX	Plane 16 Enabled

Map Mask, Planar Mode

BITS 3:0	MAP MASK
XXX0	Map 0 Disabled
XXX1	Map 0 Enabled
⇓	⇓
0XXX	Map 3 Disabled
1XXX	Map 3 Enabled

12.8 RASTER OPERATIONS

The Raster Operations register specifies a bitwise logical operation to be performed on the source and destination fields. This field is always active and must be loaded with the appropriate value even when a simple source copy is to be performed. Refer to Table 12-1.

Raster Operations, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Raster Operation CODE (abcd in Table 12-6)
7:0	Reserved

All operations apply a source color, pattern or area to a destination area. The result written to the destination is a logical function of the source and destination pixels for each location.

The Raster Operation code is defined as follows:

The Source (S) and Destination (D) form a 2-bit value. The Truth Table (Table 12-5) defines the results of the two operands, Source and Destination, for the desired function.

The four 1-bit results of the Truth Table for the desired operation (expressed as a, b, c, and d) form the Raster Operation code (abcd) used in Table 12-6. The "a" is defined as the high-order bit of the code.

While the Raster Operation code represents a 2-input operation, both inputs are not always relevant in the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination field.

Arithmetic operations are not supported.

S	D	RESULT
0	0	a
0	1	b
1	0	c
1	1	d

TABLE 12-5 RASTER OPERATION TRUTH TABLE

abcd	FUNCTION	abcd	FUNCTION
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	S X $\overline{D}$	1010	Inv Dest
0011	Src	1011	S+$\overline{D}$
0100	$\overline{S}$ X D	1100	Inv Src
0101	Dest	1101	$\overline{S}$ + D
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 12-6 RASTER OPERATION CODE

12.9 PATTERNS

The WD90C33 has a special mode to accelerate the copying of 8 by 8 source patterns. In this mode, an 8 by 8 full-color or monochrome pattern can be repetitively applied to a large destination area in an efficient manner.

To perform a pattern copy, the host first writes the 8 by 8 pattern to display memory in a linear fashion, usually to a non-visible location, depending on the current addressing mode, as described in Sections 12.5.2 and 12.5.3. The host then loads the Source registers, with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The Pattern Enable bit (Control Register 1, bit 2) must be set to 1 to enables Patterns to be used as a source.

To specify a monochrome pattern, the host must write a color pattern in the current mode, planar or packed, and then use the control registers to specify a single plane of the source to be used.

12.9.1 Pattern Storage - Monochrome And Planar Modes

In planar mode, the 8 by 8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point. This anchored point is selected by Control Register 1, bits 8 and 7, as follows:

Bit 8 = X, Bit 7 = Y

DIRECTION			ANCHOR POINT
X	Y	WRAP	
0	0	Right and Down	Top Left
0	1	Right and Up	Bottom Left
1	0	Left and Down	Top Right
1	1	Left and up	Bottom Right

ADDRESS	DISPLAY MEMORY CONTENTS
	⇩
n - 1	Any data
n* to n+3	All maps, top row of 8x8 pattern
n+4 to n+7	All maps, second row of 8x8 pattern
	⇩
n+28 to n+31	All maps, bottom row of 8x8 pattern
n+32 to...	Any data
*n must be a multiple of 32	

12.9.2 Pattern Storage - Packed Modes

In packed mode, the 8x8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, the source address may point to any pixel with the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point. The anchored point is selected by Control Register 1, Bits 8:7.

ADDRESS	DISPLAY MEMORY CONTENTS
	⇩
n - 1	Any data
n*	Top row of 8x8 pattern (leftmost pixel)
n+1	All maps, second row of 8x8 pattern
	⇩
n+7	
n+8	
	⇩
n+63	All maps, bottom row of 8x8 pattern
n+64	Any data
*n must be a multiple of 64	

NOTE

For 16-bits per pixel, the 8 by 8 source pattern must be stored in display memory in a 128 byte aligned area.

12.10 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each 0 in the source region is replaced with the specified background color, while each 1 is replaced with the foreground color. All other processing options, including masks and raster operations, remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination will be filled with the foreground color, subject to masks, raster operations and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available since the transparency color registers are in use.

12.11 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data extracted in this manner is replicated to each plane or map as if it had been read from the memory.

Monochrome data can also be extracted from host data when the BITBLT source is the I/O port. In this case, each 32-bit word written to the I/O port is treated in the same manner as if it had been read from display memory. Alternately, the host may send monochrome data through the I/O port that does not require extraction (Refer to Section 12.14).

To extract a single plane from a color source field, the Transparency Color register should be loaded with FFh (all ones), while the Transparency Mask register should be loaded with a 0 in the map or plane position to be extracted, and a 1 in all other positions.

Monochrome data is usually extracted as a specific bit of each 4-bit, 8-bit, or 16-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color 1, with all other colors returning a monochrome 0.

When the Monochrome Transparency bit is set to 1(Control Register 2, bit 7) the monochrome source pixels of 0 do not modify the destination, regardless of any selected raster operation. Refer to Table 12-2.

The Transparency Enable and Polarity bits (Control Register 2, bits 9 and 8) have no effect on monochrome data extraction.

12.12 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT operation are actually transparent, with the rest being opaque. Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color, since when ORed with the destination, it does not change.

Color destination transparency is supported by the WD90C33, in addition to the more limited monochrome transparency described elsewhere.

The Transparency Color registers specify a 4-bit, 8-bit, or 16-bit color to be used as the transparency color. Refer to Table 12-2

Transparency Color, Byte 0, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11:8	Reserved
7:0	Transparency Color *
* In Planar Modes only the four low-order bits are used.	

Transparency Color, Byte 1, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11:8	Reserved
7:0	Transparency Color *
* For 16-bit color.	

The Transparency Mask registers specify a 4-bit, 8-bit, or 16-bit mask to compare with the transparency color. Refer to Table 12-2.

BITBLT Transparency Mask, Byte 0, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Reserved
7:0	Transparency Mask *
* In Planar Modes only the four low-order bits are used.	

Transparency Mask, Byte 0, Index 9

BIT	FUNCTION
15:12	1001 (Index)
11:8	Reserved
7:0	Transparency Mask *
* For 16-bit color.	

The pixels of the destination are compared against the Transparency Color under control of the Transparency Mask. Each bit of the Transparency Mask that is a 1 makes the corresponding bit of the Transparency Color a "don't care".

The Transparency Enable bit of the Control Register 2 (Table 12-4) specifies whether Color Transparency is enabled or disabled. The Transparency Polarity bit specifies whether pixels matching the Transparency Color are considered transparent. In this case, only destination pixels matching the transparent color can be overwritten, or transparent, and only non-matching pixels can be overwritten.

12.13 FILLED RECTANGLES

Filled rectangles can be drawn very efficiently by the hardware. A filled rectangle is simply a BITBLT operation with a source of a fixed color. To draw a filled rectangle, the host sets the Source Format field in Control Register 1 to "Fixed Color" and the Foreground Color Registers, Index 2 and 3, (refer to Table 12-2) to the desired fill color. A source X and Y are not required. All other options are available in a normal manner.

12.14 HOST BIT BLOCK TRANSFER (HBLT)

HBLT has two major functions:

- Image Transfer
- Color Expand

HBLT Image Transfer is used to transfer a bitmap from the host to the screen or from the screen to the host. The bitmap can contain all colors in a mode. HBLT transfers support 8-bit, 16-bit, or 32-bit memory access.

For HBLT to transfer a bitmap from the host to the screen, set the Control Register 1"Source Select" bit (I/O Port 23C0h, Index 0, bit 5) to 1. Refer to Table 12-3. To transfer a bitmap from the scree to the host, set the Control Register 1"Destination Select" bit (23C0h, Index 0, bit 1) to 1. Only one of the bits should be set at the same time.

When a bitmap, such as a font, that needs only one or two colors is transferred, the HBLT Color Expand function provides faster transfers since only one-bit-per-pixel transfers are performed. That one bit is then expanded into two colors (foreground and background) or an one color (foreground) and transparent. However, HBLT color expand is limited to a maximum of 16-bit transfers because memory bandwidth would hold IOCHRDY low too long for 32-bit transfers. Fewer bits may be required for some situations.

12.14.1 HBLT Data Access

After starting a Bit-Block-Transfer (BITBLT) operation, the host writes lines of the bitmap to the read_back_latch. This access can be done through memory or I/O.

The HBLT access then occurs through one of the following:

- 8-bit I/O accesses at addresses 23C4h, 23C5h, 23C6h*, and 23C7h* in sequence
- 16-bit I/O access at addresses 23C4h and 23C6h* in sequence
- 32-bit I/O access at address 23C4h*

NOTE

The asterisk (*) indicates these must be image transfers only.

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Memory access is normally faster due to shorter AT bus cycles and freedom from the operating system protection of I/O Port.

The selection of memory or I/O access for HBLT data is controlled through the Control Register 2 "HBLT Through Memory" bit (I/O Port 23C2h, Block 1, Index 1, bit 3) as follows:

0 = Screen memory normal (use I/O Port 23C4h for data transfer).

1 = All screen memory is decodes for HBLT image data

During HBLT through memory transfers, the destination address is set with the Destination X and Destination Y registers (I/O Port 23C4h, Index 4 and 5, respectively. The transfer address is used only to align byte and word transfers.

For memory writes or reads (8-bit, 16-bit, or 32*-bit) from any enabled memory address, the memory address depends upon address 3CFh Index 6, bits 3:2, the same as VGA. Bits 3:2 select address ranges as follows:

BIT		HOST ADDRESS RANGE
3	2	
0	0	A000:0h - BFFF:Fh
0	1	A000:0h - AFFF:Fh
1	0	B000:0h - B7FF:Fh
1	1	B800:0h - BFFF:Fh

NOTE

Transfers of 32-bits must be image transfers only. Color expand accommodates 16-bit transfers maximum.

For I/O transfers, HBLT data access occurs through writes and reads as described in the following to section.

12. 14.1.1 HBLT Writes

When a source read is required and data from the host is not available, the Drawing Engine suspends the HBLT operation until the data becomes available. If data comes from the host and the Drawing Engine is not ready, the data is placed in the Control Register 2 "Host Write" buffer (I/O Port 23C4h, Index 1, bits 2:0). If the Host Write buffer is full, IOCHRDY is used to hold off the host.

12. 14.1.2 HBLT Reads

For a HBLT read, data from the screen source is transferred to the data path FIFO where it waits for a host read. This allows reads with zero wait states, and is usually faster for large areas than direct memory reads. If the FIFO is full, the Drawing Engine suspends operation until the host catches up. If the host tries to read before the data is available, IOCHRDY is used to hold off the host.

12.14.2 Programming Sequence for HBLT

The sequence of programming for HBLT bitmap data transfers is given in the following steps:

1. Wait for the Command Buffer locations to be available for parameters (For Command Buffer description, refer to Section 13.)
2. Enter set-up parameters including destination, width, height, FGC, BGC, etc.
3. Use CLI to disable host interrupts that could cause conventional VGA access during a HBLT data transfer.
4. Wait for Command Buffer Locations Available = 0000 (for all eight locations). This allows the Control Register 1 writes to reach the Drawing Engine. A previous operation may have the Drawing Engine busy, and hold Control Register 1 in the command buffer until the previous operation is complete.
5. Transfer image or bit plane through I/O Port 23C4h or memory.
6. Wait for Drawing Engine busy to equal 0 (not required for screen to host transfers).
7. Use STI to enable interrupts.

NOTE

Steps 3, 6, and 7 are required when host interrupts that access VGA are present in the system. These interrupts could be from a network, communications program, TSR programs, keyboard, etc. Any conventional VGA host access during a HBLT operation will confuse HBLT.

12.14.3 Image Transfer

For Image Transfer every transfer of a line of host data must end on a 32-bit boundary. Pad bits can be added before and after the image to complete 32-bit blocks. Any read_back_latch read or write contains data for one line only. The least significant bit (LSB) is displayed on the left for X Direction = 0.

The 32-bit of image data are accumulated in the read_back_latch. When the host transfers less than 32-bits in a write, address bits 0 and 1 determine which bytes to write.

READ_BACK_LATCH			
BYTE 3	BYTE 2	BYTE 1	BYTE 0

Data Available triggers the Drawing Engine to write data when either:

- X Direction is positive and three bytes are loaded
- X Direction is positive and three bytes are loaded

For an example of an Image transfer, consider the following parameters:

1. Selected mode is 8-bits per pixel.
2. X Direction is Positive.
3. Y Direction is Positive.
4. Source X is set to 1. This selects byte 1 of the Read_Back_Latch for the leftmost pixel of the destination.
5. Destination X is set to 1.
6. Destination Y is set to 2.
7. Dimension X is set to 4 (for 5 pixels).

Then:

TRANSFER ADDRESS	DATA	FUNCTION
A000:0	84	Before Pad (Optional)
A000:1	85	First Pixel, First Line
A000:2	86	Second Pixel, First Line
A000:3	87	Third Pixel, First Line
32-Bit Boundary		
A000:4	88	Fourth Pixel, First Line
A000:5	89	Fifth Pixel, First Line
A000:6	8A	After Pad, (Required)
A000:7	8B	After Pad, (Required)
32-Bit Boundary		
A000:8	8C	Before Pad, (Optional)
A000:9	8D	First Pixel, Second Line
A000:A	8E	Second Pixel, Second Line
A000:B	8F	Third Pixel, Second Line
32-Bit Boundary		
A000:C	90	Fourth Pixel, Second Line
A000:D	91	Fifth Pixel, Second Line
A000:E	92	After Pad, (Required)
A000:F	93	After Pad, (Required)

Screen

	85	86	87	88	89			
	8D	8E	8F	90	91			

Destination

NOTES

1. In the figure above, pad bytes are outside the destination area (white), and do not appear on the screen.
2. Byte access is shown to clarify pads. In practice, 32-bit transfers would be faster.

12.14.4 Color Expand Function

For the color expand function, lines of the bitmap are transferred directly. Pad bits are required only to the next 8-bit boundary. Any write contains data for one line only. The most significant bit (MSB) is displayed on the left when X Direction = 0.

For an example of the color expand function, consider the following parameters:

1. X Direction is Positive.
2. Y Direction is Positive.
3. Monochrome Transparency is set to 0.
4. Source X is set to 0.
5. Destination X is set to 1.
6. Destination Y is set to 2.
7. Dimension X is set to 4 (for 5 pixels).

Then:

TRANSFER ADDRESS	DATA
A000:0	1000 1000*
A000:1	1110 0111*
*Bits 2:0 are ignored	

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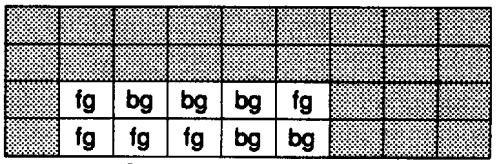

Destination

fg = foreground
bg = background

NOTE

In the figure above, pad bits are outside the destination area (white), and do not appear on the screen.

When a slow MCLK is used, there is less time available for memory access. This limits the number of color expand bits that can be written to memory while using CHRDY to hold off subsequent writes. Generally, the modes listed in Table 12-7 should use less than 16-bits per host write operation.

MCLK[1]	VCLK[2]	ROP[3]	BITS/ PIXEL	X RES	VERTICAL REF	VCLK/ PIXEL	MAXIMUM CHRDY[4]	MAXIMUM BITS PER HOST WRITE[5]
33	51	s	16	640	60	2	2.13	4
33	51	ds	16	640	60	2	2.13	2
33	44.9	ds	8	1024	43	1	1.89	8
44.9	51	ds	16	640	60	2	1.44	8
44.9	65	s	16	640	70	2	1.61	8
44.9	65	ds	16	640	70	2	1.61	4
44.9	65	ds	8	1024	60	1	1.61	8
44.9	75	s	8	1024	70	1	2.16	8
44.9	75	ds	8	1024	70	1	2.16	4
50	65	ds	16	640	70	2	1.83	8
50	75	ds	8	1024	70	1	1.60	8

NOTES:

1. The MCLK rate is related to the speed of the DRAMs used and is usually set by the board manufacturer.
2. The VCLK rate is determined by the current display mode. For an external clock generator, the VCLK rate is set with PR32 (3C5h, Index 12, bit 2) write only, and Miscellaneous Output Register (Write 3C2h, Read 3CCh, bits 3:2).
3. ROP = s includes single operation ROPs 0, 3, 5, A, C, and F.
   ROP = ds includes destination and source ROPs 1, 2, 4, 6, 7, 8, 9, B, D, and E.
4. More bits per write can be used if software guarantees enough time between writes to allow the VGA to write memory. The time necessary can be computed from:
   wait = bits_written * Max CHRDY[4] / Max_Bits/Host Write[5]

   Where: "wait" is the time in microseconds between host writes.
   "bits_written is the desired number of bits per host write.

TABLE 12-7 COLOR EXPAND FUNCTION MODES

12.15 DRAWING MODES

The WD90C33 supports four drawing modes. The drawing modes are selected by Control Register 1, bits 11:9 (refer to Table 12-3).

The drawing modes are:

- BITBLT
- Line Strip
- Trapezoidal Fill Strip
- Bresenham Line

12.15.1 Line Strip

The Line Strip drawing mode is supported to satisfy the need for a line draw algorithm other than Bresenham lines. The Bresenham Line drawing mode is described in Section 12.15.3.

Line strip provides flexibility in selecting the pixel to be drawn. Depending on the setting of the Major bit (Control Register 1, bit 6), Line Strip will draw a horizontal or vertical strip.

When Control Register 1, bits 11:9 are set to 010, Line Strip is selected and the hardware will draw one strip with the length specified in Dimension X. At the end of the strip, if the X Direction bit (bit 8) is set to 0, the operation increments 1 to Destination X. If the X Direction bit is set to 1, the operation decrements 1 to Destination X.

The same operation is done to Dimension Y depending on Y Direction bit (7), and the same hardware operations are then repeated in Dimension Y

The user may write to Dimension X with a new value, and the hardware will again draw strips with the new length. Dimension Y may be changed also, but it has to be changed before writing to Dimension X. When the drawing mode is set to line strips, writing to Dimension X will start the hardware to draw.

The Line Strip operation may be repeated as many times as required. However, following the last operation, Control Register 1, bits 11:9 must be set to 000 (No Operation). This ensures that subsequent writes to Dimension X will not start a Drawing Mode operation.

The following example draws a line from (5, 3) to (20, 8) and the pixels to be drawn are:

```
                    1 1 1 1 1 1 1 1 1 1 2
X =   5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0

Y = 3 o o o
    4       o o o
    5             o o
    6                   o o o
    7                         o o o
    8                               o o
```

For this example, the registers are programmed in the following sequence.

I/O Port 23C2h Setup

Destination X = 5
Destination Y = 3
Dimension Y = 1 (2 minus 1)
Dimension X = 2 (3 minus 1)

Control Register 1, Index 0, Line Strip Setup

BITS	FUNCTION	LOGIC	NOTES
11:9	Drawing Mode	010	Line Strip
8	X Direction	0	Positive (To the Right)
7	Y Direction	0	Positive (Downward)
6	Major	0	X Major (Horizontal Strip)
4:3	Source Format	10	Fixed Color
-	Other Bits	0	

I/O Port 23C2h Writes

Dimension Y = 0 (1 minus 1)
Dimension X = 1 (2 minus 1)
Dimension Y = 1 (2 minus 1)
Dimension X = 2 (3 minus 1)
Dimension Y = 0 (1 minus 1)
Dimension X = 1 (2 minus 1)

During Line Strip writes, if the Command Buffer is disabled, the writes to Dimension X and Dimension Y must wait until the Drawing Engine is not

busy. If the Command Buffer is enabled, the buffer should be checked to ensure that enough locations are available. For Command Buffer operation refer to Section 13.

Control Register 1, Index 0, No Operation

BITS	FUNCTION	LOGIC	NOTES
11:9	Drawing Mode	000	No Operation
8	X Direction	0	Positive (To the Right)
7	Y Direction	0	Positive (Downward)
6	Major	0	X Major (Horizontal Strip)
4:3	Source Format	10	Fixed Color
-	Other Bits	0	

This operation prevents subsequent writes to Dimension X from starting a drawing operation.

12.15.2 Trapezoid Fill Strip

The Trapezoid Fill Strip drawing mode is supported to quickly fill arbitrary shaped objects. Operation is similar to Line Strip except that Trapezoid Fill Strip does not use Dimension Y as a count number and it does horizontal strips only.

Following the last Trapezoid Fill Strip operation, Control Register 1, bits 11:9 must be set to 000 (No Operation). This ensures that subsequent writes to Dimension X will not start a Drawing Mode operation.

The following example can be used to fill a symbol.

```
        1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2
X =     2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7

Y = 2   o o o o o
    3       o o o o o
    4           o o o o
    5           o o o o
    6         o o o o
    7   o o o o o o o o o o o o o o o o
    8 o o o o o o o o o o o o o
```

For this example, the registers are programmed in the following sequence.

I/O Port 23C2h Setup

Destination X = 12
Destination Y = 2
Dimension X = 4 (5 minus 1)

Control Register 1, Index 0, Trapezoid Fill Strip Setup

BITS	FUNCTION	LOGIC	NOTES
11:9	Drawing Mode	011	Trapezoid Fill Strip
8	X Direction	0	Positive (To the Right)
7	Y Direction	0	Positive (Downward)
6	Major	0	X Major (Horizontal Strip)
4:3	Source Format	10	Fixed Color
-	Other Bits	0	---

I/O Port 23C2h Writes

Destination X = 14
Dimension X = 4 (5 minus 1)
Destination X = 16
Dimension X = 3 (4 minus 1)
Destination X = 16
Dimension X = 3 (4 minus 1)
Destination X = 15
Dimension X = 3 (4 minus 1)
Destination X = 13
Dimension X= 14 (15 minus 1)
Destination X = 12
Dimension X = 11 (12 minus 1)

During Trapezoid Fill Strip writes, if the Command Buffer is disabled, the writes to Destination X and Dimension X must wait until the Drawing Engine is not busy. If the Command Buffer is enabled, the buffer should be checked to ensure that enough locations are available. For Command Buffer operation refer to Section 13.

I/O Port 23C2h, Index 0, Control Register 1, No Operation

BITS	FUNCTION	LOGIC	NOTES
11:9	Drawing Mode	000	No Operation
8	X Direction	0	Positive (To the Right)
7	Y Direction	0	Positive (Downward)
6	Major	0	X Major (Horizontal Strip)
4:3	Source Format	10	Fixed Color
-	Other Bits	0	

This operation prevents subsequent writes to Dimension X from starting a Drawing Mode operation.

12.15.3 Bresenham Line

The WD90C33 supports line drawing using the Bresenham algorithm. In addition to the Drawing Engine registers, three other Direct I/O Port registers need to be programmed..

I/O PORT	REGISTER	
	NAME	FUNCTION
23C8h	K1	Bresenham Constant 1
23CAh	K2	Bresenham Constant 2
23CCh	ET	Bresenham Error Term

For an example, the registers are programmed as follows:

I/O Port 23C2h, Index 4 through 7 Setup

Destination X = xs
Destination Y = ys
Dimension X = max

Bresenham Values

K1 = 2 * min
K2 = 2 * (min - max) if xs is greater than xe
ET = 2 * (min - max) - 1 if xs is less than xe

Legend for Bresenham Line Register Values

xs = X coordinate of the starting point
ys = Y coordinate of the starting point
xe = X coordinate of the ending point
ye = Y coordinate of the ending point
delta x = abs (xs - xe)
delta y = abs (ys - ye)
min = min (delta x, delta y)
max = max (delta x, delta y)

I/O Port 23C2h, Index 0, Control Register 1, Bresenham Line

BITS	NAME	LOGIC	NOTES
11:9	Drawing Mode	100	Bresenham Line
8	X Direction	0	If xs is $\leq$ xe X Direction is Positive
		1	If xs > xe X Direction is Negative
7	Y Direction	0	If ys is $\leq$ ye Y Direction is Positive
		1	If ys > ye Y Direction is Negative
6	Major	0	If delta x $\geq$ delta y (X Major)
		1	If delta x < delta y (Y Major)
5	Source Select	0	Screen Memory
4:3	Source Format	10	Fixed Color
2	Pattern Enable	0	Not Used
1	Destination Select	0	Screen Memory
0	Last Pixel Off	0	Pixel ON
		1	Pixel OFF

12.16 REGISTER BLOCK INDEX, INDEX Fh

All register blocks have an Index Fh that can be used to switch the block or index. Normally, to change a register block or index requires the user to write to I/O Port 23C0h with the values of the register block or index desired. To speed up block switching or to change the register index, Index F can be used instead.

BIT	FUNCTION
15:12	1111 (Index)
11:8	Register Index
7:0	Register Block Pointer
* For 16-bit color.	

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13.0 EXTENDED REGISTER ACCESS

All of the WD90C33 enhanced functions are controlled by one or more extended registers, most of which are above and beyond standard VGA registers.

Enhanced functions are controlled by indexed register blocks. Each indexed register block can contain up to sixteen 12-bit indexed registers. The 4-bit register index is written, along with the 12-bit data field, to form a 16-bit word.

Access to VGA-type registers is described in Section 5. This section only describes the access to indexed register blocks.

13.1 ACCESSING INDEXED REGISTERS

To write to one or more indexed registers within any register block, that register block must first be selected by loading its address into the Register Block Pointer field of the Index Control register. This causes the selected register block to appear at the Register Access port.

A 16-bit word is then written to the Register Access port. The four high-order bits specify the Index of the individual register being written, while the 12 low-order bits are the data to be written. Additional registers within the same register block may then be written without re-selecting that register block.

To read one or more indexed registers within a register block, the address of that register block is written to the Register Block Pointer Field, bits 7:0 of the Index Control Register at Port 23C0h and the desired starting register to be read within the block is written to the Register Index Field, bits 11:8 of this register. Both fields are set with the same 16-bit write. This causes the selected register to appear at the Register Access Port located at 23C2h.

A 16-bit word is then read from the Register Access Port. When reading an indexed register, the value returned contains the index of the register in the four high-order bits.

If the Auto-Increment Disable bit in the Index Control register is reset, consecutive reads to the Register Access Port will return consecutively

indexed registers within the same register block. Registers are read in ascending order through register F (the 16th register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Addressing a non-existent register results in zeros being returned in the 12-bit data field.

If the Auto-Increment Disable bit is set, consecutive reads return the same indexed register.

I/O PORT	BITS	NAME
23C0	---	Index Control
	15:14	Reserved
	13	Invalid Register Block (RO)
	12	Autoincrement Disable
	11:8	Register Index
	7:0	Register Block Pointer
23C2	15:0	Register Access Port
23C4	15:0	Host Bit Block Transfer (HBLT) Port 0
23C6	15:0	Host Bit Block Transfer (HBLT) Port 1
23C8	13:0	K1 (Line Draw Constant 1)
23CA	13:0	K2 (Line Draw Constant 2)
23CC	13:0	ET (Line Draw Error Term)
23CE	10:0	Command Buffer and Interrupt

TABLE 13-1 DIRECT I/O PORT ADDRESSING

13.2 INDEX CONTROL REGISTER PORT 23C0h

Except for bit 13 which is a read only, the Index Control register is a read/write register which controls reads and writes to indexed registers blocks. Refer to Table 13-1.

Bits (15:14)

Reserved

Bit 13 - Invalid Register Block (Read Only).

0 = Currently addressed register block exists on this device.

1 = Currently addressed register block does not exist on this device.

Bit 12 - Auto-Increment Disable.

0 = Consecutive reads return consecutive indexed registers.

1 = Consecutive reads return the same indexed register.

Bits (11:8) - Register Index

The index of the desired starting register to be read within a block is written to these bits. When read, these bits return the index of the next register to be read.

Bits (7:0) - Register Block Pointer

To read one or more indexed registers within a register block, the address of that register block is written to this field.

POINTER	REGISTER ACCESS PORT ACCESSES
00	System Control Registers
01	Drawing Engine Register
02	Hardware Cursor Registers
03	Drawing Engine Register

TABLE 13-2 REGISTER BLOCK MAP

13.3 INTERRUPT STATUS REGISTER, SYSTEM CONTROL REGISTERS BLOCK - INDEX 0

Interrupt status information is provided by the Interrupt Status register in the System Control Register block. This register returns information as to which part of the WD90C33 caused an interrupt.

Reading this register does not reset any interrupts. Resetting of each interrupt is handled independently.

Unassigned interrupts are returned as zeroes.

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BITS	FUNCTION
15:12	0000 (Index)
11	Interrupt 10 Active
⇓	⇓
8	Interrupt 7 Active
7	High when at least one of interrupts 10 through 7 is active.
6	Interrupt 6 Active
⇓	⇓
1	Interrupt 1 Active
0	Any Interrupt is Active

13.3.1 Global Interrupt Map

INTERRUPT	MEANING
1	VGA interrupt
2	BITBLT interrupt

13.4 COMMAND BUFFER AND INTERRUPT CONTROL REGISTER

Address 23CE/23CFh

BITS	LOGIC	FUNCTION
15:11	---	Reserved
10	---	Vertical Retrace Interrupt Status (Read Only: Same as 3C2h, Bit 7
	0	Interrupt Cleared
	1	Interrupt Pending
9	---	DE* Not Busy Interrupt Status (Read Only)
	0	Interrupt Cleared
	1	Interrupt Pending
8	---	DE* Not Busy Interrupt Clear (Read/Write)
	0	Clear DE Not Busy Interrupt
	1	Arm for Next DE Not Busy Interrupt
7	---	DE* Busy (w/dynamic Read)
	0 (Read)	Operation from DE Finished
	1 (Read)	Operation from DE in Progress
	0 (Write)	No Effect
	1 (Write)	Abort DE and Dump Command Buffer
6	----	Command Buffer Overflow (Diagnostic Read Only)
	0	Normal Operation
	1	Command Buffer Overflow Occurred Since Last Enable
5	---	Command Buffer Enable (Read/Write)
	0	Command Buffer Disabled
	1	Command Buffer Enabled
4	---	Reserved
3:0	---	Command Buffer Locations Available (Read Only)
	0000	Empty 8 Locations Available
	0001	7 Locations Available
	0010	6 Locations Available
	0011	5 Locations Available
	0100	4 Locations Available
	0101	3 Locations Available
	0110	2 Locations Available
	0111	1 Locations Available
	1000	Full: No Locations Available
* DE refers to Drawing Engine.		

TABLE 13-3 COMMAND BUFFER AND INTERRUPT CONTROL REGISTER

TABLE 13-3 COMMAND BUFFER AND INTERRUPT CONTROL REGISTER

13.4.1 Command Buffer Description

The Command Buffer (I/O Port Register 23CEh) is a First-In First-Out (FIFO) buffer that can hold up to eight Drawing Engine register writes. When the Drawing Engine is busy, the Command Buffer allows the Host to continue sending commands instead of waiting until the Drawing Engine is finished. When the Drawing Engine completes a current operation, the contents of the Command Buffer are loaded into the Drawing Engine on a first-in first-out basis until the Command Buffer is empty or another command begins.

The Command Buffer stores only Drawing Engine writes. The Hardware Cursor and standard VGA writes do not go through the Command Buffer.

Buffered registers include:

- 23C2h Block 1 Index 0 through E
- 23C2h Block 3 Index 0 through E
- 23C8h
- 23CAh
- 23CCh

Registers 23C0h or 23C2h Index F set the block and index. These registers are buffered as part of the address for each write. Therefore, these registers do not use Command Buffer locations.

13.4.2 Command Buffer Operation

The Command Buffer is enabled by setting I/O Port Register 23CEh, bit 5 to 1. It should be left in the enabled state at all times.

Some operations can take the Drawing Engine a long time to execute, so the software should check the Command Buffer Locations Available bits before writing commands (refer to Table 13-3). The software should poll the Locations Available bits until there are enough locations to hold the Drawing Engine writes.

If the Command Buffer is written to when it is full, the information is not stored and the overflow bit (23CEh, bit 6) is set to 1. This bit can be read to determine the Command Buffer status, and is cleared by disabling the Command Buffer (23CEh, bit 5 is set to 0).

When the Command Buffer is disabled, the Locations Available bits follow the Drawing Engine Busy, and can be polled to determine if a write operation can be performed. Then, if the Buffered registers are written to, the Locations Available status indicates empty (0000) until the Drawing Engine operation starts. The status then snaps to full (1000). When the Drawing Engine finishes its operation, the Command Buffer Locations Available status returns to empty and another write operation can be performed.

The following program provides an example of Command Buffer initialization and use.

Initialization T-52-33-45

```
        OUT   23CEh,0020  ; enable command
                          ; buffer
```

Poll For Command Using Three Writes

```
loop:   IN    ax,23CEh
        AND   ax,000Fh    ; locations available
                          ; mask
        CMP   ax,5        ; locations needed -
                          ; 5 = (8-3)
        JG    loop        ; buffer full keep
                          ;polling
        OUT   23C2h,6003  ; new Dimension X
        OUT   23C2h,7002  ; new Dimension Y
        OUT   23C2,0200   ; new BITBLT
                          ; command
        RET               ; on to next task
```

14.0 APPLICATION AND PROGRAMMING NOTES

T-52-33-45

14.1 USE OF THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE

The hardware cursor, while not specifically designed for hi-color mode operation, can still be used with certain limitations in that mode.

The hardware cursor is unaware of the existence of hi-color mode but can still be used by specifying two adjacent 2-bit pixel codes for each high-color cursor pixel. A transparent hi-color pixel would be specified using two adjacent transparency codes (1010), while a "color" hi-color pixel would usually be specified using adjacent primary and secondary color codes, such as 0100. The desired 16-bit cursor color would then be split between the 8-bit primary and 8-bit secondary color registers. Inversion is also available as 1111 but the results might not be visually desirable.

This limits the effective maximum cursor width in hi-color mode to 32 pixels. Further, the cursor origin and position are defined in terms of 8-bit, not the displayed 16-bit, pixels. Therefore, these values should be horizontal multiples of two.

Secondary and auxiliary color registers may be used to create additional cursor colors by mixing cursor codes within a 16-bit pixel region. It is important to keep in mind the effects of inversion in systems that use one bit to switch between false color and hi-color modes on a pixel-by-pixel basis.

14.2 BITBLT IN VGA MODES 4, 5, AND 6

VGA modes 4, 5 and 6 are partially supported by the WD90C33. Since these modes are not commonly used in Windows, the additional hardware required to support the even/odd scan line offset technique employed in these modes is not supported.

However, a BITBLT operation in these VGA modes can often be broken up into two or three BLT operations, each of which operates on a contiguous area of memory.

When the vertical offset between source and destination is an even number of rows, the desired operation can be broken into two BITBLTs, one for the even rows and one for the odd rows. This requires careful consideration of the register parameters, especially the BITBLT Dimension Y register.

Where the offset is an odd number of rows, it may still be possible to break up the operation into only two BITBLTs, provided there is no overlap between the source and destination regions. This is because information is being swapped between the even and odd scan line regions.

Where source and destination do overlap, it may be possible to use a scratch space in off-screen memory and break up the operation into three BITBLTs.

Another possibility is to break up a BITBLT into a series of one-line high operations that can be referred to as Line-BITBLTS. In this manner, a BITBLT may be simulated by the driver as a series of Line-BITBLTs.

14.3 BITBLT OPERATIONS IN TEXT MODE

BITBLT acceleration is available in VGA Text Modes. Text Mode BITBLTs generally consist of moving only character and attribute data (in maps 0 and 1), while leaving the font data (in maps 2 and 3) alone. The BITBLT mask is set to prevent update to those maps. For this reason, Planar (not Packed) Mode must be used. Similarly, the BITBLT mask can be set to move only character data, or only font data.

Each display memory location consists of four bytes: one character, one attribute and two font plane bytes that are not part of the character but happen to fall in the same location as the character, but on maps 2 and 3. In planar mode, this is a space of eight pixels. Therefore, the source and destination of a character BLT must be multiples of eight. The X dimension is the number of character columns to be copied times eight but the Y dimension is simply the unmultiplied number of character rows. The row pitch is set to the number of characters per row times eight.

14.4 USE OF BITBLT IN 16-BIT PER COLOR MODE

The BITBLT hardware can be used in 16-bit per color hi-color mode with a few changes and a few limitations.

Hi-color BITBLTs should be performed in packed mode, remembering that each hi-color pixel takes up two adjacent normal packed pixels. The BITBLT Source and Destination registers should point to the first byte of the respective regions. Generally, the values in these register pairs are double the corresponding values for 256-color mode.

In a right-to-left BITBLT in hi-color mode, the source and destination values must point to the second byte of each pixel.

The BITBLT dimensions are twice the number of pixel columns, but the correct number of pixel rows. The Row Pitch register contains eight times the number of bytes between rows on the screen. Linear source and destination operate normally.

Monochrome to color expansion or plane masking is not generally usable. Raster operations are available, but often produce undesired results. Similarly, color transparency is seldom usable.

Pattern fills are available, however, the effective pattern is only 4 by 8 pixels. This may be usable where an 8 by 8 pattern is identical in the left and right halves.

Filled rectangles are available in two ways. First, where the desired fill color is the same in the high and low bytes (generally meaning all black or all white), rectangle fill can be used normally.

In the more general case of filling a rectangle with an arbitrary 16-bit color, the host should create a 4 by 8 pattern of the fill color and use pattern fills to create the rectangle.

Host I/O BITBLTs can operate normally be treating each 16-bit hi-color pixel as two adjacent, aligned 8-bit packed mode pixels.

Care should be used when implementing the use of one of the 16 bits in a hi-color pixel as a switch between false color and hi-color, since no mask exists to protect this flag bit during operations.

14.5 USE OF BITBLT FOR ARBITRARY SIZED PATTERNS

While the BITBLT hardware specifically accelerates 8 by 8 patterns, patterns of arbitrary size can be accelerated by use of the BITBLT, although to a lesser degree.

To copy an arbitrary size pattern to a destination region, the pattern should be stored in non-visible memory as a rectangular region, not a linear strip. With destination update enabled, one copy of the pattern should be BITBLTed to the top-left corner of the destination. The BITBLT source is then set to point to the pattern now in the destination region.

A series of BITBLTs are then performed, each doubling the width of the patterned area, simply by adjusting the X Dimensions register. (The last of this series of BITBLTs just fill out the destination region.)

A new series of BITBLTs is then performed, taking the horizontally complete pattern and doubling it in height each time. The destination update should be turned off, and the destination must be set for each new BITBLT. The final BITBLT will probably not be a double of the previous one since it just fills out the region.

14.6 PATTERNS BUILT ON-SCREEN

Normally, a pattern to be used in BITBLT is stored in a non-visible portion of display memory. This requires an aligned strip of 32 or 64 bytes to be available.

When this is not available, it may still be possible to perform a pattern BITBLT by placing the pattern in the last line of the destination region. This can be done if the raster operation is a source copy or source inversion, and if the destination region can accommodate the specified aligned strip on a single line. This technique is possible because each row of the pattern is read at the beginning of the row in which it is used, and the pattern is not overwritten until it after it has been read for the last time.

Where a full strip is unavailable, the destination can be broken up into a series of line-BITBLTs, with a one line pattern, requiring only 4 or 8

aligned bytes, placed on each destination line before the BITBLT is started for that line. This method is substantially slower than other pattern BITBLTs.

A possible alternative is to write the pattern in a visible portion of memory, first saving the underlying area and restoring it after the BITBLT. This temporary usage of a visible region might be visible to the user. This might be reduced by using the last line of the destination and saving and restoring only those regions that overhang the destination.

14.7 USE OF PATTERNS IN TEXT MODE

Patterns may be in text mode to quickly set character and/or attribute bytes in a rectangular area to a common value. A pattern space must be created containing eight consecutive copies of the four-byte area consisting of the character, the attribute and two Font Map bytes, all aligned to a 64-pixel boundary. The BITBLT map mask is then used to protect the font maps. This pattern should be created in off-screen memory.

If an off-screen pattern space is not available, one may be created on screen by loading an aligned group of eight character/attribute pairs within the destination area, then pointing to that as the pattern source.

If the first character of the destination space happens to be on an 8-byte boundary (such as the conventional top of screen) then, as long as the destination is at least eight characters wide, only the first character/attribute pair must be loaded, and the BITBLT operation creates its own pattern as it goes along. This also works if the destination is less than eight characters wide, but is still wider than it is high.

If this is not possible, then the operation can be performed one character row at a time, loading the first character of each row to be used as an on-screen pattern.

Filled rectangles have a very limited application in text mode, but could be used to clear out a section of a font map or to set a section of a character or attribute map to all zeroes or all ones. Different values are not easily set in this manner because, in order to protect the font maps, planar mode, rather than packed mode, must be used.

14.8 SUPPORT FOR KANJI CHARACTERS

The BITBLT hardware can efficiently support generation of Kanji characters. The common implementation of Kanji characters calls for a character box of 28 by 28 pixels, with five possible scoring lines for each character box.

Kanji characters are best drawn in two passes. The first pass draws the characters while erasing any old ones. The second pass adds the score lines.

The Kanji font should be stored in non-visible display memory. Since the font is monochrome, multiple characters can be stored one per plane, one under the other. The color compare registers are used to switch between banks of characters stored on different planes.

A group of 32 special characters is generated along with the font, consisting of all possible combinations of scoring lines.

The dimension registers are loaded with the size of the character box. Foreground and background colors are set as desired. Destination update and quick BITBLTs are enabled.

For each character row, the source and destination registers are set to the beginning of the row, and monochrome expansion is enabled. A series of quick BITBLTs is performed, one per character, by loading the source address of each desired character. If a font-plane change is required before any character, it is done before loading the source registers, since these start the BITBLT automatically.

After the character row is complete, the destination registers are reset to the beginning of the row. Monochrome transparency is enabled, and a second pass is done over the character drawn to add score lines as needed, one special score-line character per Kanji character.

Where a Kanji character requires no score lines, either a BITBLT of a special "blank" score-line character is performed, or the destination registers may be updated to skip the position. The driver may add additional intelligence to skip entire character rows or parts where score lines are not required.

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15.0 SIGNATURE ANALYZER

A signature analyzer is designed for use in the WD90C33. The primary purpose of the signature analyzer is to aid in IC test and board level test. The signature analyzer allows the video output path to be included in diagnostics. Signature analysis is a method of compressing large amounts of data to be compared. Each video frame (video data and mode dependent) has a unique signature capable of detecting single bit errors.

15.1 DESCRIPTION

The basis of the signature analyzer is a Linear Feedback Shift Register (LFSR). The inputs to the LFSR tap onto the VID[7:0] output of the IC. The signal path of the video outputs is not modified by adding the signature analyzer. A block diagram is shown below. The primary variables in designing a signature analyzer are length of the shift register and the feedback terms to be used. The length will affect the probability of masking an error. The chance of masking an error is approximately 1/2n, where n is the length of the shift register. A 16-bit signature register is used on the WD90C33. Selection of an optimal feedback polynomial will depend on the type of errors expected. The CRC-CCITT polynomial (x16 + x12 + x5 +1) has been implemented on the WD90C33. It was modified for multiple inputs as shown in the block diagram.

15.2 OPERATION

The signature analyzer is designed to collect signature of the VID[7:0] outputs over one vertical frame. The signal path of the VID[7:0] has not been altered. The signature analyzer register (LFSR) is enabled at the falling edge of the internal VSYNC (before polarity selection) if the start bit is high. The following rising edge of the VSYNC signal will disable the LFSR. In the case of interlaced operation, signature is collected from the beginning of the even field to the end of the odd field. The signature analyzer contains a 4-bit control register PR19 (address 3?5.3F). Power-up-reset clears this register to 00H. This register has both read and write locks. The read lock originates from PR10 Bits 7 and 3. The write lock originates from PR10 Bits 2 through 0. PR10 also serves as the lock for other registers.

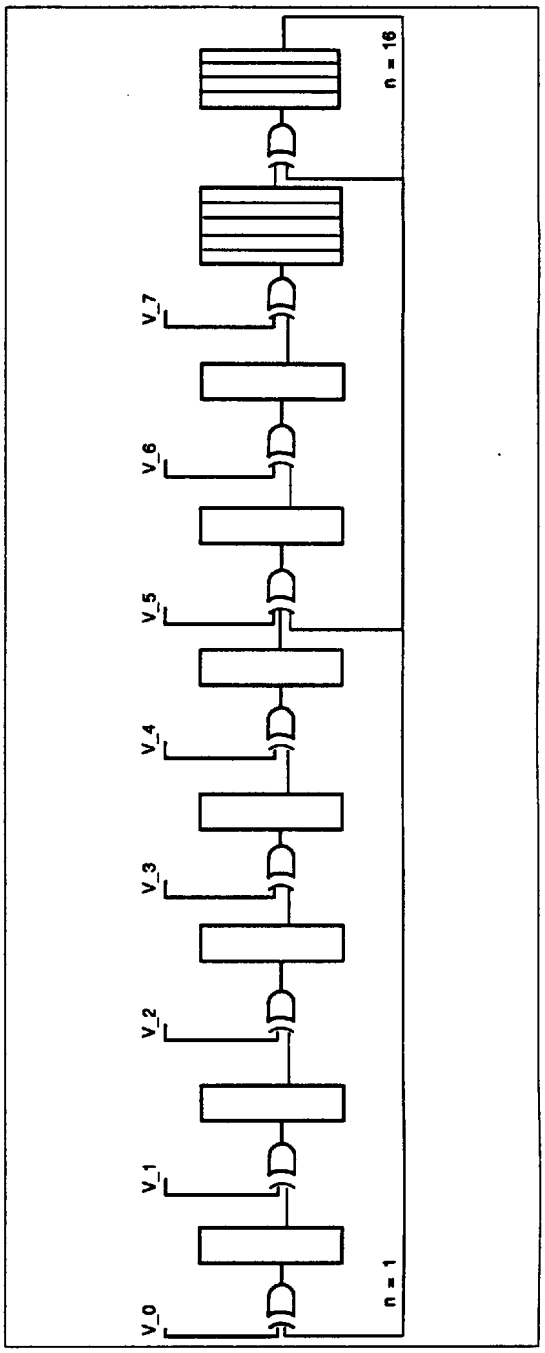

FIGURE 15-1 LINEAR FEEDBACK SHIFT REGISTER

BIT	FUNCTION	READ/ WRITE	DESCRIPTION
0	Start/Status	R/W	Writing a 1 to this bit position enables the signature analyzer to collect a signature at the falling edge of the next vertical sync pulse. This bit may be read to check status if the read lock is disabled. For status: 1 = Busy, 0 = Finished or not enabled.
1	Clear	R/W	Writing a 0 to this bit position preloads the Signal Analyzer Register (LFSR) with 0001h. This bit must be set to operate the signature analyzer. For operation: 1 = Normal operation, 0 = Preload LSFR.
2	Disable Video Input	R/W	This bit is used in a self test mode. A fixed signature will be generated for any given mode (independent of video memory data). To enable self-test: 1= Disable video inputs, 0 = Enable video inputs.
3	Lock Read Port	R/W	This bit must be set to read the video signature and status. To read: 1 = Enable read of LSFR (address 3?5h, Index 20h and 21h), 0 = Disable reads of LFSR.

TABLE 15-1 CONTROL REGISTER PR19

The following programming procedure summarizes the sequence that will setup, check, and read a video signal signature.

1. Load 85h -> 3?5.29h; Releases the Control Register (PR10) read and write lock
2. Load 00h -> 3?5.3Fh; Clears the signature analyzer
3. Load 03h -> 3?5.3Fh; Enables the signature analyzer to collect data
4. Read 3?5.3Fh; Checks status for busy:
   if LSB = 1, repeat step 4
   if LSB = 0, signature is collected, proceed to step 5.
5. Load 0Ah -> 3?5.3Fh; Enables signature analyzer to read port
6. Read 3?5.20h; Reads low byte of signature
7. Read 3?5.21h; Reads high byte of signature
8. Load 00h -> 3?5.3Fh; Clears signature analyzer and locks read port

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16.0 I/O MAPPING

The section provides the following information:

- A description of WD90C33 I/O Mapping
- A list of I/O Mapping Groups
- An I/O Mapping Group Diagram

16.1 DESCRIPTION

The I/O Mapping allows the WD90C33 to enter a test mode where all of its pins are divided into groups with inputs and outputs. The path for each group goes from the input pin(s), through the WD90C33, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table 16-1 lists each group (path) with its corresponding input and output pins.

The WD90C33 must meet the following four requirements in order to enter the I/O Mapping test mode.

- $\overline{\text{MEMR}}$ is low
- $\overline{\text{IOR}}$ is low
- CNF(2) is high (MD2 is pulled high)
- RESET is active high then goes low

If both $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in AT compatible computers and a reserved condition in the PS/2 compatible computers. AMD2 high ensures that WD90C33 is in AT mode.

Reset controls a transparent latch as shown in Figure 16-1. Reset can be dropped low to latch the test mode. All the bidirectional pins are forced to input mode when in the test mode.

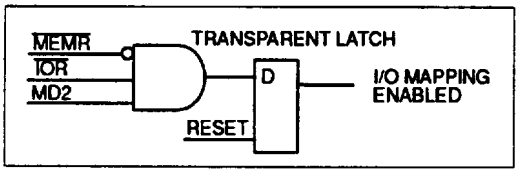

FIGURE 16-1 ENABLING I/O MAPPING ON THE WD90C24

Figure 16-2 provides a diagram of the I/O mapping groups (paths).

16.2 PIN GROUPING

The pin grouping listed in Table 16-1 was selected to minimize routing overhead of I/O pin mapping. Multiple input pins in a row are ORed together to the output shown in the following table. The input column lists the input pin number(s) along with the signal name(s). The output column lists the output pin number along with the signal names.

NOTE

Power and ground pins and pins with no connection (a total of 45 pins) are not included in I/O Mapping.

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
1	$\overline{\text{EBROM}}$	4, 200, 208	MD14, MD21, MD17
2	$\overline{\text{WE1}}$	11, 201, 206	MD8, MD20, MD16
12	$\overline{\text{WE0}}$	5, 8	MD13, MD11
25	MA8	45, 47, 82	ALE, $\overline{\text{ROM16}}$, A21
26	MA7	63, 76, 81	A5, A16, A20
27	MA6	62, 78, 83	A4, A18, A22
28	MA5	57, 79, 84	$\overline{\text{BHE}}$, A19, A23
29	MA4	21, 61, 77	MD1, A3, A17
31	MA3	17, 22, 60	MD4, MD0, A2
32	MA2	16, 20, 56	MD5, MD2, A1

TABLE 16-1 I/O MAPPING GROUPS

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INPUT		OUTPUT	
PIN	NAME	PIN	NAME
33	MA1	10, 14, 19	MD9, MD7, MD3
34	MA0	9, 23, 58	MD10, $\overline{CAS}$ A0
35	$\overline{OE}$	39, 50	$\overline{IOW}$, $\overline{IOR}$
37	$\overline{0WS}$	43, 64, 67, 72	LCLK, A6, A8, A13
40	$\overline{EBROM}$	65, 68, 70, 73	A7, A9, A11, A14
44	IRQ	39, 41, 54, 55	$\overline{IOW}$, $\overline{IOCS16}$, SYSRESET, $\overline{BE3}$
46	IOCHRDY	38, 51	EMEM, $\overline{MRD}$
49	$\overline{MEMCS16}$	52, 69, 71, 74	$\overline{MWR}$, A10, A12, A15
135	VSYNC	86, 88, 90, 92	A24, A26, A28, A30
136	HSYNC	87, 89, 91, 93	A25, A27, A29, A31
147	BA1	137, 139, 142, 144	BD0, BD2, BD4, BD6
148	BA0	138, 140, 143, 145	BD1, BD3, BD5, BD7

TABLE 16-1 I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
149	$\overline{WPLT}$	95, 100, 105, 110	D31, D27, D23, D19
150	$\overline{RPLT}$	97, 102, 107, 112	D29, D25, D21, D17
161	PCLK	178	VCLK0
162	$\overline{BLNK}$	96, 101, 106, 111	D30. D26, D22, D18
163	VID0	98, 103, 108, 179	D28, D24, D20, VCLK1
164	VID1	113, 118, 133, 180	D16, D12, D0, VCLK2
165	VID2	115, 120, 130, 182	D15, D11, D3, EXPCLK
166	VID3	116, 121, 126, 152	D14, D10, D6, EXVID
168	VID4	117, 122, 151	D13, D9, MDET
169	VID5	176	MCLK
170	VID7	123, 127, 131, 187	D8, D5, D2, MD31
171	VID7	125, 128, 132, 188	D7, D4, D1, MD30

TABLE 16-1 I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
183	USR1	189, 193, 198	MD29, MD26, MD23
184	USR0	190, 194, 204	MD28, MD25, MD18

TABLE 16-1 I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
186	$\overline{WE3}$	3, 192, 195	MD15, MD27, MD24
196	$\overline{WE2}$	199	MD22
207	$\overline{RAS}$	6, 15, 203	MD12, MD6, MD19

TABLE 16-1 I/O MAPPING GROUPS

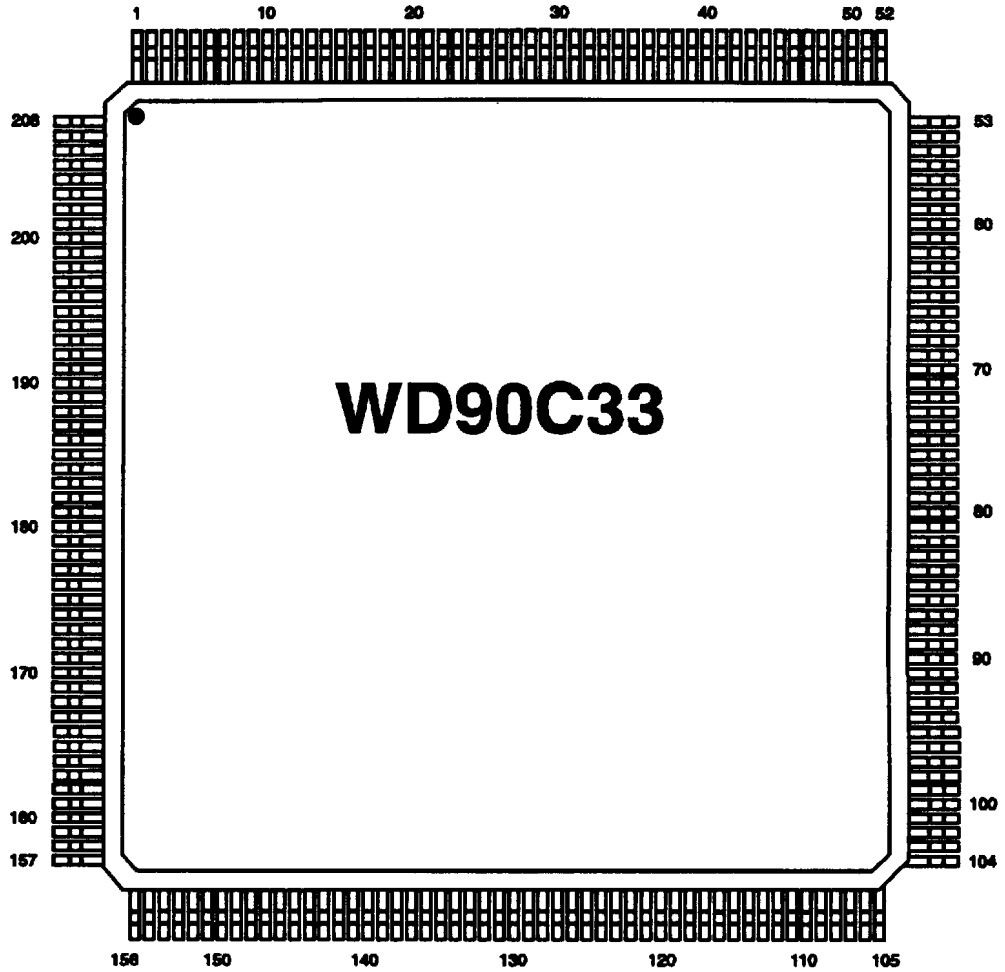

FIGURE 16-2 WD90C33 PIN SCAN MAP FOR 208-PIN PACKAGE

17.0 DC ELECTRICAL SPECIFICATIONS

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17.1 MAXIMUM RATINGS

Voltage on any pin with respect to VSS ..... -0.3 to 7 Volts

Ambient Temperature Under Bias ..... 0°C to 70°C, 32°F to 158°F

Storage Temperature ..... -40°C to 125°C, -40°F to 257°F

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

17.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range ..... 0°C to 70°C, 32°F to 158°F

Power Supply Voltage ..... 4.75 to 5.25 Volts

Power Dissipation ..... 140 mA

17.3 DC CHARACTERISTICS

With the following exceptions the WD90C33 outputs have 4.0 mA maximum source and sink capability.

- IRQ, IOCHRDY, 0WS, MEMCS16, IOCS16 = 24 mA sink.
- PCLK, VID7:0, BLANK = 10 mA source/sink.
- DRAM Interface = 4.0 mA source/sink (RAS, CAS, WE, OE, MA, MD)
- HSYNC, VSYNC, DA15:0 = 6 mA sink.
- ROM16 = 16 mA sink.

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	-0.3	0.8	V	VCC = 5V +/- 5%
V_{IH}	Input High Voltage	2.0	VCC + 0.3	V	VCC = 5V +/- 5%
I_{IL}	Input Low Current	---	+/- 10	µA	VIN = 0.0V
I_{IH}	Input High Current	---	+/- 10	µA	VIN = VCC
V_{OL}	Output Low Voltage	---	0.4	V	IOL = +2.0 mA
V_{OH}	Output High Voltage	2.4	---	V	IOH = -2.0 mA
I_{OZ}	High Impedance Leakage Current	-10.0	10.0	µA	0V < VOUT < VCC
C_{IN}	Input Capacitance	---	10	pF	FC = 1 MHz
C_{OUT}	Output Capacitance	---	10	pF	FC = 1 MHz
$C_{I/O}$	I/O Pin Capacitance	---	12	pF	FC = 1 MHz

TABLE 17-1 DC CHARACTERISTICS

18.0 AC TIMING CHARACTERISTICS

18.1 INTRODUCTION

The following information applies to all of the parameters presented in this section:

- All units are in nanoseconds unless otherwise specified.
- CL = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the number in column 1 of the same table.
- The numbers in the first column of each table are used to locate parameters on the associated diagram.

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	RESET Pulse Width	10t	-	t = 1/MCLK (For configuration at Power-On and Reset)
2	MD setup to RESET Low	50	-	
3	MD Hold from RESET Low	30	-	
4	RESET Low to First $\overline{IOW}$	10t	-	

TABLE 18-1 RESET TIMING

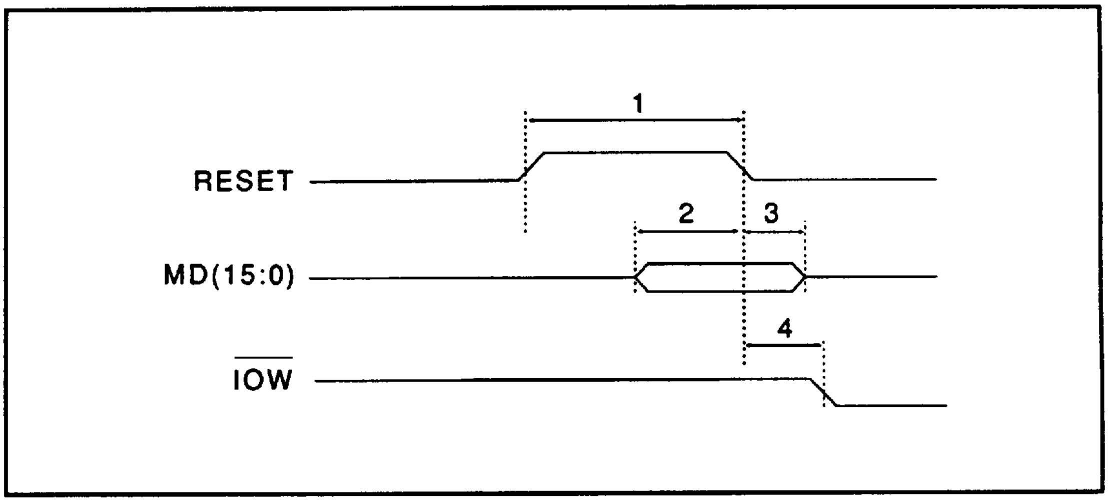

FIGURE 18-1 RESET TIMING

NO. IN DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1[1]	VCLK Clock Period	12.5	72	
2	VCLK High	5	-	At 1/2 VDD
3	VCLK Low	5	-	At 1/2 VDD
4[1]	Clock Rise Time	-	2	1V - (VDD - 1V)
5[1]	Clock Fall Time	-	2	1V - (VDD - 1V)
6	VCLK to PCLK Delay	8	20	
7a	VCLK to HSYNC Delay	8	25	
7b	VCLK to VSYNC Delay	8	25	
7c	VCLK to $\overline{\text{BLNK}}$ Delay	8	20	
7d	VCLK to VID[7:0] Delay	8	20	50 MHz maximum
8[2]	MCLK Clock Period	20	30	33.3 MHz minimum
9	MCLK High	8		At 1/2 VDD
10	MCLK Low	8		At 1/2 VDD
11	VID[7:0] Setup to PCLK	3		
12	VID[7:0] Hold from PCLK	3		

NOTES:

1. Applies to VCLK and MCLK.
2. VCLK0 and MCLK use CMOS level input buffers. V(IL) max = 1.5V, V(IH) min = VDD - 1.5V

TABLE 18-2 CLOCK TIMING

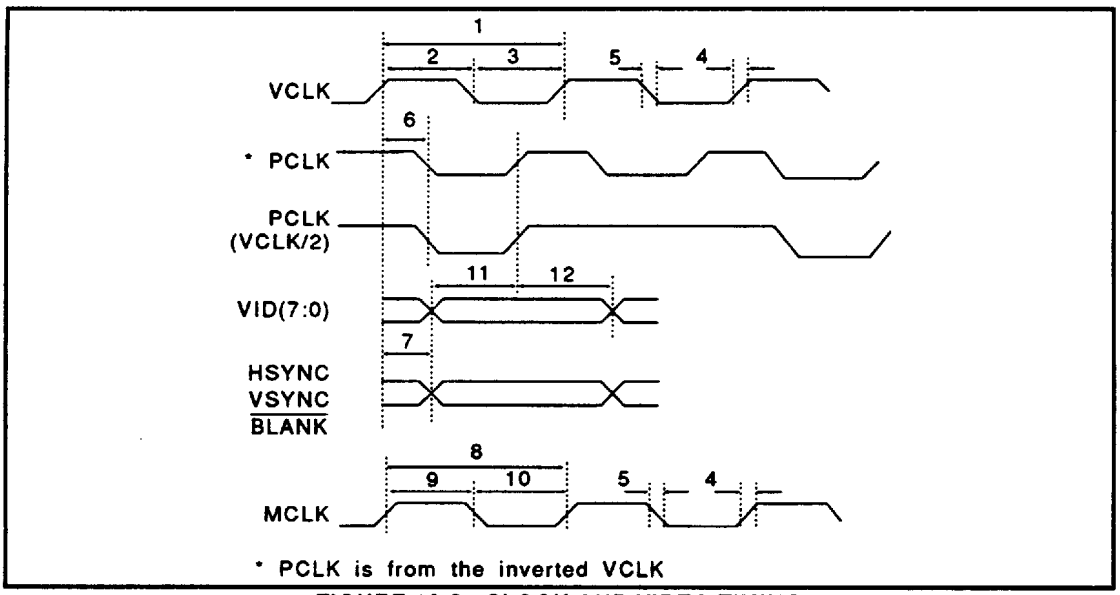

FIGURE 18-2 CLOCK AND VIDEO TIMING

NO.ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	EMEM Setup to $\overline{MRD}$, $\overline{MWR}$ Low	20	-	
2	EMEM Hold from $\overline{MRD}$, $\overline{MWR}$ High	10	-	At 1/2 VDD
3a	A[23:17] Setup to ALE Low	20	-	At 1/2 VDD
3b	BHE, DA[15:0] Setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ Low	18	-	
4a	A[23:17] Hold from ALE Low	10	-	1V - (VDD - 1V)
4b	DA[15:0] Hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ Low	10	-	
5	$\overline{EIO}$ Setup to $\overline{IOR}$, $\overline{IOW}$ Low	20	-	1V - (VDD - 1V)
6	$\overline{EIO}$ Hold from $\overline{IOR}$, $\overline{IOW}$ High	10	-	
7a	$\overline{EABUF}$ High from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ Low	9	25	
7b	$\overline{EABUF}$ Low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ Low	13.5	35	
7c	$\overline{HTL}$ Low from $\overline{MRD}$ Low	-	25	
8a	$\overline{EABUF}$ Low from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ High	14.5	35	50 MHz maximum
8b	$\overline{EABUF}$ High from $\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ High	8.5	25	33.3 MHz minimum
8c	$\overline{HTL}$ High from $\overline{MRD}$ High	-	25	
9	DIR High from $\overline{IOR}$, $\overline{MRD}$ Low	-	20	At 1/2 VDD
10	DIR Hold from $\overline{IOR}$ and $\overline{MRD}$ High	-	20	At 1/2 VDD
11	DA[15:0] Write Data Setup to $\overline{IOW}$, $\overline{MWR}$ High	20	-	
12a	DA[15:0] Read Data Hold from $\overline{IOR}$ High or $\overline{MRD}$ High	10	-	
12b	DA[15:0] Write Data Hold from $\overline{IOW}$, $\overline{MWR}$ High	10	-	
13	DA[15:0] Read Data Valid after $\overline{IOR}$, Low	-	70	
14	RDY High from $\overline{MRD}$, $\overline{MWR}$ Low	10	2.45 µs	Maximum is standard for VGA modes.
15	Memory Read Data Valid from RDY High	-	40	Note 1
16a	RDY Low from $\overline{MRD}$, $\overline{MWR}$ Low	10	25	CL = 100 pF
16b	RDY Low from $\overline{IOR}$, $\overline{IOW}$ Low	10	25	CL = 100 pF
17a	RDY Tristate from $\overline{MRD}$, $\overline{MWR}$ High	10	25	CL = 100 pF

TABLE 18-3 I/O AND MEMORY READ/WRITE TIMING FOR AT- COMPATIBLE MODE

NO.ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
17b	RDY Tristate from $\overline{IOR}$, $\overline{IOW}$ High	10	25	CL = 100 pF
18	$\overline{EBROM}$ Low from Valid A[23:15]	-	40	
19	$\overline{EBROM}$ Hold from $\overline{MRD}$ High	-	40	
20a	$\overline{WPLT}$ Low from $\overline{IOW}$ Low	-	37	
20b	$\overline{RPLT}$ Low from $\overline{IOR}$ Low	-	30	
21a	$\overline{WPLT}$ High from $\overline{IOW}$ High	9	15	
21b	$\overline{RPLT}$ High from $\overline{IOR}$ High	9	20	
22	$\overline{EBROM}$ Low from $\overline{IOW}$ Low (46E8h Port)	-	1t + 20	
23	$\overline{EBROM}$ High from $\overline{IOW}$ High (46E8h Port)	-	25	
24	VCLK1 Low from $\overline{IOW}$ Low (3C2h Port)	-	1t + 25	
25	VCLK1 High from $\overline{IOW}$ High (3C2h Port)	-	15	
26	A[15:0] Valid to $\overline{IOCS16}$ Low	-	35	CL = 100 pF
27	$\overline{IOCS16}$ Hold from $\overline{IOW}$ High	-	20	CL = 100 pF
28	A[23:17] Valid to $\overline{MEMCS16}$ or $\overline{ROM16}$ LOW	-	41	CL = 100 pF
29	$\overline{MEMCS16}$ Tristate from the Next Active ALE	-	39	CL = 100 pF
30a	$\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ High	2t + 15	-	t = 1/MCLOCK (Note 2)
30b	$\overline{IOR}$, $\overline{IOW}$, $\overline{MRD}$, $\overline{MWR}$ Low	2t	-	t = 1/MCLOCK (Note 3)
30c	ALE Pulse Width	30	-	
31	$\overline{0WS}$ Low from $\overline{IOR}$, $\overline{MWR}$ Low	-	15	CL = 100 pF

NOTES:

1. Value depends on setting of PR31 (3C5h, Index 11h), bits 4:3. t = 1/MCLOCK
   00 = 40 Max
   01 = 40 + 1t Max
   10 = 40 + 2t Max
   11 = 40 - 1t Max
2. The minimum value of (30a) should be the greater of 2t + 15 or (8a + 3b).
3. The minimum value of (30b) should be the greater of 2t or (7b + 11).
4. Numbers in parenthesis are numbers on the diagram.

TABLE 18-3 I/O AND MEMORY READ/WRITE TIMING FOR AT- COMPATIBLE MODE

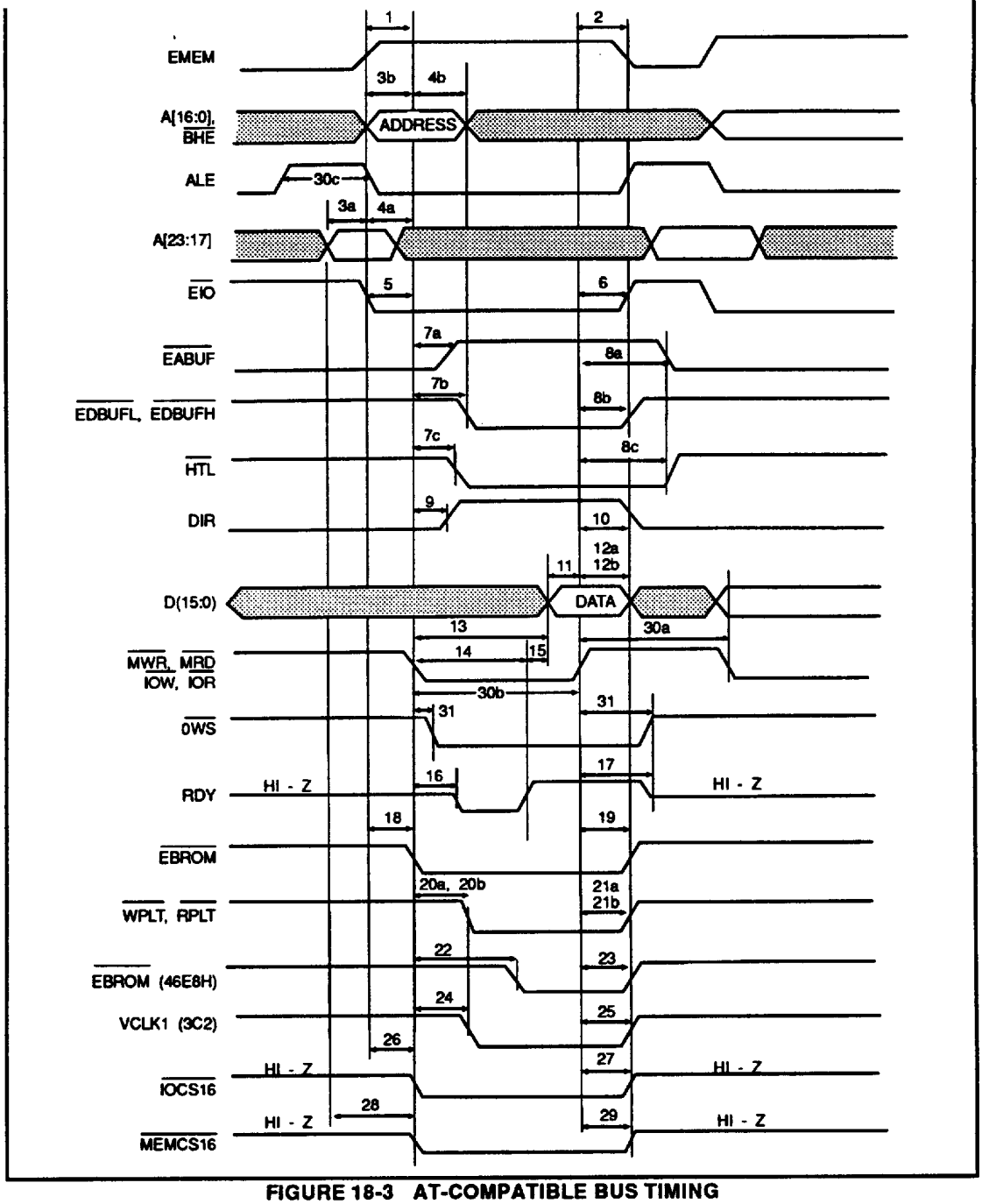

FIGURE 18-3 AT-COMPATIBLE BUS TIMING

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	A[23:0], EMEM, $\overline{BHE}$ Setup to $\overline{CMD}$ Low	20	-	
2	A[23:0], EMEM, $\overline{BHE}$ Hold from $\overline{CMD}$ Low	10	-	
3	$\overline{CDSETUP}$, $\overline{EIO}$, Setup to $\overline{CMD}$ Low	20	-	
4	$\overline{CDSETUP}$, $\overline{EIO}$, Hold from $\overline{CMD}$ Low	15	-	
5	$\overline{STATUS}$ Setup to $\overline{CMD}$ Low	20	-	
6	$\overline{STATUS}$ Hold from $\overline{CMD}$ Low	15	-	
7a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ Low from $\overline{CMD}$ Low	13.5	35	
7b	$\overline{EABUF}$ High from $\overline{CMD}$ Low	9	25	
8a	$\overline{EDBUFH}$, $\overline{EDBUFL}$ High from $\overline{CMD}$ High	8.5	25	
8b	$\overline{EABUF}$ Low from $\overline{CMD}$ High	14.5	35	
9	DIR High (Active) from $\overline{CMD}$ Low	-	20	
10	DIR Low (Inactive) from $\overline{CMD}$ High	-	20	
11	$\overline{CSFB}$ Delay from Valid Address/ Status	-	30	CL = 100 pF
12	$\overline{CSFB}$ Hold from $\overline{CMD}$ High (I/O Cycle)	-	30	CL = 100 pF
13	$\overline{CSFB}$ Hold from Invalid Address (Memory Cycle)	-	30	CL = 100 pF
14	$\overline{CDDS16}$ Delay from Valid Address	-	40	
15	$\overline{CDDS16}$ Hold from Invalid Address	-	30	
16	DA [15:0] Write Data Setup to $\overline{CMD}$ High	20	-	
17	DA [15:0] Write Data Hold After $\overline{CMD}$ High	10	-	
18	DA [15:0] I/O Read Data Valid from $\overline{CMD}$ Low	-	70	
19	RDY High Delay from $\overline{CMD}$ Low	0	2.45 µs	
20	DA [15:0] Memory Read Data Valid from RDY High	-	40	Note 1
21a	$\overline{CMD}$ High (Inactive)	2t + 15		Note 2
21b	$\overline{CMD}$ Low (Active)	2t		Note 3
22	$\overline{RDY}$ Low Delay from Valid Address/ Status	-	30	

TABLE 18-4 I/O AND MEMORY READ/WRITE TIMING FOR MICROCHANNEL- COMPATIBLE MODE

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
23	$\overline{\text{EBROM}}$ Low from Valid Address	-	40	
24	$\overline{\text{EBROM}}$ High from $\overline{\text{CMD}}$ High	-	30	
25	$\overline{\text{WPLT/RPLT}}$ Low from $\overline{\text{CMD}}$ Low	9	20	
26	$\overline{\text{WPLT/RPLT}}$ High from $\overline{\text{CMD}}$ High	9	20	
27	VCLK1 Low from $\overline{\text{CMD}}$ Low (3C2h Port)	-	1t + 30	
28	VCLK1 High from $\overline{\text{IOW}}$ High (3C2h Port)	-	25	

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NOTES:

1. Value depends on setting of PR31 (3C5h, Index 11h), bits 4:3. t = 1/MCLOCK
   00 = 40 Max
   01 = 40 + 1t Max
   10 = 40 + 2t Max
   11 = 40 - 1t Max
2. The minimum value of (21a) should be the greater of 2t + 5 or value (8b + 1).
3. The minimum value of (21b) should be the greater of 2t or value (7b + 16).
4. Numbers in parenthesis are numbers on the diagram.

TABLE 18-4 I/O AND MEMORY READ/WRITE TIMING FOR MICROCHANNEL- COMPATIBLE MODE

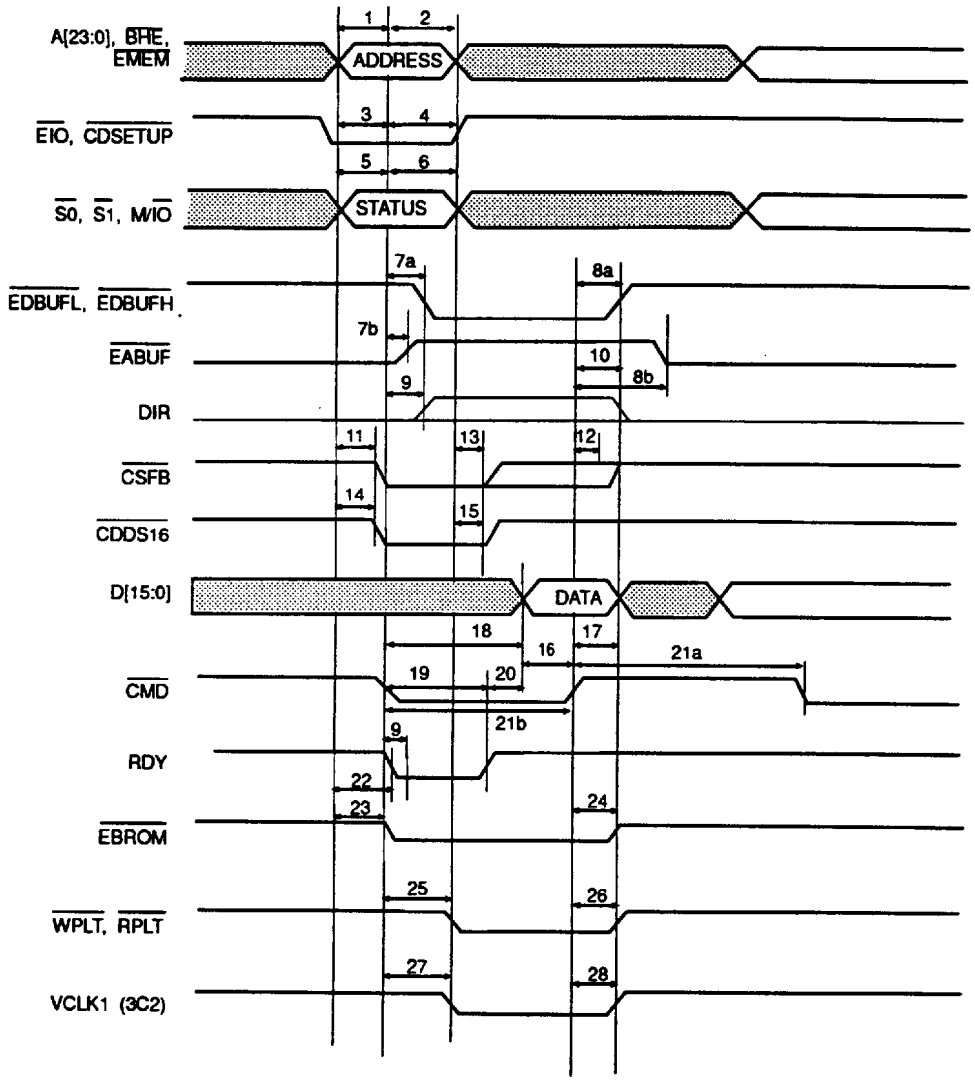

FIGURE 18-4 MICROCHANNEL-COMPATIBLE BUS TIMING

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	$\overline{RAS}$ Cycle Time	6t	-	Note 2, 3
2	$\overline{RAS}$ Pulse Width Low	3.5t - d	-	Note 2, 3, 4
3	$\overline{RAS}$ High Time (Precharge)	2.5t + d	-	Note 2, 3, 4
4	$\overline{RAS}$ Low to $\overline{CAS}$ Low	2.5t - 9	2.5t - d	Note 2, 3, 4
5	$\overline{CAS}$ Cycle Time	2t	-	Note 3
6	$\overline{CAS}$ Pulse Width Low	1t + d	-	Note 2, 3, 4
7	$\overline{CAS}$ High Time (Precharge)	1t - d	-	Note 2, 3, 4
8	Row Address Setup to $\overline{RAS}$ Low	1t - 10	-	Note 3
9	Row Address Hold Time from $\overline{RAS}$ Low	1t	-	Note 3
10	Column Address Setup to $\overline{CAS}$ Low	1t - 10	-	Note 3
11	Column Address Hold from $\overline{CAS}$ Low	1t	-	Note 3
12	Read Data Valid Before $\overline{CAS}$ High	3	-	
13	Read Data Hold After $\overline{CAS}$ High	0	-	
14	Write Data Setup to $\overline{CAS}$ Low	1t - 15	-	Note 3
15	Write Data Hold After $\overline{CAS}$ Low	1t - 5	-	Note 3
16	$\overline{WE}$ Low Setup to $\overline{CAS}$ Low	1t - 5	1t + 5	Note 3
17	$\overline{WE}$ Low Hold After $\overline{CAS}$ High	Same as (16).		Note 5
18	$\overline{OE}$ High Before $\overline{WE}$ Low	2t - 10	-	Note 3
19	$\overline{OE}$ Low After $\overline{WE}$ High	1t - 10	-	Note 3
20	$\overline{CAS}$ High for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	1t - 10	-	Note 3
21	$\overline{RAS}$ Low from $\overline{CAS}$ Low for $\overline{CAS}$ before $\overline{RAS}$ Refresh	1.5t + 10	-	Note 3

NOTES:

1. The timing in this table results from setting PR33 (3C5h, Index 13) to XXX00000b.
2. This timing is adjustable via PR33.
3. For t = 1/MCLK, the maximum MCLK frequency is:

DRAM SPEED	FREQUENCY
80 ns	37.5 MHz
80 ns (faster type)	40.0 MHz
70 ns	44.4 MHz
60 ns	49.5 MHz

4. The "d" indicates a delay of 4 ns to 7 ns.
5. Numbers in parenthesis are numbers on the diagram.
6. Memory write uses fast page early write, while keeping $\overline{OE}$ equal to 1.
   Memory read uses fast page read, while keeping $\overline{OE}$ equal to 1.

TABLE 18-5 DRAM TIMING FOR 256K BY 4 AND 256K BY 16 DRAMS

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	$\overline{RAS}$ Cycle Time	5t	-	Note 2, 3
2	$\overline{RAS}$ Pulse Width Low	3t - 7	-	Note 2, 3
3	$\overline{RAS}$ High Time (Precharge)	2t	-	Note 2, 3
4	$\overline{RAS}$ Low to $\overline{CAS}$ Low	1.5t	1.5t	Note 2, 3
5	$\overline{CAS}$ Cycle Time	2t	2t	Note 3
6	$\overline{CAS}$ Pulse Width Low	1t + 2d	-	Note 2, 3, 4
7	$\overline{CAS}$ High Time (Precharge)	1t - 2d	-	Note 2, 3, 4
8	Row Address Setup to $\overline{RAS}$ Low	1t	-	Note 3
9	Row Address Hold Time from $\overline{RAS}$ Low	0.5t	-	Note 3
10	Column Address Setup to $\overline{CAS}$ Low	1t - 10	-	Note 3
11	Column Address Hold from $\overline{CAS}$ Low	1t	-	Note 3
12	Read Data Valid Before $\overline{CAS}$ High	2	-	
13	Read Data Hold After $\overline{CAS}$ High	0	-	
14	Write Data Setup to $\overline{CAS}$ Low	1t - 15	-	Note 3
15	Write Data Hold After $\overline{CAS}$ Low	1t - 5	-	Note 3
16	$\overline{WE}$ Low Setup to $\overline{CAS}$ Low	1t - 10		Note 3
17	$\overline{WE}$ Low Hold After $\overline{CAS}$ High	Same as (16).		Note 5
18	$\overline{OE}$ High Before $\overline{WE}$ Low	1t + 2	-	Note 3
19	$\overline{OE}$ Low After $\overline{WE}$ High	1t - 16	-	Note 3
20	$\overline{CAS}$ High for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	0.5t	-	Note 3
21	$\overline{RAS}$ Low from $\overline{CAS}$ Low for $\overline{CAS}$ before $\overline{RAS}$ Refresh	1.5t	-	Note 3

NOTES:

1. The timing in this table results from setting PR33 (3C5h, Index 13) to XXX00000b.
2. This timing is adjustable via PR33.
3. For t = 1/MCLK, the maximum MCLK frequency is:

DRAM SPEED	FREQUENCY
80 ns	36 MHz

4. The "d" indicates a delay of 4 ns to 7 ns.
5. Numbers in parenthesis are numbers on the diagram.
6. Memory write uses fast page early write, while keeping $\overline{OE}$ equal to 1.
   Memory read uses fast page read, while keeping $\overline{OE}$ equal to 1.
7. The MCLK edge to $\overline{RAS}$, $\overline{CAS}$, MA[8:0] edge delay may be up to 40 ns.

TABLE 18-6 DRAM TIMING FOR 64K BY 16 DRAMS

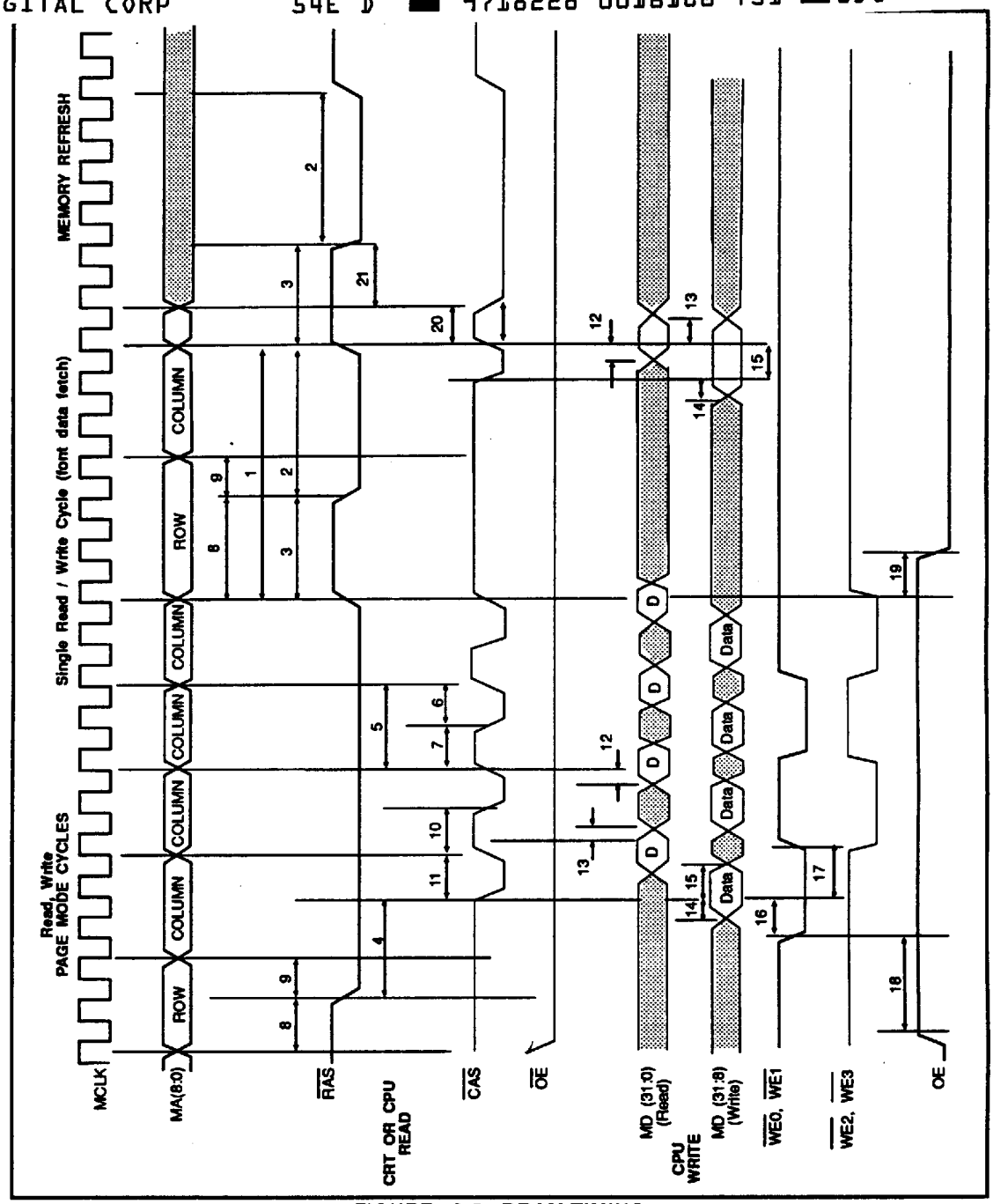

FIGURE 18-5 DRAM TIMING

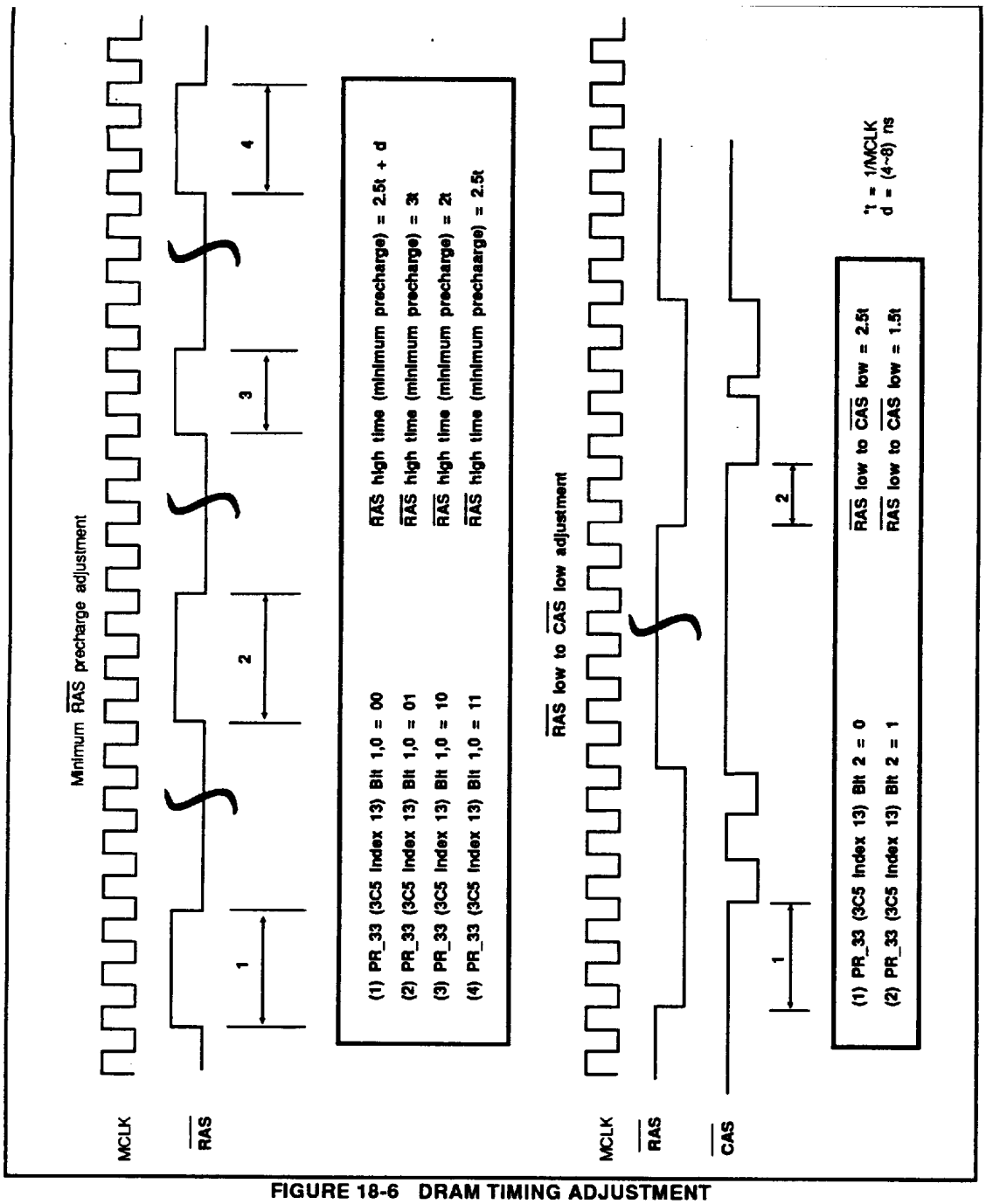

FIGURE 18-6 DRAM TIMING ADJUSTMENT

18.2 DRAM TIMING ADJUSTMENT

For DRAM timing adjustments, the $\overline{RAS}$, $\overline{CAS}$ timing can be adjusted by register PR33 (3C5h, Index 3), bits 4 through 0 (see Figures 18-5 through 18-8).

Tables 18-5 and 18-6 list the parameters (Note 2) that are adjustable via PR33.

For the CAS pulse width adjustment, the CAS cycle time is always equal to 2t (t = 1/MCLK). The delay "d" is 4 to 8 ns. Therefore, PR33, bits 4:3 set the CAS pulse width as follows:

BITS		$\overline{CAS}$ LOW =	$\overline{CAS}$ HIGH =
4	3		
0	0	1t + d	1t - d
0	1	1t + 2d	1t - 2d
1	X	1.5t	0.5t

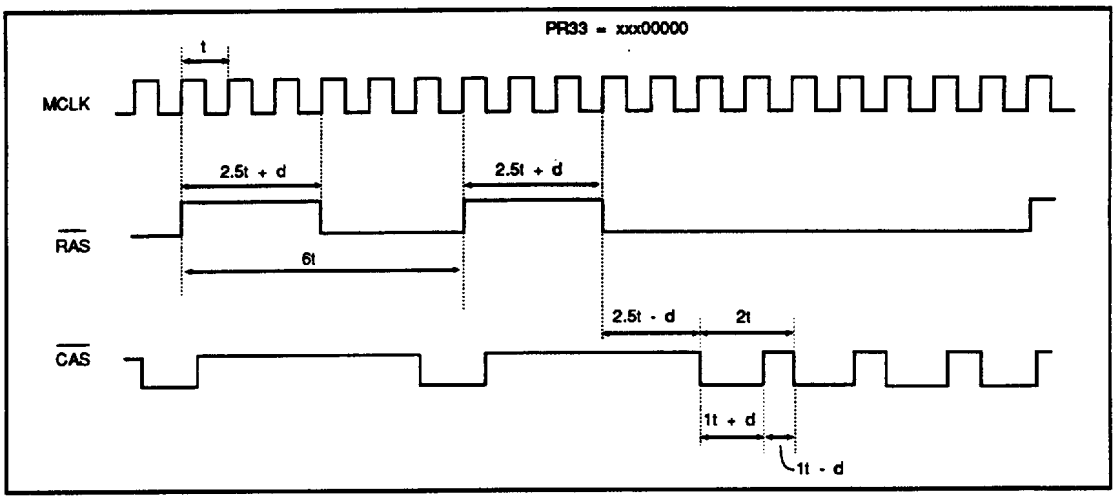

FIGURE 18-7 DRAM TIMING FOR 256K BY 4 DRAM

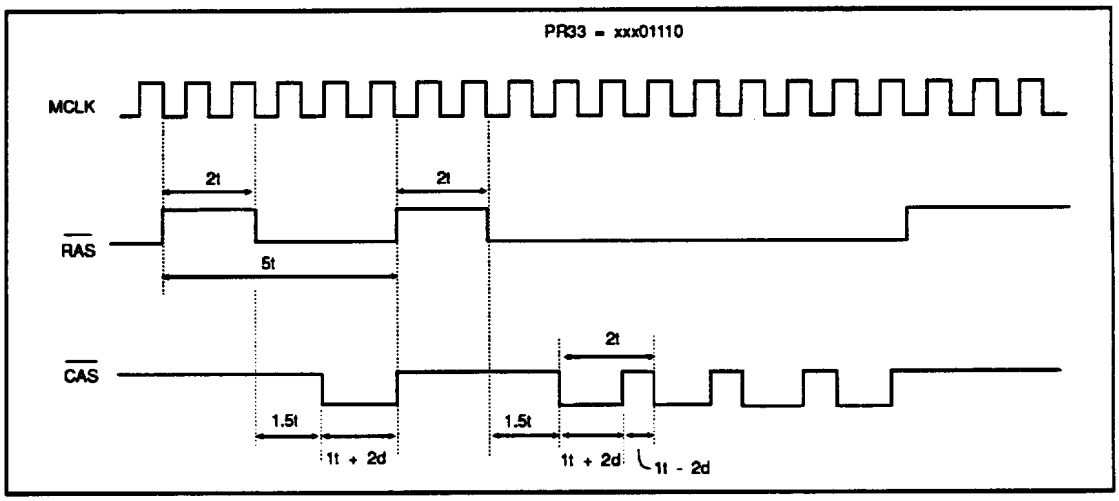

FIGURE 18-8 DRAM TIMING FOR 64K BY 16 DRAM

19.0 PACKAGE DIMENSIONS

Figure 19-1 illustrates the 208-pin MQFP package showing the dimensions in millimeters and inches.

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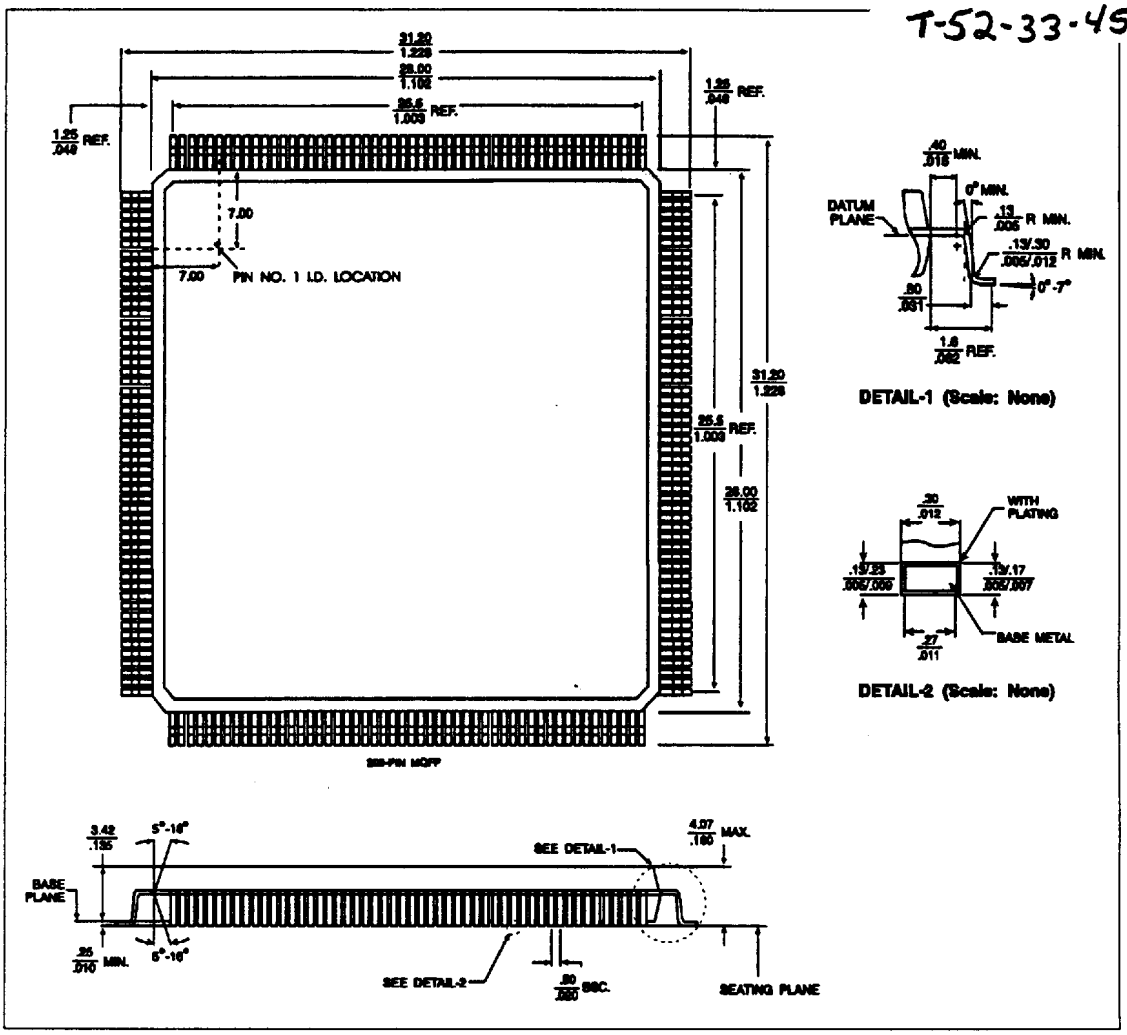

FIGURE 19-1 208-PIN MQFP PACKAGE DIMENSIONS