WD90C00

VGA

Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multi Color Graphics Array (MCGA), and the Video Graphics Array (VGA). The WDI WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device that fulfills this need and allows for the design of very high performance VGA graphics subsystems that are able to interface with the PC/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards.

A major advantage of using the WD90C00 is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, EGA, Hercules graphics, AT&T (640 by 400 graphics mode), VGA hardware and BIOS level compatibility on analog and TTL monitors. In addition, it includes full support for running extended high resolution 1024 by 768 by 16 colors interlaced graphics mode on 8514 Color Displays. A Noninterlaced 1024 by 768 by 16 colors graphics mode requires external circuitry along with a 56 MHz MCLK and 80 ns DRAMs.

1.1 FEATURES

- Provides single chip Video Graphics Solution for IBM PC/XT/AT and Personal System/2 compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% EGA, CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC/XT/AT, and Micro Channel
- 800 by 600 x 16 colors, 640 by 400 x 256 colors
- 640 by 480 x 256 colors (512 Kbytes DRAM)
- 800 by 600 x 256 colors (512 Kbytes DRAM)
- 1024 by 768 x 16 colors interlaced graphics mode support - 8514 monitor compatible
- 1024 by 768 x 16 colors noninterlaced with external logic
- 132 column text modes, with 25, 43, or 50 rows
- Up to four simultaneous displayable fonts
- Special register locking for flat panel applications
- Lockable palette, RAMDAC, and overscan registers
- Display memory offset registers to control 4 Kbyte windows or 64 Kbyte windows
- Provides adapter video BIOS ROM decoding
- True 7, 8, 9, 10, and 16 pixel wide fonts
- Supports up to 1 Mbyte display memory addressing
- Load up to 16 fonts
- Special underlining in color text mode
- Two additional bits for a total of 18 address bits for cursor location and start address
- Special double scanning
- Special display enable or blanking output signal
- Special border disable
- Page mode addressing for CRTC refresh cycles
- High performance FIFO memory architecture
- Includes 8- or 16-bit wide CPU data bus
- Support for external color lookup table (Palette Chip) with 256K available colors
- Pin for pin compatible with the PVGA1A (AT bus mode)
- Enhanced virtual VGA support
- Up to 45 MHz maximum video clock rate
- Up to 56 MHz maximum memory clock rate
- 1.25 micron CMOS VLSI technology
- 100-pin Plastic Leadless Chip Carrier (PLCC) or Plastic Quad Flat Pack (PQFP) JEDEC package
- Minimizes circuit board space requirements and lowers system cost

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1.2 DESCRIPTION

The Western Digital Imaging (WDI) WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device designed to implement the IBM Personal System/2 Standard video modes along with all of the popular modes used in the IBM PC/AT family. The WD90C00 is designed to offer more improvements for a wider range of applications. These enhancements include additional extended PR registers for EGA register level compatibility for analog and TTL monitors, high resolution interlaced graphics support, improved bus interface design, and an improved memory and video interface for higher performance.

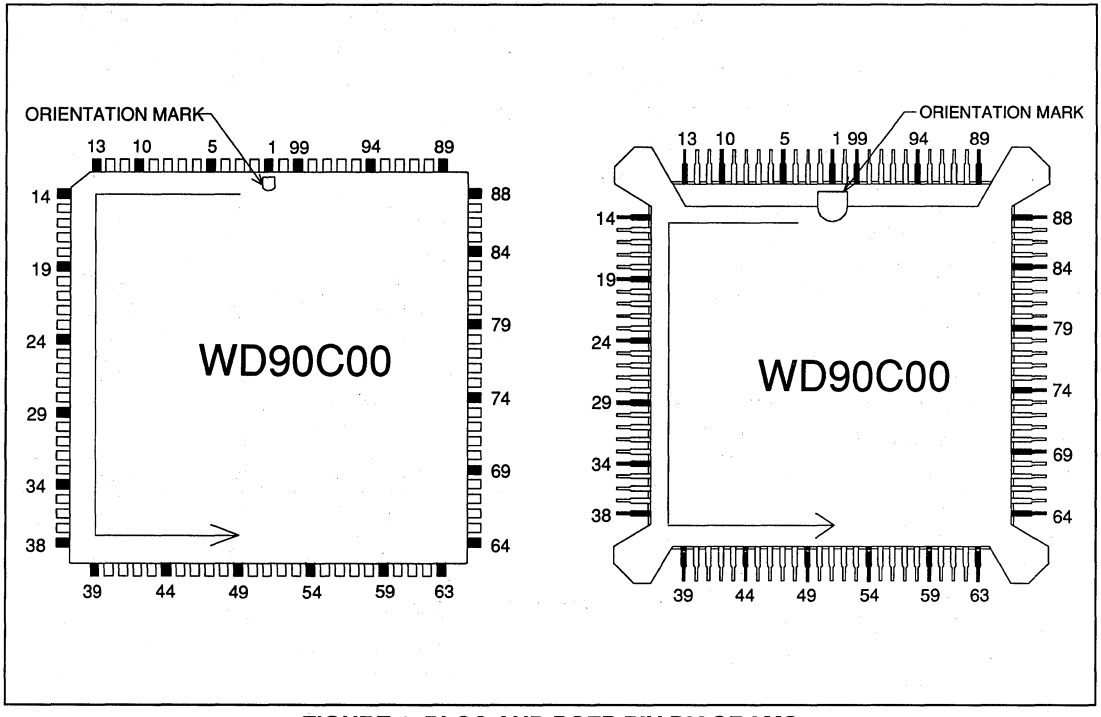

FIGURE 1. PLCC AND PQFP PIN DIAGRAMS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	26	GND	51	GND	76	MCLK
2	MD4	27	A18	52	VCC	77	GND
3	MD3	28	A19	53	VID4	78	VCC
4	MD2	29	$\overline{IOR}$	54	VID3	79	$\overline{RAS10}$
5	MD1	30	$\overline{IOW}$	55	VID2	80	$\overline{CAS10}$
6	MD0	31	$\overline{MRD}$	56	VID1	81	$\overline{OE10}$
7	$\overline{EBROM}$	32	$\overline{MWR}$	57	VID0	82	$\overline{RAS32}$
8	$\overline{DS16}$	33	$\overline{EIO}$	58	$\overline{WPLT}$	83	$\overline{CAS32}$
9	$\overline{BHE}$	34	RDY	59	PCLK	84	$\overline{OE32}$
10	$\overline{SFDBK}$	35	IRQ	60	HSYNC	85	$\overline{WE0}$
11	$\overline{EABUF}$	36	RSET	61	VSYNC	86	$\overline{WE1}$
12	DA8	37	DIR	62	$\overline{BLNK}$	87	$\overline{WE2}$
13	DA9	38	$\overline{EDBUF}$	63	MA8	88	$\overline{WE3}$
14	DA10	39	DA0	64	GND	89	MD15
15	GND	40	DA1	65	MA7	90	MD14
16	DA11	41	DA2	66	MA6	91	MD13
17	DA12	42	DA3	67	MA5	92	MD12
18	DA13	43	DA4	68	MA4	93	MD11
19	DA14	44	DA5	69	MA3	94	MD10
20	DA15	45	DA6	70	MA2	95	MD9
21	EMEM	46	DA7	71	MA1	96	MD8
22	A15	47	$\overline{RPLT}$	72	MA0	97	MD7
23	A16	48	VID7	73	VCLK2	98	MD6
24	A17	49	VID6	74	VCLK1	99	MD5
25	VCC	50	VID5	75	VCLK0	100	VCC

TABLE 1. PIN ASSIGNMENTS

2.0 ARCHITECTURE

The WD90C00 is a highly integrated device that internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics controller and the Attribute Controller.

- **CRT Controller**

The CRT Controller maintains screen refresh functions for the various display modes defined by the programming of its registers either by the BIOS ROM resident firmware or from the application program. These screen refresh functions include display page control, cursor control, sync generation and resolution.

- **Sequencer**

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock and the dot clock for the CRT, Graphics and Attribute controllers.

- **Graphics Controller**

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

- **Attribute Controller**

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, pixel panning, reverse video, overscan color and background or foreground color.

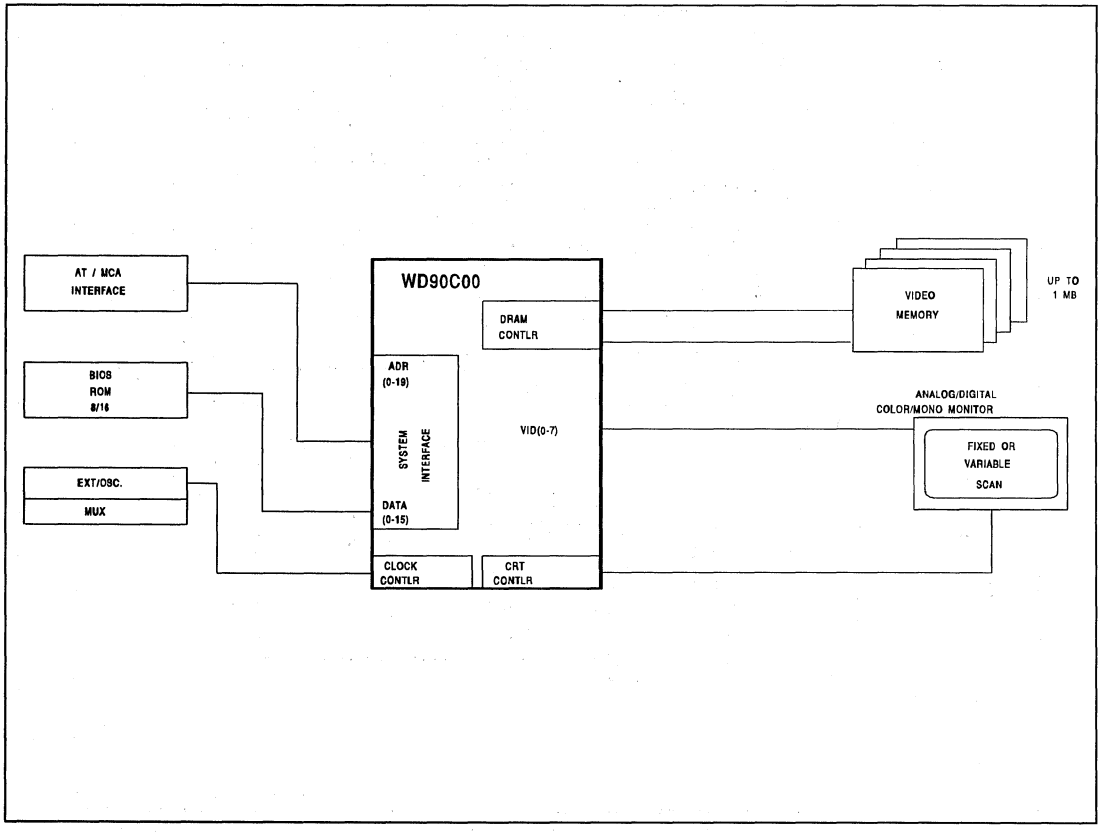

FIGURE 2. SYSTEM BLOCK DIAGRAM

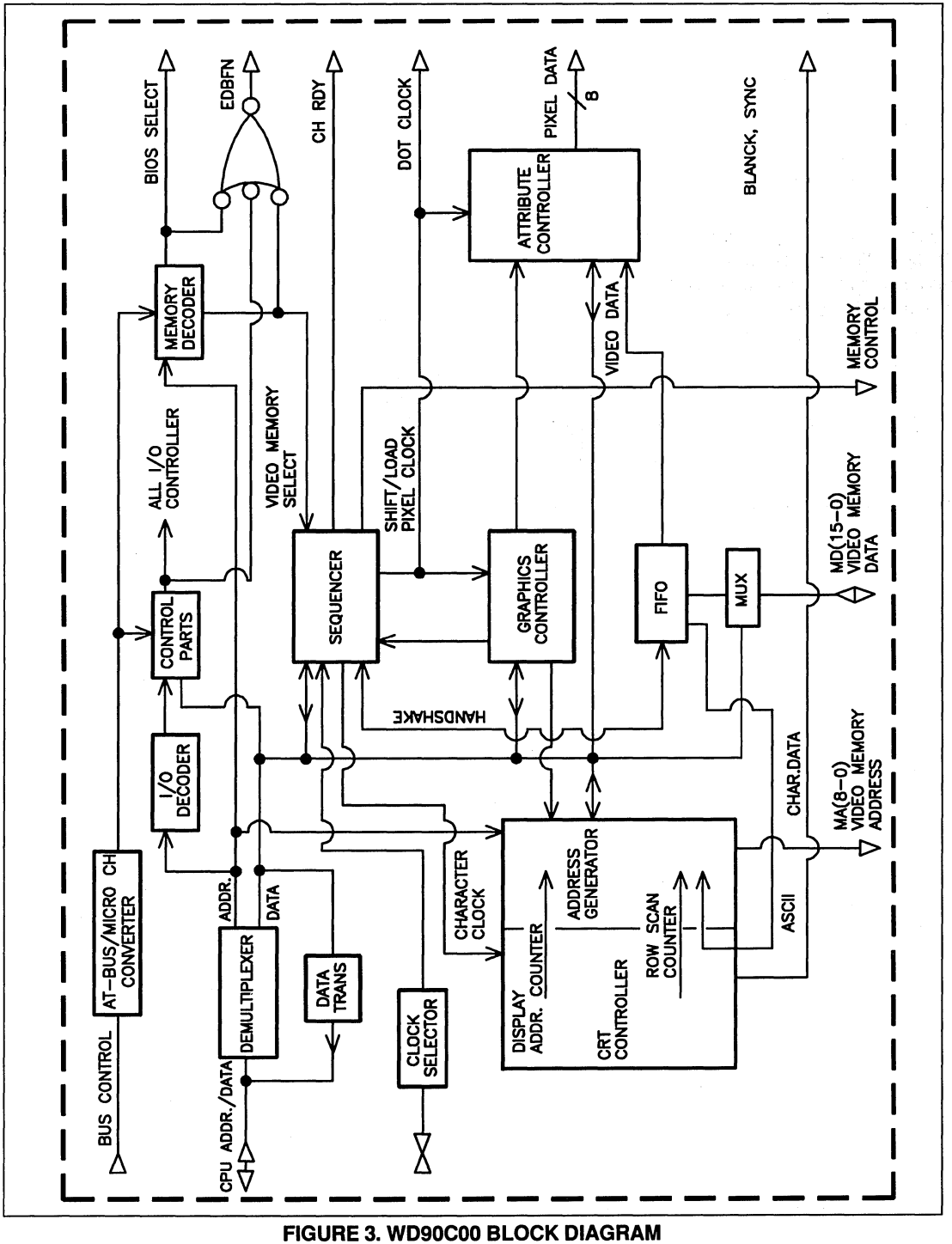

FIGURE 3. WD90C00 BLOCK DIAGRAM

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3.0 WD90C00 INTERFACES

The WD90C00 has four major interfaces: the CPU and BIOS ROM interface, the DRAM Display Buffer interface, the Video and RAMDAC interface, and the Clock interface.

3.1 CPU AND BIOS ROM INTERFACE

The WD90C00 is designed to operate in two different bus architecture configurations. These are the PC/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the pin strapping upon power up that sets Configuration Register CNF(2).

When configured for AT or Micro Channel operation, the WD90C00 operates functionally in a manner that is conducive to PC/AT or Micro Channel interfacing respectively. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C00 provides all the signals and decodes all the necessary memory and I/O addresses for either an 8 or 16 bit data bus. It also provides the necessary decoding of the Adapter Video BIOS ROM and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 Display adapter. Using the provided signals, the customer can implement designs which multiplex the address/data signals to the WD90C00 in 8 or 16 bit mode, control an 8 or 16 bit BIOS ROM, and generate the desired control and handshake signals such as -MEMCS16.

The I/O data path is eight bit. The memory display buffer data path can be eight or sixteen bits wide. EGA Planar modes have a mandatory eight bit data path with the CPU. Text modes, odd/even, and 256 color modes can support a sixteen bit data path if the video subsystem supports a 16 bit bus implementation. The WD90C00 will provide the necessary wait states for CPU accesses to the video memory. Wait states for I/O accesses and BIOS ROM accesses are not generated. Special I/O ports such as 46E8H (AT mode) and 102H for VGA Enable have been implemented internally in the WD90C00. VGA Subsystem Enable port 3C3h (MCA mode) needs to be implemented externally.

3.2 DRAM DISPLAY BUFFER INTERFACE

The WD90C00 has an optimized interface to the video memory display buffer. The video memory DRAMS can be considered as being organized as four planes. Three configurations of DRAMs exist for the WD90C00 where each plane can be configured as 64 Kbytes (256 Kbytes total), 128 Kbytes (512 Kbytes total), or 256 Kbytes (1 Mbyte total).

The Video memory address range can be up to 1 Mbyte depending on the configuration. Its range is usually from A000:0H to BFFF:FH. External circuitry can be used to map the video memory in different (up to) 1 Mbyte windows.

Eight 64K by 4 page mode DRAM chips are supported for the default IBM memory size. Sixteen 64K by 4 DRAMs and a multiplexer are needed to have a total of 512 KB DRAM. This configuration is needed to support extended video modes such as 640 by 480 x 256 colors and 1024 by 768 x 16 colors. Eight 256 KB by 4 DRAMs are needed to support 1 Mbyte total memory. The WD90C00 provides the support to access all of the available memory. As the WD90C00 has a separate memory clock, 36 MHz to 40 MHz clocks are needed to drive 120 ns DRAMs. With 100 ns DRAMs, up to a 44.9 MHz clock can be used. The WD90C00 can support up to a 56 MHz MCLK which allows it to support much higher extended resolutions such as an 800 by 600 x 256 color mode.

The combination of video clock and memory clock and DRAM speed will determine the video modes available. Usually, a 44.9 MHz MCLK and 44.9 MHz VCLK will support the 1024 by 768 resolution modes. A 42 MHz MCLK will be needed to support the extended 256 color modes but the 44.9 MHz is recommended. A 36 MHz MCLK and VCLK will support the 800 by 600 x 16 color mode.

3.2.1 DRAM Cycle Types

The WD90C00 will do standard RAS/CAS single cycle accesses to the DRAM during CPU writes and reads in graphics modes and alphanumeric modes. For CRTC display refresh cycles, the WD90C00 will do page mode access reads for all cycles in graphics modes. It will also do page mode reads to the DRAM when selected to do so to increase performance in alphanumeric modes. The default mode of DRAM access in alphanumeric mode is the standard single RAS/CAS cycle. The WD90C00 provides the necessary control signals and address/data lines to access the video memory as two 16 bit data interleaved banks. The WD90C00 will also refresh the DRAMs with 3 or 5 refresh cycles after every horizontal scan line.

3.3 VIDEO AND RAMDAC INTERFACE

3.3.1 RAMDAC

The WD90C00 is designed to connect to an analog CRT monitor through an external RAMDAC, but it may also be used to drive other types of displays such as TTL monitors along with the correct register programming and clocks. All the necessary signals to interface to the video RAMDAC are provided.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C00 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color). In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel such as a 1024 by 768 noninterlaced mode.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to the WD90C00. The WD90C00 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

3.4 CLOCK INTERFACE

The WD90C00 has four clock input signal pins. These are: separate memory clock, MCLK, which drives the DRAM timing in graphics and alpha modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. WD90C00 also provides the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as the video dot clock.

3.5 WD90C00 POWER-UP CONFIGURATION

The WD90C00 uses the memory data pins that are "strapped" to ground or Vcc through resistors to configure an internal configuration register upon powerup/reset. CNF(2) will determine whether the WD90C00 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by WD90C00 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C00 power-up configuration, refer to the PR Register section of this data sheet.

4.0 PIN DESCRIPTION

The following tables provide WD90C00 pin definitions for the 100-Pin Plastic Leadless Chip Carrier (PLCC) and Plastic Flat Pack (PQFP) package.

The WD90C00 mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO	PIN SYMBOL	TYPE	DESCRIPTION
		POWER ON	
36	RSET	I	RESET: This signal input will reset the WD90C00 in order for the WD90C00 to initialize during Reset. PR registers PR1, PR11, and CNF are initialized at power-up reset based on the logic level on the MD(7:0), MD(15:11) bus as determined by pull-up/pull-down resistors. Outputs $\overline{\text{EABUF}}$ and $\overline{\text{EDBUF}}$ are tri-stated during reset. The active high reset pulse width should be at least ten MCLK clock periods.
		CLOCK SELECTION	
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics and alpha mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be equal to or greater than VCLK. It is 36 to 40 MHz for 120 ns DRAMs, and recommended to be 44.9 MHz for 100 ns DRAMs.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be either the second video display clock input or an output selection signal to the external clock selection module. Pin direction is determined on Reset by a pull-up/down register on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 can be an active low pulse during I/0 writes to port 3C2H or the state of 3C2H bit 2 as per PR15(5). Refer to the Configuration Register description.
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user defined external clock input, or as an output reflecting the content of bit PR2(1) or the state of 3C2H bit 3 as per PR15(5) if CNF(3) is set to 1 . Refer to the Configuration Register description.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			CLOCK SELECTION (CONT)
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register (3C2H) bits 3 and 2 when both are set to 0 will select this clock.
			CPU ADDRESS BUS
28	A19	I	ADDRESS ONLY BUS A(19:15): These active high inputs form the high-order five bits of video memory address. These addresses (19:16) are not decoded during I/O accesses in AT or MCA implementation. These inputs are directly connected to the system bus.
27	A18	I	
24	A17	I	
23	A16	I	
22	A15	I	
			CPU DATA BUS
20	DAI5(*)	I/O	DATA/ADDRESS BUS DA(15:0): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information. NOTE: "*" DA15 signal is multiplexed with data bit 15 and CRT monitor sense input for auto monitor detection.
19	DA14	I/O	
18	DA13	I/O	
17	DA12	I/O	
16	DA11	I/O	
14	DA10	I/O	
13	DA9	I/O	
12	DA8	I/O	
46	DA7	I/O	
45	DA6	I/O	
44	DA5	I/O	
43	DA4	I/O	
42	DA3	I/O	
41	DA2	I/O	
40	DA1	I/O	
39	DA0	I/O	
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the WD90C00 video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the WD90C00. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

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PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
10	$\overline{\text{ROM16}}$ $\overline{\text{SFDBK}}$	O	16 BIT WIDE BIOS ROM: In AT mode this active low status signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the signal -MEMCS16 in AT mode. In Micro Channel mode, $\overline{\text{SFDBK}}$ is the unlatched address decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the CPU bus cycles during video memory accesses. It is pulled inactive by WD90C00 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. This is a tri-state signal.
35	IRQ	O	INTERRUPT REQUEST: It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of a Vertical Display occurs, this signal will transition active at the start of vertical retrace, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In a AT mode, IRQ is tri-state upon power up reset and may be enabled by PR14(7). In Micro Channel mode, PR14(7) will power up IRQ enabled. This is a tri-state signal.
8	$\overline{\text{DS16}}$	O	DATA SIZE 16: Active low enable for 16 bit video memory word transfers. It is a mode dependent signal. In AT mode, $\overline{\text{DS16}}$ is a status signal as programmed in bit PR1(2) (and other registers) and is used to control the high and low byte 16 bit external data buffers. See the PR Register (PR1) description for further details. This status signal is also used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR(1) and/or during memory 16 bit data path access (if enabled by PR1(2)).

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
33	$\overline{EIO}$ VGASETUP	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the WD90C00. In Micro Channel mode, this signal is the VGASETUP input pin and is connected to the latched card setup or the VGA setup. The externally designed system I/O port signals (96H for Adapter card or 94H bit 5 for system board design) is connected to the $\overline{EIO}$ pin. When this signal is high, the WD90C00 is enabled or in the operating state. An active low signal on this pin puts the WD90C00 into set up mode. During the set up mode, write logic 1H to WD90C00 internal port 102H to awaken the WD90C00 after power on.
9	$\overline{BHE}$	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates a 16 bit transfer of data
31	$\overline{MRD}$ M/-I/O	I	MEMORY READ: In AT mode, this is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-I/O) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process.
32	$\overline{MWR}$ -S0	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands.
29	$\overline{IOR}$ -S1	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle.
30	$\overline{IOW}$ -CMD	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write cycle. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle.

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PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY DATA
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA MD(15:0): These lines are the data bus to the video display DRAMS. Data lines MD(7:0) are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD — Power-Up Function — Register (Bit) 15 EGA SW4 PR11(7)+ 14 EGA SW3 PR11(6)+ 13 EGA SW2 PR11(5)+ 12 EGA SW1 PR11(4)+ 11 ANALOG/TTL Display CNF(8) * 7 General Purpose CNF(7) * 6 General Purpose CNF(6) * 5 General Purpose CNF(5) * 4 General Purpose CNF(4) * 3 VCLK1,2 Input/Output CNF(3) + 2 AT/MicroChannel Mode CNF(2) + 1 BIOS ROM Data Path PR1(1) * 0 BIOS ROM Mapout PR1(0) * NOTE: "*" Pulldown resistor sets these bits to logic 1. "+" Pullup resistor sets these bits to logic 1. For more details refer to PR Registers.
			VIDEO MEMORY ADDRESS
63 65 66 67 68 69 70 71 72	MA8+ MA7+ MA6+ MA5+ MA4+ MA3+ MA2+ MA1+ MA0+	O	MEMORY ADDRESS MA(8:0): Display memory DRAM address. NOTE: "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
			VIDEO MEMORY CONTROL SIGNALS
80	$\overline{\text{CAS10}}$+	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	$\overline{\text{CAS32}}$+	O	COLUMN ADDRESS STROBE: Active low memory maps 3 & 2 CAS output signal.
79	$\overline{\text{RAS10}}$+	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
82	$\overline{RAS32}$+	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	$\overline{OE10}$+	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	$\overline{OE32}$+	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	$\overline{WE0}$+	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, upper byte (Memory map 0).
86	$\overline{WE1}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1)
87	$\overline{WE2}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	$\overline{WE3}$+	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3). NOTE: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(4) = 1.
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7* VID6* VID5* VID4* VID3* VID2* VID1* VID0*	O	VIDEO VID(7:0): Pixel video data output to DAC. NOTE: "*" For testing purposes, these pins can be tri-stated by setting PR Register PR4 (5) = 1.
47	$\overline{RPLT}$	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses at 3C6H, 3C8H, and 3C9H.
58	$\overline{WPLT}$	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses at 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the RAMDAC to latch video signals VID(7:0). Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1, or 2 is divided by two in 320/360 pixel display mode to derive PCLK. MCLK can be the source of this clock.
62	$\overline{BLNK}$ *	O	BLANK: Active low RAMDAC blank pulse. NOTE: "*" For testing purposes, this pin can be tri-stated by setting PR Register PR4 (5) = 1.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
		CRT CONTROL	
60	HSYNC+	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming. SEE NOTE BELOW.
61	VSYNC+	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register. NOTES: 1. "+" For testing purposes, these pins can be tri-stated by setting PR Register PR4(5)=1.
		BIOS ROM CONTROL	
7	$\overline{\text{EBROM}}$	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C000:0H-C7FF:FH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C600:0H-C67F:FH. However, the C600:0H-C67F:FH address range can be mapped in to increase BIOS space by setting PR17(0) = 0. In AT mode only, a write to the WD90C00 internal I/0 port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
		BUFFER CONTROL	
11	$\overline{\text{EDBUFH}}$	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing aqyddress and data to WD90C00. It is tri-stated while Reset is active. When in MCA implementation, this output becomes the high byte data bus enable signal during the 16 bit data transfers and is referred as $\overline{\text{EDBUFH}}$.
38	$\overline{\text{EDBUF}}$	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to WD90C00. It is tri-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the DA(15:0) data bus in AT and MCA implementation. The default state is low until a read cycle occurs, and the WD90C00 will drive DIR high to change the direction of the data buffers.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
POWER AND GROUND			
25	VCC	—	+5VDC
52	VCC	—	+5VDC
78	VCC	—	+5VDC
100	VCC	—	+5VDC
1	GND	—	Ground
15	GND	—	Ground
26	GND	—	Ground
51	GND	—	Ground
64	GND	—	Ground
77	GND	—	Ground

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0 °C to 70 °C
Storage temperature	- 40 °C to 125 °C
Voltage on all inputs and outputs to Vss	- 0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

6.0 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the reference pin.

Operating temperature range	0° C to 7 °C
Power supply voltage	4.75 to 5.25 Volts

7.0 D.C CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS
V(IL)	Input Low Voltage	--	0.8	V	VCC=5V±5%
V(IH)	Input High Voltage	2.0	--	V	VCC=5V±5%
I(IL)	Input Low Current	--	±10	uA	VIN=0.0V
I(IH)	Input High Current	--	±10	uA	VIN=VCC
V(OL)	Output Low Voltage	--	0.4	V	IOL +4.0mA[1]
V(OH)	Output High Voltage	2.4	--	V	IOH=4.0mA[1]
I(OZ)	High Impedance Leakage Current	-10.0	10.0	uA	0V
I(CC)	Stand By Current (All Inputs at TTL Levels)	--	22	mA	VCC=5.25 VDC TA=0 °C, Static
I(DD)	Operating current	--	130	mA	VCC=5.25V, MCLK=VCLK=45 MHz
C(IN)	Input Capacitance	--	10	pF	FC=1 MHz
C(OUT)	Output Capacitance	--	10	pF	FC=1 MHz

TABLE 2. DC CHARACTERISTICS

NOTES

1. WD90C00 outputs have 4.0 mA maximum source and sink capability except for pin RDY = 24.0 mA sink and 4.0 mA source and pin IRQ = 24.0 mA sink and 4.0 mA source.

2. Pullups on MD(0:15), DA(0:15), $\overline{\text{EDBUF}}$, $\overline{\text{EABUF}}$ = 100 K ohms. Pullup on $\overline{\text{BHE}}$ = 50 K ohms.

8.0 AC TIMING CHARACTERISTICS

C_L = load capacitance = 70 pf unless specified otherwise.

t=1/MCLK in all modes
Units are in nanoseconds (ns).

NUMBER	PARAMETER	MIN	MAX	NOTES
	RESET TIMING			
1	Reset Pulse Width	10t		1
2	MD Setup to RSET low	2t		
3	MD Hold from RSET low	2t		
4	Vcc high to RSET high setup	100		
5	RSET low to first $\overline{MRD}$/ $\overline{IOW}$	10t		
	CLOCK TIMING			
1	Input Clock (MCLK or VCLK) Period	t	t	
2	Clock low	40%t		2
3	Clock high		60%t	2
4	Clock Rise Time		3	3
5	Clock Fall Time		3	3
6	Input VCLK to PCLK Delay		13	
9a	PCLK to Hsync and Vsync Delay		6.5	
9b	PCLK to $\overline{BLNK}$ Delay		6.5	
9c	PCLK to VID(7:0) Delay		3	
	AT MODE I/O & MEMORY READ/WRITE TIMING			
1	$\overline{EIO}$ setup to $\overline{IOR}$ and $\overline{IOW}$ active	8		
2	$\overline{EIO}$ hold from $\overline{IOR}$ and $\overline{IOW}$ inactive	5		
3	EMEM setup to $\overline{MR}$ and $\overline{MW}$ active	4		
4	EMEM hold from $\overline{MR}$ and $\overline{MW}$ inactive	4		
5	$\overline{EABUF}$ inactive from $\overline{IOR}$/ $\overline{W}$, $\overline{MR}$/ $\overline{W}$ active		30	
6a	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (I/O R&W)		21	
6b	$\overline{EABUF}$ active from $\overline{EDBUF}$ inactive (M R&W)		15	
7a	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (I/O R&W)		13	
7b	$\overline{EDBUF}$ active from $\overline{EABUF}$ inactive (M R&W)		35	

TABLE 3. AC TIMING CHARACTERISTICS

1. The MCLK should be running with the reset applied.
2. Measured at 1.4V.
3. Measured between 0.8V and 2.0V.

NUMBER	PARAMETER	MIN	MAX	NOTES
AT MODE I/O & MEMORY READ/WRITE TIMING (CONTINUED)				
8	EDBUF inactive from IOR/ W, MR/ W inactive		21	
9	DIR active from IOR and MR active		24	
10	DIR inactive from IOR and MR inactive		21	
11a	BHE setup to MR and MW active	4		
11b	Address setup to IOR and IOW active	8		
11c	Address setup to MR and MW active	4		
12a	BHE hold to MR and MW active	6		
12b	Address hold to IOR and IOW active	4		
12c	Address hold to MR and MW active	6		
13	DA(15:0) valid address setup to IOR/ W, MR/ W	13		
14	DA(15:0) valid address hold from IOR/ W, MR/ W	4		
15	Data setup to IOW inactive	10		
16	Data hold from IOR/ W, MR/ W inactive	8		
17a	Data valid from IOR active		2t + 42	
17b	Data valid (CAS32 inactive) from MR active	11.5t		
17c	Write data valid from MW active	4.5t-50		4
18	Read data setup to RDY high	3.5t-40		5
19	RDY inactive from MR and MW active		13	
20	RDY active from MW, MR active	15t		
21	RDY tri-state from MW, MR inactive		10	
22	WPLT active from IOW active		2t+35	
23	WPLT inactive from IOW inactive		22	
24	RPLT active from IOR active		31	
25	RPLT inactive from IOR inactive		21	
26	EBROM active from IOW active (46E8)		2t+29	
27	EBROM inactive from IOW inactive		20	
28	EBROM active from valid address		20	
29	EBROM inactive from MRD inactive		23	
30	VCLK1 (as output) delay from IOW		2t+33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

4. This spec includes 50 ns worst case delay from DA to MD bus.
5. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	MICRO CHANNEL I/O & MEMORY READ AND WRITE TIMING			
1	$\overline{\text{CDSETUP}}$ setup to $\overline{\text{CMD}}$ active	0		
2	$\overline{\text{CDSETUP}}$ hold from $\overline{\text{CMD}}$ inative	4		
3	EMEM, $\overline{\text{BHE}}$, Address setup to $\overline{\text{CMD}}$	10		
4	EMEM, $\overline{\text{BHE}}$, Address hold from $\overline{\text{CMD}}$	6		
5	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ setup to $\overline{\text{CMD}}$	10		
6	$\overline{\text{S1}}$, $\overline{\text{S0}}$, M/ $\overline{\text{IO}}$ hold from $\overline{\text{CMD}}$	6		
7	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ active from $\overline{\text{CMD}}$ active		26	
8	$\overline{\text{EABUF}}$, $\overline{\text{EDBUF}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
9	DIR active from $\overline{\text{CMD}}$ active		22	
10	DIR inactive from $\overline{\text{CMD}}$ inactive		22	
11a	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (IO R&W)		27	
11b	$\overline{\text{SFDBK}}$ active from $\overline{\text{CMD}}$ active (M R&W)		19	
12a	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(IO R&W)		25	
12b	$\overline{\text{SFDBK}}$ inactive from $\overline{\text{CMD}}$ inactive(M R&W)		19	
13	$\overline{\text{SFDBK}}$ inactive from invalid address		25	
14	$\overline{\text{DS16}}$ active from valid address (M R&W)		29	
15	$\overline{\text{DS16}}$ inactive from invalid address		20	
16	Address setup to $\overline{\text{CMD}}$ active	7		
17	DA (15:0) valid address hold from $\overline{\text{CMD}}$ active	4		
18	Write data setup to $\overline{\text{CMD}}$ inactive	10		
19	Write data hold from $\overline{\text{CMD}}$ inactive	7		
20a	Read data valid from $\overline{\text{CMD}}$ active	11.5t		
20b	Write data valid from $\overline{\text{CMD}}$ active	4.5t-50		6
21	Read data setup to RDY high	3.5t-40		7
22	RDY inactive from status (MR)		22	
23	RDY active from $\overline{\text{CMD}}$ active	15t		
24	RDY inactive from $\overline{\text{CMD}}$ inactive		41	
25	$\overline{\text{EBROM}}$ active from valid address		22	
26	$\overline{\text{EBROM}}$ inactive from $\overline{\text{CMD}}$ inactive		29	
27	$\overline{\text{WPLT}}$ active from $\overline{\text{CMD}}$ active		41	
28	$\overline{\text{WPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		22	
29	$\overline{\text{RPLT}}$ active from $\overline{\text{CMD}}$ active		31	
30	$\overline{\text{RPLT}}$ inactive from $\overline{\text{CMD}}$ inactive		23	
31, 32	VCLK1 delay from $\overline{\text{CMD}}$		33	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

6. This spec includes 50 ns worst case delay from DA to MD bus.
7. This spec includes 40 ns worst case delay from MD to DA bus.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM TIMING, CPU READ AND WRITE			
1	$\overline{RAS10}$, $\overline{RAS32}$ cycle time	9t		
2a	$\overline{RAS10}$, $\overline{RAS32}$ pulse width low	5t-8	5t	
2b	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ high	5t-11	5t-2	
3	$\overline{RAS10}$, $\overline{RAS32}$ precharge	4t+1	4t+8	
4	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ low	2t-11	2t+2	
5a	$\overline{CAS10}$, $\overline{CAS32}$ low to $\overline{RAS10}$, $\overline{RAS32}$ high	3t-8	3t+3	
5b	$\overline{CAS10}$, $\overline{CAS32}$ pulse width low	3t-4	3t	
6	$\overline{CAS10}$, $\overline{CAS32}$ high to $\overline{RAS10}$, $\overline{RAS32}$ low	4t+2	4t+14	
7	Row Address setup to $\overline{RAS10}$, $\overline{RAS32}$ low	1t-10	1t+5	
8	Row Address hold from $\overline{RAS10}$, $\overline{RAS32}$ low	1t-6	1t+8	
9	Column address setup to $\overline{CAS10}$, $\overline{CAS32}$ low	1t-12	1t+1	
10	Column address hold from $\overline{CAS10}$, $\overline{CAS32}$ low	1.5t	1.5t+14	
11	$\overline{CAS10}$, $\overline{CAS32}$ precharge high	6t	6t+4	
12	WE0:1 low setup to $\overline{CAS10}$, $\overline{RAS10}$ high	2.5t-7	2.5t+4	
13a	WE3:2 low setup to $\overline{CAS32}$, $\overline{RAS32}$ high	5t-7	5t+4	
13b	$\overline{WE3}$, $\overline{WE2}$ pulse width low	5t-2	5t+2	
17	$\overline{WE0}$, $\overline{WE1}$ pulse width low	3t-2	3t+2	
18	Data hold from $\overline{WE0}$, $\overline{WE1}$ active	2t-5		
19	Data setup to $\overline{WE0}$, $\overline{WE1}$ active	1t-5		
20	$\overline{WE0}$, $\overline{WE1}$ low from $\overline{CAS10}$ low	.5t-7	.5t+4	
21	$\overline{WE3}$, $\overline{WE2}$ setup to $\overline{CAS32}$ low	2t-4	2t+7	
22	$\overline{OE10}$, $\overline{OE32}$ low after $\overline{CAS10}$, $\overline{CAS32}$ low	1t-6	1t+5	
23	$\overline{OE10}$, $\overline{OE32}$ high after $\overline{CAS10}$, $\overline{CAS32}$ high	1t-5	1t+5	
24	$\overline{OE10}$, $\overline{OE32}$ pulse width low	3t-3	3t+1	
25	Read data setup to CAS inactive	10		
26	Read data hold from CAS inactive	10		
27	$\overline{RAS32}$ low after $\overline{RAS10}$ low	4.5t-7	4.5t+7	
28	Write data setup to $\overline{CAS\ 32}$	2t-5		
29	Write data hold from $\overline{CAS32}$	1t-5		
30	$\overline{CAS10}$, $\overline{CAS32}$ high after $\overline{OE10}$, $\overline{OE32}$ low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM PAGE MODE READ AND WRITE TIMING			
1	$\overline{RAS10}$, $\overline{RAS32}$ pulse duration	7t		
2	Page mode $\overline{CAS10}$ cycle time	5t		8
3	$\overline{RAS10}$, $\overline{RAS32}$ precharge	4t	4t+8	
4	$\overline{RAS10}$ low to first $\overline{CAS10}$ high	5t-14	5t-2	
5	$\overline{RAS10}$, $\overline{RAS32}$ low to $\overline{CAS10}$, $\overline{CAS32}$ low	2t-11	2t+2	
7	$\overline{CAS10}$, $\overline{CAS32}$, $\overline{OE10}$, $\overline{OE32}$ pulse width high	2t	2t+4	9
8	$\overline{CAS10}$, low to $\overline{RAS10}$ high	3t-8	3t+3	
9	$\overline{CAS32}$ low to $\overline{RAS32}$ high	5t-8	5t+3	
10, 14	Row address setup to $\overline{RAS10}$, $\overline{RAS32}$ low	1t-10	1t+5	
11, 15	Row address hold from $\overline{RAS10}$, $\overline{RAS32}$ low	1t-6	1t+8	
12, 16	Column address setup to $\overline{CAS10}$, $\overline{CAS32}$ low	1t-12	1t+1	
13, 17	Column address hold from $\overline{CAS10}$, $\overline{CAS32}$ low	1.5t	1.5t+14	
18	$\overline{RAS32}$ low after $\overline{RAS10}$ low	4.5t-7	4.5t+7	
19	Read data setup to CAS inactive	10		
20	Read data hold from CAS inactive	10		
21	$\overline{OE10}$, $\overline{OE32}$ pulse width low	3t-3	3t+1	
22	$\overline{OE10}$, $\overline{OE32}$ low after $\overline{CAS10}$, $\overline{CAS32}$ low	1t-6	1t+5	
23	$\overline{OE10}$, $\overline{OE32}$ high after $\overline{CAS10}$, $\overline{CAS32}$ high	1t-5	1t+5	
24	$\overline{CAS10}$, $\overline{CAS32}$ pulse width low	3t-4	3t	
25	$\overline{CAS10}$, $\overline{CAS32}$ high after $\overline{OE10}$, $\overline{OE32}$ low	2t-8	2t+2	

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

8. First cycle is two mclocks longer than this spec.
9. $\overline{CAS10}$ and $\overline{OE10}$ are two mclocks longer for the first cycle.

NUMBER	PARAMETER	MIN	MAX	NOTES
	DRAM REFRESH TIMING			
1	Address Setup to $\overline{RAS10}$ active	2t-5		10
2	Address Hold from $\overline{RAS32}$ active	3t-5		
3	$\overline{RAS10}$ low time	5t-8		
4	$\overline{RAS10}$ high time	4t+1		
5	$\overline{RAS32}$ low time	5t+1		
6	$\overline{RAS32}$ high time	4t-8		
7	RAS cycle time	9t		

TABLE 3. AC TIMING CHARACTERISTICS (CONT)

10. This spec is shorter by 1 mclock for the first cycle.

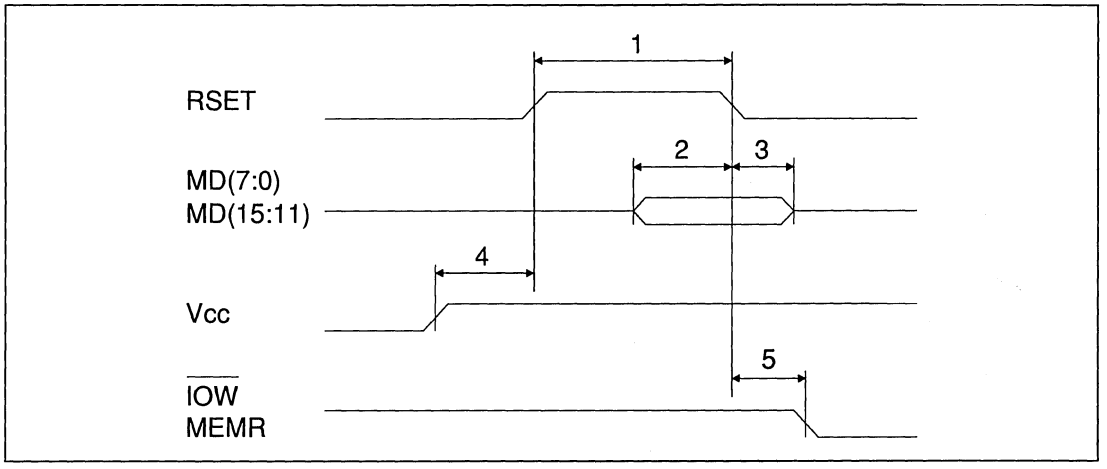

FIGURE 4. RESET TIMING

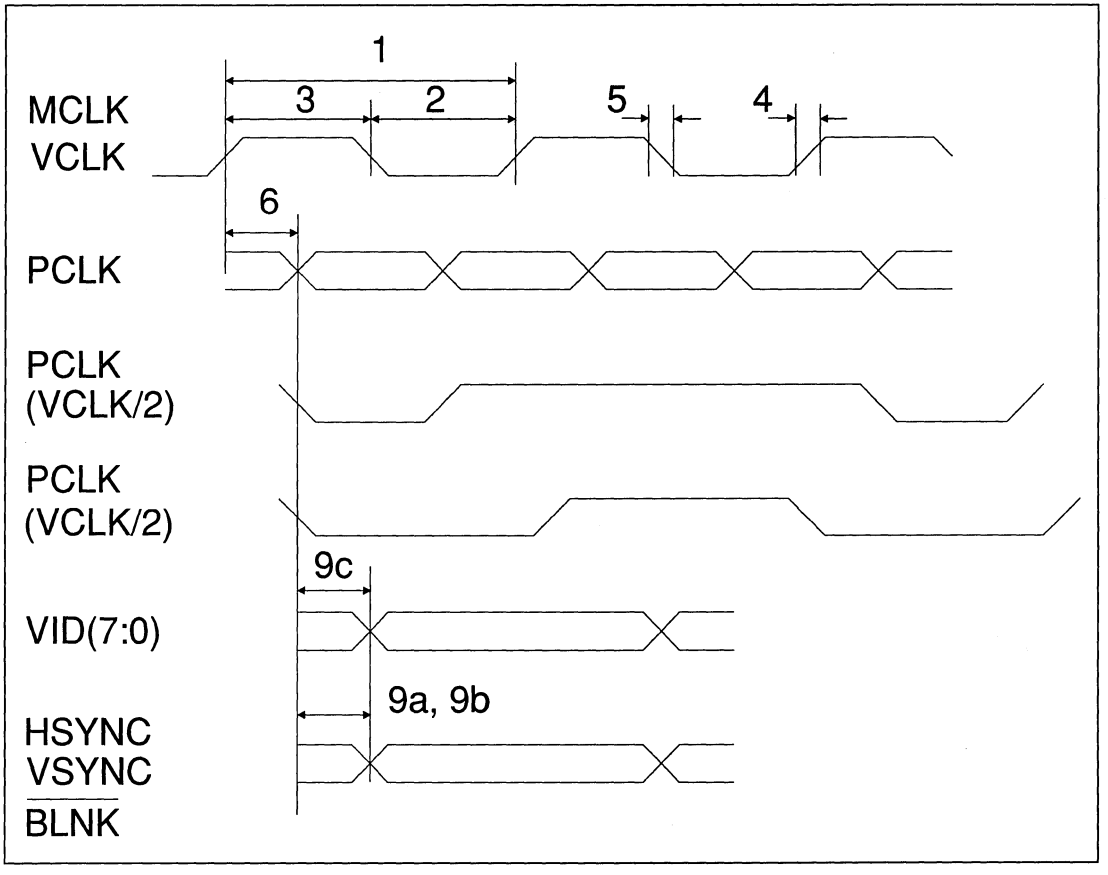

FIGURE 5. CLOCK AND VIDEO TIMING

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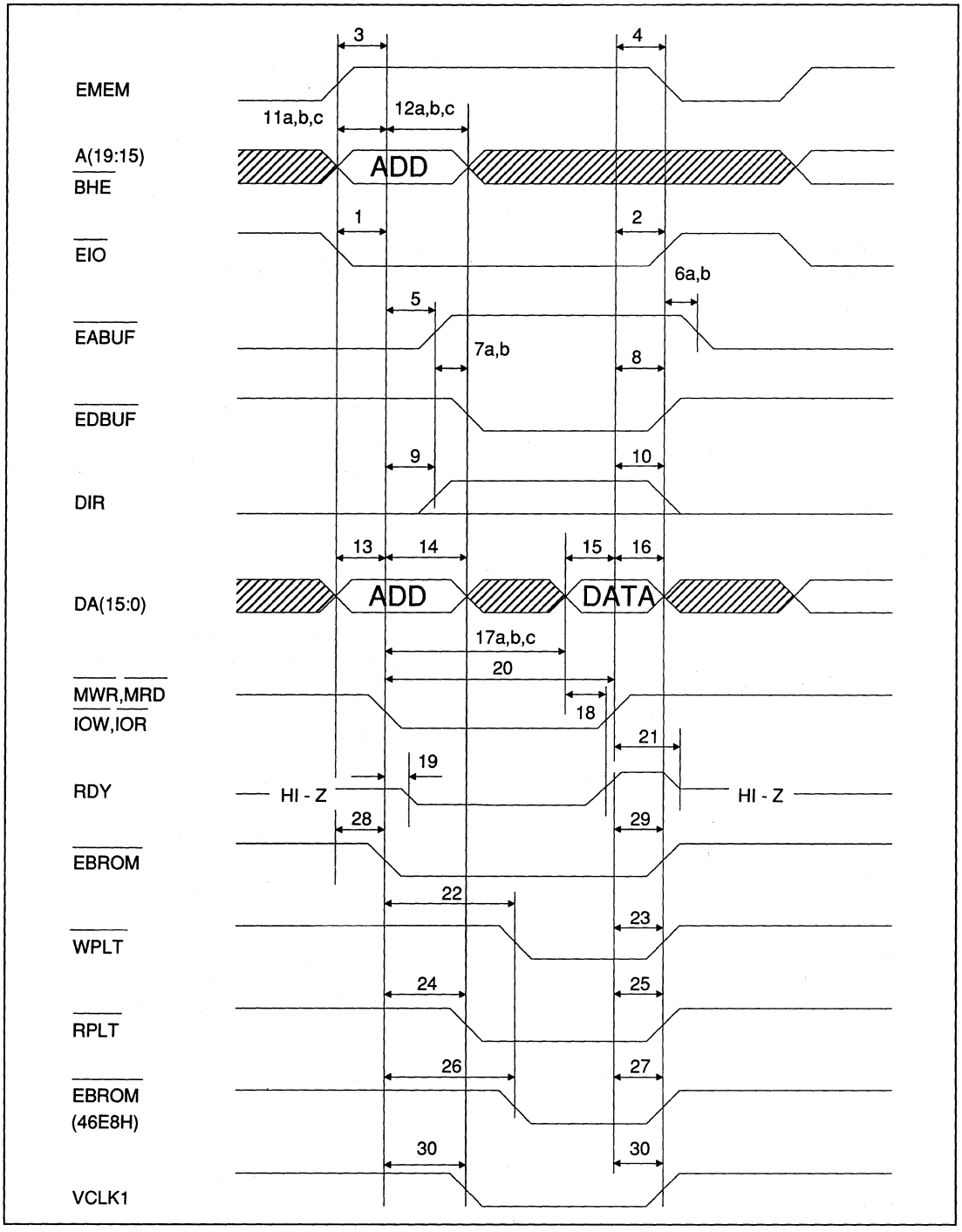

FIGURE 6. AT MODE I/O & MEMORY READ/WRITE TIMING

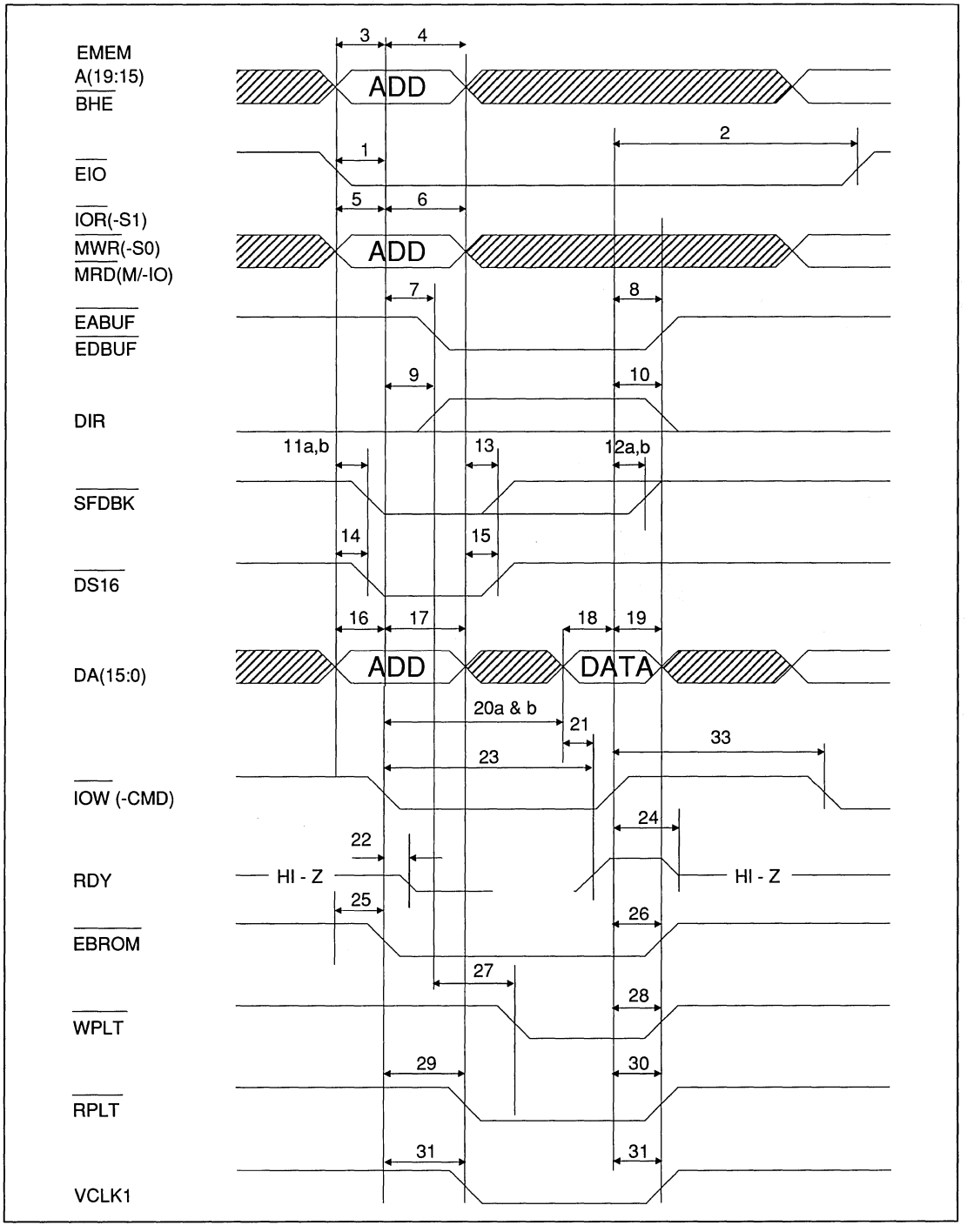

FIGURE 7. MICRO CHANNEL I/O & MEMORY READ & WRITE TIMING

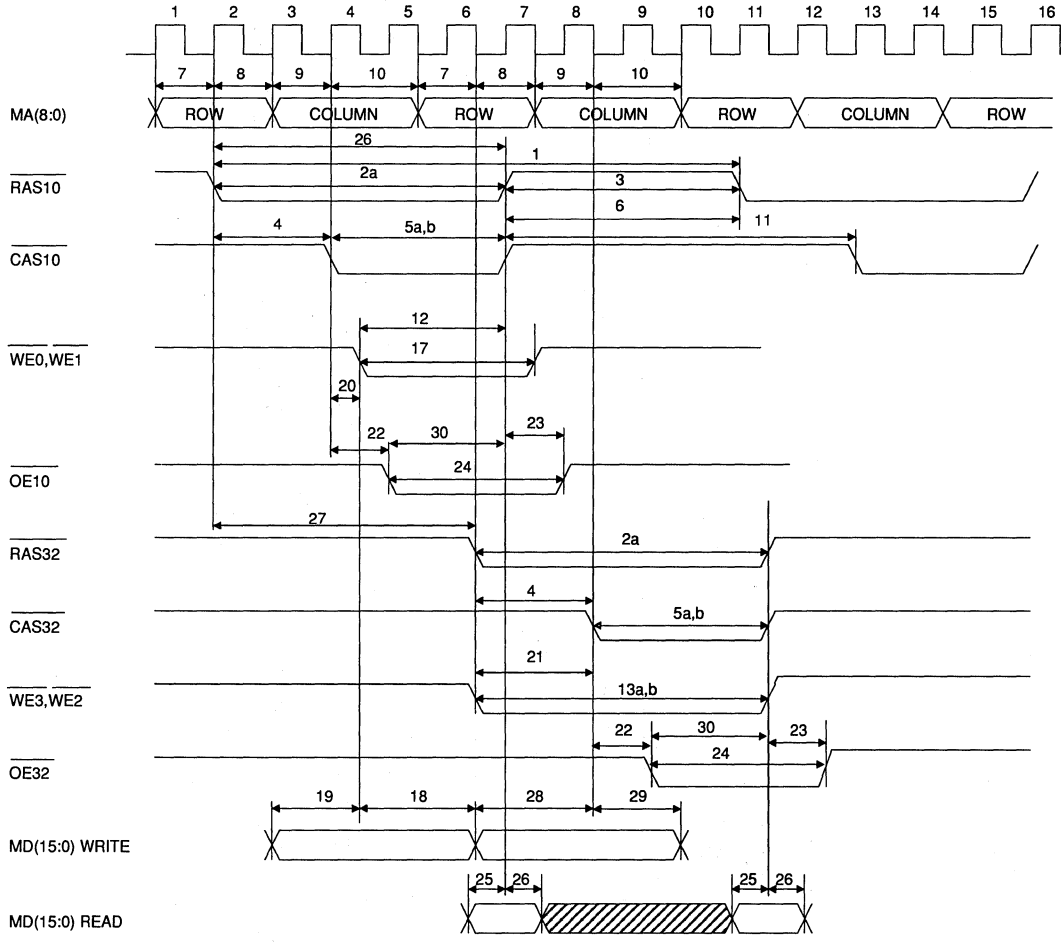

FIGURE 8. CPU READ/WRITE DRAM TIMING

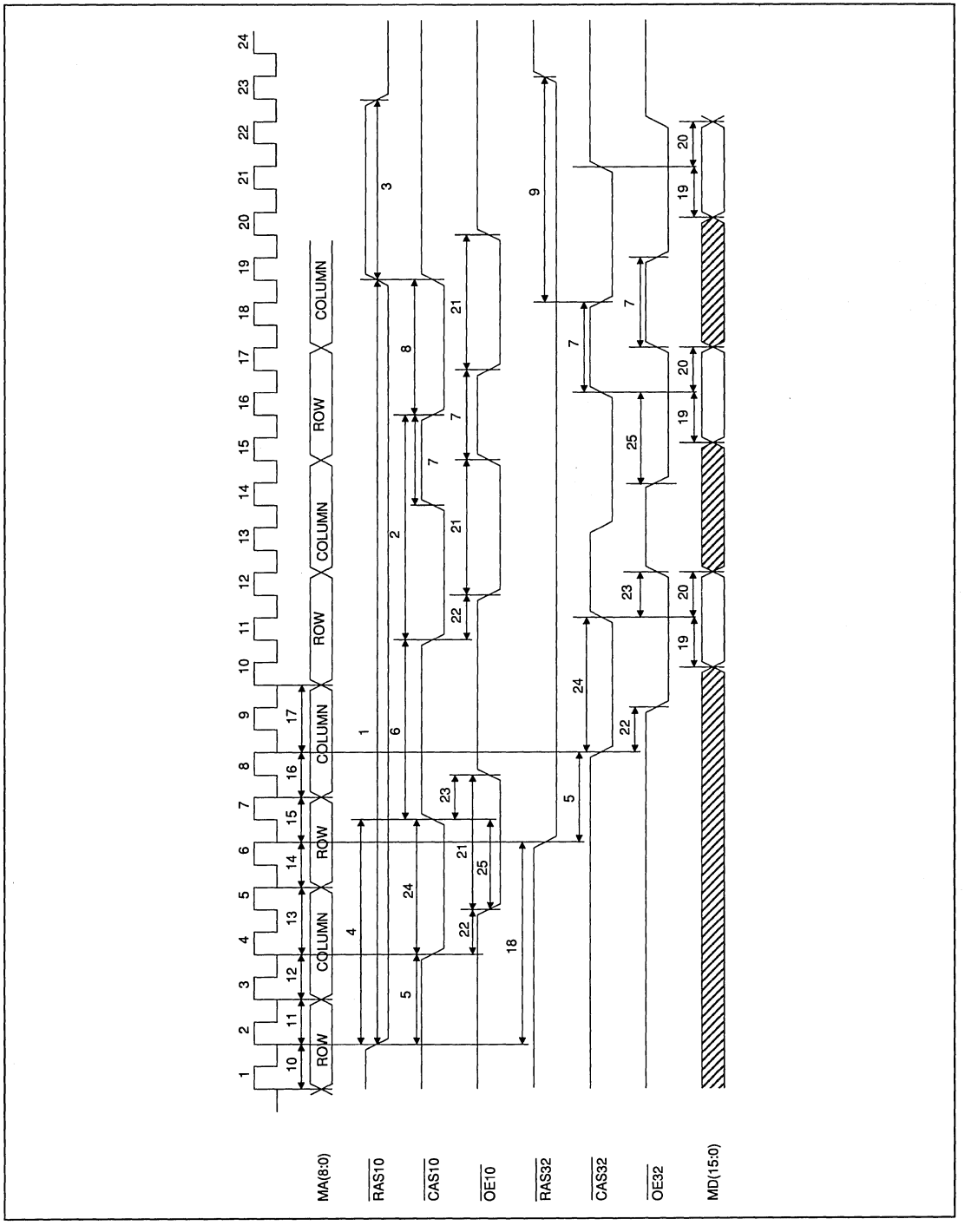

FIGURE 9. DRAM PAGE MODE READ TIMING

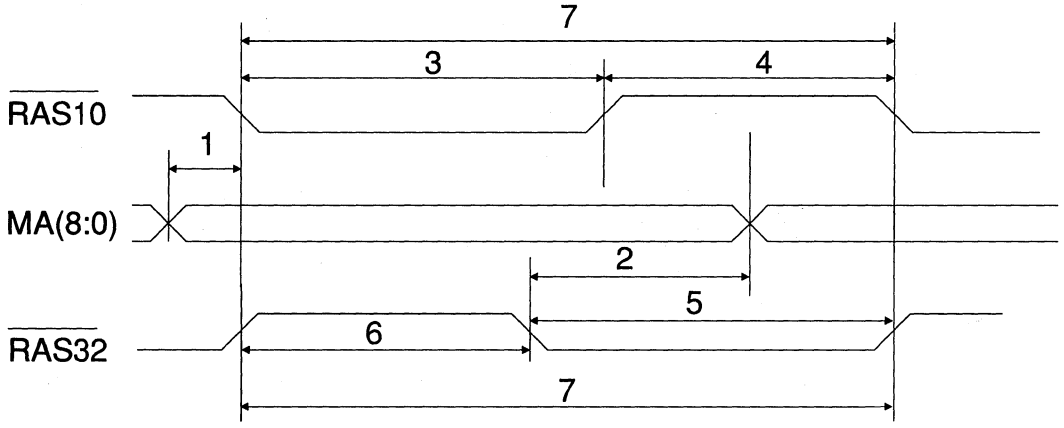

FIGURE 10. DRAM REFRESH TIMING

9.0 WD90C00 REGISTERS

All of the standard IBM registers incorporated inside the WD90C00 are functionally equivalent to the VGA implementation while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the WD90C00 registers in greater detail.

9.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
+Video Subsystem Enable	RW			3C3
NOTE: + Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Read Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 4. VGA REGISTERS SUMMARY

9.2 PR REGISTERS SUMMARY

REGISTERS	RW	MONOCHROME	COLOR
PR Register Index	RW	3CE	3CE
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0-PR4)/Status	RW	3CF.0F	3CF.0F
PR10-PR17 INDEX	RW	3B4	3D4
PR10 Unlock (PR11-PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved 3X5.31- 3X5.3F			

TABLE 5. PR REGISTERS SUMMARY

NOTE: ALL THE PR REGISTERS ARE WRITE PROTECTED. SEE THE PR REGISTERS' DESCRIPTION FOR MORE DETAILS.

9.3 COMPATIBILITY REGISTERS SUMMARY

FUNCTIONS	RW	MDA	CGA	AT&T	HERCULES
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
+CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 6. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers

9.4 VGA REGISTERS

Throughout this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

9.5 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:

1. Reserved bits should be set to zero.

2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes

   1 = D in Color Modes

9.5.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0= Positive vertical sync polarity.
1= Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0= Positive horizontal sync polarity.
1= Negative horizontal sync polarity.

NOTE:

*These bits determined the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0-5, one memory page is selected from the two 64KB pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0= CRTC and status addresses for MDA mode (3BX).
1= CRTC and status addresses for CGA mode (3DX).

9.5.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit(3:0)

Reserved.

9.5.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0= Vertical frame is displayed.
1= Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

9.5.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control:
0: Vsync output enabled
1: Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved

9.6 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to zero.

9.6.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

9.6.2 Reset Register, Read/Write Port = 3C5, Index = 00

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

NOTE:

Due to the improved design of the WD90C00, the fuction of Bits (1:0) are not required and are instead implemented as shadow registers.

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

9.6.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels).

Bit 2

Shift Load. Effective only if bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

9.6.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing To Memory Maps (0-3) respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

9.6.5 Character Map Select Register Read/Write Port = 3C5, Index = 03

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit 4

Character Map B MSB Select.
The MSB of character map B along with bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 KByte
0 0 1	1	3rd 8 KByte
0 1 0	2	5th 8 KByte
0 1 1	3	7th 8 KByte
1 0 0	4	2nd 8 KByte
1 0 1	5	4th 8 KByte
1 1 0	6	6th 8 KByte
1 1 1	7	8th 8 KByte

Bit(3:2)

Character Map Select A.
Refer to bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to bit 4 table.

9.6.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0

Reserved.

9.7 CRT CONTROLLER REGISTERS

PORT	INDEX	VGA REGISTER NAME	*6845 REG NAME
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	+
3?5	03	End Horizontal Blanking	+
3?5	04	Start Horizontal Retrace	+
3?5	05	End Horizontal Retrace	+
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	+
3?5	08	Preset Row Scan	+
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	+
3?5	13	Offset	+
3?5	14	Underline Location	+
3?5	15	Start Vertical Blank	+
3?5	16	End Vertical Blank	+
3?5	17	CRTC Mode Control	+
3?5	18	Line Compare	+

TABLE 7. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0=B in Monochrome Modes and
1=D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.

3. "+" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

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9.7.1 CRT Address Register Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

9.7.2 Horizontal Total Register Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

9.7.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

Horizontal blanking begins when the horizontal character counter reaches this character clock value.

9.7.4 Start Horizontal Blanking Register Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.5 End Horizontal Blanking Register Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Bit(6:5)

Display Enable Signal Skew Control.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

End Horizontal Signal Width.
End Horizontal Blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05H) bit 7.

9.7.6 Start Horizontal Retrace Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.7 End Horizontal Retrace Register Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bit 7

MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

9.7.8 Vertical Total Register Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total Scan Lines

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.7.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vert. Ret. Start Bit 9
6	Vert. Display Enable End Bit 9
5	Vert. Total Bit 9
4	Line Compare Bit 8
3	Start Vert. Blank Bit 8
2	Vert. Ret. Start Bit 8
1	Vert. Display Enable End Bit 8
0	Vert. Total Bit 8

++Bit 7
Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**
Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5
Vertical Total Bit 9 (index = 06H).

Bit 4
Line Compare Bit 8 (index = 18H).

++Bit 3
Start Vertical Blank Bit 8 (index =15H).

++Bit 2
Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**
Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0
Vertical Total Bit 8 (index = 06H).

NOTES:
** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

9.7.10 Preset Row Scan Register Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7
Reserved.

Bit(6:5)
Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit(4:0)
Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

9.7.11 Maximum Scan Line Register Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4 - 0	Maximum Scan Line

Bit 7

200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

9.7.12 Cursor Start Register Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0=Cursor on.
1=Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

9.7.13 Cursor End Register Read/Write Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

9.7.14 Start Address High Register Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits. Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The PR Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

9.7.15 Start Address Low Register Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

9.7.16 Cursor Location High Register Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

9.7.17 Cursor Location Low Register Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 mode.

9.7.18 Vertical Retrace Start Register Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits. The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 - 0 as the light pen read back value, and bits 6 an 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

9.7.19 Vertical Retrace End Register Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) an internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

9.7.20 Vertical Display Enable End Register Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower eight bits)

Bit(7:0)

Vertical Display Enable End Lower Eight Bits.
The eight lower bits of ten bit register that defines where the active display frame ends.
The programmed count is in scan lines minus 1.
Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6 respectively.

9.7.21 Offset Register Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:
Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

9.7.22 Underline Location Register Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

9.7.23 Start Vertical Blank Register Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

9.7.24 End Vertical Blank Register Read/Write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:
8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

9.7.25 CRT Mode Control Register Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE:
* See bit 5, defining address wrap. This table is only applicable when PR Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.
The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.
0 = In word address mode, this bit enables bit 13 to appear at MA0, otherwise bit 0 appears on MAO.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2
0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

9.7.26 Line Compare Register Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared. This creates a split screen where the lower screen does not scroll.

9.8 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE:
1. Reserved bits should be set to zero.

9.8.1 Graphics Index Register Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

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9.8.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE:
*The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

9.8.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

9.8.4 Color Compare Register, Read/Write Port 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

9.8.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

9.8.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11b to select the chained maps 2 & 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

9.8.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all of the maps are shifted out of even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.
The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

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9.8.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128KB
0	1	A000:0H-AFFF:FH	64KB
1	0	B000:0H-B7FF:FH	32KB
1	1	B800:0H-BFFF:FH	32KB

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

9.8.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

9.8.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

9.9 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CO	——	Index Register
3CO	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes and
1 = D in Color Modes

9.9.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits

NOTE:
The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

9.9.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

9.9.3 Attribute Mode Control Register Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

9.9.4 Overscan Color Register Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.

They determine the overscan or border color.
For monochrome display, this register is set to 0.
Border colors are set as shown above.

9.9.5 Color Plane Enable Register Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

9.9.6 Horizontal Pel Panning Register Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

9.9.7 Color Select Register Read Port 3C1/Write Port 3CO, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 an VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

9.10 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
0 = B in Monochrome Modes
1 = D in Color Modes

9.10.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video enable.
0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFH enable.
0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode. Should be 1.
0 = High resolution disabled.
1 = High resolution is enabled.

9.10.2 Hercules Compatibility Register Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)
Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

9.10.3 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)
Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2

B/W or Color Display Mode.
0= Color mode selected.
1= B/W mode selected.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

9.10.4 CGA Color Select Register Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2

Red Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 by 200 Graphics Mode.
1 = Selects red background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

9.10.5 CRT Status Register MDAOperation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

9.10.6 CRT Status Register CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

9.10.7 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 KB length).
1 = Display memory address starts at BC00:0H (16 KB length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode. A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

9.11 WD90C00 PR REGISTERS

NAME	DESIGNATION	I/0 LOCATION
Address Offset A	PR0A(6:0)	3CF.09
Alternate Address Offset B	PR0B(6:0)	3CF.0A
Memory Size	PR1(7:0)	3CF.0B
Video Select	PR2(7:0)	3CF.0C
CRT Control	PR3(7:0)	3CF.0D
Video Control	PR4(7:0)	3CF.0E
Unlock PRO-PR4	PR5(7:0)	3CF.0F
Unlock PR11 - PR17	PR10(7:0)	3?5.29
EGA Switches	PR11(7:0)	3?5.2A
Scratch Pad	PR12(7:0)	3?5.2B
Interlace H/2 Start	PR13(7:0)	3?5.2C
Interlace H/2 End	PR14(7:0)	3?5.2D
Miscellaneous Control 1	PR15(7:0)	3?5.2E
Miscellaneous Control 2	PR16(7:0)	3?5.2F
Miscellaneous Control 3	PR17(0)	3?5.30
Reserved	---	3?5.31-3?5.3F

The WD90C00 has additional features that enhance the performance and functions of the Western Digital Imaging PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C00 architecture is optimized with additional I/O registers.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

NOTES:

1. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2. PR register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F--3CEH (Select Index register) followed by (Data byte) -- 3CF (Data Port)

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit 1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power on reset except where noted.

9.11.1 Address Offset Registers PR0A & PR0B

PR0A - Address Offset Register A
Read/Write Port = 3CF, Index = 09H

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B
Read/Write Port = 3CF, Index = 0AH

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C00 can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. To allow a second video card to co-exist, this space is further limited to a 64 Kbyte video memory partition.

The WD90C00 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 bit 3 is set to 1. PR0A and PR0B provide a seven bit offset that is added to address bits A (18:12) of the system address to form a 20-bit address. It can be thought of as being like segment register DS and ES of the 8088/80X86 architecture. PR0A and PR0B will then provide 4 Kbyte segments.

When PR0B is enabled by setting PR1 bit 3 = 1, PR address offset registers, in a 64K VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), PR0A and Alternate Offset Address register (PR0B) may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H-AFFF:FH while PR0B is mapped from A000:0H-A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register bits 3 and 2), PR0A is mapped from B000:0H-BFFF:FH while PR0B is mapped from A000:0H-AFFF:FH when the Alternate Offset register is enabled.

9.11.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map select
3	Enable Alternate Address Offset Register PR0B
2	16-Bit Video Memory
1	16-Bit BIOS ROM
0	BIOS ROM Map Out

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6

Memory Size.

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 KB STANDARD VGA	VGA*
0	1	0	256 KB WD90C00 VGA	PVGA**
1	0	0	512 KB WD90C00 VGA	PVGA
1	1	0	1024 KB WD90C00 VGA	PVGA
X	X	1	ANY OF THE ABOVE	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
** WDI extended modes can fully utilize up to 256 Kbytes.

According to the VGA video memory organization, 256 KB of the available memory space is divided into four 64 KB maps (0-3), each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane. The starting address of the 256 KB video memory buffer can be configured to match other video adapters, and/or, application programs. For example, 256 KB video display buffer with 128 KB or 64 KB segments can start at address A000:0 (Hex) while 32KB segments start at address B000:0 (Hex) or B800:0 (Hex). WD90C00 enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512 KB or 1024 KB. The DRAM organizations supported by the WD90C00 and its associated video space table are shown below.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64Kx4	N/U	256 KB	Four (64KB Per Plane)
64Kx4	BANK SELECT	512 KB	Four (128KB Per Plane)
256Kx4	DRAM PIN A8	1024KB	Four (256KB Per Plane)

When video memory size is 512 KB, and 64Kx4 DRAMs are used two banks of 64 KB form 128 KB per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the $\overline{CAS10}$ and $\overline{CAS32}$ signals. Four planes form the desired 512 KB video memory space. For 1024 KB video memory size, MA8 is directly connected to the A8 address pin of the 256Kx4 DRAMS, and two DRAMS form a 256 KB per plane. Four planes make the desired 1024 KB video memory space.

PR1 bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is same as IBM VGA regardless of PR1 (6) and PR1(7).

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 0 256K TOTAL;64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:

PR1(7) **PR1(6)**
0 1 256K TOTAL;64K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

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RAM ADDRESSING:

PR1(7)	PR1(6)	
1	0	512K TOTAL;128KB/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

NOTE: "*" Controls CAS external to WD90C00

RAM ADDRESSING:

PR1(7)	PR1(6)	
1	1	1024K TOTAL IN FOUR PLANES;256K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:

1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 bit 3 or bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 bit 5 = 0.

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping in 64 KB space - A000:0H to BFFF:FH Address Range
0	1	First 256 KB in 1MB space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 KB in 1MB space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 KB in greater or equal to 1 MB space - 0000:0H to FFFF:FH Address Range

Bits 5 and 4 can be used in conjunction with external control of EMEM to map video memory decode above the 1 Mbyte address space.

Bit 3

Enable Alternate Address Offset Register PR0B

Bit 2

Enable 16-bit bus for Video Memory
When set to 1, $\overline{DS16}$ will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ be inactive.

Bit 1

This bit will directly reflect signal pin $\overline{ROM16}$ in AT mode or $\overline{CDDS16}$ in MCA mode.
When set to 1, the BIOS ROM has 16 bits data path.

If set to 0, the BIOS ROM data path is 8 bits wide. A pull-up on MD (1) sets this bit to 0 at power on reset. $\overline{ROM16}$ will have the value of 0 when this bit is set.

Bit 0

If set to 1 the BIOS ROM is mapped out. Pull-up resistor latches 0 after power up. A pull-up on MD(0) sets this bit to 0 at power on reset.

9.11.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode

Bit 6

0: VGA or EGA mode
1: Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overridden by setting PR15(2). This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE:
Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane selected table shown above.

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Bit(4:3)

Character clock period control

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE:
The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK.
Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

9.11.4 PR3 - CRT Lock Control Register Read/Write Port=3CF, Index = 0H

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

9.11.5 WD90C00 CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT controller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the sections below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 --Horizontal Total Characters per scan
CRT controller register 01 --Horizontal Display Enable End
CRT controller register 02 --Start Horizontal Blanking
CRT controller register 03 --End Horizontal Blanking
CRT controller register 04 --Start Horizontal Retrace
CRT controller register 05 --End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) - Vert. Display Enable End bit 9
CRT controller register 07(Bit1) - Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 --- Vertical Total
CRT controller register 07(Bit7) ---Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ---Vertical Total bit 9
CRT controller register 07(Bit3) ---Start Vertical Blank bit 8
CRT controller register 07(Bit2) ---Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ---Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ---Start Vertical Blank bit 9
CRT controller register 10 ---Vertical Retrace Start
CRT controller register 11 [Bits(3:0)] ---Vertical Retrace End
CRT controller register 15 ---Start Vertical Blanking
CRT controller register 16 ---End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ---Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock horizontal timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7=1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7=0.

9.11.6 PR4- Video Control Register Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).

Bit 6

Select PCLK equal to VCLK.
0=PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1=PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

Bit 4

Tri-state the memory control outputs. The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Shift register control. It configures the video shift registers for extended 256-color mode.

9.11.7 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PRO-PR4 Unlock
1	PRO-PR4 Unlock
0	PRO-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

Bit 7 CNF(7) [READ ONLY]
Bit 6 CNF(6) [READ ONLY]
Bit 5 CNF(5) [READ ONLY]
Bit 4 CNF(4) [READ ONLY]
Bit 3 CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits and cleared to 0 by reset. They control writing to PR registers PR0-PR4 as follows:

2 1 0	PR0-PR4
0 X X	Write protected
X 1 X	Write protected
X X 0	Write protected

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9.11.8 PR10 Unlock PR11-PR17 Read/Write Port = 3?5, Index = 29

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to PR registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

9.11.9 PR11 EGA Switches Read/Write Port = 3?5, Index = 2a

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

9.11.10 PR12 Scratch Pad Read/Write Port = 3?5, Index = 2b

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power up.

9.11.11 PR13 Interlace H/2 Start Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE:
In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

9.11.12 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2d

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in MICRO CHANNEL operation.

Bit 6

Vertical double scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N=2(n+1)

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced mode.
Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 end bits (4:0). Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

9.11.13 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2e

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

Bit 6

Low VCLK. Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ)>2

Bit 5

Latched VCLK1 and VCLK2. This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting This bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.
Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30-40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to 1 in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.
The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

Note:
The above Character Map Select functions override the functions override the functions of PR2(5) and PR2(2).
This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin $\overline{BLNK}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0=$\overline{BLNK}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = $\overline{BLNK}$ supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

9.11.14 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External reg. 46E8H lock
6	CRTC Address count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H register.

Setting this bit to 1 causes $\overline{EBROM}$ output to be forced high (Inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64 K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256KB
0	1	128K
1	X	64K

Bit (4:3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

Bit 1

VGA Memory Mapping
Setting this bit to 1, selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H)
Programming this bit to 1 causes output $\overline{\text{WPLT}}$ to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C00 is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

9.11.15 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30H

BIT	FUNCTION
7 - 1	Reserved
0	Map out 2K of BIOS ROM

Bit (7:1)

Reserved.

Bit (0)

Map out 2K of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0H - C67F:FH.
Power on reset sets this bit to 1. Clearing this bit to 0, enables access of all 32K addresses of the BIOS ROM from C000:0H - C7FF:FH.

9.12 INTERNAL I/O PORTS

9.12.1 AT Mode Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused

Bit 4

Setup
Puts WD90C00 into setup mode where only I/O port 102H is accessible.

Bit 3

Enable I/O and Memory Accesses. Does not affect Port 46E8H and 102H.

Bit(2:0)

Unused Internally
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4K pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

9.12.2 Setup Mode Video Enable (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C00 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C00 after power on in the MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the VGASETUP ($\overline{EIO}$) signal pin is active low, the WD90C00 is in setup mode and port 102H can be accessed.

9.13 VIDEO RAMDAC PORTS

The Video RAMDAC is implemented externally to the WD90C00. However, the $\overline{WPLT}$ and $\overline{RPLT}$ signals required by the RAMDAC are provided by the WD90C00. Setting PR(16) bit 0 to a 1 forces $\overline{WPLT}$ to a high level disabling I/O writes to the RAMDAC. Normally, the $\overline{WPLT}$ and $\overline{RPLT}$ signals to the RAMDAC are generated when the following I/O ports are written to or read from.

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
*3C7H	*DAC state (read only)	*If bits 0/1 =1, DAC in read operation. When bits 0/1=0,DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	Read/write
3C9H	PEL data register (read/write)	Three successive read/write bytes.

* NOTE: This port is internal to WD90C00.

9.13.1 WD90C00 Configuration Bits CNF (8:2) Non-Read/Non-Write Hardware Port

BIT	FUNCTION
8	Display Status
7 - 4	General Purpose Status
3	Video Clock Source Control
2	Bus Architecture Select

Bits CNF (3:2) are latched internally at power on reset from the corresponding memory data bus pins MD (3:2) while CNF (8) is latched from MD (11). They are connected to the external pull-up or pull-down resistors. Pull-up resistor sets MD(3:2) to logic 1 while pull down resistor sets MD(11) to logic 1. Note, that the configuration bits (3:2) are not readable since they are latched after power up. However, the configuration register bits (8:4) are readable after power up as PR5 bits (7:3). They appear as general purpose read only status bits in the PR5 register.

CNF (8)

ANALOG/TTL DISPLAY STATUS BIT
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched Low. This bit controls no internal functions and is read only as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F).

0 = Analog (VGA - compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

GENERAL PURPOSE STATUS BITS
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

VIDEO CLOCK SOURCE CONTROL
This bit cannot be written or read as I/O port pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C00 pins VCLK1 and VCLK2 as inputs or outputs.

0=For inputs.
1=For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. Also, VCLK1 and VCLK2 outputs equal to bits 2 and 3 of the Miscellaneous output register at 3C2H respectively when PR15 bit 5 is set to 1.

CNF (2)

Bus Architecture Select
This bit cannot be written or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.

0 =Micro Channel architecture

1=AT BUS architecture

9.14 EXTERNAL I/O PORT CONSIDERATIONS

9.14.1 Video Subsystem Enable Register Micro Channel Only Read/Write Port 3C3H

BIT	FUNCTION
7 - 1	Unused
0	Video Subsystem Enable

Bit(7:1)

Reserved

Bit 0

When this bit is set to 1, the I/O and memory address decoding for the video subsystem are enabled. When set to 0, this bit disables the video I/O and memroy address decoding. Accessing this register does not affect addressing port 102h POS register.

The WDI WD90C00 does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I/O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I/O port 102H bit O) of the Programmable Option Select (POS). When, WD90C00 is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally.

A.0 APPENDIX

A.1 EGA MODE

For the register definitions that have not changed from the VGA modes, refer to the VGA description. Only the differences between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0 unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are not covered in this procedure. These steps are briefly defined to outline the EGA mode entry.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pull-up or pull-down resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.
2. Unlock all the PR registers.
3. Program PR2(6) to 0 for EGA mode.
4. Set PR4 bit 1 to logic 1 for EGA compatibility.
5. Load PR11(7:4) with EGA Configuration switches by using pull-up or pull-down resistors on pins MD(15:12). (Pull-up resistor causes logic 1 to be latched after power on reset.)
6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the suggested steps listed below:

a) Initialize all the registers.
b) Lock CRT controller registers.
c) Force Clock Control rate of the CRT controller.
d) Set EGA emulation mode by programming:
PR11(3)=1; Set EGA emulation on PS/2 type display
PR14(6)=1; Vertical double scan
PR11(2)=1; Lock clock select
PR11(0)=1; Lock 8/9 dot timing.
PR14(7)=1; Enable IRQ (optional)
e) Lock the PR registers PRO-PR5 and PR10-PR17.
f) Read protect PR registers.

8. When EGA is required on a TTL monitor, the suggested steps are:

a) Initialize all the registers.
b) Set EGA TTL mode by programming:
PR11(3)=0;EGA TTL
PR14(7)=1;Enable IRQ
PR15(6)=1;Set Low Clock
PR14(7)=1;Enable IRQ
c) Lock PR registers PRO-PR5 and PR10-PR17
d) Read protect PR registers.

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlights all the EGA mode registers.

A1.1 EGA Registers Summary

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All Register addresses are in hex.
3. "?"= "B" in Monochrome modes or "D" in Color modes.
4. "*" = Identical responses from I/O ports 3C0 and 3C1.

A.2 GENERAL REGISTERS

Only the general registers and the bit definitions that differ between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

A.2.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Not used.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 Mhz clock (VCLK0) is selected.
0	1	16.257 Mhz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

A.2.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not used

Bit 4

EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not used = 1

A.2.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not used

Bit 6

EGA: Not used = 1

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: Not used = 1

Bit 1

EGA: Unused

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

A.2.4 Feature Control Register (Write Port 3?A)

Bits (7:0)
EGA: Not used

A.3 SEQUENCER REGISTERS INDEX PORT = 3C4, PORT 3C5

A.3.1 Clocking Mode Register (Index = 01)

Bits (7:4)
EGA: Not Used

Bits (3,2)
EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1
EGA: Set to zero

Bit (0)
EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

A.3.2 Character Map Select Register (Index 03)

Bits (7:4)
EGA: Not Used

Bits (3:2)
EGA: Character Map Select A

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

Bits (1:0)
EGA: Character Map Select B

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8K
0	1	1	Second 8K
1	0	2	Third 8K
1	1	3	Fourth 8K

A.3.3 Memory Mode Register (Index = 04)

Bits (7:3)
EGA: Not Used

Bits (2:1)
EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0
EGA: Alpha mode bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

A.4 CRT CONTROLLER REGISTERS INDEX PORT= 3?4 DATA PORT = 3?5

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, "?" implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

A.4.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Registers Address index where the data is to be written.

A.4.2 Horizontal Total Register (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

A.4.3 End Horizontal Blanking Register (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: They define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

A.4.4 End Horizontal Retrace Register (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

A.4.5 Vertical Total Register (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

A.4.6 CRT Controller Overflow Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to CRT Controller Overflow Register bits (4:0) in the VGA section.

A.4.7 Preset Row Scan Register (Index = 08)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bits (4:0) definitions in the VGA section.

A.4.8 Maximum Scan Line Register (Index = 09)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Maximum Scan Line Register Bits (4:0) definition in the VGA section.

A.4.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

A.4.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

A.4.11 Vertical Retrace Start Register (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

A.4.12 Vertical Retrace End Register (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not used

Bit 5

Enable Vertical Retrace Interrupt.
EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

Clear Vertical Retrace Interrupt.
EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

A.4.13 Underline Location Register (Index = 14)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

A.4.14 End Vertical Blanking Register (Index = 16)

Bits (7:5)

EGA: Not used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

A.4.15 Mode Control Register (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.5 GRAPHICS CONTROLLER REGISTERS INDEX PORT = 3CEH DATA PORT = 3CFH

A.5.1 Read Map Select Register (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

A.5.2 Mode Register (Index = 05)

Bit (7:6)

EGA: Not Used

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per the table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

A.6 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

A.6.1 Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec. Green/Inten	VID 4
3	Sec. Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

A.6.2 Mode Control Register (Index = 10)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

A.6.3 Overscan Color Register (Index = 11)

Bits (7:6)

EGA: Not Used

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

A.6.4 Color Plane Enable Register (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer per the table listed:

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (Port 3?A)	
		BIT 5	BIT 4
0	0	VID 2(Red)	VID 0 (Blue)
0	1	VID 5(SRed)	VID 4 (SGreen)
1	0	VID 3(SBlue)	VID 1 (Green)
1	1	VID 5(SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

A.6.5 Horizontal PEL Panning Register (Index = 13)

Bits (7:4)

EGA: Not Used

Bits (3:0)

EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

A.7 APPLICATIONS

The WD90C00 applications section is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), monitor, and clock. The description and block diagrams are generic. No attempt is made to present schematic level details. Currently available application notes, technical briefs, and referenced literature at the end of the data book should supplement the information provided in this section. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 11 through 20 are shown along with their brief description on the subsequent pages.

Figure 11 highlights the various WD90C00 Processor, memory, and I/0 interfaces.

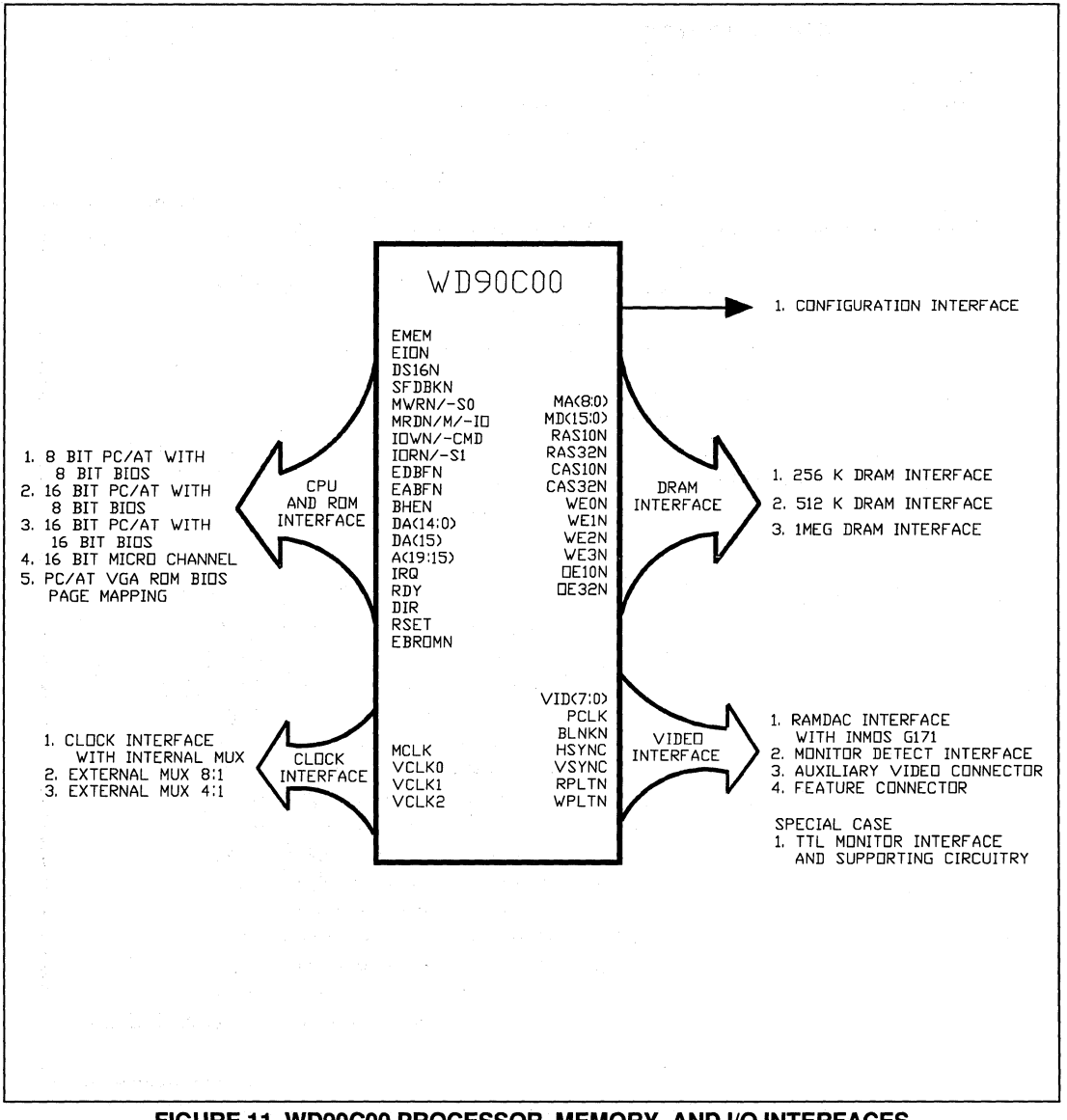

FIGURE 11. WD90C00 PROCESSOR, MEMORY, AND I/O INTERFACES

Figure 12 shows a block diagram of the WD90C00 with 8-bit PC/AT interface using an 8-bit BIOS. The system data bus SD(7:0) and address bus SA(19:0) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: "*" = Logic AND function, "/" = Inverted function, and "+" = Logic OR function.

"*" NOTE PA(14:12) CAN BE FROM PAGE MAPPING LOGIC.

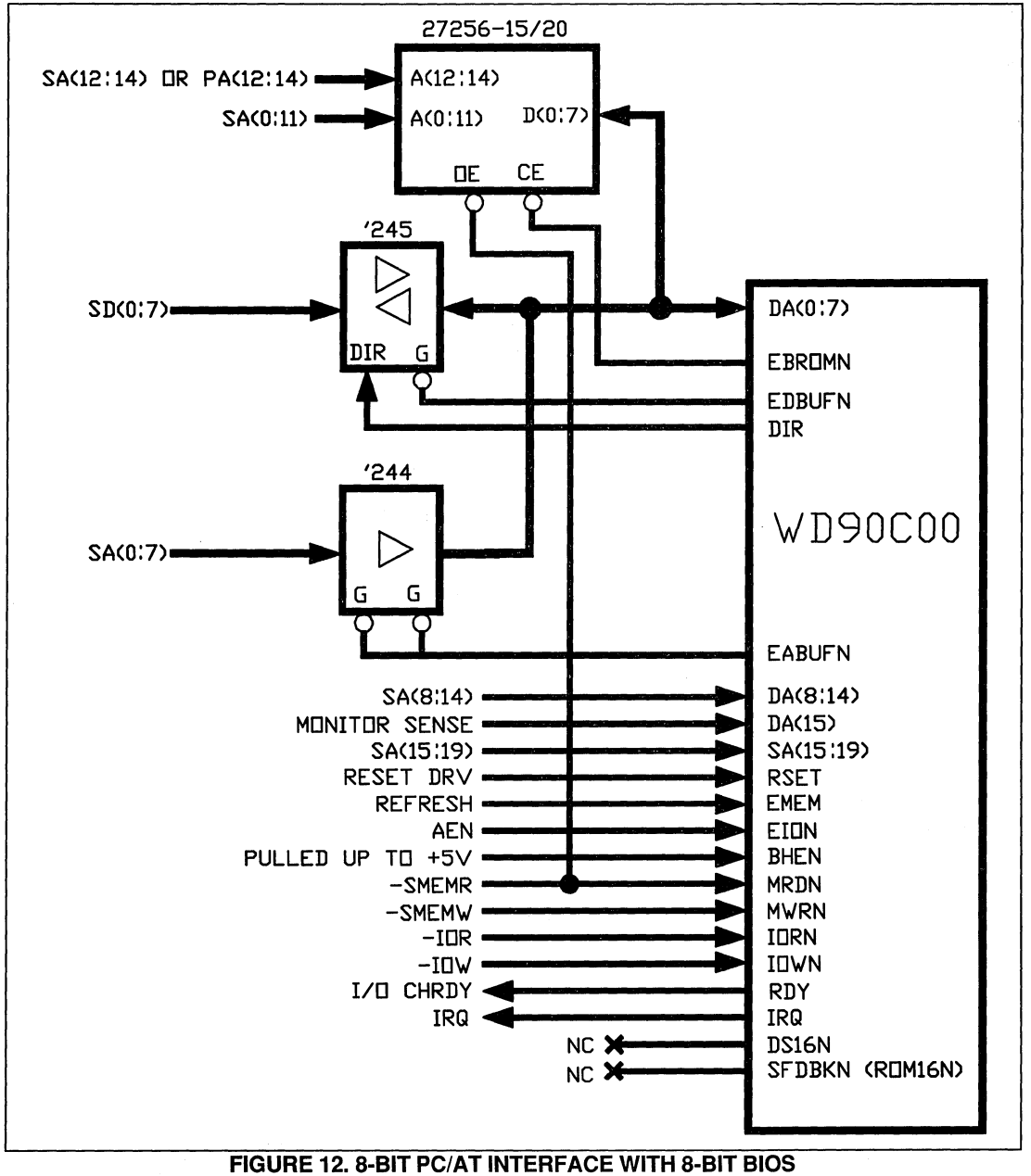

FIGURE 12. 8-BIT PC/AT INTERFACE WITH 8-BIT BIOS

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Figure 13 illustrates 16-bit PC/AT interface with 8-bit BIOS using WD90C00. The processor data bus SD(15:0), and the system address bus SA(19:0) are shown. Associated address and data bus buffers, BIOS ROM, and auto monitor sense are also shown in it. Note, PA (14:12) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBFN1.

/EDBFN1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N + EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N.

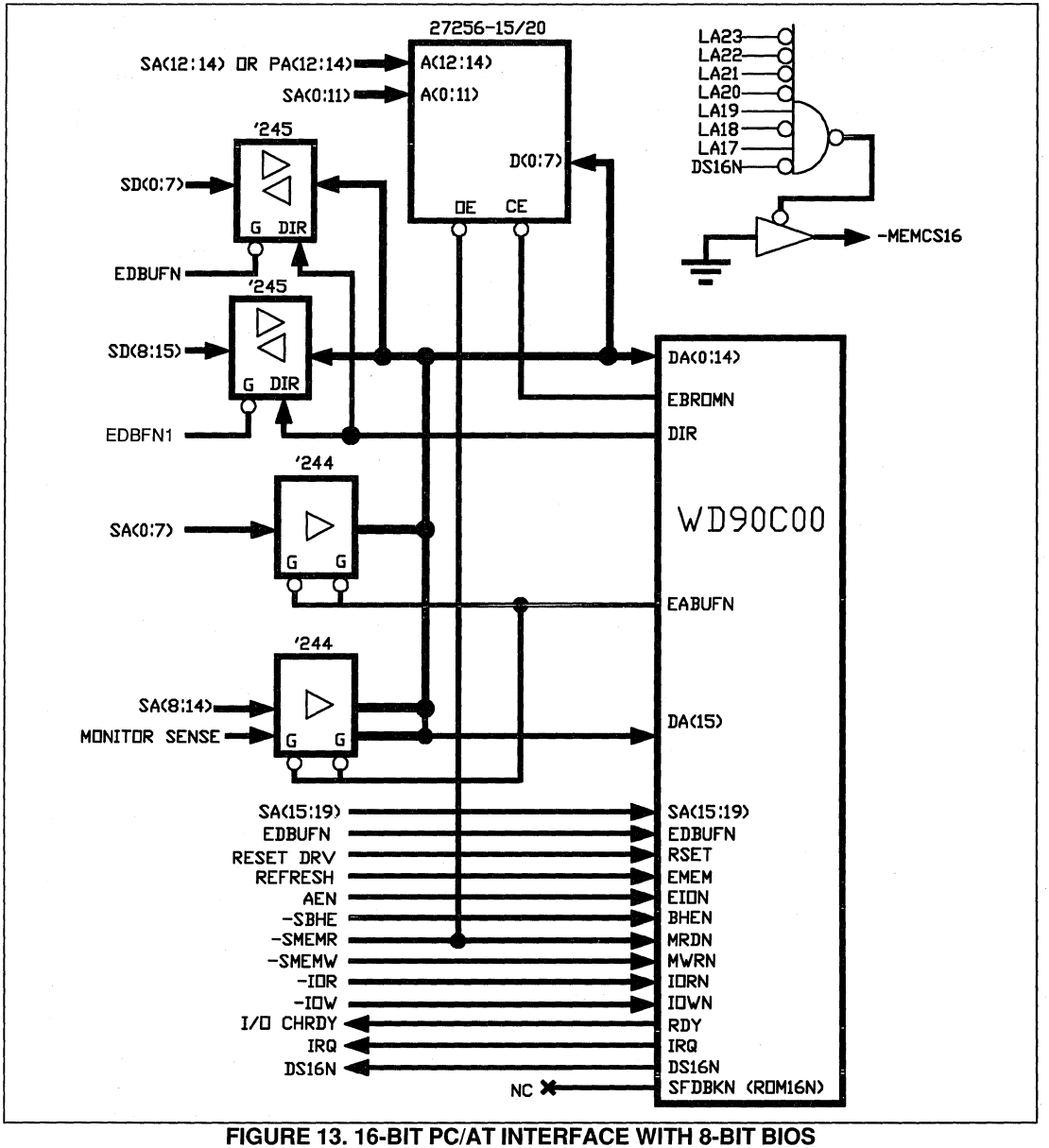

FIGURE 13. 16-BIT PC/AT INTERFACE WITH 8-BIT BIOS

Figure 14 illustrates a 16-bit PC/AT interface with a 16-bit BIOS ROM implementation using WD90C00. The system data bus SD(15:0), address and data bus buffers, and auto monitor sense input is presented. The (16K X 8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation is limited to certain bus speeds as SA15 and SA16 are used.

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N + /EBROMN * /SBHE * SA0 * /ROM16N * /SMEMR

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N + /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN.

12

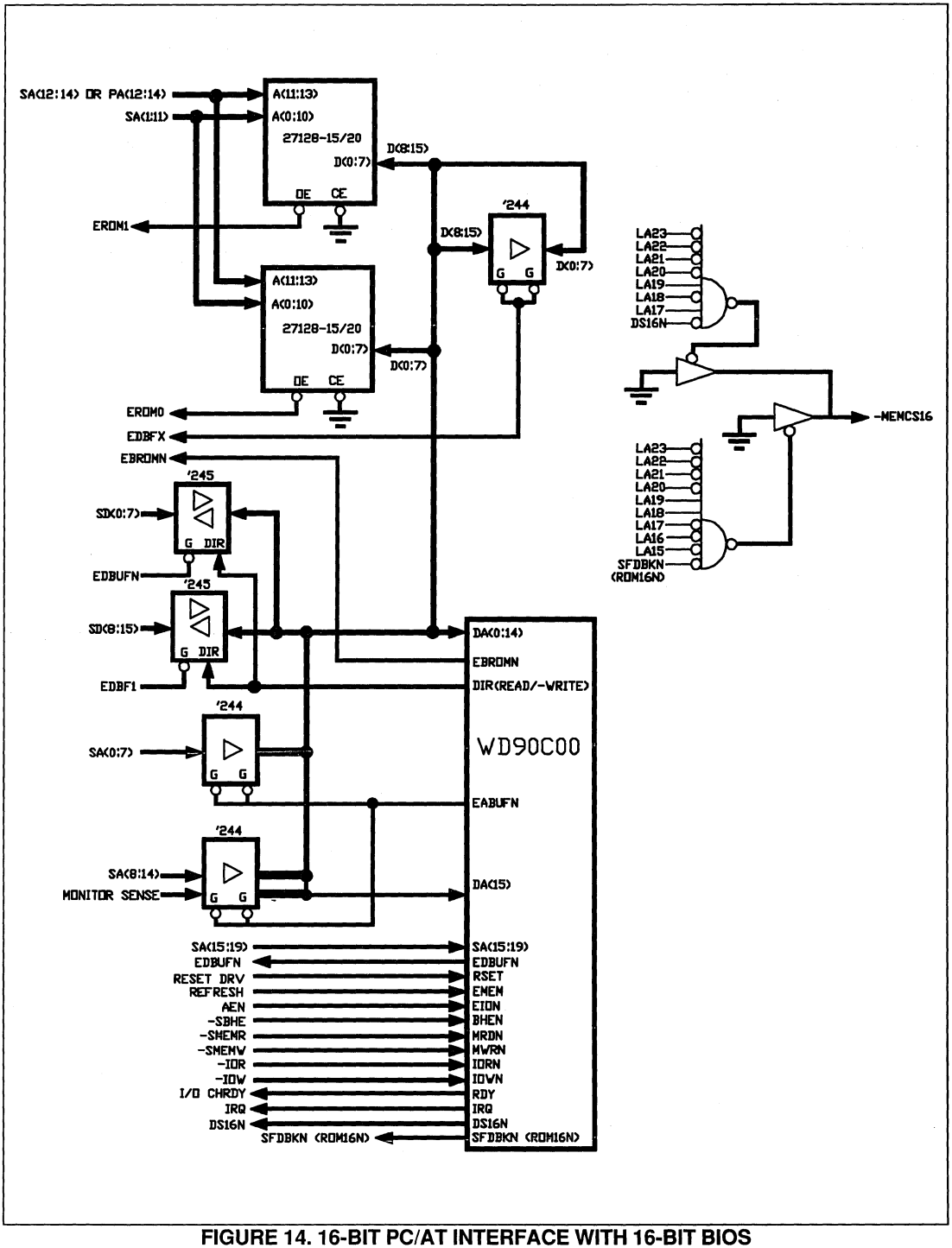

FIGURE 14. 16-BIT PC/AT INTERFACE WITH 16-BIT BIOS

Figure 15 illustrates the WD90C00 and a 16-bit Micro Channel interface. The system data bus upper byte bits D(14:8) and lower data bus byte D(7:0) are sampled and buffered for the WD90C00 input pins DA(14:0). Likewise, system address byte upper bits A(14:8) and lower address byte A(7:0) are buffered and gated to the WD90C00 input pins DA(14:0). The monitor sense input buffer and D15 are gated into the DA15 input of the WD90C00. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the WD90C00. Setup must be latched (OFF) with -CMD.

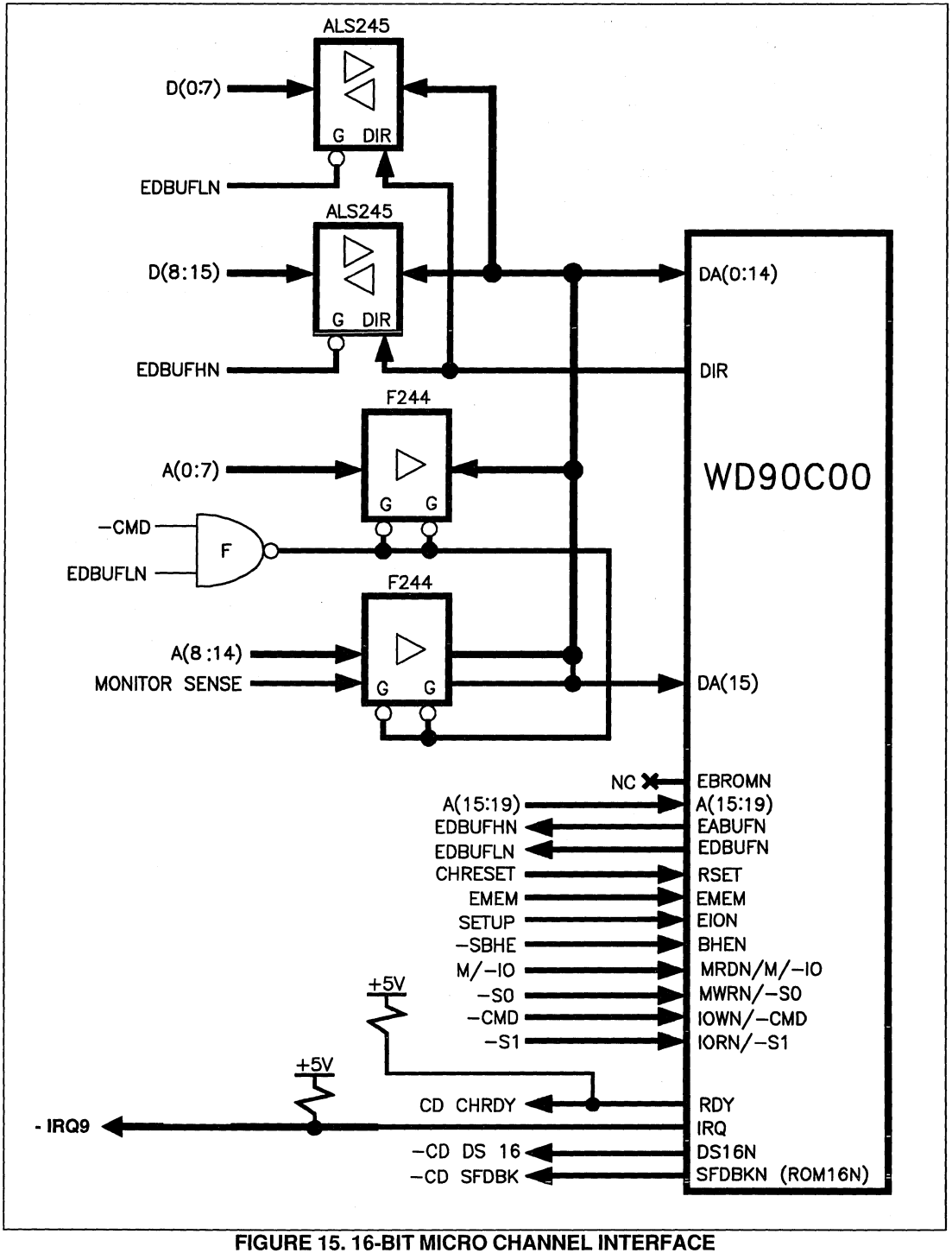

FIGURE 15. 16-BIT MICRO CHANNEL INTERFACE

Figure 16 illustrates the WD90C00 with 1024 KB video memory organization using four 256 KB maps. Each 256 KB map is made from two (256K X 4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles. The WD90C00 also supports 256 KB, or 512 KB video memory organization using (64K X 4) DRAM modules. The 256 KB configuration just does not have MA8 connected to the DRAMs. The 512 KB configuration uses MA8 as select to multiplex the $\overline{CAS10}$ and $\overline{CAS32}$ signals to two 256 KB banks of eight 64K X 4 DRAMs.

Figure 17 illustrates the WD90C00 and RAMDAC (INMOS G171) interface block diagram for analog monitors.

NOTE:
LA(1), LA(0) ARE LATCHED ADDRESSES.
DA(7:0) ARE MULTIPLEXED DATA BITS.

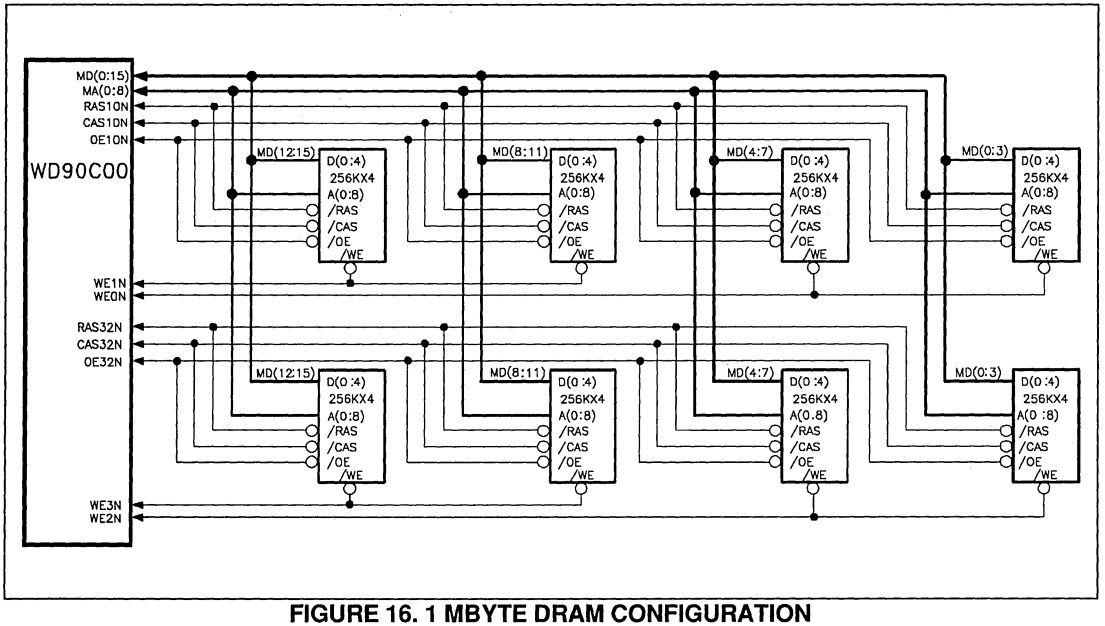

FIGURE 16. 1 MBYTE DRAM CONFIGURATION

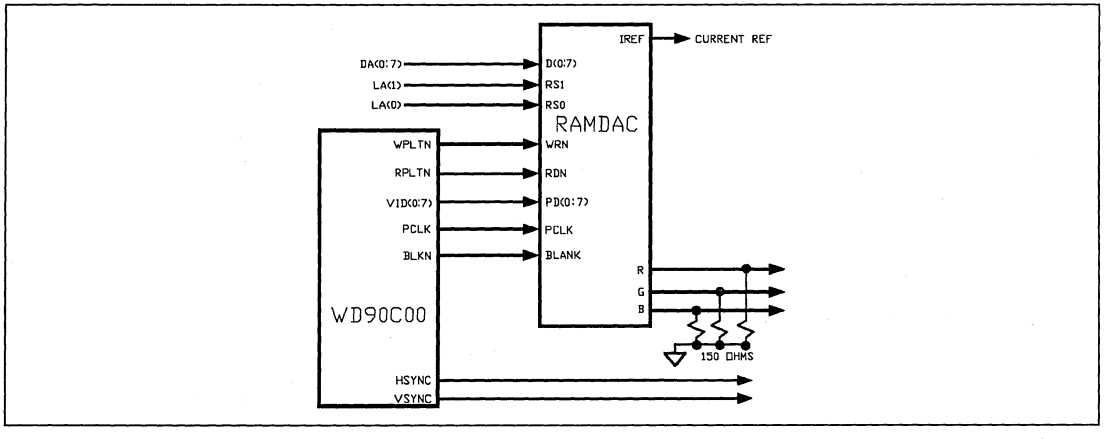

FIGURE 17. RAMDAC INTERFACE

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Figure 18 illustrates the WD90C00 and TTL monitor connections.

NOTE:
1. VGA/TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.
2. MD(15:12) may also be connected as the EGAswitches if desired. See PR register and Pin out sections for more details.
3. For AT applications using WD90C00, install the IRQ9 resistor.
4. Transistor 2N2222A is used to emulate a Monochrome and a Color Display connection.

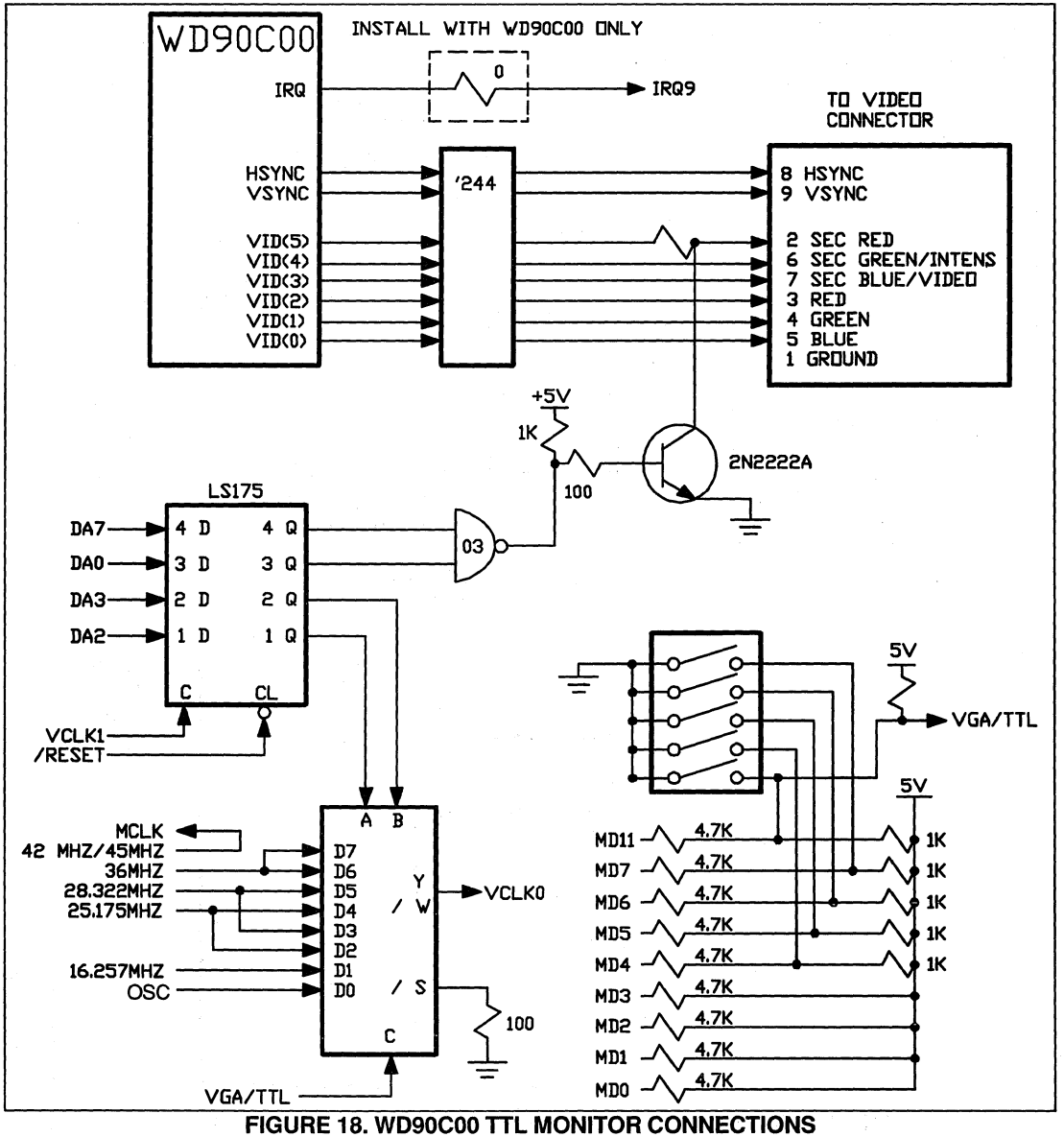

FIGURE 18. WD90C00 TTL MONITOR CONNECTIONS

Figure 19 presents WD90C00 with external oscillators at the clock pins configured as inputs. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H BIT 3	3C2H BIT 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C00 signal pins (VCLK1, VCLK2) inputs with a 10K Ohm resistor.

Figure 20 illustrates WD90C00 pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high with a 4.7K Ohm resistor and PR 15 bit 5 = 1 .

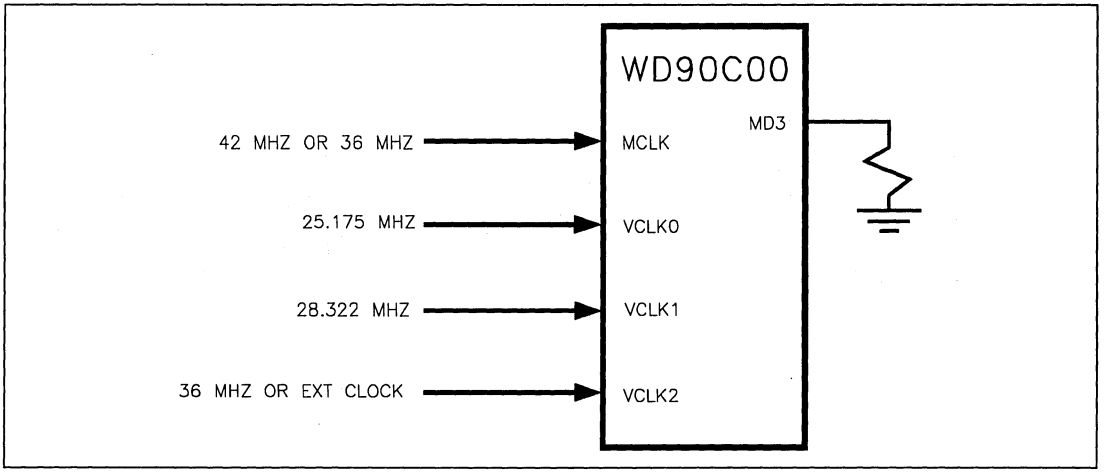

FIGURE 19. CLOCK INTERFACE

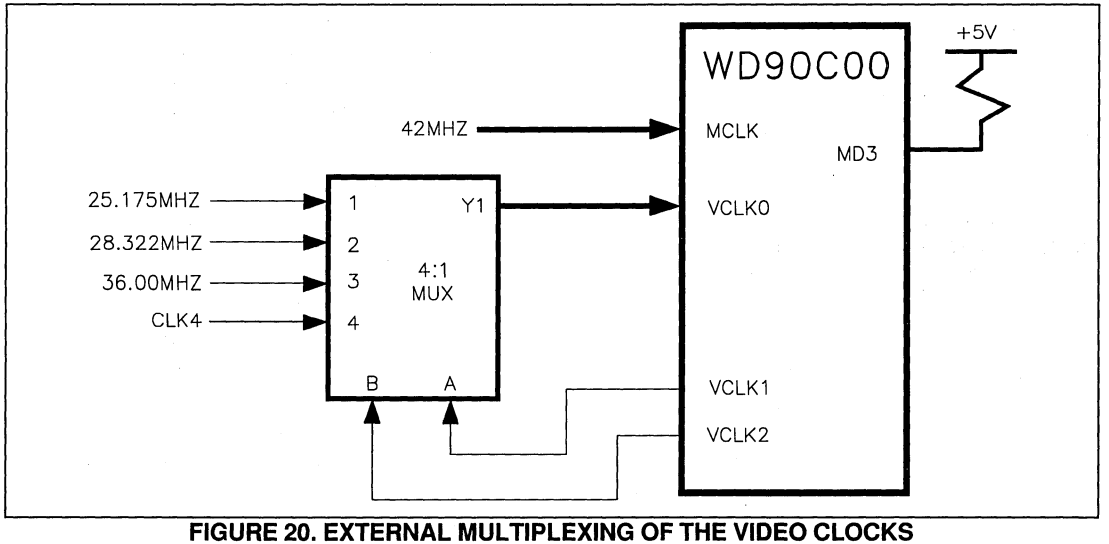

FIGURE 20. EXTERNAL MULTIPLEXING OF THE VIDEO CLOCKS

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A.8 WD90C00 POWER UP CONFIGURATION

The WD90C00 uses the MD(0:7) and MD(11:15) input pins to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0), PR11(7:4), and CNF(8:2) are the internal registers that are configured on power up. CNF(3:2) and PR11(7:4) will latch a noninverted value (pull up register = 1) into it and the other will latch an inverted value. For more details see the PR register and Pin out sections.

PR 1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the WD90C00. A value will map it in.

PR 1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the WD90C00 that the ROM BIOS data path is 16 bits. The WD90C00 will bring SFDBKN active low in AT mode (static signal) and SFKBKN can be used to externally generate -MEMCS16 (of the AT bus) for 16 bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

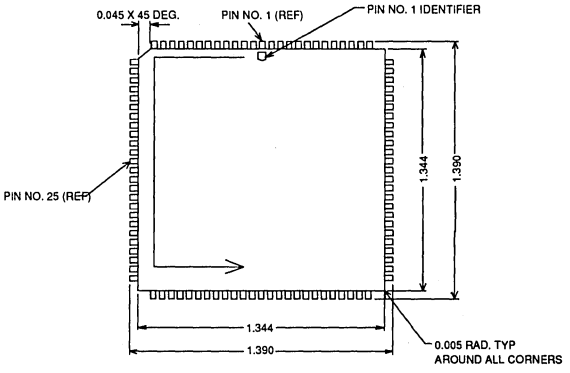
PR11(4:7) bits will latch the EGA switch settings (SW4:SW1) after power up. A pull up resistor will set the appropriate PR11 register bit (4:7) to a logic 1.

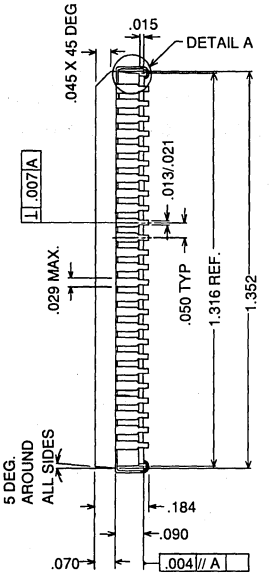
CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the WD90C00 for IBM PC/XT/AT architecture. A value of 0 will configure the WD90C00 for IBM PS/2 Micro Channel Architecture. WD90C00 Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the WD90C00 pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

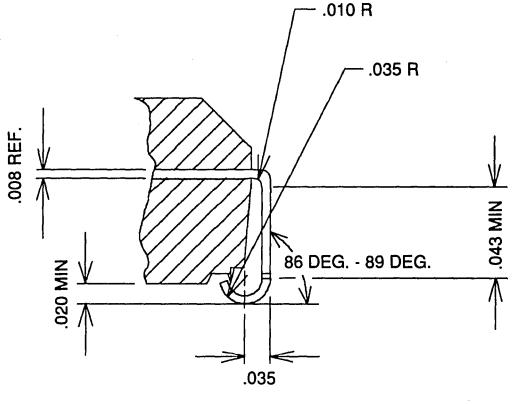
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through PR Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If unused by the BIOS, they are available to the application software.

CNF(8) will indicate that a TTL display or an analog monitor is present in the video subsystem. A Pull up resistor on MD(11) causes CNF(8) to be latched 0 indicating that VGA compatible analog display is in the video subsystem.





DETAIL A



NOTE: ALL DIMENSIONS ARE IN INCHES.

FIGURE 21. 100-PIN PLCC PACKAGE DIMENSIONS

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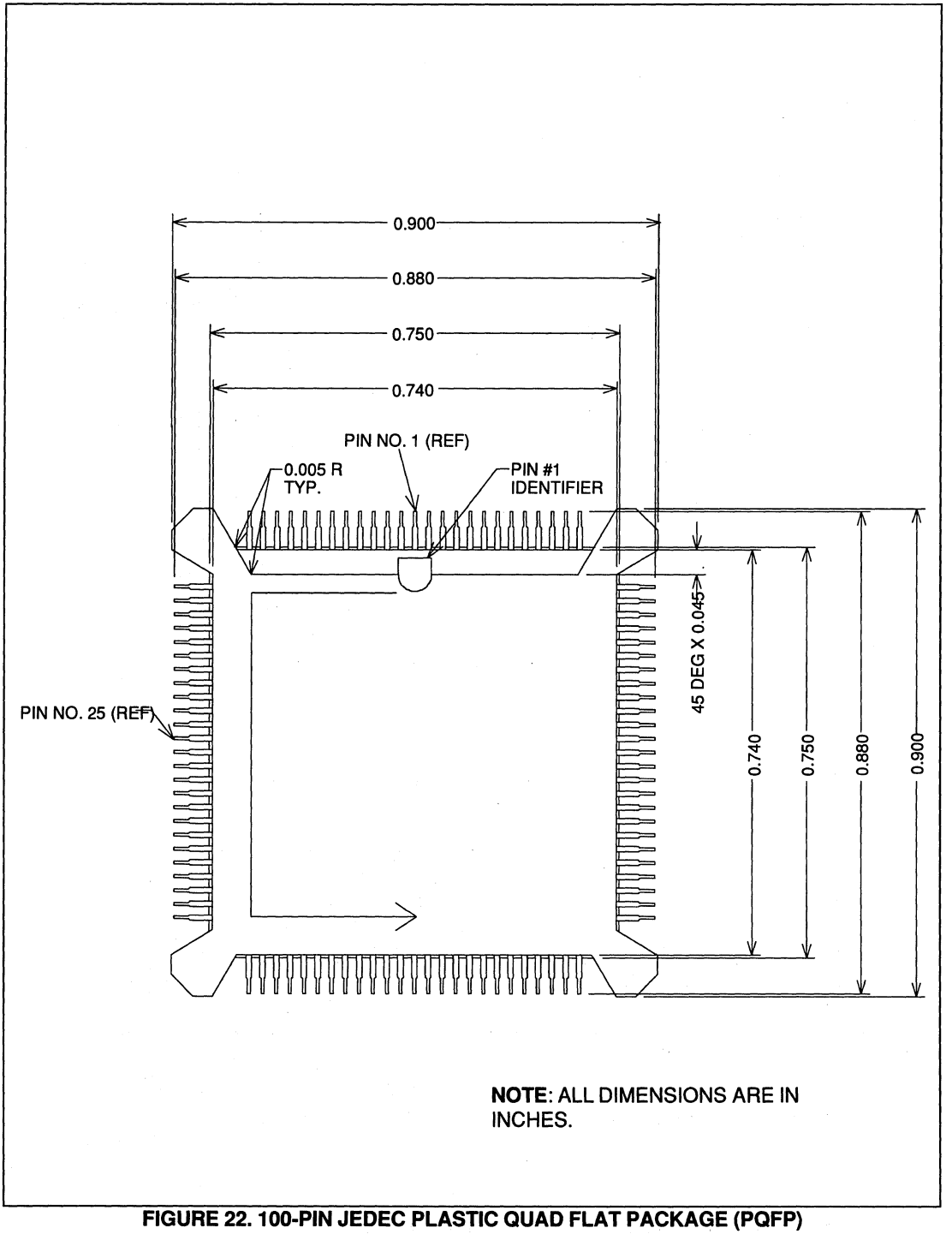
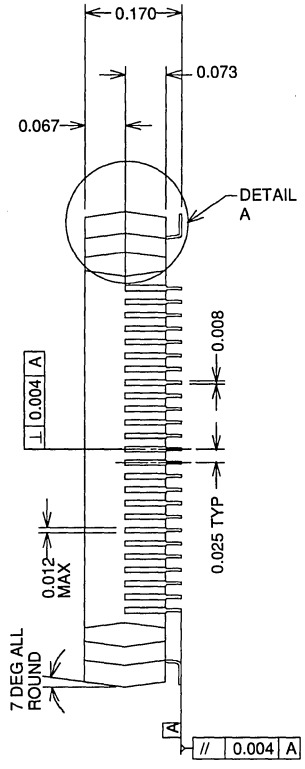
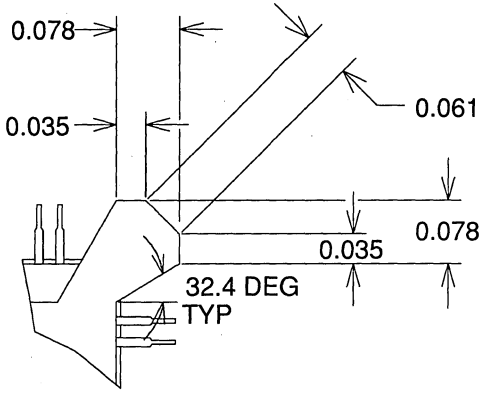


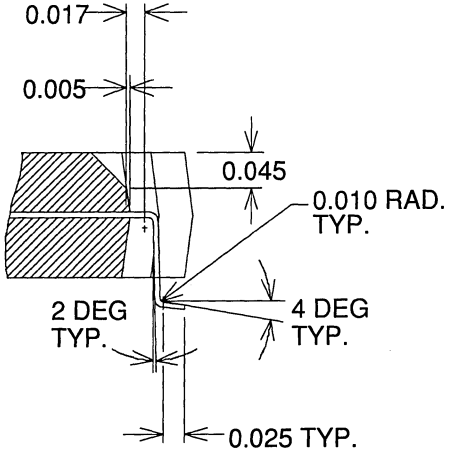
FIGURE 22. 100-PIN JEDEC PLASTIC QUAD FLAT PACKAGE (PQFP)



SIDE VIEW



BUMPER DETAIL



DETAIL A

NOTE: ALL DIMENSIONS ARE IN INCHES.

FIGURE 23. 100-PIN JEDEC (PQFP) PACKAGE DIMENSIONS

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A.9 REFERENCES

A list of references for generating the WD90C00 data sheet is shown below:

- IBM Personal Computer Hardware User Guide (IBM # 6322510)
- IBM Personal Computer XT Hardware User Guide (IBM # 6322511)
- IBM Personal Computer AT hardware User Guide (IBM # 6280066)
- IBM Personal System 2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM Personal Computer AT Technical Reference Manual (IBM # 6280070)
- IBM Personal System 2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM Personal System 2 BIOS Reference Manual (IBM # 68x2260)
- Personal Computer Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual
- Paradise OEM Technical Publication Manual

The customers are urged to refer to the manuals listed above and supplement their knowledge from other books and literature available in the market.