WD90C24A/A2 Windows Accelerated High Resolution VGA LCD Controller for Low-Power Applications

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

LIST OF TABLES (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

This document introduces and describes the Western Digital® WD90C24A and WD90C24A2 Windows Accelerated High Resolution VGA LCD Controllers for Low Power Applications (hereinafter referred to as the WD90C24A/A2 Controller). Unless otherwise specified, all information in this document applies to both controllers. Specific differences in the two controllers are described in Appendix C.

The Western Digital WD90C24A is a 0.8 micron CMOS VLSI device and the WD90C24A2 is a 0.9 micron CMOS VLSI device. Both devices have the capability to drive flat panel displays and standard CRTs. The WD90C24A/A2 allows simultaneous display for a CRT and a monochrome dual-panel, or a CRT and a color panel. Both devices are backwards compatible with previous video standards including MDA, EGA, and CGA.

The WD90C24A/A2 provides enhanced power management with 3.3 VDC power input or a mix of 3.3 VDC and 5 VDC power input. Its performance-scaling capability makes it an ideal video solution for low battery drain portable computer applications.

1.2 WD90C24A/A2 FEATURES

- Hardware Windows Acceleration
- Hardware Bit Block Transfers (BITBLT)
- Hardware line draw
- Programmable Hardware Cursor (64 by 64 by 2)
- Simultaneous Display on all CRT and LCDs for all Standard Modes
- Programmable Power Management
- Support for 256K color STN and color TFT LCDs
- Single chip for 8-bit or 16-bit AT Bus Interface and 32-bit VESA VL-Bus (local bus) interface
- Supports 16-bit or 32-bit memory interface
- Integrated 16-bit High Color RAMDAC
- Integrated Programmable Pixel Clock Synthesizer
- Integrated Programmable Dithering Logic for the Highest Contrast Video with Utility Support.
- Support for 64K simultaneous colors on CRT, single-panel color STN LCD, and color TFT LCD
- Direct interface to single-panel (1/480) or dual-panel (1/240) monochrome STN LCD, single or dual panel color STN or color TFT LCD and plasma display
- Provides 64 True Shade gray scale support for monochrome STN LCD flat panel display
- Up to 65 MHz video clock for the CRT display, up to 65 MHz for color TFT LCD display, and up to 50 MHz video clock for the monochrome STN LCD display
- Up to 50 MHz memory clock
- Supports memory configuration of 256 Kbytes to 1 Mbyte with 256K by 16, or 256K by 4 DRAMs
- With 256K of DRAM installed, supports all IBM VGA modes for CRT and LCD display
- With 1 Mbyte of DRAM installed, supports high resolution graphics with up to 1024 by 768 by 256 colors in CRT and flat-panel modes.
- Provides host data bus interface for 8- or 16-bit CPU I/O and memory cycles.
- Supports high 16-bit color for CRT or flat panel display at up to 640 by 480 resolution for 64K color simultaneous display on one frame for CRT, color STN LCD, and color TFT LCD displays
- Fast page display memory fetching for both graphic and text modes
- Programmable virtual memory addressing for CPU memory address space
- Four levels of write cache for zero wait state CPU operation during memory write
- Emulates planar mode addressing for packed pixel mode operation to achieve faster block transfers
- Operates with 5 volt and 3.3 volt power supplies (mixed voltage operation)

- Intelligent power management control to reduce the power requirement for the display subsystem
- Supports 132-column text mode
- Provides a signature analyzer to help with IC and board-level test of video data output from the controller.
- PINSCAN I/O mapping allows the WD90C24A/A2 to enter a test mode to enable quick open and short checks for board-level test
- Uses 208-pin EIAJ package
- Directly drives all 640 by 480 (400) monochrome and color flat panel displays, such as STN, TFT, EL, and plasma displays without external components

1.3 ENHANCEMENT FEATURES

The following features were added to the WD90C24A/A2 controller to enhance its performance over the WD90C24 controller.

- Provides a Dual panel (1/240) color STN LCD interface.
- Supports monochrome 640 by 480 single-panel (1/480) STN, 4-bit or 8--bit, flat-panel
- Provides algorithm enhancement to support vertical screen expansion in text mode. Raster lines are duplicated above or below the character block. This takes care of not creating breaks in continuous vertical lines.
- A Strip Line Draw algorithm is implemented in hardware to further improve Windows performance.
- I/O pins are remapped to improve the ICT (In-Circuit Test) of the device. Because there are more input pins than output pins, pairs of input pins had to be ORed to each output. There was a conflict in 3 pairs of pins in that they were next to each other, which would not allow for a "short test" on those pins. These 3 pairs of pins were AMD12 and AMD3, BMD12 and BMD3, and EBROM and VLBICS.
- Supports hardware cursor for Dual panel (1/240) monochrome STN LCD panels.
- The PCLK output (pin 175) can now be turned off by a programmable bit to reduce EMI emissions.
- Configuration bit (CNF15) is added to accept the 2X clock from the new Intel S-series 486 microprocessors.
- Supports 800 by 600 color TFT panel.
- Supports enhanced power-down mode on VESA-VL local bus (REFLCL)
- In Power-down mode, register PR4 bit 5 is used to turn off the panel data and control pins (XSCLK, RPTL/, WPTL/, UD(7:0), LD(7:0), FP, LP and FR). In the WD90C24 these pins are tristated.

1.4 ADDTIONAL FEATURES OF THE WD90C24A2 CONTROLLER

The following features and characteristics apply only to the WD90C24A2 controller.

- Supports Monochrome TFT LCD Interface
- Provides fixed high-color modes (32K and 64K) so that these modes operate with the normal VCLK/MCLK ratio
- Drive strength for the VLBICS signal is increased from 8 mA to 16 mA
- Drive strength for the Local Bus data signals PD[30:16] is increased from 3 mA to 8 mA. The drive strength of PD31 and SD[15:0]) remains as it was.

1.5 ORDERING INFORMATION

The WD90C24A and WD90C24A2 controllers are supplied in a 208-pin MQFP package under the following order numbers:

CONTROLLER	ORDER NUMBER
WD90C24A	90C24AZZ00
WD90C24A2	90C24A2ZZ00

1.6 DOCUMENT SCOPE

In addition to this introduction to the WD90C24A and WD90C24A2 controllers, the following sections of this document provide a description of the controller architecture and related interfaces, memory configurations, signal descriptions, and internal register descriptions. In addition, this document contains application information for the

hardware cursor, hardware BITBLT, hardware line drawing, embedded clock generator, internal RAMDAC, configuration registers, and associated application and program notes. Also included are the device specifications, timing information, and package dimensions. Special features of the WD90C24A/A2 including the signature analyzer, and I/O mapping for test purposes are also described.

This document includes the following four appendices:

Appendix A lists reference documents that may be useful to users of this document.

Appendix B describes the design and operational differences between the WD90C24A controller and the WD90C24 controller.

Appendix C describes the design and operational differences between the WD90C24A controller and the WD90C24A2 controller.

Appendix D provides a change history for this document.

2.0 ARCHITECTURE

2.1 INTRODUCTION

The WD90C24A/A2 is made up of the following major internal modules:

- CRT Controller
- Sequencer
- Graphics Controller
- Attribute Controller
- Flat Panel Controller and Interface
- VESA VL-Bus (Local Bus) Interface
- Hardware Cursor
- Dithering Engine
- Weight and Mapping Logic
- RAMDAC
- Clock Synthesizer
- Power-down Management
- Hardware Bit Block Transfer (BITBLT)
- Hardware Line Drawing
- Frame Buffer Controller

Each module is described in this section. Their interconnections are shown in Figures 2-1 and 2-2.

The WD90C24A/A2 uses a four-level write cache to achieve fast memory writes. Therefore, with a 32-bit display memory interface, zero wait states can be realized for most memory write operations.

Fast Page mode memory fetching is used to improve memory bandwidth. The WD90C24A/A2 uses a FIFO to provide the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

Weighting and Mapping Logic provides color-to-gray-scale mapping, and a dithering engine, that works like a digital DAC, generating the gray scale level for monochrome flat-panel displays. The dithering engine also generates colors for color flat-panel display. While driving the flat panel, a Row Buffer supports the split screen displays.

To support a split screen display when driving a flat panel and a CRT simultaneously, an external Frame Buffer may be required

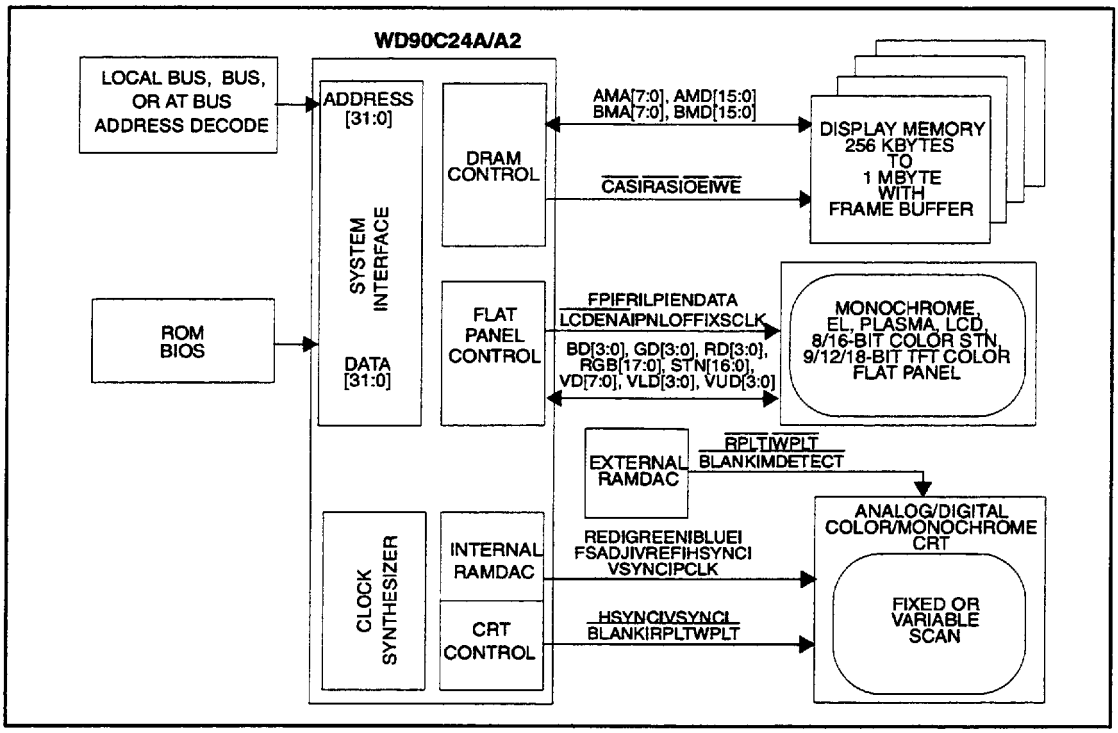


FIGURE 2-1. SYSTEM BLOCK DIAGRAM

2.2 CRT CONTROLLER

The CRT Controller performs the following functions:

- Generates horizontal sync (HSYNC) and vertical sync (VSYNC) for the CRT display monitor
- Simultaneous CRT and dual flat panel display is performed using frame buffer architecture
- Hidden display timing registers meet the fixed display timing for the flat panel display
- CRT display screen refresh is maintained for the various display modes defined by the BIOS ROM resident firmware
- Performs video split screen refresh and screen size mapping

2.3 SEQUENCER

The Sequencer performs the following functions:

- Timing generator for the display memory cycles
- Character clock in the alphanumeric mode, and the dot clock in the graphics mode
- Arbitrates between the video display refresh, memory refresh, and CRT access of the display memory for CRT only, flat panel only, or simultaneous CRT and single panel displays
- Arbitrates between the video display refresh, frame buffer access, memory refresh, and CRT access of the display memory for simultaneous CRT and dual panel displays
- Arbitrates cursor pattern access to the off-screen display memory when the hardware cursor is activated
- Provides the write cache control for CPU memory write to the video display memory

2.4 GRAPHICS CONTROLLER

The Graphics Controller manipulates the data flow between the CPU and the display memory for CPU write and read cycles. The Graphics Controller also controls data written to the CPU display memory.

2.5 ATTRIBUTE CONTROLLER

The Attribute Controller allows the following functions:

- Serializes the display memory data into a video data stream according to different display formats
- Controls the following features in all display modes:
  - Blinking
  - Underlining
  - Text cursor
  - Pixel panning
  - Reverse video
  - Background and foreground color
  - Border Controller

2.6 FLAT PANEL CONTROLLER AND INTERFACE

The Flat Panel Controller and Interface Module performs the following functions:

- Controls the video data flow after video data exits the RAMDAC palette RAM until the video data is output to the flat panel interface
- Generates the flat panel control signals:
  - Frame Rate (FR)
  - Frame Pulse (FP)
  - Latch Pulse (LP)
  - Shift Clock (XSCLK)
  - Data Enable (ENABLE)

These signals are generated with different timing and polarity in order to drive different types of panels without external components

- Split screen refresh for dual panel display and screen size mapping for both single and dual panel displays
- Performs split screen refresh and screen size mapping using frame buffer architecture (screen mapping includes vertical expansion and auto-centering)
- Controls the video data flow into and out of the row buffer (using frame buffer architecture)
- Controls the video data flow into and out of the frame buffer (using frame buffer architecture)

2.7 VESA VL-BUS INTERFACE

The WD90C24A/A2 provides a VESA VL-Bus (local bus) Interface for both the 486 and 386 CPU architectures. This interface can be implemented directly on the system motherboard or on a separate option card without adding extra glue logic. Through this interface, the WD90C24A/A2 connects directly to the host CPU address, data, and control lines. Using the VESA VL-Bus significantly improves system performance.

2.8 FRAME BUFFER CONTROLLER

The Frame Buffer Controller supports simultaneous display on a dual-flat panel or on a flat panel and CRT. This feature is fully supported for memory configuration 2 (refer to Section 4).

2.9 WEIGHT AND MAPPING LOGIC

For monochrome panel displays, the weight and mapping logic converts color information from the palette RAM into gray scale information using the following weighting equation:

I =.3R +.59G +.11B.

For monochrome display panels, the output code generated by the weighting equation selects gray shades depending on the modulation type:

- **Frame-Rate Modulation**

  The weighting code selects gray shades from the mapping RAM, which is loaded with 64 user-selected codes of shades with the optimum intensity.

- **Pulse-Width Modulation**

  The weighting code truncates or rounds off the shading information and sends it to the panel directly. With this information, the panel uses pulse-width modulation to generate related gray shades.

For color panel displays, the red, green, and blue color information that comes from the palette RAM provides the code for each color. Colors are selected depending on the color panel modulation type as follows:

- **Frame-Rate Modulation**

  The red, green, blue color data selects color shades from the dithering engine.

- **Pulse-Width Modulation**

  The color data can be sent directly to the panel or truncated and then sent to the panel.

2.10 DITHERING ENGINE

The Dithering Engine uses a dithering pattern and frame-rate modulation to constantly generate 64 gray shades. The dithering pattern for each shade is designed so that it creates minimum flicker on the panel screen.

2.11 HARDWARE BIT BLOCK TRANSFER (BITBLT)

The WD90C24A/A2 was designed with hardware support for Microsoft Windows, which supports accelerated Windows performance.

The WD90C24A/A2 Bit Block Transfer (BITBLT) increases speed. With BITBLT, blocks of pixels are transferred directly between regions of display memory and between display memory and system memory through a system I/O or memory port. For additional BITBLT information refer to Section 19.

2.12 HARDWARE LINE DRAWING

The WD90C24A/A2 provides a hardware line drawing engine that implements the Microsoft strip line algorithm. With this algorithm, the line draw engine interacts with software to determine the slope of the line and the number of pixels to be turned on. Line Draw operation is described in Section 20.

2.13 HARDWARE CURSOR

The Hardware Cursor provides up to a 64 by 64 pattern. Each pixel in the pattern is represented by two bits. These two bits determine how the cursor is displayed based on the color mode selected. The pattern is stored in the off-screen display memory. The hardware cursor is controlled by the following registers:

- Cursor Control
- Cursor Pattern Address

- Cursor Primary Color
- Cursor Secondary Color
- Cursor Auxiliary Color
- Cursor Origin
- Cursor Display Address X
- Cursor Display Address Y

The Cursor Display Address is the location for the origin of the cursor on the display screen. The Cursor Pattern Address is the starting memory location where the cursor pattern is stored in the display memory.

The Cursor Origin and the Cursor Display Address are used to calculate the cursor's starting display address. The cursor pattern is displayed on the window and the controller clips off the pattern. The pattern fetching request is sent to the sequencer. The cursor pattern is displayed when the display location matches the cursor start location. For additional information on the Hardware Cursor, refer to Section 18.

2.14 RAMDAC

The on-chip RAMDAC is low-power, PS/2-compatible with power-down control and built-in monitor detection logic with the following features:

- Three 256 by 6 RAMs as the R, G, B Color look-up tables
- Three 6-bit DACs
- Mask register
- Supports 16-bit high color

The 16 bits of video data are formed by five red bits, six green bits, and five blue bits, or five bits of each color with one bit ignored.

When in high color mode, video data bypasses the color palette RAM.

The LSB bit of the three DACs are forced to zero for 5-bit color configuration. The LSB bits of the Red DAC and Blue DAC are forced to zero for the 5-bit red, 6-bit green, and 5-bit blue configuration.

The DAC generates RS-343A/RS-170 compatible output and has ±1/2 LSB of integral and differential linearity errors.

2.15 CLOCK SYNTHESIZER

The on-chip Clock Synthesizer is a dual clock generator for VGA applications. It simultaneously generates display memory clock (MCLK) and video dot clock (VCLK).

Both clock frequencies can be programmed by the user and are derived from the 14.318 MHz system clock available in the IBM PC/XT/AT and PS/2 computer systems.

The clock synthesizer has power-down control to achieve a low power consumption.

When programing a new clock frequency for both MCLK and VCLK, the Clock Synthesizer requires 20 ms to achieve a stable frequency. All the registers, palette RAM, and Mapping RAM must be reloaded after the clock frequency is stable.

2.16 POWER-DOWN MANAGEMENT

The WD90C24A/A2 provides four major power down modes:

- Deep Sleep Mode
- Suspend/Resume Mode (System Power-down Mode)
- General Power Down Mode (Internal)
- Display Idle Mode

Each of the power-down management modes is described briefly in the following paragraphs. Additional information about power-down management is provided in Section 26.

Deep Sleep Mode is used when the entire display subsystem can be turned off. This mode is designed to conserve the most power and also requires the most system overhead. In this mode, the WD90C24A/A2 current sink is less than 1 mA.

Suspend/Resume mode (also called System Power Down Mode) is used when a display is not required but minimum access to the display registers is required. In this mode, all supply voltages (VDD) remain active, but the Clock Synthesizers are shut down. For Suspend/Resume mode the WD90C24A/A2 current sink is less than 10 mA.

General Power Down Mode is used to turn off the display when the keyboard has been idle for a preset time interval. In this mode all the supply voltages (VDD) and the Clock Synthesizers remain on. The MCLK and VCLK clock rates can be slowed down to 1/8 of their normal frequency.

The Display Idle Mode is used to turn off the display when the keyboard has been idle for a preset time interval. The DAC and LCD panel interfaces are turned off in this mode. The CPU can access I/O registers of the WD90C24A/A2, but it can not access display memory.

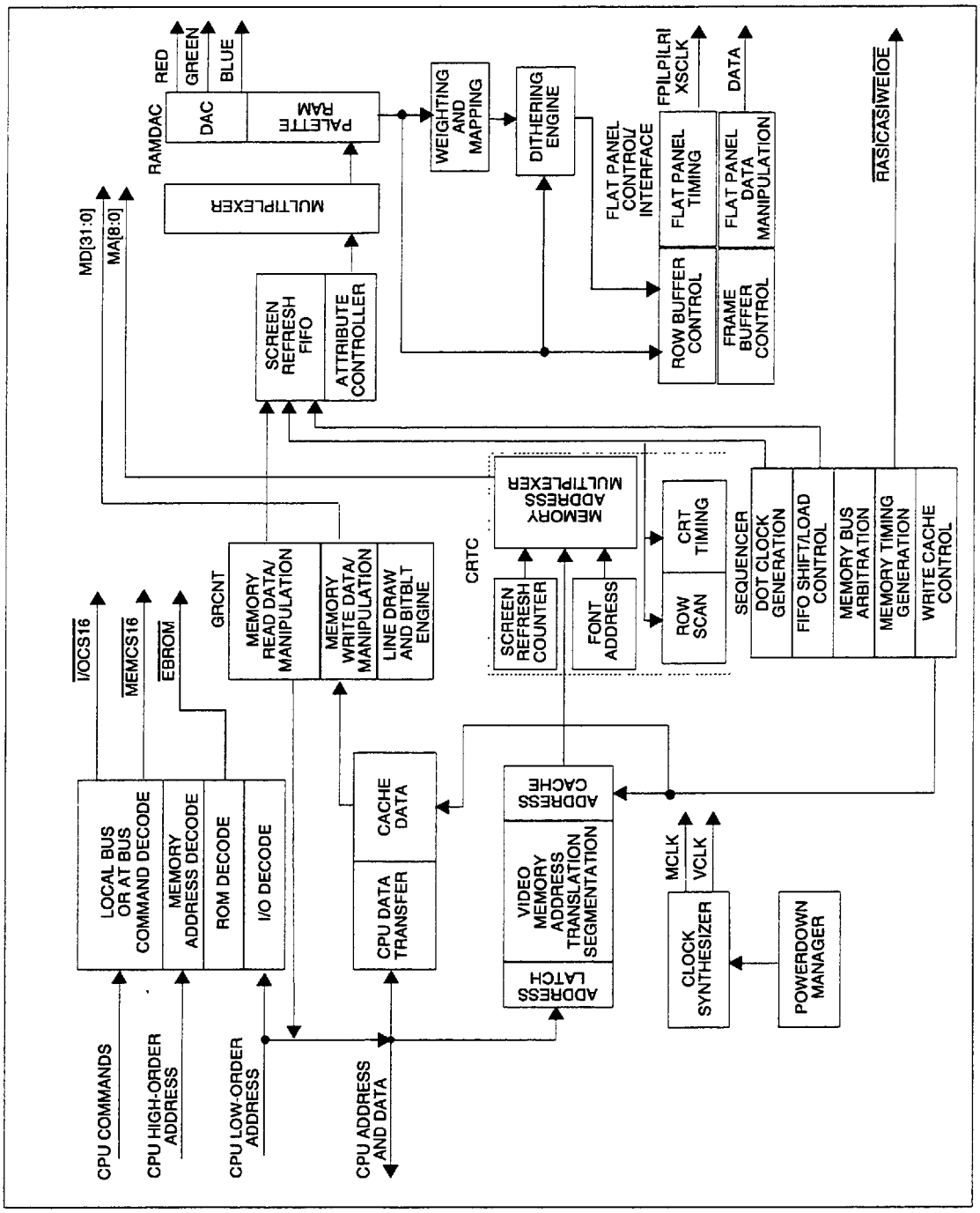


FIGURE 2-2. WD90C24A/A2 BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

The WD90C24A/A2 has five major interfaces, which are described in this section.

- System Interface
- BIOS ROM Interface
- Display Memory Interface
- ISA Bus Interface
- VESA VL-Bus Interface
- CRT Display Interface
- Flat Panel Display Interface

3.2 SYSTEM INTERFACE

The system interface operates with the following bus architectures:

- PC/XT/AT (ISA) bus (see Figure 3-1)
- VESA VL- Bus (local bus) (see Figure 3-3)
- Intel 386 DX local bus
- Intel 486 SX/DX local bus

The selection of the bus architecture depends on the setting of configuration bits CNF17 and CNF2 as listed in Table 3-1.

CNF17	CNF2	SYSTEM MODES
0	0	Reserved
0	1	ISA Bus
1	0	Reserved
1	1	Local Bus including VESA VL-Bus

TABLE 3-1. BUS ARCHITECTURE SELECTION

The bus architecture is selected during power-on and reset as described in Section 24 *WD90C24A/A2 Configuration Registers.*

Other features of the system interface include:

- $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ signals are generated to indicate 16-bit operation
- Minimal use of external circuitry
- Provides all signals, decodes all memory and I/O addresses to interface with any of the bus configurations in 8-bit or 16-bit mode.
- Decoding for video BIOS ROM while in extension card application (8-bit operation only)
- Reduced CPU wait states while writing to display memory with use of a display memory data and address write cache that holds CPU write data until it can be transferred to the display memory
- Improved performance of CPU display memory access -- PR0(A) and PR0(B) registers may be addressed indirectly
- Improved performance of CPU display memory access -- 32-bit memory data latch is addressable by the I/O port
- Sixteen segments of 1 Mbyte virtual memory addressing range or 32 segments of 512K-byte virtual memory addressing range for flexibility in memory allocation

3.3 BIOS ROM INTERFACE

The WD90C24A/A2 can be configured to provide an enable signal ($\overline{\text{EBROM}}$) for an external 8-bit video BIOS PROM. The WD90C24A/A2 is then configured to automatically map this video BIOS into the system memory map during power-on and reset. The external video BIOS can be selectively mapped out of system memory as required. Decodes are provided for 64 Kbytes of VGA video BIOS address space as defined in the VGA architecture.

3.4 DISPLAY MEMORY INTERFACE

For a 16-bit display memory interface, the following DRAM configurations can be used:

- One 256K by 16 DRAM or four 256K by 4 DRAMs
- Two 256K by 16 DRAMs

For a 32-bit memory interface, the following DRAM configurations can be used:

- Two 256K by 16 DRAMs
- Eight 256K by 4 DRAMs

Refer to Section 4 for a summary of display memory configurations.

In all cases, WD90C24A/A2 uses DRAM fast page mode for optimum performance.

3.4.1 Minimum Configuration

In the minimum configuration, which is one 256K by 16 DRAM, the WD90C24A/A2 can support all standard IBM VGA modes.

When additional DRAMs are installed, the WD90C24A/A2 is capable of supporting high color resolution video modes of up to 1024 by 768 by 256 colors, non-interlaced and 1280 by 1024 by 16 colors, interlaced.

3.4.2 Display Memory Features

- Supports 70 ns, 80 ns, and 100 ns DRAMs with the dedicated MCLK which can operate from 37.5 MHz to 44.3 MHz

NOTE

Longer DRAM access times require slower clock frequencies. Table 3-2 lists typical DRAM access times and memory clock limitations.

DRAM ACCESS TIME IN NANOSECONDS	MCLK FREQUENCY IN MEGAHERTZ (MAX)
70	44.3
80	39.8
100	37.5

TABLE 3-2. DRAM ACCESS TIME VERSUS MEMORY CLOCK FREQUENCY

- Fast page DRAM timing is used for all CPU access, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes)
- Generates $\overline{CAS}$-before-$\overline{RAS}$ DRAM refresh for the display memory

3.4.3 VCLK to MCLK Ratio

The VCLK to MCLK ratio for the WD90C24A/A2 controller is specified as 1.6 or less. Exceeding this ratio may cause FIFO underflow problems.

The following table lists the VCLK and MCLK frequencies, their ratios, and recommended DRAM speed for two high resolution displays.

	RESOLUTION	
	1024X768X256 NON-INTERLACED (60 Hz)	1024X768X16 INTERLACED (43hZ)
VCLK (MHz)	65	44.5
MCLK (MHz)	44.3	39.8
VCLK/MCLK RATIO	1.5	1.1
DRAM SPEED (ns)	70	80

TABLE 3-3. VCLK TO MCLK RATIOS

3.5 ISA BUS INTERFACE

The WD90C24A/A2 interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The WD90C24A/A2 supports full 16-bit I/O and memory transfers. Support of 16-bit memory transfers is independent of whether the WD90C24A/A2 has an 8-bit or 16-bit display memory path, although increased performance occurs when a 16-bit display memory is available (See Figure 3-1).

LA(23:17) addresses are latched internal to the WD90C24A/A2 by the ALE signal to eliminate bus timing problems in some common system implementations.

I/O and memory operation (8/16-bit I/0 and 8/16 bit memory) can be separately enabled by selectively enabling $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ bus interface signals.

The following ISA Bus signals are directly supported by the WD90C24A/A2:

AEN	$\overline{\text{MEMR}}$
$\overline{\text{BALE}}$	$\overline{\text{MEMW}}$
LA[23:17]	$\overline{\text{0WS}}$
$\overline{\text{IOCHRDY}}$	$\overline{\text{REFRESH}}$
$\overline{\text{IOCS16}}$	RESET
$\overline{\text{IOR}}$	SA [16:0]
$\overline{\text{IOW}}$	$\overline{\text{SBHE}}$
$\overline{\text{MCS16}}$	SD[15:0]

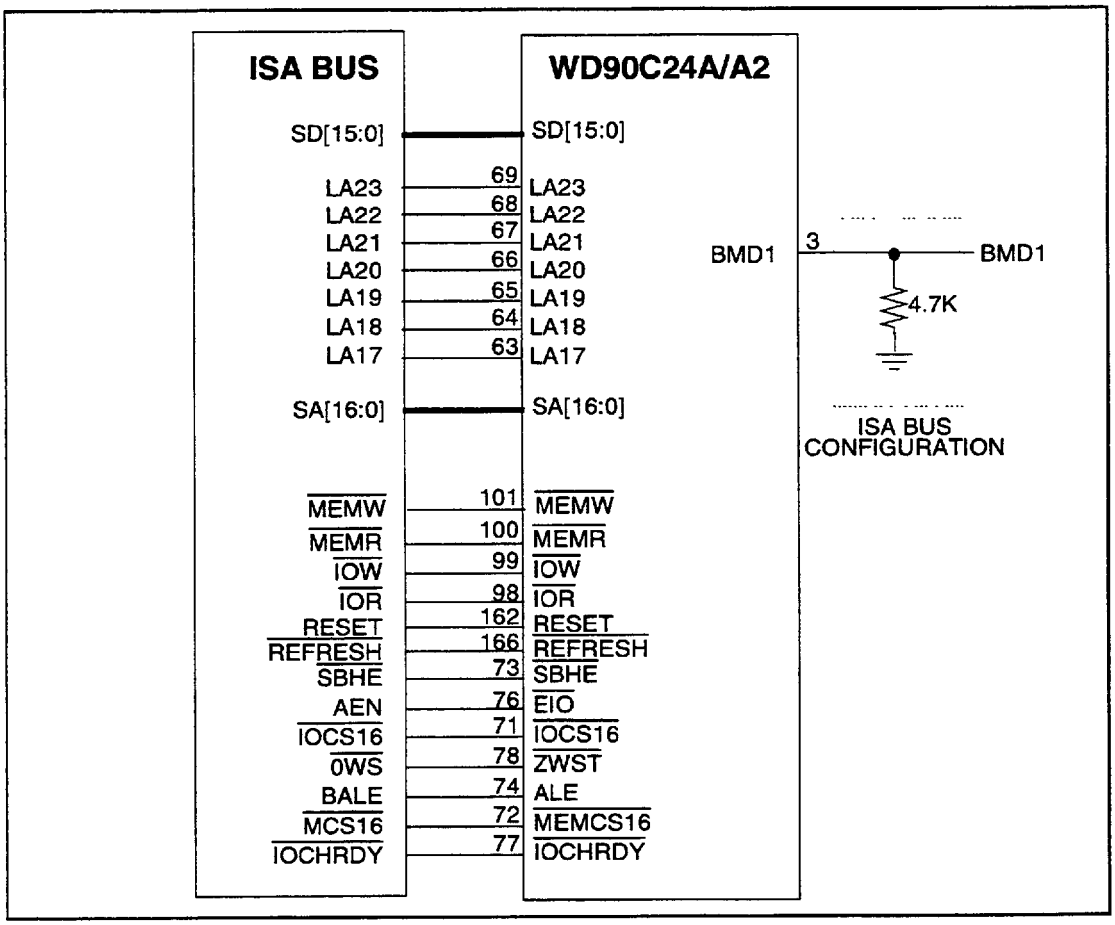


FIGURE 3-1. ISA BUS INTERFACE DIAGRAM

3.6 VESA VL-BUS INTERFACE

The WD90C24A/A2 directly supports the following VESA VL-Bus interface signals (see Figure 3-3).

ADR[31:2]	$\overline{\text{LDEV}}$
$\overline{\text{ADS}}$	$\overline{\text{LRDY}}$
$\overline{\text{BE}}$[3:0]	M/$\overline{\text{IO}}$
DAT[31:0]	$\overline{\text{RESET}}$
D/$\overline{\text{C}}$	$\overline{\text{RDYRTN}}$
LCLK	W/$\overline{\text{R}}$

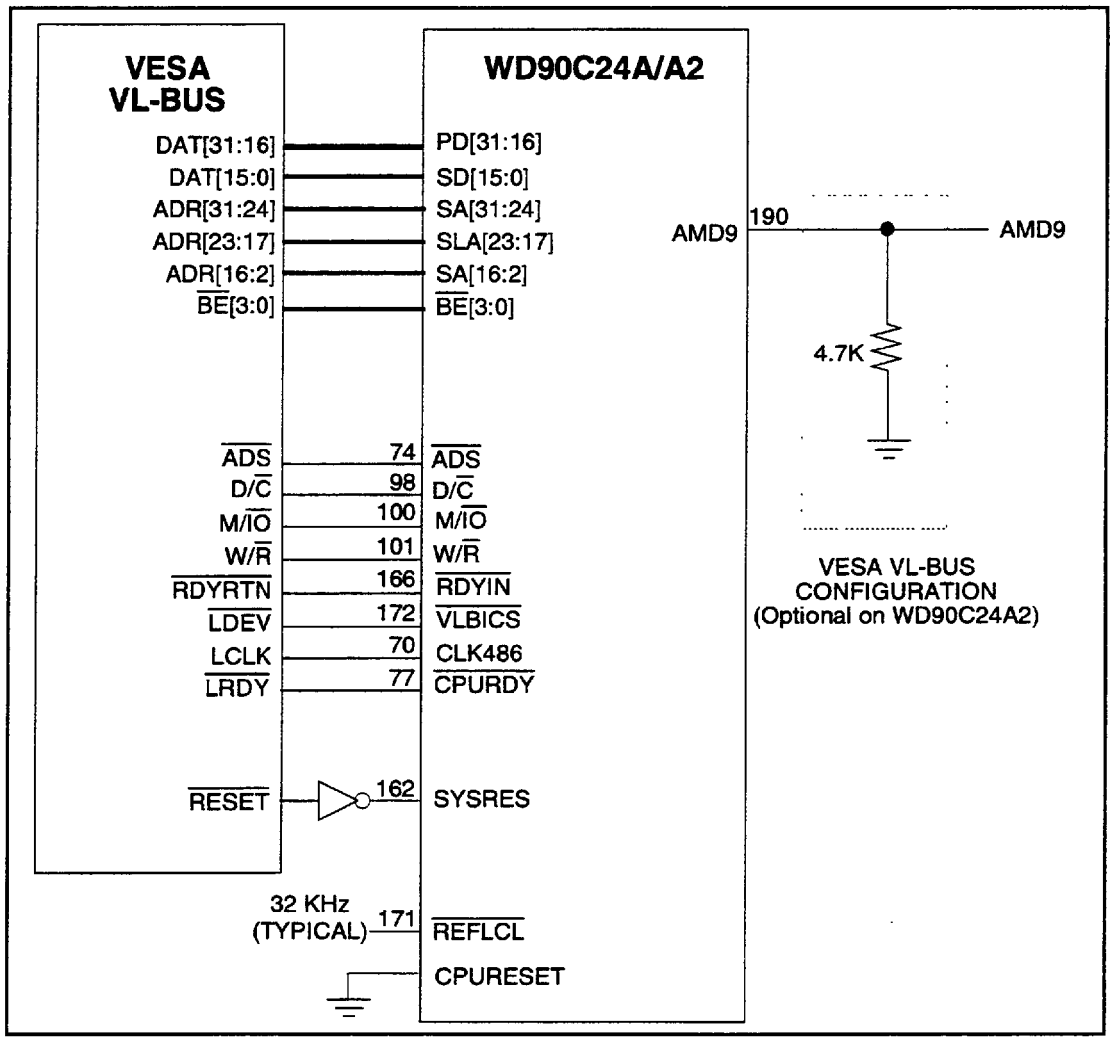


FIGURE 3-2. VESA VL-BUS INTERFACE DIAGRAM

3.7 CRT DISPLAY INTERFACE

- On-chip RAMDAC provides the RED, GREEN, and BLUE signals directly to the analog CRT monitor
- Provides HSYNC and VSYNC signals to control the monitor
- Allows use of an external RAMDAC to drive the CRT
- Supports Bt/471/478/476 compatible RAMDAC interface

3.8 FLAT PANEL DISPLAY INTERFACE

Features of the flat panel display interface include:

- Direct interface with 640 by 480 (400) STN, TFT, 1024 by 768 LCD, EL, and plasma panels
- Flat panel interface signals change function to support the panel type chosen
- Programmable timing and polarity for the flat panel control signals to meet the requirements of different panels
- Video data groupings to meet the requirements for different panels
- Controller supplies 8 pixels per shift clock with 8-bits of data for monochrome STN panels
- Controller supplies one pixel per shift clock with 4-bits of data for 16 shades for plasma panels
- Controller supplies 8-bit (2 and 2/3 pixel per shift clock) interface, and 16-bit (5 and 1/3 pixel per shift clock) interface for color STN panels
- Controller supplies 9-bit, 12-bit 18-bit (all are one pixel per shift clock) interface for TFT panels

4.0 MEMORY CONFIGURATIONS

4.1 MEMORY MODE SETUP

The following table defines how to set up the configuration registers for the desired memory mode. Refer to subsequent paragraphs for descriptions of the memory modes

The memory modes listed in Table 4-1 are selected at power-on or reset depending upon configuration bits CNF16, CNF14, and CNF13. For information about the configuration registers, refer to Section 24.

MODE	MEMORY DRAMS TYPE	MEMORY DRAMS QTY	CNF16 PR11[7]	CNF14 PR11[6]	CNF13 PR11[5]
1	256K by 16	1	1	0	1
2[3]	256K by 16	2	1	0	0

NOTES:
1. With CNF[16] set to 0, display memory uses 256K by 16 DRAMs.
2. CNF(16), CNF(14), and CNF(13) are readable via PR 11 bits 7, 6, and 5, respectively (refer to Section 24).
3. Mode 2 has no frame buffer.

TABLE 4-1. MEMORY MODE SETUP

In memory mode 1 the display memory data path is 16 bits wide.

Memory mode 2 is used with a 32-bit wide display memory data path, unless one of the DRAM banks is used as the LCD panel frame buffer. For example, one DRAM bank is used as the LCD panel frame buffer when simultaneous display with an LCD panel and CRT is used, and also when 16-bit dual-panel color STN is used.

4.2 MEMORY CONFIGURATION DESCRIPTIONS

Memory for the WD90C24A/A2 can be configured in two memory modes as listed in Table 4-1. Table 4-2 summarizes how the memory modes support combinations of memory configurations and displays. The following block diagrams are provided show how the external DRAMs are connected in typical memory configurations.

1. Single DRAM Memory Interface Configuration
2. Memory Configuration with 1 Mbyte.
3. Simultaneous Display Memory Configuration
4. High-Performance 512 Kbyte Simultaneous Display Memory Configuration

Table 4-2 lists the memory modes and which of the memory modes supports each display resolution. Where the memory mode is available, the table lists whether it supports CRT only, LCD only, or simultaneous displays (dual panel and CRT).

MEMORY CONFIGURATIONS	MEMORY MODES[1] 1[2]	2[3]
1024 x 768 x 256	---	C,L
1024 x 768 x 16	C,L	C,L
800 x 600 x 256	C	C
800 x 600 x 16	C,L	C,L
640 x 480 x 256	C,L	S,C,L
640 x 480 x 32K/64K	---	C,L
640 x 400 x 256	C,L	S,C,L
640 x 400 x 32K/64K	C,L	C,L
320 x 200 x 32K/64K	C,L	C,L
All IBM Standard Modes	S,C,L	S,C,L
Memory Data Bus Width	16 bits	32 bits

NOTES

S = Simultaneous display (dual panel and CRT)
C = CRT only
L = LCD only

1. These memory modes are also listed in Table 4-1.
2. Supports a 16-bit interface in C and L modes.
3. Supports a 32-bit interface in C and L modes.

TABLE 4-2. MEMORY CONFIGURATIONS AND MODES SUPPORTED

4.3 MEMORY MODE 1 INTERFACE CONFIGURATION

Figure 4-1 shows memory mode No. 1 with 512 Kbytes of display memory using one 256K by 16 DRAM.

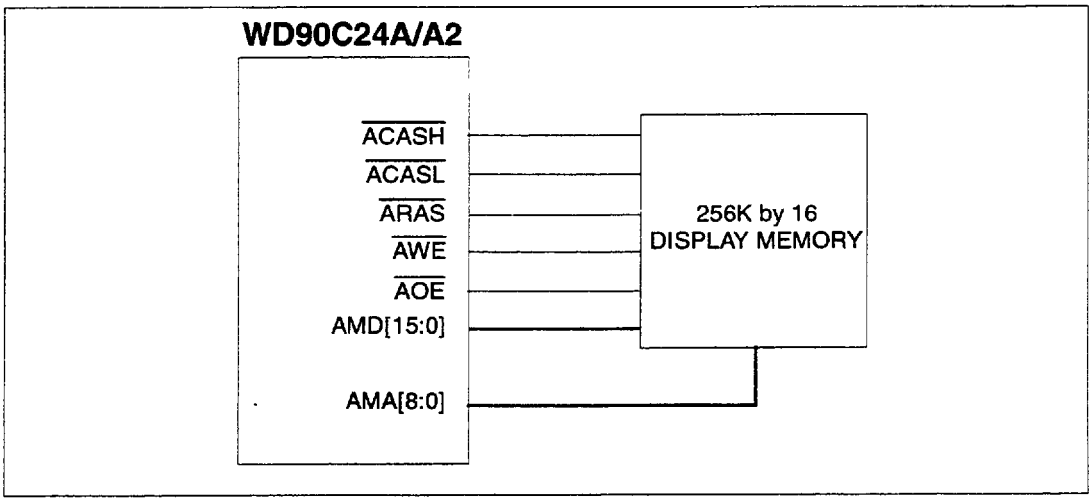


FIGURE 4-1. MEMORY MODE 1 INTERFACE CONFIGURATION

4.4 MEMORY MODE 2 INTERFACE CONFIGURATION

Figure 4-2 shows memory mode No. 2 with 1 Mbyte of display memory using two 256K by 16 DRAMs.

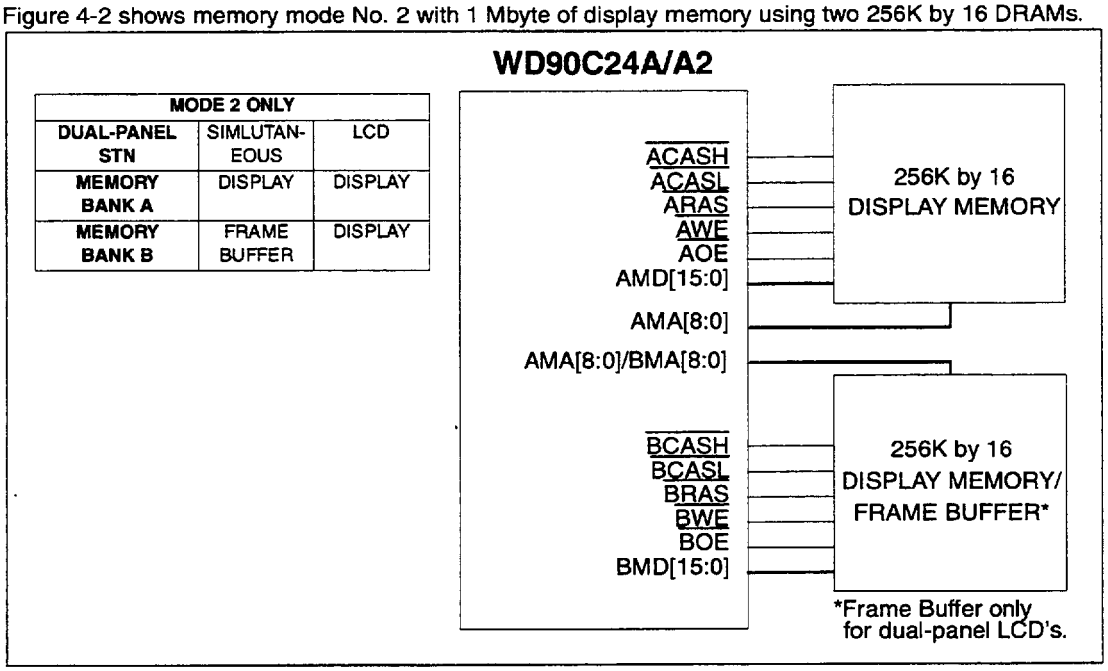


FIGURE 4-2. MEMORY MODE 2 INTERFACE CONFIGURATION USING TWO 256K BY 16 DRAMS

Figure 4-3 shows memory mode No. 2 with 1 Mbyte of display memory using eight 256K by 4 DRAMs.

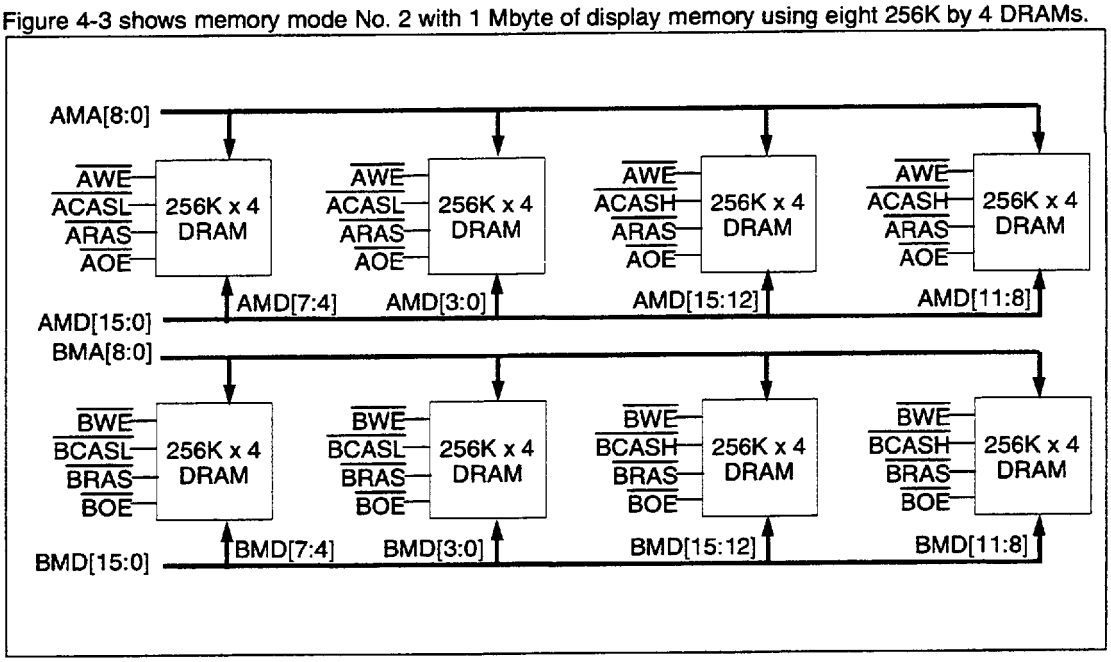


FIGURE 4-3. MEMORY MODE 2 INTERFACE CONFIGURATION USING EIGHT 256K BY 4 DRAMS

5.0 SIGNAL DESCRIPTIONS

5.1 INTRODUCTION

This section contains detailed information concerning signals and connector pins for the WD90C24A/A2 controller 208-pin MQFP package. The following information is contained in this section:

- Signal to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Pin Multiplexing Reference Tables

NOTES FOR TABLE 5-1

Where multiple signal names are assigned to a pin, the names are separated by a vertical bar (|). The use for each pin depends on the bus that the pin is connected to. For additional information about the busses refer to Section 5-3. For additional information about pins with multiplexed signals, refer to Section 5.4.

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates VDD and VSS supply pins.

Signal names not otherwise indicated are both input and output.

5.2 SIGNAL MNEMONIC TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - BMD0	32 - BMA2[1]	63 - SLA17[2]	94 - SA13[2]
2 - BMD15	33 - BMA5[1]	64 - SLA18[2]	95 - SA14[2]
3 - BMD1	34 - BMA3[1]	65 - SLA19[2]	96 - SA15[2]
4 - BMD14	35 - BMA4[1]	66 - SLA20[2]	97 - SA16[2]
5 - VSS[3]	36 - VSS[3]	67 - SLA21[2]	98 - $\overline{IOR}$[2]ID/$\overline{C}$[2]
6 - BMD2	37 - PD29	68 - SLA22[2]	99 - $\overline{IOW}$[2]$\overline{BE1}$[2]
7 - BMD13	38 - PD28	69 - SLA23[2]	100 - $\overline{MEMR}$[2]M/$\overline{IO}$[2]
8 - BMD3	39 - PD27	70 - CLK486[2]	101 - $\overline{MEMW}$[2]W/$\overline{R}$[2]
9 - BMD12	40 - PD26	71 - $\overline{IOCS16}$[1]$\overline{BOFF}$[1]	102 - AVDD1[3]
10 - VDD[3]	41 - PD25	72 - $\overline{MEMCS16}$[1]PD31	103 - XMCLK[2]
11 - BMD4	42 - PD24	73 - $\overline{SBHE}$[2] CPURESET[2]	104 - MCAP[2]
12 - BMD11	43 - VDD[3]	74 - ALE[2]$\overline{ADS}$[2]	105 - VCAP[2]
13 - BMD5	44 - PD23	75 - IRQ[1]PD30	106 - VCLK2
14 - BMD10	45 - PD22	76 - $\overline{EIO}$[2]$\overline{BE0}$[2]	107 - AVSS1[3]
15 - BMD6	46 - PD21	77 - $\overline{IOCHRDY}$[1] $\overline{CPURDY}$[1]	108 - RVSS[3]
16 - BMD9	47 - PD20	78 - $\overline{ZWST}$[1]VLBIBUSY	109 - SD0
17 - BMD7	48 - VSS[3]	79 - VSS[3]	110 - SD1
18 - BMD8	49 - PD19	80 - SA0[2]$\overline{BE3}$[2]	111 - SD2
19 - MVDD[3]	50 - PD18	81 - SA1[2]$\overline{BE2}$[2]	112 - SD3
20 - $\overline{BCASL}$[1]	51 - PD17	82 - SA2[2]	113 - BVDD[3]
21 - VSS[3]	52 - PD16	83 - SA3[2]	114 - SD4
22 - $\overline{BWE}$[1]	53 - SD15	84 - SA4[2]	115 - SD5
23 - $\overline{BCASH}$[1]	54 - SD14	85 - SA5[2]	116 - SD6
24 - $\overline{BRAS}$[1]	55 - SD13	86 - SA6[2]	117 - SD7
25 - $\overline{BOE}$[1]	56 - SD12	87 - SA7[2]	118 - VSS[3]
26 - VDD[3]	57 - BVDD[3]	88 - RVDD[3]	119 - XSCLK[1]IXSCLKL[1]I XSCLKU[1]IBD5[1]
27 - BMA8	58 - SD11	89 - SA8[2]	120 - $\overline{WPLT}$[1]IBD4[1]
28 - BMA0[1]	59 - SD10	90 - SA9[2]	121 - $\overline{RPLT}$[1]IBD3[1]I STN15[1] IUD7[1]
29 - BMA7[1]	60 - SD9	91 - SA10[2]	122 - STN14[1]IBD2[1]I UD6[1]
30 - BMA1[1]	61 - SD8	92 - SA11[2]	123 - STN13[1]IBD1[1]I IUD5[1]
31 - BMA6[1]	62 - VSS[3]	93 - SA12[2]	124 - STN12[1]IBD0[1]I IUD4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1. SIGNAL TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
125 - VDD[3]	146 - SA24[2]	167 - FPUSR0[1]	188 - AMD10
126 - STN11[1]/GD5[1]/UD3[1]	147 - SA25[2]	168 - VCLK1[1]/ FPUSR1[1]	189 - AMD6
127 - STN10[1]/GD4[1]/UD2[1]	148 - SA26[2]	169 - PVDD[3]	190 - AMD9
128 - STN9[1]/RD5[1]/UD1[1]	149 - SA27[2]	170 - CKIN[2]/VCLK[2]	191 - AMD7
129 - STN8[1]/RD4[1]/UD0[1]	150 - SA28[2]	171 - $\overline{\text{EBROM}}$[1]/ $\overline{\text{REFLCL}}$[2]	192 - AMD8
130 - FPVDD[3]	151 - SA29[2]	172 - $\overline{\text{VLBICS}}$[1]	193 - MVDD[3]
131 - VUD3[1]/D7[1]/RD3[1]/STN7[1]/ STN0[1]/LD7[1]/VD7/P7[2]	152 - SA30[2]	173 - VSYNC[1]	194 - $\overline{\text{ACASL}}$[1]
132 - VUD2[1]/D6[1]/RD2[1]/STN6[1]/ STN1[1]/LD6[1]/VD6/P6[2]	153 - SA31[2]	174 - HSYNC[1]	195 - VSS[3]
133 - VUD1[1]/D5[1]/RD1[1]/STN5[1]/ STN2[1]/LD5[1]/VD5/P5[2]	154 - AVDD2[3]	175 - PCLK	196 - $\overline{\text{AWE}}$[1]
134 - VUD0[1]/D4[1]/RD0[1]/ STN4[1]/ STN3[1]/LD4[1]/ VD4/P4[2]	155 - $\overline{\text{MDETECT}}$[2]/FSADJ[2]	176 - VSS[3]	197 - $\overline{\text{ACASH}}$[1]
135 - VLD3[1]/D3[1]/GD3[1]/ STN3[1]/ STN4[1]/LD3[1]/ VD3/P3[2]	156 - VREF[2] (Analog)	177 - AMD0	198 - $\overline{\text{ARAS}}$[1]
136 - VLD2[1]/D2[1]/GD2[1]/ STN2[1]/ STN5[1]/LD2[1]/ VD2/P2[2]	157 - BLUE[1] (Analog)	178 - AMD15	199 - $\overline{\text{AOE}}$[1]
137 - VLD1[1]/D1[1]/GD1[1]/STN1[1]/ STN6[1]/LD1[1]/ VD1/P1[2]	158 - GREEN[1] (Analog)	179 - AMD1	200 - AMA8[1]
138 - VLD0[1]/ D0[1]/GD0[1]/ STN0[1]/ STN7[1]/LD0[1]/ VD0/P0[2]	159 - RED[1] (Analog)	180 - AMD14	201 - AMA0[1]
139 - VSS[3]	160 - AVSS2[3]	181 - AMD2	202 - AMA7[1]
140 - XSCLK[1]/XSCLKL[1]/ XSCLKU[1]	161 - EXCKEN[2]	182 - AMD13	203 - AMA1[1]
141 - RVDD[3]	162 - RESET[2]/SYSRES[2]	183 - AMD3	204 - AMA6[1]
142 - LP[1]	163 - $\overline{\text{PDOWN}}$[2]	184 - AMD12	205 - AMA2[1]
143 - FP[1]	164 - $\overline{\text{LCDENA}}$[1]	185 - AMD4	206 - AMA5[1]
144 - FR[1]/$\overline{\text{BLANK}}$[1]/ ENDATA[1]	165 - PNLOFF[1]	186 - AMD11	207 - AMA3[1]
145 - RVSS[3]	166 - $\overline{\text{REFRESH}}$[2]/ $\overline{\text{RDYIN}}$[2]	187 - AMD5	208 - AMA4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1 SIGNAL TO PIN LOCATIONS (Continued)

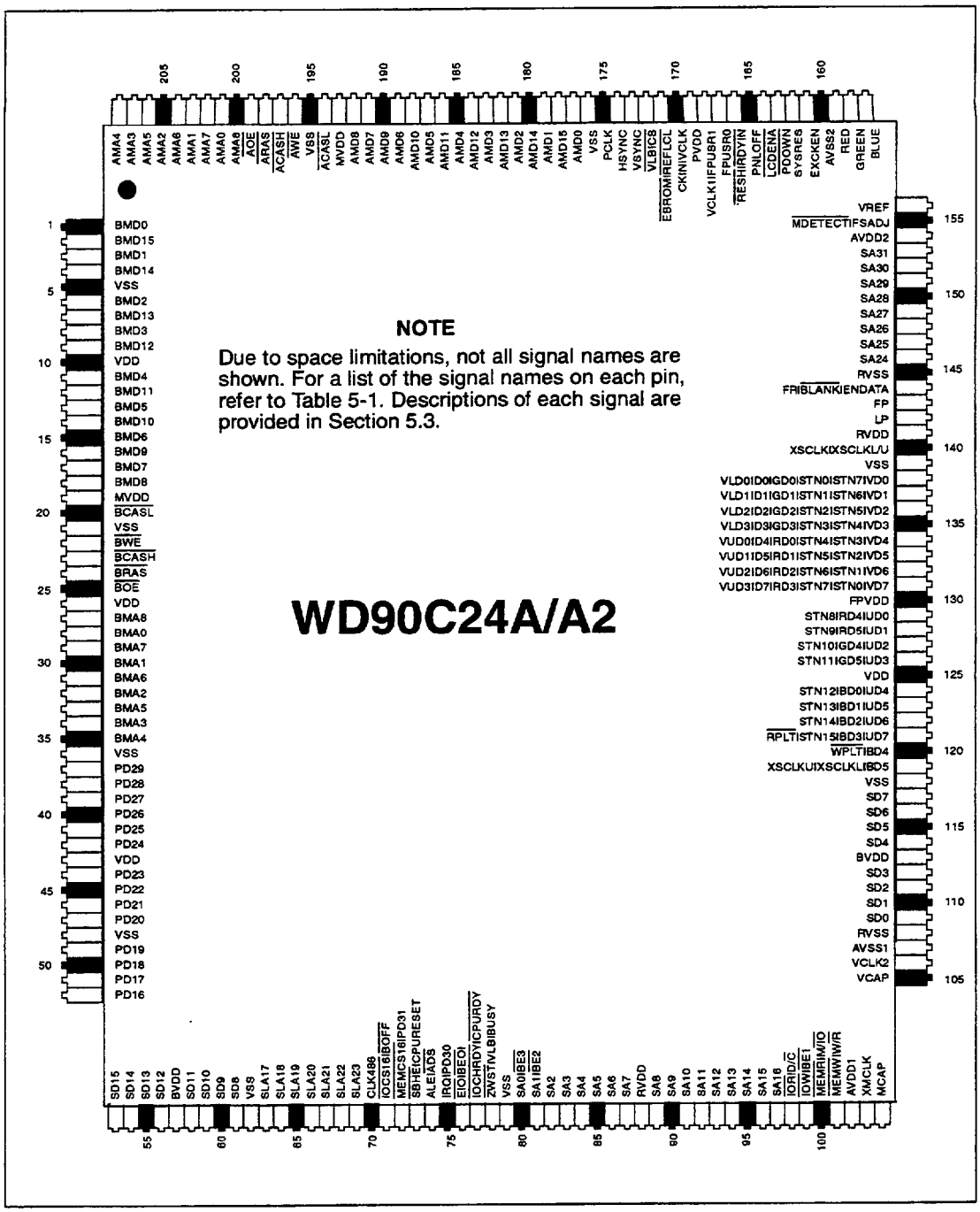


FIGURE 5-1. PIN CONFIGURATION

5.3 DETAILED SIGNAL DESCRIPTIONS

The following tables provide detailed signal descriptions for the WD90C24A/A2 controller 208-pin MQFP package. The signal descriptions are listed by the pin number and mnemonic given in Table 5-1. The definitions are listed in pin number order, as far as practical, within functional groups. Some signal definitions may appear in more than one functional group, if applicable, to aid the user in quick recovery of information for a particular group. The functional groups are listed below:

- Host Interface Pins
- Display Buffer Memory Interface Pins
- RAMDAC Interface Pins
- Clock Generation Interface Pins
- Panel Interface Pins
- Power and Ground Pins

Where more than one signal name is indicated on the same pin, the signal names are separated by a vertical bar (|) in Table 5-1. The pin usage, as described in Table 5-2, changes for each signal name depending upon the bus interface as follows:

1. The letters AT in the bus column indicate an Industry Standard Architecture (ISA) bus compatible signal. The terms AT bus and ISA bus are used interchangeably unless otherwise indicated.
2. The letters LOC in the bus column indicate a VESA VL-Bus (local bus) compatible signal.

5.3.1 Host Interface Pin Definitions

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
71	$\overline{\text{IOCS16}}$	AT	Active Low Output	**I/O Chip Select 16** In AT mode, this signal used to respond to the host to allow 16-bit access to the I/O bus.
	$\overline{\text{BOFF}}$	LOC	Active Low Output	**Bus Backoff** Connects to the 80486 BOFF pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus.
72	$\overline{\text{MEMCS16}}$	AT	Active Low Output	**Memory Chip Select 16 Bits** This line is used to respond to the host to enable 16-bit display memory data transfer.
	PD31	LOC	Active High Input/Output	**CPU Data Bus Bit 31** Provides bit 31 on the Local bus. This bit is combined with PD30 (pin 75), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
73	$\overline{\text{SBHE}}$	AT	Active Low Input	**System Byte High Enable** Indicates a data transfer on the upper byte of the data bus (SD15:8).
	CPURESET	LOC	Active High Input	**CPU Reset** Local bus reset operation similar to AT bus RESET. This signal is used, primarily for the 386-based systems, to synchronize the divided-by-2 clock (internal working clock) on the Local Bus Interface. For 486-based systems this line should be tied to VSS (ground).
74	ALE	AT	Active High Input	**Address Latch Enable** Address bits SLA23:SLA17 are latched internally on the falling edge of the ALE. (Tied High)
	$\overline{\text{ADS}}$	LOC	Active Low Input	**Address Status** Indicates the start of a Local bus cycle.
75	IRQ	AT	Active High Output	**Interrupt Request** Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal goes active, causing an interrupt. It stays active until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired.
	PD30	LOC	Active High Input/Output	**CPU Data Bus Bit 30** Provides bit 30 on the Local bus. This bit is combined with PD31 (pin 72), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
76	$\overline{EIO}$	AT	Active Low Input	**Enable I/O** This signal is used to enable I/O address decoding and is connected directly to the system bus signal $\overline{AE}$ (address enable).
	$\overline{BE0}$	LOC	Active Low Input	**Byte Enable 0** Byte enable for Local bus data bits SD7:SD0. $\overline{BE3}$:$\overline{BE1}$ are located on pins 80, 81, and 99, respectively.
77	$\overline{IOCHRDY}$	AT	Active Low Output (Tristate)	**I/O Channel Ready** Indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during display memory accesses. It may be pulled inactive by the WD90C24A/A2 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
	$\overline{CPURDY}$	LOC	Active Low Output, (Tristate)	**CPU Ready** Ready signal to host processor or Local Bus controller for the termination of the current instruction cycles.
78	$\overline{ZWST}$	AT	Active Low Output	**Zero Wait State** This signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33A register, bits 7,6 in the following ways: **A.** $\overline{0WS}$ = 0 if write cache is not full. **B.** $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full. In this case $\overline{0WS}$ = 0 should be ANDed externally with $\overline{MWR}$ to generate zero wait state strobe. **C.** $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full, AND $\overline{MWR}$ is active. **D.** $\overline{0WS}$ = 0 if valid memory address decode AND write cache is not full AND $\overline{MWR}$ is active, OR valid I/O address decode AND $\overline{IOW}$ is active.
	VLBIBUSY	LOC	Active High Output, Tristate	**VGA Local Bus Busy Signal** Local bus interface busy signal.
98	$\overline{IOR}$	AT	Active Low Input	**I/O Read** I/O read strobe. This strobe signals an I/O read.
	D/$\overline{C}$	LOC	Active High/ Low Input	**Data or Code Indicator** Provides data or code indicator for the local bus.
99	$\overline{IOW}$	AT	Active Low Input	**I/O Write** I/O write strobe. This strobe signals an I/O write.
	$\overline{BE1}$	LOC	Active Low Input	**Byte Enable 1** Byte enable for Local bus data bits SD15:SD8. $\overline{BE3}$, $\overline{BE2}$, and $\overline{BE0}$ are located on pins 80, 81, and 76, respectively.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
100	$\overline{\text{MEMR}}$	AT	Active Low Input	**Memory Read** This signal indicates that a memory read cycle is occurring. $\overline{\text{MEMR}}$ is internally gated with $\overline{\text{REFRESH}}$.
	M/$\overline{\text{IO}}$	LOC	Active High/Low Input	**Memory or I/O Cycle** Local bus indicator for memory or I/O cycle. Low indicates I/O cycle and high indicates memory cycle.
101	MEMW	AT	Input	**Memory Write** This signal indicates that a memory write cycle is occurring. $\overline{\text{MEMW}}$ is internally gated with $\overline{\text{REFRESH}}$.
	W/$\overline{\text{R}}$	LOC	Active High/Low Input	**Write or Read Cycle** Indicates the type of access occurring on the Local bus. When high, the access is a write operation, and when low the access is a read operation.
162	RESET	AT	Active High Input	**Reset** This signal resets the WD90C24A/A2. MCLK and VCLK should be connected to WD90C24A/A2 in order for the WD90C24A/A2 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK periods.
	SYSRES	LOC		**System Reset** This signal resets the Local Bus Logic. Western Digital configuration bits are initialized at power-up/reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors.
166	REFRESH	AT	Active Low Input	**DRAM Refresh** Initiates video buffer memory refresh. This signal must be inactive for memory reads or writes to occur.
	$\overline{\text{RDYIN}}$	LOC	Active Low Input	**Ready In** This signal is used for synchronizing the local bus with the host processor.
171	$\overline{\text{EBROM}}$	AT	Active Low Output	**Enable BIOS ROM** This is an active low signal to enable BIOS ROM (C0000h - C7FFFh) if enabled by PR1(0). A write to WD90C24A/A2 internal I/O port address 46E8h causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping. **NOTE:** To unlock port 46E8h for writing, the value ACh must be written to port A875h.
	$\overline{\text{REFLCL}}$	LOC	Active Low Input	**Refresh Clock Input** Provides the refresh clock input (typically 32 KHz) during power-down mode operation. This signal is selected when PR57, bit 6 is set to 1.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
172	$\overline{\text{VLBICS}}$	LOC	Active Low Output	**Video Local Bus Interface Chip Select** Local bus chip select. This line is driven low only if the current cycle requires service by the Local bus interface.
153 152 151 150 149 148 147	SA31 SA30 SA29 SA28 SA27 SA26 SA25	LOC	Active High Input	**Host System Address Bus (SA31 - SA25)** These local address bits should be connected to the host CPU address bus. These bits are combined with SLA23:SLA17, SA24 and SA16:SA2 to provide a 30-bit Local Bus Address. Internal pullup resistors are provided on these pins.
146	SA24	LOC	Active High Input	**Host System Address Bus (SA24)** This bit is combined with SLA23:SLA17 and SA16:SA2 to provide a 30-bit Local Bus Address. An internal pullup resistor is provided on this pin.
69 68 67 66 65 64 63	SLA23 SLA22 SLA21 SLA20 SLA19 SLA18 SLA17	All	Active High Input	**Host System/Latchable Address Bus (SLA23:SLA17)** These address bits should be connected to the host CPU address bus. For the AT bus interface, these bits are combined with SA16:SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SA16:SA2 to provide a 30-bit Address Bus.
97 96 95 94 93 92 91 90 89 87 86 85 84 83 82	SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2	All	Active High Input	**Host System Address Bus (SA16 - SA2)** These address bits should be connected to the host CPU address bus. For the AT bus interface, these bits are combined with SLA23:SLA17, SA1, and SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SLA23:SLA17 to provide a 30-bit Address Bus.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
81	SA1	AT	Active High Input	**Host System Address Bus (SA1)** This address bit should be connected to the host CPU address bus. For the AT interface, this bit is combined with SLA23:SLA17, SA16:SA2, and SA0 to provide a 24-bit address bus.
	$\overline{BE2}$	LOC	Active Low Input	**Byte Enable 2** Local bus Byte Enable: for a 16-bit host CPU, $\overline{BE2}$ = SA1; for a 32-bit host CPU, $\overline{BE2}$ enables SD[23:16] $\overline{BE3}$, $\overline{BE1}$, and $\overline{BE0}$ are located on pins 80, 99, and 76, respectively.
80	SA0	AT	Active High Input	**Host System Address Bus (SA0)** This address bit should be connected to the host CPU address bus. For the AT bus interface, this bit is combined with SLA23:SLA17, SA16:SA2, and SA1 to provide a 24-bit address bus.
	$\overline{BE3}$	LOC	Active Low Input	**Byte Enable 3** Local bus Byte Enable: for a 16-bit host CPU, $\overline{BE3}$ is tied to an external pullup resistor; for a 32-bit host CPU, $\overline{BE3}$ enables SD[31:24] $\overline{BE2}$:$\overline{BE0}$ are located on pins 81, 99, and 76, respectively.
53 SD15 54 SD14 55 SD13 56 SD12 58 SD11 59 SD10 60 SD9 61 SD8 117 SD7 116 SD6 115 SD5 114 SD4 112 SD3 111 SD2 110 SD1 109 SD0		All	Active High Input/ Output	**DATA BUS (SD15 - SD0)** These bidirectional signals may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external buffers. One external buffer for SD15:8 and the other external buffer for SD7:SD0. For the AT bus interface, these bits provide a 16-bit system data bus. For the Local bus, these bits are combined with PD31 (pin 72), PD30 (pin 75), and PD29:PD16 to provide a 32-bit data bus.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
37 38 39 40 41 42 44 45 46 47 49 50 51 52	PD29 PD28 PD27 PD26 PD25 PD24 PD23 PD22 PD21 PD20 PD19 PD18 PD17 PD16	LOC	Active High Input/ Output	**CPU Data Bus Bits (PD29:PD16)** Provide bits 29:16 on the WD90C24A/A2 Local bus. These bits are combined with PD30 (pin 75), PD31 (pin 72), and SD15:SD0 to provide a 32-bit Local Data bus. The source/sink drive capability of these pins is 3 mA on the WD90C24A and 8 mA on the WD90C24A2.
163	$\overline{\text{PDOWN}}$	All	Active Low Input	**Power-down Control** This active low input signal is used to activate the various power-down modes in conjunction with system power management (refer to *Power-down Management* in Section 26).

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS (Continued)

5.3.2 Display Buffer Memory Interface Pins

The display buffer memory interface is designed for connection of up to four 256K by 4 or one 256K by 16 fast-page-mode DRAMs. Also, memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data (CNF[31:0]) at system power up and reset. For additional information on configuration bits, refer to the *WD90C24A/A2 Configuration Register* description in Section 24.

This section is divided into the following subsections, which list the bus lines as follows:

- Bank A display memory Bus
- Bank B display memory Bus

5. 3.2.1 Bank A Display Memory Bus

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK A DISPLAY MEMORY DATA/CONFIGURATION BITS			
178	AMD15	I/O	Bank A Memory Data Bit 15:Configuration Bit CNF15
180	AMD14	I/O	Bank A Memory Data Bit 14:Configuration Bit CNF14
182	AMD13	I/O	Bank A Memory Data Bit 13:Configuration Bit CNF13
184	AMD12	I/O	Bank A Memory Data Bit 12:Configuration Bit CNF12
186	AMD11	I/O	Bank A Memory Data Bit 11:Configuration Bit CNF8
188	AMD10	I/O	Bank A Memory Data Bit 10:Configuration Bit CNF10
190	AMD9	I/O	Bank A Memory Data Bit 9:Configuration Bit CNF9
192	AMD8	I/O	Bank A Memory Data Bit 8:Configuration Bit CNF11
191	AMD7	I/O	Bank A Memory Data Bit 7:Configuration Bit CNF7
189	AMD6	I/O	Bank A Memory Data Bit 6:Configuration Bit CNF6
187	AMD5	I/O	Bank A Memory Data Bit 5:Configuration Bit CNF5
185	AMD4	I/O	Bank A Memory Data Bit 4:Configuration Bit CNF4
183	AMD3	I/O	Bank A Memory Data Bit 3:Configuration Bit CNF3
181	AMD2	I/O	Bank A Memory Data Bit 2:Configuration Bit CNF2
179	AMD1	I/O	Bank A Memory Data Bit 1:Configuration Bit CNF1
177	AMD0	I/O	Bank A Memory Data Bit 0:Configuration Bit CNF0
NOTE: AMD15 through AMD0 have internal 100 Kohm pullup resistors.			
BANK A DISPLAY MEMORY ADDRESS BITS			
200	AMA8	Output	Bank A Memory Address Bit 8
202	AMA7	Output	Bank A Memory Address Bit 7
204	AMA6	Output	Bank A Memory Address Bit 6
206	AMA5	Output	Bank A Memory Address Bit 5

TABLE 5-3. BANK A DISPLAY MEMORY SIGNALS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
			BANK A DISPLAY MEMORY ADDRESS BITS (Continued)
208	AMA4	Output	Bank A Memory Address Bit 4
207	AMA3	Output	Bank A Memory Address Bit 3
205	AMA2	Output	Bank A Memory Address Bit 2
203	AMA1	Output	Bank A Memory Address Bit 1
201	AMA0	Output	Bank A Memory Address Bit 0
NOTE: AMA8 through AMA0 form the primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			
			BANK A DISPLAY MEMORY CONTROL SIGNALS
194	$\overline{\text{ACASL}}$	Active Low Output	**CAS Bank A Low** Lower column address strobe for display memory buffer DRAM bank A.
196	$\overline{\text{AWE}}$	Active Low Output	**Write Enable Bank A** Write Enable control for display memory buffer DRAM bank A. When a 256K by 16 DRAM is used this is the DRAM write enable output.
197	$\overline{\text{ACASH}}$	Active Low Output	**CAS Bank A High** Upper column address strobe for display memory buffer DRAM bank A.
198	$\overline{\text{ARAS}}$	Active Low Output	**RAS Bank A** Row address strobe for display memory buffer DRAM bank A.
199	$\overline{\text{AOE}}$	Active Low Output	**Output Enable Bank A** Output Enable control for display memory buffer DRAM bank A. When a 256K by 16 DRAM is used, this is the DRAM output enable strobe.

TABLE 5-3. BANK A DISPLAY MEMORY SIGNALS (Continued)

5. 3.2.2 Bank B Display Memory Bus

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK B DISPLAY MEMORY DATA BITS/CONFIGURATION BITS			
2	BMD15	I/O	Bank B Memory Data Bit 15:Configuration Bit CNF31
4	BMD14	I/O	Bank B Memory Data Bit 14:Configuration Bit CNF30
7	BMD13	I/O	Bank B Memory Data Bit 13:Configuration Bit CNF29
9	BMD12	I/O	Bank B Memory Data Bit 12:Configuration Bit CNF28
12	BMD11	I/O	Bank B Memory Data Bit 11:Configuration Bit CNF27
14	BMD10	I/O	Bank B Memory Data Bit 10:Configuration Bit CNF26
16	BMD9	I/O	Bank B Memory Data Bit 9:Configuration Bit CNF25
18	BMD8	I/O	Bank B Memory Data Bit 8:Configuration Bit CNF24
17	BMD7	I/O	Bank B Memory Data Bit 7:Configuration Bit CNF23
15	BMD6	I/O	Bank B Memory Data Bit 6:Configuration Bit CNF22
13	BMD5	I/O	Bank B Memory Data Bit 5:Configuration Bit CNF21
11	BMD4	I/O	Bank B Memory Data Bit 4:Configuration Bit CNF20
8	BMD3	I/O	Bank B Memory Data Bit 3:Configuration Bit CNF19
6	BMD2	I/O	Bank B Memory Data Bit 2:Configuration Bit CNF18
3	BMD1	I/O	Bank B Memory Data Bit 1:Configuration Bit CNF17
1	BMD0	I/O	Bank B Memory Data Bit 0:Configuration Bit CNF16
NOTE: BMD15 through BMD0 have internal 100 Kohm pullup resistors.			
BANK B DISPLAY MEMORY ADDRESS BITS			
27	BMA8	Output	Bank B Memory Address Bit 8
29	BMA7	Output	Bank B Memory Address Bit 7
31	BMA6	Output	Bank B Memory Address Bit 6
33	BMA5	Output	Bank B Memory Address Bit 5
35	BMA4	Output	Bank B Memory Address Bit 4
34	BMA3	Output	Bank B Memory Address Bit 3
32	BMA2	Output	Bank B Memory Address Bit 2
30	BMA1	Output	Bank B Memory Address Bit 1
28	BMA0	Output	Bank B Memory Address Bit 0

TABLE 5-4. BANK B DISPLAY MEMORY SIGNALS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
			BANK B DISPLAY MEMORY ADDRESS CONTROL SIGNALS
20	$\overline{\text{BCASL}}$	Active Low Output	**CAS Bank B Low** Lower column address strobe for display memory buffer DRAM bank B.
22	$\overline{\text{BWE}}$	Active Low Output	**Write Enable Bank B** Write Enable control for display memory buffer DRAM bank B.
23	$\overline{\text{BCASH}}$	Active Low Output	**CAS Bank B High** Upper column address strobe for display memory buffer DRAM bank B.
24	$\overline{\text{BRAS}}$	Active Low Output	**RAS Bank B** Row address strobe for display memory buffer DRAM bank B.
25	$\overline{\text{BOE}}$	Active Low Output	**Output Enable Bank B** Output Enable control for display memory buffer DRAM bank B.

TABLE 5-4. BANK B DISPLAY MEMORY SIGNALS (Continued)

5.3.3 RAMDAC/CRT Interface Pins

Internal RAMDAC interface pins are described in the following table.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
155	FSADJ	Analog Input	**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DACs. FSADJ if PR18, bit 7 = 0 (internal RAMDAC mode). **CAUTION:** Do not ground this pin.
	$\overline{\text{MDETECT}}$	Active Low Input	**Monitor Detect** When PR18, bit 7 = 1 (external RAMDAC mode), this pin is used as a monitor detect input. The result of this input is read from 3C2h bit 4. $\overline{\text{MDETECT}}$ if PR18, bit 7 = 1 (external RAMDAC mode).
156	VREF	Analog Input	**Voltage Reference Input** An external voltage reference of 1.235V is connected to this input for normal operation of the internal RAMDAC.
157	BLUE	Analog Output	**Blue Current Output** High impedance current source can directly drive a 50-Ohm load.
158	GREEN	Analog Output	**Green Current Output** High impedance current source can directly drive a 50-Ohm load.

TABLE 5-5. INTERNAL DAC INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
159	RED	Analog Output	**Red Current Output** High impedance current source can directly drive a 50-Ohm load.
173	VSYNC	Active High Output	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register (3C2h).
174	HSYNC	Active High Output	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register (3C2h).
175	PCLK	Active High Input/ Output	**Pixel Clock** Video pixel clock output used by the external RAMDAC to latch pixel data from the WD90C24A/A2 controller's video output bus into an external RAMDAC or panel interface. Pixel data from the WD90C24A/A2 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or panel interface by the falling edge of PCLK. In Auxiliary Video Extender (AVE) Mode, this pin provides the input for the internal RAMDAC PCLK signal. (PR66 bit 7 is set to 1.)

TABLE 5-5. INTERNAL DAC INTERFACE PINS (Continued)

5.3.4 Clock Generation Interface Pins

Clock generation interface pins are described in the following table.

PIN	MNEMONIC	TYPE	DESCRIPTION
70	CLK486	Input	**CPU Clock** Provides the clock input for the Local bus. This pin has an internal 100 Kohm pulldown resistor.
103	XMCLK	Input	**External Memory Clock** In external clock mode, this signal is the MCLK input. In internal clock mode this pin is used for test.
104	MCAP	Analog Input	**Analog Input** Connects to discrete filter network.
105	VCAP	Analog Input	**Analog Input** Connects to discrete filter network.
106	VCLK2	Input/ Output	**Video Clock 2** In external PCLK clock mode, VCLK2 is one of three possible video clock inputs to the WD90C24A/A2. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types. When CNF3 is set to 1, this pin outputs either 3C2h bit 3 or PR2 bit 1. In internal clock mode this pin is used for test.
161	EXCKEN	Active High Input	**External Clock Enable** Asserted to select external clock mode.
168	VCLK1	Input/ Output	**Video Clock 1** In external PCLK clock mode, VCLK1 is one of three possible video clock inputs to the WD90C24A/A2. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types. When CNF3 is set to 1, this pin outputs either 3C2h bit 2 or the external PCLK latch enable signal.
	FPUSR1	Output	**User Programmable Output 1** In internal PCLK mode, VCLK1 is an output configured as FPUSR1. FPUSR1 is a panel interface signal that can be programmed by the user to initiate or confirm an action.
170	CKIN	Input	**System Clock Input** In internal PCLK mode, CKIN provides the CPU clock (14.318 MHz), which is the default mode. This pin has an internal 100 Kohm pulldown resistor.
	VCLK	Input	**External Video Clock** In external PCLK clock mode, VCLK is one of three possible video clock inputs to the WD90C24A/A2. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.

TABLE 5-6. CLOCK GENERATION INTERFACE PINS

5.3.5 Panel Interface Pins

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
119	XSCLKL	Active High Output	**External Shift Clock Lower** Used for single-panel 8-bit color STN LCD (Seiko).
	XSCLKU		**External Shift Clock Upper** Used for single-panel 8-bit color STN LCD (Sharp).
	XSCLK		**External Shift Clock** Used for single- and dual-panel 16-bit color STN LCD.
	BD5		**Blue Data Bit 5** This bit is used for 18-bit color TFT LCD.
120	$\overline{\text{WPLT}}$	Active Low Output	**Write Palette** If not configured for a TFT 18-bit interface, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
	BD4	Active High Output	**Blue Data Bit 4** This bit is used for 18-bit color TFT LCD.
121	$\overline{\text{RPLT}}$	Active Low Output	**Read Palette** If not configured for TFT or color STN interface, $\overline{\text{RPTL}}$ is the active low read pulse to the external RAMDAC or equivalent circuit.
	STN15	Active High Output	**Super Twisted Nematic Bit 15** Data bit 15 for 16-bit color STN LCD, single panel.
	BD3		**Blue Data Bit 3** This bit is used for 12-bit and 18-bit color TFT LCD.
	UD7		**Upper Video Data Bit 7** Data bit 7 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
122	STN14	Active High Output	**Super Twisted Nematic Bit 14** Data bit 14 for 16-bit color STN LCD, single panel.
	BD2		**Blue Data Bit 2** Data bit 2 for 9-bit, 12-bit, and 18-bit color TFT LCD.
	UD6		**Upper Video Data Bit 6** Data bit 6 for the upper 8-bits of a 16-bit color STN LCD, dual panel.

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
123	STN13	Active High Output	**Super Twisted Nematic Bit 13** Data bit 13 for 16-bit color STN LCD, single panel.
	BD1		**Blue Data Bit 1** This bit is used for 9-bit, 12-bit, and 18-bit color TFT LCD.
	UD5		**Upper Video Data Bit 5** Data bit 5 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
124	STN12	Active High Output	**Super Twisted Nematic Bit 12** Data bit 12 for 16-bit color STN LCD, single panel.
	BD0		**Blue Data Bit 0** This bit is used for 9-bit, 12-bit, and 18-bit color TFT LCD.
	UD4		**Upper Video Data Bit 4** Data bit 4 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
126	GD5	Active High Output	**Green Data Bit 5** This bit is used for 18-bit color TFT LCD.
	STN11		**Super Twisted Nematic Bit 11** Data bit 11 for 16-bit color STN LCD, single panel.
	UD3		**Upper Video Data Bit 3** Data bit 3 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
127	GD4	Active High Output	**Green Data Bit 4** This bit is used for 18-bit color TFT LCD.
	STN10		**Super Twisted Nematic Bit 10** Data bit 10 for 16-bit color STN LCD, single panel.
	UD2		**Upper Video Data Bit 2** Data bit 2 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
128	RD5	Active High Output	**Red Data Bit 5** This bit is used for 18-bit color TFT LCD.
	STN9		**Super Twisted Nematic Bit 9** Data bit 9 for 16-bit color STN LCD, single panel.
	UD1		**Upper Video Data Bit 1** Data bit 1 for the upper 8-bits of a 16-bit color STN LCD, dual panel.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
129	RD4	Active High Output	**Red Data Bit 4** This bit is used for 18-bit color TFT LCD.
	STN8		**Super Twisted Nematic Bit 8** Data bit 8 for 16-bit color STN LCD, single panel.
	UD0		**Upper Video Data Bit 0** Data bit 0 for the upper 8-bits of a 16-bit color STN LCD, dual panel.
131	D7	Active High Output	**Data Bit 7** This bit is used for monochrome STN LCD, single panel bit 7 is the left-most bit on 8-bit panels and bit 3 is the left-most bit on 4-bit panels.
	RD3		**Red Data Bit 3** This bit is used for 12-bit and 18-bit color TFT LCD.
	STN7		**Super Twisted Nematic Bit 7** Data bit 7 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN0		**Super Twisted Nematic Bit 0** Data bit 0 for 8-bit (Sharp) color STN LCD, single panel.
	LD7		**Lower Video Data Bit 7** Data bit 7 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD7		**Video Data Bit 7** Data bit 7 for the 8-bit external RAMDAC interface.
	VUD3		**UPPER PANEL DATA BIT 3** In a monochrome dual-panel LCD interface, VUD3 through VUD0 are used for the upper panel data bus. In a monochrome single panel LCD interface these pins also provide video data to the panel. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits of pixel video outputs to the RAMDAC. Fourth Pixel VUD3 Pin 131 Third Pixel VUD2 Pin 132 Second Pixel VUD1 Pin 133 First Pixel VUD0 Pin 134
	P7	Active High Input	**AVE Mode P7** In Auxiliary Video Extender (AVE) Mode, this pin provides the P7 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
132	D6	Active High Output	**Data Bit 6** This bit is used for monochrome STN LCD, single panel.
	RD2		**Red Data Bit 2** This bit is used for 9-bit, 12-bit, and 18-bit color TFT LCD.
	STN6		**Super Twisted Nematic Bit 6** Data bit 6 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN1		**Super Twisted Nematic Bit 1** Data bit 1 for 8-bit (Sharp) color STN LCD, single panel.
	LD6		**Lower Video Data Bit 6** Data bit 6 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD6		**Video Data Bit 6** Data bit 6 for the 8-bit external RAMDAC interface.
	VUD2		**Upper Panel Data Bit 2** Refer to VUD3, pin 131.
	P6	Active High Input	**AVE Mode P6** In Auxiliary Video Extender (AVE) Mode, this pin provides the P6 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)
133	D5	Active High Output	**Data Bit 5** This bit is used for monochrome STN LCD, single panel.
	RD1		**Red Data Bit 1** This bit is used for 9-bit, 12-bit, and 18-bit color TFT LCD.
	STN5		**Super Twisted Nematic Bit 5** Data bit 5 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN2		**Super Twisted Nematic Bit 2** Data bit 2 for 8-bit (Sharp) color STN LCD, single panel.
	LD5		**Lower Video Data Bit 5** Data bit 5 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD5		**Video Data Bit 5** Data bit 5 for the 8-bit external RAMDAC interface.
	VUD1		**Upper Panel Data Bit 1** Refer to VUD3, pin 131.
	P5	Active High Input	**AVE Mode P5** In Auxiliary Video Extender (AVE) Mode, this pin provides the P5 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
134	D4	Active High Output	**Data Bit 4** This bit is used for monochrome STN LCD, single panel.
	RD0		**Red Data Bit 1** This bit is used for 9-bit, 12-bit, and 18-bit color TFT LCD.
	STN4		**Super Twisted Nematic Bit 4** Data bit 4 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN3		**Super Twisted Nematic Bit 3** Data bit 3 for 8-bit (Sharp) color STN LCD, single panel.
	LD4		**Lower Video Data Bit 4** Data bit 4 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD4		**Video Data Bit 4** Data bit 4 for the 8-bit external RAMDAC interface.
	VUD0		**Upper Panel Data Bit 0** Refer to VUD3, pin 131.
	P4	Active High Input	**AVE Mode P4** In Auxiliary Video Extender (AVE) Mode, this pin provides the P4 input for the internal RAMDAC.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
135	D3	Active High Output	**Data Bit 3** This bit is used for monochrome STN LCD, single panel. bit 3 is the left-most bit on 4-bit panels and bit 7 is the left-most bit on 8-bit panels.
	GD3		**Green Data Bit 3** This bit is used for 12-bit and 18-bit color TFT LCD.
	STN3		**Super Twisted Nematic Bit 3** Data bit 3 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN4		**Super Twisted Nematic Bit 4** Data bit 4 for 8-bit (Sharp) color STN LCD, single panel.
	LD3		**Lower Video Data Bit 3** Data bit 3 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD3		**Video Data Bit 7** Data bit 7 for the 8-bit external RAMDAC interface.
	VLD3		**Lower Panel Data Bit 3** In a dual-panel LCD interface, VLD3 through VLD0 are used for the lower panel data bus. In a 4-bit plasma interface, they are reserved. In an 8-bit plasma interface they provide the second pixel of video data to the panel. In a CRT interface, they are the lower four bits of pixel video outputs to the RAMDAC.
	P3	Active High Input	**AVE Mode P3** In Auxiliary Video Extender (AVE) Mode, this pin provides the P3 input for the internal RAMDAC.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
136	D2	Active High Output	**Data Bit 2** This bit is used for monochrome STN LCD, single panel.
	GD2		**Green Data Bit 2** This bit is used for 9-bit, 12-bit and 18-bit color TFT LCD.
	STN2		**Super Twisted Nematic Bit 2** Data bit 2 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN5		**Super Twisted Nematic Bit 5** Data bit 5 for 8-bit (Sharp) color STN LCD, single panel.
	LD2		**Lower Video Data Bit 2** Data bit 2 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD2		**Video Data Bit 2** Data bit 2 for the 8-bit external RAMDAC interface.
	VLD2		**Lower Panel Data Bit 2** Refer to VLD3, pin 135.
	P2	Active High Input	**AVE Mode P2** In Auxiliary Video Extender (AVE) Mode, this pin provides the P2 input for the internal RAMDAC.
137	D1	Active High Output	**Data Bit 1** This bit is used for monochrome STN LCD, single panel.
	GD1		**Green Data Bit 1** This bit is used for 9-bit, 12-bit and 18-bit color TFT LCD.
	STN1		**Super Twisted Nematic Bit 1** Data bit 1 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN6		**Super Twisted Nematic Bit 6** Data bit 6 for 8-bit (Sharp) color STN LCD, single panel.
	LD1		**Lower Video Data Bit 1** Data bit 1 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD1		**Video Data Bit 1** Data bit 1 for the 8-bit external RAMDAC interface.
	VLD1		**Lower Panel Data Bit 1** Refer to VLD3, pin 135.
	P1	Active High Input	**AVE Mode P1** In Auxiliary Video Extender (AVE) Mode, this pin provides the P1 input for the internal RAMDAC.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
138	D0	Active High Output	**Data Bit 0** This bit is used for monochrome STN LCD, single panel.
	GD0		**Green Data Bit 0** This bit is used for 9-bit, 12-bit and 18-bit color TFT LCD.
	STN0		**Super Twisted Nematic Bit 0** Data bit 0 for 8-bit (Seiko) and 16-bit color STN LCD, single panel.
	STN7		**Super Twisted Nematic Bit 7** Data bit 7 for 8-bit (Sharp) color STN LCD, single panel.
	LD0		**Lower Video Data Bit 0** Data bit 0 for the lower 8-bits of a 16-bit color STN LCD, dual panel.
	VD0		**Video Data Bit 0** Data bit 0 for the 8-bit external RAMDAC interface.
	VLD0		**Lower Panel Data Bit 0** Refer to VLD3, pin 135.
	P0	Active High Input	**AVE Mode P0** In Auxiliary Video Extender (AVE) Mode, this pin provides the P0 input for the internal RAMDAC.
140	XSCLK	Active High Output	**X Driver Shift Clock** With a single- or dual-panel monochrome STN or TFT panel interface, this signal is used to shift the data into the X-driver. Refer to Table 5-13, *Panel Interface Pin Multiplexing.*
	XSCLKL		**External Shift Clock Lower** Used for single-panel 8-bit color STN LCD (Sharp).
	XSCLKU		**External Shift Clock Upper** Used for single-panel 8-bit color STN LCD (Seiko).
142	LP	Active High Output	**Latch Pulse** The LP output is intended to be used by a panel to latch all the current panel data into the current scan line of the panel.
143	FP	Active High Output	**Frame Pulse** FP is output as an indication to attached panels that a frame has begun.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
144	FR	Active High Output	**Frame Rate** Whenever the WD90C24A/A2 is operating in any panel mode, FR is a free-running clock, which is intended to be connected to FR inputs on some LCD panels. Frequency of its signal is programmable and is controlled by setting PR62.
	$\overline{\text{BLANK}}$	Active Low Input/ Output	**Blanking Control** $\overline{\text{BLANK}}$ is the standard analog VGA RAMDAC blanking signal. This signal is an output when the WD90C24A/A2 is operating in any CRT modes. In Auxiliary Video Extender (AVE) Mode, this pin provides the $\overline{\text{BLANK}}$ input for the internal RAMDAC.
	ENDATA	Active High Output	**Enable Data** This is a data enable output for panels such as TFT. In a plasma interface, it is an "enable video" signal.
164	$\overline{\text{LCDENA}}$	Active Low Output	**LCD Panel Enable** Provides the power off signal to the bias supply circuit of an LCD panel. The $\overline{\text{LCDENA}}$ signal is used as a power enable/disable to the high voltage bias inverter of a panel, and is tied to the WD90C24A/A2 controller's power management circuit. The WD90C24A/A2 sequences this signal as part of the panel power-on/power-off procedures designed to the protect panel power circuit. A high at this output indicates power-off to the panel and a low power-on.
165	PNLOFF	Active High Output	**Panel Power Off** PNLOFF can be used to control the power supply for the attached panel. When a panel is enabled (PR19 bit 4 is set to 1), setting PR57 bit 2 to 0 causes the PNLOFF signal to be driven high. Setting PR57 to 1 causes a low level to appear at PNLOFF.
167	FPUSR0	Output	**User Programmable Output 0** This line can be programmed by the user to initiate or confirm an action.
168	FPUSR1	Output	**User Programmable Output 1** This line can be programmed by the user to initiate or confirm an action. **NOTE:** In external PCLK mode, FPUSR1 is configured as VCLK1.

TABLE 5-7. PANEL INTERFACE PINS (Continued)

5.3.6 Power and Ground Pins

PIN NO.	MNEMONIC	DESCRIPTION
5, 21, 36, 48, 62, 79, 118, 139, 176, 195	VSS	Ground VSS=0V
10, 26, 43, 125	VDD	Main VDD Power to Core Logic
19,193	MVDD	Memory Interface VDD Supply
57,113	BVDD	System Bus Interface VDD Supply
88,141	RVDD	RAM Filtered Palette VDD Supply
108,145	RVSS	RAM Palette VSS Ground
102	AVDD1	PCLK Analog Power
107	AVSS1	PCLK Analog Ground
130	FPVDD	Panel Interface VDD Supply
154	AVDD2	RAMDAC Analog Power
160	AVSS2	RAMDAC Analog Ground
169	PVDD	Power-Down Section VDD Supply

TABLE 5-8. POWER AND GROUND SIGNAL DEFINITIONS

5.4 PIN MULTIPLEXING REFERENCE TABLES

This subsection contains the following tables:

- Host Interface Pin Multiplexing (refer to Table 5-9)
- Display Buffer Memory Interface Pin Multiplexing (refer to Table 5-10)
- RAMDAC/CRT Interface Pin Multiplexing (refer to Table 5-11)
- Clock Generation Interface Pin Multiplexing (refer to Table 5-12)
- Panel Interface Pin Multiplexing (refer to Table 5-13)

5.4.1 Host Interface Pins

PIN NO.	AT BUS	LOCAL BUS
37-42, 44-47, 49-52	Reserved	PD(29:16)
53-56, 58- 61, 117 -114, 112-109	SD(15:0)	SD(15:0)
69	SLA23	SA23
68	SLA22	SA22
67	SLA21	SA21
66	SLA20	SA20
65	SLA19	SA19
64	SLA18	SA18
63	SLA17	SA17
71	$\overline{\text{IOCS16}}$	$\overline{\text{BOFF}}$
72	$\overline{\text{MEMCS16}}$	PD31
73	$\overline{\text{SBHE}}$	CPURESET
74	ALE	$\overline{\text{ADS}}$
75	IRQ	PD30
76	$\overline{\text{EIO}}$	$\overline{\text{BE0}}$
77	$\overline{\text{IOCHRDY}}$	$\overline{\text{CPURDY}}$
78	$\overline{\text{ZWST}}$	VLBIBUSY
97	SA16	SA16
96	SA15	SA15
95	SA14	SA14
94	SA13	SA13
93	SA12	SA12
92	SA11	SA11
91	SA10	SA10
90	SA9	SA9
89	SA8	SA8
87	SA7	SA7

TABLE 5-9. HOST INTERFACE PIN MULTIPLEXING

PIN NO.	AT BUS	LOCAL BUS
86	SA6	SA6
85	SA5	SA5
84	SA4	SA4
83	SA3	SA3
82	SA2	SA2
81	SA1	$\overline{BE2}$
80	SA0	$\overline{BE3}$
99	$\overline{IOW}$	$\overline{BE1}$
98	$\overline{IOR}$	D/$\overline{C}$
100	$\overline{MEMR}$	M/$\overline{IO}$
101	$\overline{MEMW}$	W/$\overline{R}$
153	Reserved	SA31
152		SA30
151		SA29
150		SA28
149		SA27
148		SA26
147		SA25
146	Refer to Note	SA24
162	RESET	SYSRES
163	$\overline{PDOWN}$	$\overline{PDOWN}$
166	$\overline{REFRESH}$	$\overline{RDYIN}$
171	$\overline{EBROM}$	$\overline{REFLCL}$
172	Reserved	$\overline{VLBICS}$

NOTES:

In AT Bus interface mode, an external resistor (pull up or pull down) is needed.

TABLE 5-9. HOST INTERFACE PIN MULTIPLEXING (Continued)

5.4.2 Display Buffer Memory Interface Pin Multiplexing

Table 5-10 lists the pin numbers and signal names for each display memory mode. For additional information on display memory modes, refer to Section 4.

PIN NO.	ONE 256K x 16 MODE 1	EIGHT 256K x 4 OR TWO 256K x 16 MODE 2
2	Reserved	BMD15
4	Reserved	BMD14
7	Reserved	BMD13
9	Reserved	BMD12
12	Reserved	BMD11
14	Reserved	BMD10
16	Reserved	BMD9
18	Reserved	BMD8
17	Reserved	BMD7
15	Reserved	BMD6
13	Reserved	BMD5
11	Reserved	BMD4
8	Reserved	BMD3
6	Reserved	BMD2
3	Reserved	BMD1
1	Reserved	BMD0
20	Reserved	$\overline{\text{BCASL}}$
22	Reserved	$\overline{\text{BWE}}$
23	Reserved	$\overline{\text{BCASH}}$
24	Reserved	$\overline{\text{BRAS}}$
25	Reserved	$\overline{\text{BOE}}$
27	Reserved	BMA8
29	Reserved	BMA7
31	Reserved	BMA6
33	Reserved	BMA5
35	Reserved	BMA4
34	Reserved	BMA3

TABLE 5-10. DISPLAY MEMORY INTERFACE PIN MULTIPLEXING

PIN NO.	ONE 256K x 16 MODE 1	EIGHT 256K x 4 OR TWO 256K x 16 MODE 2
32	Reserved	BMA2
30	Reserved	BMA1
28	Reserved	BMA0
178	AMD15	AMD15
180	AMD14	AMD14
182	AMD13	AMD13
184	AMD12	AMD12
186	AMD11	AMD11
188	AMD10	AMD10
190	AMD9	AMD9
192	AMD8	AMD8
191	AMD7	AMD7
189	AMD6	AMD6
187	AMD5	AMD5
185	AMD4	AMD4
183	AMD3	AMD3
181	AMD2	AMD2
179	AMD1	AMD1
177	AMD0	AMD0
194	$\overline{\text{ACASL}}$	$\overline{\text{ACASL}}$
196	$\overline{\text{AWE}}$	$\overline{\text{AWE}}$
197	$\overline{\text{ACASH}}$	$\overline{\text{ACASH}}$
198	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$
199	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$
200	AMA8	AMA8
202	AMA7	AMA7
204	AMA6	AMA6
206	AMA5	AMA5
208	AMA4	AMA4
207	AMA3	AMA3
205	AMA2	AMA2
203	AMA1	AMA1
201	AMA0	AMA0

TABLE 5-10. DISPLAY MEMORY INTERFACE PIN MULTIPLEXING (Continued)

5.4.3 RAMDAC/CRT Interface Pin Multiplexing

PIN NO.	INTERNAL RAMDAC MODE	EXTERNAL RAMDAC MODE	NON-RAMDAC FUNCTIONS
120		$\overline{\text{WPLT}}$	RGB4
121		$\overline{\text{RPLT}}$	RGB3ISTN15IBD3IVD7
144		$\overline{\text{BLANK}}$	FRIENDATA
155	FSADJ	$\overline{\text{MDETECT}}$	---
156	VREF	VREF	---
157	BLUE		---
158	GREEN		---
159	RED		---
173	VSYNC		---
174	HSYNC		---
175	PCLK	PCLK	---

NOTE:
1. For internal RAMDAC mode, PR18, bit 7 = 0.
2. For external RAMDAC mode, PR18, bit 7 = 1.

TABLE 5-11. RAMDAC PIN MULTIPLEXING

5.4.4 Clock Generation Interface Pin Multiplexing

PIN NO.	INTERNAL PCLK MODE	EXTERNAL PCLK MODE	NON-CLOCK FUNCTIONS
70	CLK486	CPU Clock	---
103	---	XMCLK	---
104	MCAP	MCAP	---
105	VCAP	VCAP	---
106	---	VCLK2	---
119	---	XSCLKL	RGB17
140	---	XSCLK	---
	XSCLK	---	---
161	---	EXCKEN	---
168	FPUSR1	VCLK1	---
170	CKIN	VCLK	---

NOTE:
1. For internal PCLK mode, EXCKEN (pin 161) = 0.
2. For external PCLK mode, EXCKEN (pin 161) = 1.

TABLE 5-12. CLOCK SYNTHESIZER INTERFACE PIN MULTIPLEXING

5.4.5 Panel Interface Pin Multiplexing

PIN NO.	CRT	MONOCHROME STN		COLOR STN LCD			COLOR TFT LCD		
		DUAL LCD	SINGLE LCD	8-BIT[1]	8-BIT[2]	16-BIT	9-BIT	12-BIT	18-BIT
119	Res	Res	Res	XSCLKL	XSCLKU	XSCLK	Res	Res	BD5
120	$\overline{WPLT}$	Res	Res	Res	Res	Res	Res	Res	BD4
121	$\overline{RPLT}$	Res	Res	Res	Res	STN15|UD7	Res	BD3	BD3
122	Res	Res	Res	Res	Res	STN14|UD6	BD2	BD2	BD2
123	Res	Res	Res	Res	Res	STN13|UD5	BD1	BD1	BD1
124	Res	Res	Res	Res	Res	STN12|UD4	BD0	BD0	BD0
126	Res	Res	Res	Res	Res	STN11|UD3	Res	Res	GD5
127	Res	Res	Res	Res	Res	STN10|UD2	Res	Res	GD4
128	Res	Res	Res	Res	Res	STN9|UD1	Res	Res	RD5
129	Res	Res	Res	Res	Res	STN8|UD0	Res	Res	RD4
131	VD7|P7	VUD3	D7[3]	STN7	STN0	STN7|LD7	Res	RD3	RD3
132	VD6|P6	VUD2	D6	STN6	STN1	STN6|LD6	RD2	RD2	RD2
133	VD5|P5	VUD1	D5	STN5	STN2	STN5|LD5	RD1	RD1	RD1
134	VD4|P4	VUD0	D4	STN4	STN3	STN4|LD4	RD0	RD0	RD0
135	VD3|P3	VLD3	D3[3]	STN3	STN4	STN3|LD3	Res	GD3	GD3
136	VD2|P2	VLD2	D2	STN2	STN5	STN2|LD2	GD2	GD2	GD2
137	VD1|P1	VLD1	D1	STN1	STN6	STN1|LD1	GD1	GD1	GD1
138	VD0|P0	VLD0	D0	STN0	STN7	STN0|LD0	GD0	GD0	GD0
140	Res	XSCLK	XSCLK	XSCLKU	XSCLKL	Res	XSCLK	XSCLK	XSCLK
142	Res	LP	LP	LP	LP	LP	LP	LP	LP
143	Res	FP	FP	FP	FP	FP	FP	FP	FP
144	$\overline{BLANK}$	FR	FR	FR	FR	FR	ENDATA	ENDATA	ENDATA
164	Res	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
165	Res	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5
167	Res	Note 6	Note 6	Note 6	Note 6	Note 6	Note 6	Note 6	Note 6
168	Res	Note 7	Note 7	Note 7	Note 7	Note 7	Note 7	Note 7	Note 7

NOTES:

1. SEIKO version of 8-bit color STN LCD panel.
2. SHARP version of 8-bit color STN LCD panel.
3. Bit 7 is the left-most pixel on 8-bit panels and bit 3 is the left-most pixel on 4-bit panels.
4. Pin 164 is $\overline{LCDENA}$ for all applications listed.
5. Pin 165 is PNLOFF for all applications listed.
6. Pin 167 is FPUSR0 for all applications listed.
7. Pin 168 is FPUSR1 for all applications listed.
8. In Auxiliary Video Extender (AVE) mode (PR66, bit 7 = 1), the PCLK (pin 175), $\overline{BLANK}$ (pin 144), and P[7:0] (pins 131 through 138, respectively) become direct inputs to provide an external source with direct access to the internal RAMDAC
9. In External PCLK mode, FPUSR1 (Pin No. 168) is configured as VCLK1.
10. Res indicates a reserved location.

TABLE 5-13. PANEL INTERFACE PIN MULTIPLEXING

5.5 PANEL INTERFACE CONNECTIONS

Tables 5-14 through 5-16 provide panel interface connections for specific LCD panels. Each table lists the interface connections for a general panel type (refer to the table tile) as they apply to specific LCD panels (refer to column headings).

WD90C24A/A2		SHARP			HITACHI			NEC	TOSHIIBA	MATSUSHITA
PIN NO.	SIGNAL	LQ9D011 (9-BIT), LQ10D011 (9-BIT), LQ10D311 (9-BIT)	LQ10D311 (18-BIT)	LQ12D011 (9-BIT)* x 2 PIXELS	TX24D55VCICAA (12-BIT)	TX26D51VCIAA (9-BIT)	TX26A02VC (9-BIT)	NL6448AC30-03 (12-BIT)	LTM10C015K (9-BIT)	AA95VA3D (9-BIT)
128	RD5		R5	REQUIRES EXTERNAL LOGIC						
129	RD4		R4							
131	RD3	---	R3		R3	---	---	R3	---	---
132	RD2	R2	R2		R2	R2	R5	R2	R2	R3
133	RD1	R1	R1		R1	R1	R4	R1	R1	R2
134	RD0	R0	R0		R0	R0	R3	R0	R0	R1
126	GD5		G5							
127	GD4		G4							
135	GD3	---	G3		G3	---	---	G3	---	---
136	GD2	G2	G2		G2	G2	G5	G2	G2	G3
137	GD1	G1	G1		G1	G1	G4	G1	G1	G2
138	GD0	G0	G0		G0	G0	G3	G0	G0	G1
119	BD5		B5							
120	BD4		B4							
121	BD3	---	B3		B3	---	--	B3	---	---
122	BD2	B2	B2		B2	B2	B5	B2	B2	B3

TABLE 5-14. INTERFACE PIN CONNECTIONS FOR TFT LCD PANELS

	WD90C24A/A2	SHARP			HITACHI			NEC	TOSHIIBA	MATSUSHITA
PIN NO.	SIGNAL	LQ9D011 (9-BIT), LQ10D011 (9-BIT), LQ10D311 (9-BIT)	LQ10D311 (18-BIT)	LQ12D011 (9-BIT)* x 2 PIXELS	TX24D55VCICAA (12-BIT)	TX26D51VCIAA (9-BIT)	TX26A02VC (9-BIT)	NL6448AC30-03 (12-BIT)	LTM10C015K (9-BIT)	AA95VA3D (9-BIT)
123	BD1	B1	B1	REQUIRES EXTERNAL LOGIC	B1	B1	B4	B1	B1	B2
124	BD0	B0	B0		B0	B0	B3	B0	B0	B1
140	XSCLK	CK	CK		DCLK	DCLK	DCLK	CLK	NCLK	DCLK
142	LP	HSYNC	HSYNC		HSYNC	HSYNC	HSYNC	HSYNC	---	HD
143	FP	VSYNC	VSYNC		VSYNC	VSYNC	VSYNC	VSYNC	---	VD
144	ENDATA	ENAB	ENA		DTMG	DTMG	DTMG	DE	ENAB	DENA

NOTE:
*The panel resolution for this column only is 1024 by 768 (2 pixels with 9 bits per pixel). The resolution for all other columns is 640 by 480.

TABLE 5-14. INTERFACE PIN CONNECTIONS FOR TFT LCD PANELS (Continued)

WD90C24A/A2		SANYO	MATSUSHITA	TOSHIIBA	HITACHI			SHARP	EPSON			
PIN NO.	SIGNAL	LM-KE55-22NEZ, LCM-5505-22NTK	EDMGPN5WIF	TLX-5152S-C3M1, TLX-1832S-C3M1	LM8373DX	LM65160XUFC, LM65360XUFC, LM65262XUFC, LM65268XUFC	LMG9060ZZFC[1]	LM64P80, LM64148Z, LM64P10	EG9011D	TCM-A0610, EG9007	ECM-A9071[1]	EG9013[2]
131	VUD3/LD7	UD0	D0U	UD0	UD0	UD0	LD0	DU0	DU0	UD0	LD0	D7
132	VUD2/LD6	UD1	D1U	UD1	UD1	UD1	LD1	DU1	DU1	UD1	LD1	D6
133	VUD1/LD5	UD2	D2U	UD2	UD2	UD2	LD2	DU2	DU2	UD2	LD2	D5
134	VUD0/LD4	UD3	D3U	UD3	UD3	UD3	LD3	DU3	DU3	UD3	LD3	D4
135	VLD3/LD3	LD0	D0L	LD0	LD0	LD0	LD4	DL0	DL0	LD0	LD4	D3
136	VLD2/LD2	LD1	D1L	LD1	LD1	LD1	LD5	DL1	DL1	LD1	LD5	D2
137	VLD1/LD1	LD2	D2L	LD2	LD2	LD2	LD6	DL2	DL2	LD2	LD6	D1
138	VLD0/LD0	LD3	D3L	LD3	LD3	LD3	LD7	DL3	DL3	LD3	LD7	D0
121	UD7	---	---	---	---	---	UD0	---	---	---	UD0	---
122	UD6	---	---	---	---	---	UD1	---	---	---	UD1	---
123	UD5	---	---	---	---	---	UD2	---	---	---	UD2	---
124	UD4	---	---	---	---	---	UD3	---	---	---	UD3	---
126	UD3	---	---	---	---	---	UD4	---	---	---	UD4	---
127	UD2	---	---	---	---	---	UD5	---	---	---	UD5	---
128	UD1	---	---	---	---	---	UD6	---	---	---	UD6	---
129	UD0	---	---	---	---	---	UD7	---	---	---	UD7	---
140	XSCLK	CL2	CPX	SCP	CL2	CP	CL2	CP2	CP2	XSCL	XSCL	XSCL
143	FP	FLM	FRM	FP	FLM	FRAME	FLM	S	S	DIN	DIN	DIN
142	LP	CLI	LOAD	LP	CLI	LOAD	CL1	CP1	CP1	LP	LP	LP
144	FR	---	---	---	---	---	M	---	---	---	---	---

NOTE:

1. The resolution for these dual panels is 1024 by 768 (1 by 386 duty cycle).
2. This panel is single (1 by 480 duty cycle) with 640 by 480 resolution. All other panels listed are dual panels.
3. Resolution is 640 by 480 for all panels listed unless otherwise described in 1 or 2 above.

TABLE 5-15. INTERFACE PIN CONNECTIONS FOR MONOCHROME STN LCD PANELS

WD90C24A/A2		SANYO (16-BIT)		SHARP (8-BIT)	SHARP (16-BIT)	EPSON (8-BIT)	MATSUSHITA (16-BITS)	TOSHIBA (8-BIT)	HITACHI (16-BIT)		CITIZEN, (16-BIT)	KYOCERA (16-BIT)
PIN NO.	SIGNAL	LCM-5330-22NTK, LCM-5327-24NAK, LCM-5313-22NAK	LCM-5331-22NTK, 1/240 DUTY CYCLE	LM64C05P, LM64C031	LM64C08P 1/240 DUTY CYCLE)			TLX-8052S-C3X	LMG9710VUFC	LMG972XUFC 1/240 DUTY CYCLE	1/240 DUTY CYCLE	KCL6448HSTT 1/240 DUTY CYCLE
121	STN15	UD7	UD7	---	DU7	---	DU7	---	UD7	UD7	UD0	HD0
122	STN14	UD6	UD6	---	DU6	---	DU6	---	UD6	UD6	UD1	HD1
123	STN13	UD5	UD5	---	DU5	---	DU5	---	UD5	UD5	UD2	HD2
124	STN12	UD4	UD4	---	DU4	---	DU4	---	UD4	UD4	UD3	HD3
126	STN11	UD3	UD3	---	DU3	---	DU3	---	UD3	UD3	UD4	HD4
127	STN10	UD2	UD2	---	DU2	---	DU2	---	UD2	UD2	UD5	HD5
128	STN9	UD1	UD1	---	DU1	---	DU1	---	UD1	UD1	UD6	HD6
129	STN8	UD0	UD0	---	DU0	---	DU0	---	UD0	UD0	UD7	HD7
131	STN7	LD7	LD7	D7	DL7	D0	DL7	D7	LD7	LD7	LD0	LD7
132	STN6	LD6	LD6	D6	DL6	D1	DL6	D6	LD6	LD6	LD1	LD6
133	STN5	LD5	LD5	D5	DL5	D2	DL5	D5	LD5	LD5	LD2	LD5
134	STN4	LD4	LD4	D4	DL4	D3	DL4	D4	LD4	LD4	LD3	LD4
135	STN3	LD3	LD3	D3	DL3	D4	DL3	D3	LD3	LD3	LD4	LD3
136	STN2	LD2	LD2	D2	DL2	D5	DL2	D2	LD2	LD2	LD5	LD2
137	STN1	LD1	LD1	D1	DL1	D6	DL1	D1	LD1	LD1	LD6	LD1
138	STN0	LD0	LD0	D0	DL0	D7	DL0	D0	LD0	LD0	LD7	LD0
119	XSCLK/ XSCLKL	CL2	CL2	XCKU	XSCK	XSCLL	LCK	XCKU	CL2	CP	CL2	CP
140	XSCLKU	...	...	XCKL	...	XSCLU	...	XCKL	...	...	...	...
143	FP	FLM	FLM	YD	YD	DIN	LVS	FP	FLM	FRAME	FLM	FLM
142	LP	CLI	CLI	LP	LP	LP	LHS	LP	CLI	LOAD	CLI	LOAD
144	FR	M	M	---	---	---	M	---	M	---	--	---

TABLE 5-16. INTERFACE PIN CONNECTIONS FOR COLOR STN LCD PANEL WITH 640 BY 480 RESOLUTION

6.0 REGISTER SUMMARY

6.1 INTRODUCTION

All the standard IBM registers incorporated in the WD90C24A/A2 are functionally equivalent to the VGA implementation. Additional Western Digital registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes all registers in detail. For more information, refer to the reference literature listed in Appendix A.

6.2 VGA GENERAL REGISTERS

REGISTERS[1]	RW[2]	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Register	W	3C2	3C2	
	R	3CC	3CC	
Input Status Register 0	RO	3C2	3C2	
Input Status Register 1	RO	3BA	3DA	
Feature Control Register	W	3BA	3DA	
	R	3CA	3CA	
Video Subsystem Enable Register[3]	RW	3C3	3C3	

NOTES:
1. All Register addresses are in hexadecimal.
2. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
3. I/O Port 3C3h can be used to replace 46E8h [if CNF9 = 0] for setup in AT mode.

TABLE 6-1. VGA REGISTERS SUMMARY

6.3 VGA SEQUENCER REGISTERS

REGISTERS[1]	RW[2]	MONO	COLOR	EITHER
Sequencer Index Register	RW			3C4h
Sequencer Data Register	RW			3C5h

NOTES:
1. All Register addresses are in hexadecimal.
2. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.

TABLE 6-2. SEQUENCER REGISTERS SUMMARY

6.4 VGA CRT CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW	3B4h	3D4h	
CRT Controller Data Register	RW	3B5h	3D5h	

TABLE 6-3. CRT CONTROLLER REGISTERS SUMMARY

6.5 GRAPHICS CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW			3CEh
Other Graphics Register	RW			3CFh

TABLE 6-4. GRAPHICS CONTROLLER REGISTERS SUMMARY

6.6 ATTRIBUTE CONTROLLER REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Index Register	RW			3C0h
Attribute Controller Data Register	W			3C0h
	R			3C1h

TABLE 6-5. ATTRIBUTE CONTROLLER REGISTERS SUMMARY

6.7 RAMDAC VIDEO PALETTE REGISTERS

REGISTERS	RW	MONO	COLOR	EITHER
Write Address	RW			3C8
Read Address	W			3C7
RAMDAC State	R			3C7
Pixel Data	RW			3C9
Pixel Mask	RW			3C6

NOTES

1. RO = Read-Only, RW = Read/Write, W = Write, and R = Read.
2. All Register addresses are in hexadecimal.

TABLE 6-6. RAMDAC VIDEO PALETTE REGISTERS SUMMARY

6.8 PARADISE REGISTERS

There are three sets of Paradise Registers in the WD90C24A/A2:

- General Paradise Registers
- Extended Paradise Registers
- Flat Panel Paradise Registers

Each category of Paradise Registers is summarized in the following tables, and described in the subsequent sections of this document.

6.8.1 General Paradise Registers

REGISTERS	RW[1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0 (A)	3CF.09	13.1
Address Offset B	RW	PR0 (B)	3CF.0A	13.1
Memory Size	RW	PR1	3CF.0B	13.2
Video Select	RW	PR2	3CF.0C	13.3
CRT Lock Control	RW	PR3	3CF.0D	13.4
Video Control	RW	PR4	3CF.0E	13.5
Unlock PR0 - PR4/General Purpose Status	RW RO	PR5, bits 2:0 PR5, bits 7:3	3CF.0F	13.6
Unlock PR11 - PR17	RW	PR10	3?5.29[4]	13.7
EGA Switches	RW	PR11	3?5.2A[4]	13.8
Scratch Pad/LP Counter	RW	PR12	3?5.2B[4]	13.9
Interlace H/2 Start	RW	PR13	3?5.2C[4]	13.10
Interlace H/2 End	RW	PR14	3?5.2D[4]	13.11
Miscellaneous Control 1	RW	PR15	3?5.2E[4]	13.12
Miscellaneous Control 2	RW	PR16	3?5.2F[4]	13.13
Miscellaneous Control 3	RW	PR17	3?5.30[4]	13.14
CRTC Vertical Timing Overflow	RW	PR18A	3?5.3D[4]	13.15
NOTE: Refer to notes following Table 6-9.				

TABLE 6-7. GENERAL PARADISE REGISTERS

6.8.2 Paradise Extended Registers

REGISTERS	RW[1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Unlock Paradise Extended[6]	RO RW	PR20, bits 7:4 PR20, bits 3:0	3C5.06	14.1
Display Configuration and Scratch Pad[6]	RW	PR21	3C5.07	14.2
Scratch Pad[6]	RW	PR22	3C5.08	14.3
Scratch Pad[6]	RW	PR23	3C5.09	14.4
Write Buffer and FIFO Control[6]	RW	PR30A	3C5.10	14.5
System Interface Control[6]	RW	PR31	3C5.11	14.6
Miscellaneous Control 4[6]	RW	PR32	3C5.12	14.7
DRAM Timing and ZERO Wait State Control[6]	RW	PR33A	3C5.13	14.8
Display Memory Mapping[6]	RW	PR34A	3C5.14	14.9
FPUSR0, FPUSR1 Output Select[6]	RW	PR35A	3C5.15	14.10
Video Signature Analyzer Control[7]	RW	PR45	3C5.16	14.11
Signature Analyzer Data I[7]	RO	PR45A	3C5.17	14.11.1
Signature Analyzer Data II[7]	RO	PR45B	3C5.18	14.11.2
Feature Register I[7]	RW	PR57	3C5.19	14.12
Feature Register II[7]	RW	PR58	3C5.20	14.13
Memory Map to I/O Register for BLT Access in Local Bus mode[8]	RW	PR58A	3C5.26	14.14
Memory Arbitration Cycle Setup[7]	RW	PR59	3C5.21	14.15
FR Timing[7]	RW	PR62	3C5.24	14.16
Read/Write FIFO Control[8]	RW	PR63	3C5.25	14.17
CRT Lock Control II[8]	RW	PR64	3C5.27	14.18
Reserved for Future Need[8]	RW	PR65	3C5.28	14.19
Feature Register III[8]	RW	PR66	3C5.29	14.20
Programmable Clock Selection[8]	RW	PR68	3C5.31	14.21
Programmable VCLK Frequency[8]	RW	PR69	3C5.32	14.22
Mixed Voltage Override[8]	RW	PR70	3C5.33	14.23
Programmable REFRESH Timing[8]	RW	PR71	3C5.34	14.24
Programmable Clock Unlock[8]	RW	PR72	3C5.35	14.25
VGA Status Detect[8]	RW	PR73	3C5.36	14.26
NOTE: Refer to notes following Table 6-9.				

TABLE 6-8. PARADISE EXTENDED REGISTERS SUMMARY

6.8.3 Flat Panel Paradise Registers

REGISTERS	RW[1]	LOCATION		SECTION
		MONO-CHROME	COLOR	
PR18 Flat Panel Status	RW	3B5.31	3D5.31	15.1
PR19 Flat Panel Control I	RW	3B5.32	3D5.32	15.2
PR1A Flat Panel Control II	RW	3B5.33	3D5.33	15.3
PR1B Flat Panel Unlock	RW	3B5.34	3D5.34	15.4
PR30 Mapping RAM Unlock	RW	3B5.35	3D5.35	15.5
PR33 Mapping RAM Address Counter	RW	3B5.38	3D5.38	15.6
PR34 Mapping RAM Data	RW	3B5.39	3D5.39	15.7
PR35 Mapping RAM and Powerdown Control[5]	RW	3B5.3A	3D5.3A	15.8
PR36 LCD Panel Height Select	RW	3B5.3B	3D5.3B	15.9
PR37 Flat Panel Blinking Control	RW	3B5.3C	3D5.3C	15.10
PR39 Color LCD Control	RW	3B5.3E	3D5.3E	15.11
PR41 Vertical Expansion Initial Value	RW	3B5.37	3D5.37	15.12
PR44 Power Down Memory Refresh Control	RW	3B5.3F	3D5.3F	15.13

TABLE 6-9. FLAT PANEL PARADISE REGISTERS SUMMARY

NOTES FOR TABLES 6-7, 6-8 and 6-9

1. RO - Read-Only, WO = Write-only, RW = Read/Write
2. In the PR register notation, XXX.YY, XXX is the data port address and YY is the register index.
3. All register addresses are in hexadecimal.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. This register is loaded during power turn-on and reset.
6. These registers are compatible with registers in the WD90C31 VGA controller.
7. These registers are compatible with registers in the WD90C26 VGA controller.
8. These registers were not used in any previous Western Digital VGA controller.

6.8.4 Local Bus Registers

ADDRESS	DEFAULT VALUE	PROGRAMMED BY	DESCRIPTION
2DF2[7:0]	00	BIOS	**High Address A[31:24] decode compare**
2DF1[7]	---	---	**Reserved**
2DF1[6]	1	BIOS	**Enable Wait State** 0 = 0 Wait States 1 = 1 Wait State
2DF1[5] 2DF1[4]	11	BMD[11] BMD[10]	**$\overline{IOR}$ or $\overline{IOW}$ High/Low Duration Bits[5:4]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks (Default)
2DF1[3] 2DF1[2]	11	BMD[9] BMD[8]	**Memory Read or Write High Duration Bits[3:2]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks (Default)
2DF1[1] 2DF1[0]	11	BMD[7] BMD(6]	**Memory Read or Write Low Duration Bits[1:0]** 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = 5 clocks (Default)
2DF0[7]	1	BMD[15]	**External/Local Bus BIOS** 0 = External BIOS 1 = Local Bus BIOS (Default)
2DF0[6]	1	BMD[14]	**External/Local Bus RAMDAC** 0 = External RAMDAC 1 = Local Bus RAMDAC (Default)
2DF0[5]	1	BMD[13]	**Enable Local Bus Interface Logic** 0 = Disable Logic 1 = Enable Logic (Default)
2DF0[4]	1	BMD[12]	**Determines the pulse width of RAMDAC IOR and IOW command, high/low duration** 0 = 9 clocks 1 = 18 clocks (Default)
2DF0[3]	0	BIOS	**VGA Data Path** 0 = 16-bit Data Path 1 = Reserved
2DF0[2]	1	BIOS	**Enable $\overline{BOFF}$** 0 = Enable $\overline{BOFF}$ 1 = Disable $\overline{BOFF}$ (Use this setting)
2DF0[1:0]	00	BIOS	**Enable dual display Bits[1:0]** **1 0 CGA MDA** 0 0 = Disable Disable 0 1 = Disable Disable 1 0 = Disable Enable 1 1 = Enable Disable
NOTE: To unlock port 2DFXh, write the value ACh to port A875h.			

TABLE 6-10. LOCAL BUS REGISTERS

6.8.5 Local Bus Lock Register

The Local Bus Lock register is a write only register located at address A875h. Following power-on or reset, the default value of this register is 00. To unlock the Local Bus registers, write A875h = ACh.

6.9 COMPATIBILITY REGISTERS

FUNCTIONS	RW[1]	MDA	CGA	AT&T	HERCULES
Mode Control Register	WO	3B8	3D8	3D8	3B8
Color Select Register	WO		3D9	3D9	
Status Register	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Register	WO			3DE	
Hercules Register	WO				3BF
CRTC[3]	RW	3B0 - 3B7	3D0 - 3D7	3D0 - 3D7	3B0 - 3B7

NOTES

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hexadecimal.
3. 6845 Mode Registers.

TABLE 6-11. COMPATIBILITY REGISTERS SUMMARY

7.0 VGA GENERAL REGISTERS

This section contains complete descriptions of all the VGA General Registers. Refer to Section 6 for a register summary.

7.1 MISCELLANEOUS OUTPUT REGISTER

Read Port = 3CCh, Write Port = 3C2h

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3:2	Video Dot Clock Select Bits 1:0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.

0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6*

Horizontal Sync Polarity Selection.

0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

NOTE

Bits indicated by an asterisk (*) determine the vertical size of the vertical frame by the monitor. Their encoding is shown in the following list:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.

When in modes 0 through 5, one memory page is selected from the two 64KB pages as follows.

0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bits 3:2

Video Dot Clock Select Bits 1:0

These bits are used with PR68[4:3] to select the VCLK frequency for internal PCLK mode. For additional information refer to Section 22, *Embedded Clock Generator.*

Bit 1

System Processor Video RAM Access Enable.

0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection

Selects Monochrome (3B4h and 3B5h), or Color (3D4h and 3D5h mode. Bit 0 also maps Input Status Register 1 at MDA (3BAh) or CGA (3DAh).

0 = CRTC and status addresses for MDA mode (3BXh).
1 = CRTC and status addresses for CGA mode (3DXh).

7.2 INPUT STATUS REGISTER 0

Read Only Port = 3C2h

BITS	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.

0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit s 6:5

Reserved in VGA.

Bit 4

Monitor Detection in VGA mode. The internal monitor status is sampled and can be read from this bit. In external RAMDAC mode, the $\overline{\text{MDETECT}}$ input can be read from this bit.

0 = No Monitor Detected
1 = Monitor Detected

Bit s 3:0

Reserved.

7.3 INPUT STATUS REGISTER 1

Read Only Port = 3?Ah

BITS	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2	Reserved
0	Display Enable

Bits 7:6

Reserved.

Bits 5:4

Color Plane Diagnostics.

These bits allow the processor to set two out of eight colors by activating the Attribute Controller Color Plane Enable Register, bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.

0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bits 2:1

Reserved.

Bit 0

Display Enable Status.

0 = CRT screen display is process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

7.4 FEATURE CONTROL REGISTER

Read Port = 3CAh
Write Port = 3?Ah

BITS	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits 7:4

Reserved.

Bit 3

Vertical Sync Control:

0 = VSYNC output enabled
1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

Bits 2:0

Reserved.

7.5 VIDEO SUBSYSTEM ENABLE REGISTER

Read/Write Port = 3C3h

BITS	FUNCTION
7:1	Reserved
0	Enable Video Subsystem

Bits 7:1

Reserved.

Bit 0

In AT mode, if Configuration register CNF9 is set to 0, I/O Port 3C3h can be used to replace registers 46E8h and 102h.

PORT 3C3h	AT MODE
X0	Port 3C3h replaces registers 46E8h and 102h.
X1	Port 3C3h is not used
NOTE: With CNF9 set to 0.	

8.0 VGA SEQUENCER REGISTERS

This section contains complete descriptions of all VGA Sequencer Registers. Refer to Section 6 for a summary of all VGA registers. The port address and index for each VGA Sequencer Registers is given in the following list.

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE

Reserved bits should be set to zero.

8.1 SEQUENCER INDEX REGISTER

Read/Write Port = 3C4h

BITS	FUNCTION
7:6	Reserved
4:0	Sequencer Address/Index Bits

Bits 7:6

Reserved.

Bits 5:0

Sequencer Address/Index.

The Sequencer Address Register is written with the index value (00h through 04h) of the Sequencer register to be accessed. Sequencer extension registers are also indexed by this register.

8.2 RESET REGISTER

Read/Write Port = 3C5h, Index 00h

BITS	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bits 7:2

Reserved.

Bit 1

Synchronous Reset.

0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (bit 0 = 1).

Bit 0

Asynchronous Reset.

0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (bit 1 = 1).

8.3 CLOCKING MODE REGISTER

Read/Write Port = 3C5h, Index 01h

BITS	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bits 7:6

Reserved.

Bit 5

Screen Off

0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.

0 = Serial shift registers loaded every character or every other character clock depending on bit 2.
1 = Serial shift registers loaded every 4th character clock (32-bit fetches).

Bit 3

Dot Clock Selection

0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360) pixels).

Bit 2

Shift Load. (Effective only if bit 4 = 0).

0 = Video serializer is loaded every character clock.
1 = Video serializer are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.

Commands Sequencer to generate 8 or 9 dot wide character clock.

0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

8.4 MAP MASK REGISTER

Read/Write Port 3C5h, Index 02h

BITS	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bits 7:4

Reserved

Bits 3:0

Controls Writing to Memory Maps 0 through 3 respectively.

0 = Writing to maps 0 through 3 disallowed.
1 = Maps 0 through 3 are accessible.

8.5 CHARACTER MAP SELECT REGISTER

Read/Write Port = 3C5h, Index 03h

BITS	FUNCTION
7:6	Reserved
5	Character map Select A Bit 2
4	Character map Select B Bit 2
3	Character map Select A Bit 1
2	Character map Select A Bit 0
1	Character map Select B Bit 1
0	Character map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets. A 0 selects character map B. A 1 selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bits 7:6

Reserved.

Bit 5

Character Map A MSB Select.

The Most Significant Bit (MSB) of character map A along with bits 3 and 2, select the location of character map A as shown in the following table:

BITS			MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
5	3	2		
0	0	0	0	1st 8 Kbyte
0	0	1	1	3rd 8 Kbyte
0	1	0	2	5th 8 Kbyte
0	1	1	3	7th 8 Kbyte
1	0	0	4	2nd 8 Kbyte
1	0	1	5	4th 8 Kbyte
1	1	0	6	6th 8 Kbyte
1	1	1	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.

The MSB of character map B along with bits 1 and 0, select the location of character map B as shown in the following table:

BITS			MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
4	1	0		
0	0	0	0	1st 8 Kbyte
0	0	1	1	3rd 8 Kbyte
0	1	0	2	5th 8 Kbyte
0	1	1	3	7th 8 Kbyte
1	0	0	4	2nd 8 Kbyte
1	0	1	5	4th 8 Kbyte
1	1	0	6	6th 8 Kbyte
1	1	1	7	8th 8 Kbyte

Bits 3:2

Character Map Select A.

Refer to table under bit 5.

Bits 1:0

Character Map Select B.

Refer to table under bit 4.

8.6 MEMORY MODE REGISTER

Read/Write Port = 3C5h, Index 04h

BITS	FUNCTION
7:4	Reserved
3	Chain 4 mode
2	Odd/Even mode
1	Extended Memory
0	Reserved

Bits 7:4

Reserved

Bit 3

Chains 4 Maps.

0 = Processor sequentially accesses data using map mask register.

1 = Directs the two lower order display memory address pins (AMA0, AMA1) to select the map to be addressed. The map selections are listed in the following table.

AMA1	AMA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.

0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.

1 = sequential processor access as defined by map mask register.

Bit 1

Extended display memory.

0 = 64 KB of display memory.

1 = Greater than 64 KB of memory for VGA/ EGA modes.

Bit 0

Reserved.

9.0 VGA CRT CONTROLLER REGISTERS

This section contains complete descriptions of all VGA CRT Controller Registers. Refer to Section 6 for a summary of all VGA registers.

9.1 CRT INDEX REGISTER

Read/Write Port = 3?4h

BITS	FUNCTION
7:6	Reserved
5:0	Index Bits

Bits 7:6

Reserved

Bits 5:0

Index Bits.

CRT Controller Index pointer bits to specify the register to be addressed. Its value is programmed in hex.

9.2 HORIZONTAL TOTAL REGISTER

Read/Write Port = 3?5h, Index 00h

BITS	FUNCTION
7:0	Count Plus Retrace Less 5

Bits 7:0

Count Plus Retrace Less 5.

In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

9.3 HORIZONTAL DISPLAY ENABLE END REGISTER

Read/Write Port = 3?5h, Index 01h

This register is locked if PR3(5) = 1 or the Vertical Retrace End Register bit 7 = 1.

BITS	FUNCTION
7:0	Total Displayed Characters less 1

Bits 7:0

The total displayed characters less one are programmed in this register.

9.4 START HORIZONTAL BLANKING REGISTER

Read/Write Port = 3?5h, Index 02h.

This register is locked if PR3(5) = 1 or Vertical Retrace End Register bit 7 = 0.

BITS	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking starts when the horizontal character counter reaches this character clock value.

9.5 END HORIZONTAL BLANKING REGISTER

Read/Write Port = 3?5h, Index 03h.

This register is locked if PR3(5) = 1 or Vertical Retrace End Register bit 7 = 1

BITS	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

Bit 7

Reserved

Returns 0 on reads of the End Horizontal Blanking Register. No function is defined on writes.

Bits 6:5

Display Enable Signal Skew Control

These bits define the display enable signal skew time in relation to horizontal synchronization pulses.

The skew values are given in the following list

BIT 6	BIT 5	DISPLAY ENABLE SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

Bits 4:0

End Horizontal Blank

Start blanking register plus the width of the horizontal blank in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05h) bit 7. When the least significant five bits of the horizontal character counter matches these six bits, the horizontal blanking is ended.

9.6 START HORIZONTAL RETRACE PULSE REGISTER

Read/Write Port = 3?5h, Index 04h

This register is locked if PR3(5) = 1 and Vertical Retrace End Register bit 7 = 0.

BITS	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bits 7:0

Start Horizontal Retrace Character Count.

Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1

9.7 END HORIZONTAL RETRACE REGISTER

Read/Write Port = 3?5h, Index 05h

This register is locked if PR3 (5) = 1 or Vertical Retrace End Register bit 7 = 1.

BITS	FUNCTION
7	End Horizontal Blank Bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal

Bit 7

MSB (Sixth) Of End Horizontal Blanking Register.

Bits 6:5

Horizontal Retrace Delay.

These bits define horizontal retrace signal delay.

Refer to the following table.:

BIT6	BIT5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bits 4:0

End Horizontal Retrace

Start retrace register value is added to the width of the horizontal retrace in character clock count. The least significant five bits are programmed in this register. When the least significant five bits of the Horizontal character counter matches these five bits. the horizontal retrace signal is turned off.

9.8 VERTICAL TOTAL REGISTER

Read/Write Port = 3?5h, Index 06h

BITS	FUNCTION
7:0	Vertical Total Scan Lines

Bits 7:0

Raster Scan Line Total Less 2

The least significant eight bits of a eleven bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical

sync are also included. Bits 8 and 9 of this count are loaded into the Vertical Overflow Register (Index 07h) bits 0 and 5, respectively. Bit 10 of this count is loaded in the Vertical Timing Overflow Register (Index 3Dh), bit 0. In 6845 modes, total vertical display time in rows is programmed into bit 6 through bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (Index 09h, bits 4:0). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register bit 7 = 1.

9.9 VERTICAL OVERFLOW REGISTER

Read/Write Port = 3?5h, Index 07h

For register lock information, refer to the individual bit descriptions.

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7[1]

Vertical Retrace Start Bit 9 (Index 10h).

Bit 6[2]

Vertical Display Enable End Bit 9.

The Vertical Display Enable End register count bit 9, which is appended, along with bit 1 of this register, to the Vertical Display Enable End register at index 12h to provide a 10-bit Vertical Display Enable End count.

Bit 5[1]

Vertical Total Bit 9.

The Vertical Total register count value bit 9, which is appended, along with bit 0 of this register, to the value in the CRTC Vertical Total register at index 06h to provide a 10-bit Vertical Total count.

Bit 4

Line Compare Bit 8.

The Line Compare count value bit 8, which is appended, along with bit 6 of the CRTC Maximum Scan Line register, to the CRTC Line Compare register at index 18h to provide a 10-bit line compare value.

Bit 3[1]

Start Vertical Blank Bit 8.

The Start Vertical Blank count value bit 8, which is appended, along with bit 5 of the CRTC Maximum Scan Line register, to the CRTC Vertical Blanking register at index 15h to provide a 10-bit Vertical Blank Count value.

Bit 2[1]

Vertical Retrace Start Bit 8.

The Vertical Retrace Start count value bit 8, which is appended to the CRTC Vertical Retrace register at index 10h to provide a 9-bit Vertical Retrace Start value.

Bit 1[2]

Vertical Display Enable End Bit 8.

The Vertical Display Enable End register count bit 8, which is appended, along with bit 6 of this register, to the CRTC Vertical Display Enable End register at index 12h to provide a 10-bit Vertical Display Enable End count.

Bit 0[1]

Vertical Total Bit 8

The Vertical Total register count value bit 8, which is appended, along with bit 5 of this register, to the value in the CRTC Vertical Total register at index 06h to provide a 10-bit Vertical Total count.The Vertical Total register count value bit 8, which is appended to the value in the CRTC Vertical Total register at index 06h.

NOTES

1. This register is locked if PR3 bit 0 is set to 1 or the Vertical Retrace End register bit 7 is set to 1.
2. This register is locked if PR3 bit 1 is set to 0 and the Vertical Retrace End register bit 7 is set to 1.

9.10 PRESET ROW SCAN REGISTER

Read/Write Port = 3?5h, Index 08h

BITS	FUNCTION
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved.

Bits 6:5

Byte Panning Control.

These bits allow up to 3 byte to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bits 4:0

Preset Row Scan count.

These bits preset the vertical row scan counter once after each vertical retrace. This counter is advanced one increment after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

9.11 MAXIMUM SCAN LINE REGISTER

Read/Write Port = 3?5h, Index 09h

BITS	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4:0	Maximum Scan Line

Bit 7

200 to 400 Line conversion.

0= Normal operation.

1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.

Bit 9 of the Line Compare Register (Index 18h).

Bit 5

Start Vertical Blank.

Bit 9 of the Start Vertical Blank Register (Index 15h). This register is locked if the PR Register PR3 (0) = 1.

Bits 4:0

Maximum Scan Line.

Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 7:5 are reserved, and bits 4:0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported

9.12 CURSOR START REGISTER

Read/Write Port = 3?5h, Index 0Ah

BITS	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bits 7:6

Reserved.

Bit 5

Cursor control.

0 = Cursor on.
1 = Cursor off.

Bits 4:0

These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (Index 0Bh), no cursor is generated. For 6845 modes, bit 7 is reserved. bit 5 controls the cursor operation and bits 4:0 contain the cursor start value. Bit 6 is not used.

9.13 CURSOR END REGISTER

Read/Write Port = 3?5h, Index 0Bh

BITS	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

Bit 7

Reserved.

Bits 6:5

Cursor Skew Bits.

Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the following table.

:

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits 4:0

these bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7:5 are reserved and bits 4:0 contain row value of the cursor end.

NOTE

There are three types of cursors generated, depending upon the mode i.e., EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

9.14 START ADDRESS HIGH REGISTER

Read/Write Port = 3?5h, Index 0Ch

BITS	FUNCTION
7:0	Start Address High Byte

Bits 7:0

Display Screen Start Address Upper Byte Bits.

Eight high order bits of the 16 bit display memory address, used for screen refresh. The low order eight bit register is at index 0Dh. The PR Register PR3 bits 3 and 4 extend this display memory start register to 18 bits. In 6845 modes bits 6 & 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0Dh.

9.15 START ADDRESS LOW REGISTER

Read/Write Port = 3?5, Index 0Dh

BITS	FUNCTION
7:0	Start Address Low Byte

Bits 7:0

The lower order eight bits of the 16 bit display memory address in VGA or 6845 modes.

9.16 CURSOR LOCATION HIGH REGISTER

Read/Write Port = 3?5h, Index 0Eh

BITS	FUNCTION
7:0	Cursor Location High Byte

Bits 7:0

Cursor Address Upper Byte Bits.

The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0Fh. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5:0 are the high order bits of the cursor.

9.17 CURSOR LOCATION LOW REGISTER

Read/Write Port = 3?5h, Index 0Fh

BITS	FUNCTION
7:0	Cursor Location Low Byte

Bits 7:0

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16 bit display memory address in VGA or 6845 mode.

9.18 VERTICAL RETRACE START REGISTER

Read/Write Port = 3?5h, Index 10h

BITS	FUNCTION
7:0	Vertical Retrace Start (lower eight bits)

Bits 7:0

Vertical Retrace Start Pulse Lower Eight Bits.

The lower eight bits of the 11-bit vertical retrace start register. bits 8 and 9 are located in the Overflow Register (Index 07h). bit 10 of this count is loaded in the Vertical Timing Overflow Register (Index 3Dh), bit 2. In 6845 compatible mode, this register shows the high order six bits in positions 5:0 as the light pen read back value, and bits 6 and 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11h. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

9.19 VERTICAL RETRACE END REGISTER

Read/Write Port = 3?5h, Index 11h

BITS	FUNCTION
7	CRTC 0:7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

This register is locked if the PR Register PR3 (0) is set to 1.

Bit 7

CRTC Registers Write Protect.

0 = Enables writes to CRT index registers 00h through 07h.
1 = Write protects CRT Controller index registers in the range of index 00h through 07h. The line compare bit 4 in the Overflow Register (07h) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.

Selects DRAM refresh cycles per horizontal scan line.

0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.

0 = Enables vertical retrace interrupt.
1 = Disables vertical retrace interrupt and tristates the IRQ output pin.

Bit 4

Clear Vertical Retrace Interrupt.

0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e. the start of the bottom border).

Bits 3:0

Vertical Retrace End.

They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan counter for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of Light Pen Register.

9.20 VERTICAL DISPLAY ENABLE END REGISTER

Read/Write Port = 3?5h, Index 12h

BITS	FUNCTION
7:0	Vertical Display Enable End (lower eight bits)

Bits 7:0

Vertical Display Enable End Lower Eight Bits.

The eight lower bits of this 11-bit register define where the active display frame ends. The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (Index 07h) at bit 1 and 6 respectively. bit 10 of this count is loaded in the Vertical Timing Overflow Register (Index 3Dh), bit 1.

9.21 OFFSET REGISTER

Read/Write Port = 3?5h, Index 13h

BITS	FUNCTION
7:0	Logical Line Screen width

Bits 7:0

Logical Line Screen Width.

NOTE

Offset Register bits 9:8 come from PR18A bits 7:6, respectively.

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row scan Start Address + (K * Value in Offset Register), where K=2 in byte mode and K=4 in word mode.

9.22 UNDERLINE LOCATION REGISTER

Read/Write Port = 3?5h, Index 14h

BITS	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.

0 = Display memory address for byte or word access.
1 = Display memory address for double word access.

NOTE

Refer to Mode Control Register (Index 17h) bit 6.

Bit 5

Count By 4 for Double word Access

0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bits 4:0

Underline Location

These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

9.23 START VERTICAL BLANK REGISTER

Read/Write Port = 3?5h, Index 15h

This register is locked if PR3 (0) = 1.

BITS	FUNCTION
7:0	Start Vertical Blank (lower eight bits)

Bits 7:0

Start Vertical Blank Lower Eight Bits.

The lower eight bits of this 11-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (Index 07h) and bit 9 is in the Maximum Scan Line Register (Index 09h). Bit 10 of this count is loaded in the Vertical Timing Overflow Register (Index 3Dh), bit 3. The 11-bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

9.24 END VERTICAL BLANK REGISTER

Read/Write Port = 3?5h, Index 16h

This register is locked if PR3, bit 0 is set to = 1.

BITS	FUNCTION
7:0	End Vertical Blank

Bits 7:0

Vertical Blank Inactive Count.

End Vertical is an 8-bit value calculated as follows:

The 8-bit End Vertical Blank value =

(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

9.25 CRT MODE CONTROL REGISTER

Read/Write Port = 3?5h, Index 17h

This register is locked if PR3, bit 5 is set to 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.

0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.

0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. Refer to the following table.
1 = Byte address mode

INDEX 14h BIT 6	INDEX 17h BIT 6	ADDRESS MODE
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables bit 13 to appear at AMA0, otherwise bit 0 appears on AMA0.
1 = Select AMA15 for odd/even mode when 256KB of display memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2

0 = Character clock increments memory address counter.
1 = Character clock divided by 2 increments the address counter.

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter bit 1 as output at AMA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at AMA14 pin.

Bit 0

CRT Controller 6845 compatibility mode support for CGA operation.

0 = Row scan address bit 0 is substituted for memory address bit 13 at AMA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at AMA13 address pin.

MEMORY ADDRESS MODE	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLE WORD ADDRESS MODE
AMA0/RF0	AMA0	*AMA15 OR AMA13	AMA12
AMA1/RF1	1	0	AMA13
AMA2/RF2	2	1	0
AMA3/RF3	3	2	1
AMA4/RF4	4	3	2
AMA5/RF5	5	4	3
AMA6/RF6	6	5	4
AMA7/RF7	7	6	5
AMA8/RF8	8	7	6
AMA9	9	8	7
AMA10	10	9	8
AMA11	11	10	9
AMA12	12	11	10
AMA13	13	12	11
AMA14	14	13	12
AMA15	15	14	13

NOTE: * See bit 5, defining address wrap. This table is only applicable when Register PR1, bits 7 and 6 are set to 0, or PR16, bit 1 is set to 1. The CRT Underline Location Register (Index 14h) bit 6 also controls addressing. However, when CRT 14h, bit 6 is set to 0, only the CRT Mode Control Register (index 17h) bit 6 controls addressing.

9.26 LINE COMPARE REGISTER

Read/Write Port = 3?5h, Index 18h

BITS	FUNCTION
7:0	Line Compare (lower eight bits)

Bits 7:0

Line Compare Lower Eight Bits.

Lower eight bits of the 11-bit Scan Line Compare Register. Bbitit 8 is in the Overflow Register (Index 07h) and bit 9 is in the Maximum Scan Line Register (Index 09h). Bit 10 of this count is loaded in the Vertical Timing Overflow Register (Index 3Dh), bit 4. When the vertical counter reaches this value, the internal start of the line counter is cleared.

10.0 GRAPHICS CONTROLLER REGISTERS

This section contains complete descriptions of all Graphics Controller Registers. Refer to Section 6 for a summary of all registers.

10.1 GRAPHICS INDEX REGISTER

Read/Write Port = 3CEh

BITS	FUNCTION
7:4	Reserved
3:0	Graphics Address Bits

Bits 7:4

Reserved

Bits 3:0

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

10.2 SET/RESET REGISTER

Read/Write Port = 3CFh, Index 00h

BITS	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bits 7:4

Reserved.

Bits 3:0

Set/Reset Map.

When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (Index 01h) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined in the following list:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE

* The selection of Write Mode 0 is determined by the Graphics Mode Register (Index 05h) bit 1 and bit 0.

10.3 ENABLE SET/RESET REGISTER

Read/Write Port = 3CFh, Index 01h

BITS	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bits 7:4

Reserved

Bits 3:0

Enable Set/Reset Register (Index 00h)

0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (Index 00h) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (Index 00h), and the respective memory map is written with the bit value in the Set/Reset Register (Index 00h).

10.4 COLOR COMPARE REGISTER

Read/Write Port 3CFh, Index 02h

BITS	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bits 7:4

Reserved

Bits 3:0

Color Compare.

The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (Index 05h), data is returned without comparison. Color compare map coding is shown on the next page.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

10.5 DATA ROTATE REGISTER

Read/Write Port = 3CFh, Index 03h

BITS	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 2
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bits 7:5

Reserved

Bits 4:3

Function Select.

Function select for any of the write mode operations defined in the Graphics Mode Register (Index 05h), is defined as follows:

BIT 4	BIT3	FUNCTION *
0	0	Data unmodified
0	1	Data ANDed with the data the read latches
1	0	Data ORed with the data the read latches
1	1	Data XORed with the data the read latches

NOTES:

* The data refers to CPU data after going through the data rotation.
* The latches contain the memory data from the last memory read.

Bits 2:0

Rotate Count

It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (Index 05h)

10.6 READ MAP SELECT REGISTER

Read/Write Port = 3CFh, Index 04h

BITS	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bits 7:2

Reserved

Bits 1:0

Map Select.

These bits select Memory Map in memory read operations. It has no effect on the color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 & 1 or value 10b or 11b to select the chained maps 2 & 3. Map read is defined as follows:

BIT1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

10.7 GRAPHICS MODE REGISTER

Read/Write Port = 3CFh, Index 05h

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode Bit 1
0	Write Mode Bit 0

Bit 7

Reserved

Bit 6

256 Color Mode.

0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through the internal palette and is sent out on the lower six bits (VD5 through VD0) pins every dot clock. The remaining two video outputs (VD6, VD7) are determined by bits 2 and 3 of the Color Select Register located at Index 14h within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.

Shift Register Load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = For Map 0 through Map 3 data is loaded into the shift register for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the sequencer memory mode register (Index 04h). Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (Index 04h) This setting has no effect if bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved

Bits 1:0

Write Mode.

The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	**Write Mode 0** If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data rotate Register, with the old LSB now the new MSB.
0	1	**Write Mode 1** This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2** Memory maps are filled with the 8 bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the bit Mask Register and the resulting data is written to the four memory maps.
1	1	**Write Mode 3** Eight bits of the value contained in the Set/Reset Register (Index 00h) is written into the corresponding map, regardless of the Enable Set/Reset Register (Index 01h). The right rotated CPU data (see Write Mode 0) is ANDed with bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

TABLE 10-1. WRITE MODES

10.8 MISCELLANEOUS REGISTER

Read/Write Port = 3CFh, Index 06h

BITS	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bits 7:4

Reserved.

Bits 3:2

Memory Map 1,0

Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0h	128KB BFFF:Fh
0	1	A000:0h	64KB AFFF:Fh
1	0	B000:0h	32KB B7FF:Fh
1	1	B800:0h	32KB BFFF:Fh

Bit 1

Odd/Even Mode.

0 = CPU address bit A0 is the memory address bit AMA0.

1 = CPU address bit A is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode

This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.

0 = Alphanumeric mode selects.
1 = Graphics mode selected.

10.9 COLOR DON'T CARE REGISTER

Read/Write Port 3CFh, Index 07h

BITS	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bits 7:4

Reserved.

Bits 3:0

Memory Map Color Compare Operation.

0 = Disable color compare operation.
1 = Enable color compare operation.

10.10 BIT MASK REGISTER

Read/Write Port = 3CFh, Index 08h

BITS	FUNCTION
7:0	Bit Mask

Bits 7:0

Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable
1 = Bit position value is unmasked and can be changed in the corresponding map.

11.0 ATTRIBUTE CONTROLLER REGISTERS

This section contains complete descriptions of all Attribute Controller Registers. Refer to Section 6 for a summary of all registers.

11.1 ATTRIBUTE INDEX REGISTER

Read/Write Port = 3C0h

BITS	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

Bits 7:6

Reserved.

Bit 5

Palette Address Source.

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 through 0Fh).
1 = Enable internal color palette and normal video translation.

Bits 4:0

Attribute Controller Index Register Address Bits

NOTE

The Attribute Index register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?Ah) clears the flip-flop and selects the Address Register, which is read through address 3C1h and written at address 3C0h. Once the Address Register has been loaded with an index the next write operation to 3C0h loads the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0h, but does not toggle for reads to address 3C1h.

11.2 PALETTE REGISTERS (00h THROUGH 0Fh)

Read Port = 3C1h/Write Port = 3C0h

BITS	FUNCTION
7:6	Reserved
5	VD5
4	VD4
3	VD3
2	VD2
1	VD1
0	VD0

Bits 7:6

Reserved.

Bits 5:0

Palette Pixel Colors.

They are defined as follows:

0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the following table.

Bit 5	VD5
Bit 4	VD4
Bit 3	VD3
Bit 2	VD2
Bit 1	VD1
Bit 0	VD0

11.3 ATTRIBUTE MODE CONTROL REGISTER

Read Port = 3C1h
Write Port = 3C0h, Index 10h

BIT	FUNCTION
7	VD5, VD4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VD5, VD4 Select

0 = VD5 and VD4 palette register outputs are selected.
1 = Color Select Register (index 14h) bits 1 and 0 are selected for outputs at VD5 and VD4 pins.

Bit 6

Pixel Width

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility Line Compare in the CRT Controller.

0 = A line compare has no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.

0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code. Set this bit to zero for character fonts that do not utilize line graphics character codes.

0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.

0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable.

0 = Alphanumeric mode.
1 = Graphics mode.

11.4 OVERSCAN COLOR REGISTER

Read Port = 3C1h
Write Port = 3C0h, Index 11h

BIT	FUNCTION
7	VD7
6	VD6
5	VD5
4	VD4
3	VD3
2	VD2
1	VD1
0	VD0

Bits 7:0

Overscan/Border Color.

These bits determine the overscan or border color. For Monochrome display, this register is set to 0. Border colors are set as shown above.

11.5 COLOR PLANE ENABLE REGISTER

Read Port = 3C1h
Write Port = 3C0h, Index 12h

BITS	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bits 7:6

Reserved.

Bits 5:4

Video Status Control.

These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VD 2	VD 0
0	1	VD 5	VD 4
1	0	VD 3	VD 1
1	1	VD 7	VD 6

Bits 3:0

Color Plane Enable.

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

11.6 HORIZONTAL PEL PANNING REGISTER

Read Port = 3C1h
Write Port = 3C0h, Index 13h

BITS	FUNCTION
7:4	Reserved
3:0	Horizontal PEL Panning

Bits 7:4

Reserved

Bits 3:0

Horizontal pixel Panning.

It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to a 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots/ Character	8 Dots/ Character	256 Color Mode
0	1	0	0
1	2	1	---
2	3	2	1
3	4	3	---
4	5	4	2
5	6	5	---
6	7	6	3
7	8	7	---
8	0	---	---

11.7 COLOR SELECT REGISTER

Read Port = 3C1h
Write Port = 3C0h, Index 14h

BITS	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bits 7:4

Reserved.

Bits 3:2

Color Value MSB

Two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.

Bit 3 = Set color bit VD 7.
Bit 2 = Set color bit VD 6.

Bits 1:0

Substituted Color Value Bits.

These bits can be substituted for VD 5 and VD 4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (Index 10h).

12.0 RAMDAC VIDEO PALETTE REGISTERS

This section contains complete descriptions of all RAMDAC Video Palette registers. Refer to Section 6 for a summary of all registers.

12.1 RAMDAC WRITE ADDRESS REGISTER

Read/Write Port=3C8h

BITS	FUNCTION
7:0	RAMDAC Write Address

Bits 7:0

RAMDAC Write Address

This register contains the 8-bit address used to access one of the 256 Color Registers during a write operation. During reads, the RAMDAC Write Address is the address of the next location to be modified during write operations.

The RAMDAC Write Address should be read only after completion of a 3-write (red-green-blue) sequence. Reads in the middle of this sequence can produce unpredictable results.

Also, the user cannot interrupt a block of reads by doing a write when using the auto-increment feature.

12.2 RAMDAC READ ADDRESS REGISTER

Write Port = 3C7h

BITS	FUNCTION
7:0	RAMDAC Read Address

Bits 7:0

RAMDAC Read Address

This register contains the 8-bit address used to access one of the 256 Color Registers during a read operation.

12.3 RAMDAC STATE REGISTER

Read Port = 3C7h

BITS	FUNCTION
7:0	RAMDAC State

Bits 7:0

RAMDAC State

These RAMDAC State bits indicate whether a read or a write operation is in effect:

03h = A read operation is in effect. The address read register was accessed last.
00h = A write operation is in effect. The address write register was accessed last.

12.4 RAMDAC PIXEL DATA REGISTER

Read/Write Port = 3C9

BITS	FUNCTION
7:0	RAMDAC Pixel Data Register

Bits 7:0

RAMDAC Pixel Data Register

This is an 18-bit wide data register used for reading and writing RAMDAC color values. Three sequential reads or writes to this register are required to access all 18-bits of data at a particular read or write address.

12.5 RAMDAC PIXEL MASK REGISTER

Read/Write Port = 3C6

BITS	FUNCTION
7:0	Mask Value

Bits 7:0

Mask Value

This register is a read/write register. However, it is not to be modified by applications programs. It should be initialized to FFh by BIOS firmware during a Mode Set call.

13.0 REGULAR PARADISE REGISTERS

This section contains complete descriptions of all Regular Paradise registers. The Paradise Extended Registers are described in Section 14. Refer to Section 6 for a summary of all registers.

13.1 ADDRESS OFFSET REGISTERS PR0(A) and PR0(B)

PR0(A) - Address Offset Register A
Read/Write Port = 3CFh, Index 09h

BITS	FUNCTION
7:0	Primary Address Offset Bits

PR0(B) - Address Offset Register B
Read/Write Port = 3CFh, Index 0Ah

BITS	FUNCTION
7:0	Alternate Address Offset Bits

The WD90C24A/A2 can control up to 1 Mbytes of display memory. However, DOS only assigns 128 Kbytes total memory space for display memory, which starts at A0000h and ends at BFFFFh. To help VGA to reach the memory beyond this range, the WD90C24A/A2 has two CPU address offset registers PR0(A) and PR0(B) which can be used to support more than 128 Kbytes of linear display memory address space.

The contents of PR0(A) (bits 7:0) or PR0(B) (bits 7:0) are always added to the CPU address A(19:12) before they are translated to display memory address. This can be thought of as segment register DS and ES in the 8088/80X86 architecture, PR0(A) and PR0(B) then provide a 4 Kbyte segment of the display memory. (Increment PR0(A) or PR0(B) by one equivalents to a jump from a 4 Kbyte segment to another 4 Kbyte segment of the display memory.)

PR0(A) and PR0(B) are all set to zero value at Power on Reset. There are two ways to control whether PR0(A) or PR0(B) gets added into the CPU address.

- Sequencer extension register 3C5h (index 11) bit 7 = 0.

Case 1: PR1 bit 3 = 0, Then PR0(A) is always selected as the CPU address offset Register.

Case 2: PR1 bit 3 = 1; depending on memory mapping, if the display memory is mapped into A0000h through BFFFFh (128K bytes), the PR0(A) offset CPU address range from B0000h through BFFFFh, and the PR0(B) offset CPU address range from A0000h through AFFFFh. (CPU address A16 = 1, selects PR0(A). Otherwise PR0(B) is selected)

If the display memory is mapped into A0000h through AFFFFh (64KB) or B0000h through B7FFFh or B8000h through BFFFFh (32KB), then PR0(B) offset CPU address range from A0000h through A7FFFh or B0000h through B7FFFh. The PR0(A) offset CPU address range from A8000h through AFFFFh or B8000h through BFFFFh. (CPU address A15 = 1, selects PR0(A). Otherwise PR0(B) is selected)

- Sequencer extension register 3C5h (index 11) bit 7 = 1.

Both PR0(A) and PR0(B) are enabled, A CPU memory write selects PR0(B) as the offset register. Otherwise, PR0(A) is selected as the offset register.

13.2 PR1 - MEMORY SIZE

Read/Write Port = 3CFh, Index 0Bh

BITS	FUNCTION
7:6	Memory Size Select
5:4	Memory Mapping
3	Enable Alternate address Offset Register PR0(B)
2	16-bit Display Memory
1	Reserved
0	BIOS ROM Map Out

This register is 8 bit wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins AMD(1:0), using either pullup or pulldown external resisters.

Pull-up resistors on AMD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7:6

Memory Size.

These two bits control memory size and memory organization. They both must be set to reflect the amount of memory installed. These bits in conjunction with PR0(A), PR0(B), PR16 (1) select the way memory is mapped into the CPU address space. If PR16 (1) is set to 1, the IBM compatible memory mapping is selected regardless of PR1 (7), or PR1 (6).

The following tables list the different settings on these two bits for different memory organizations.

Also, refer to the notes following the tables

Refer to notes following Table 13-4.

PR1(7) = 0, PR1(6) = 0						
ADDRESS FROM CPU OR CRTC						ADDRESS TO DISPLAY MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA5	PA	PA	PA	PA	PA	AMA(17)
0	0	0	0	0	0	AMA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	AMA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	AMA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	AMA(2)
A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)	AMA(1)
A(0)	CA(0)	A(14) or3 XRN(5)	CA(15) or4 CA(13)	A(14)	CA(12)	AMA(0)

TABLE 13-1. IBM COMPATIBLE VGA MEMORY ORGANIZATION - 256K TOTAL

Refer to notes following Table 13-4.

PR1(7) = 0, PR1(6) = 1						
ADDRESS FROM CPU OR CRTC						ADDRESS TO DISPLAY MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA5	PA	PA	PA	PA	PA	AMA(17)
0	0	0	0	0	0	AMA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	AMA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	AMA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	AMA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	AMA(1)
A(0)	CA(0)	A(16) or3 XRN(5)	CA(15)	A(14)	CA(12)	AMA(0)

TABLE 13-2. WD90C24A/A2 MEMORY ORGANIZATION - 64K/PLANE - 256K TOTAL

Refer to notes following Table 13-4.

PR1(7) = 1, PR1(6) = 0						
ADDRESS FROM CPU OR CRTC						ADDRESS TO DISPLAY MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
PA5	PA	PA	PA	PA	PA	AMA(17)
A(16)	CA(16)	A(17)	CA(16)	A(18)	CA(16)	AMA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	AMA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	AMA(14)
---	---	---	---	---	---	---
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	AMA(2)
A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)	AMA(1)
A(0)	CA(0)	A(16) or3 XRN(5)	CA(15)	A(16)	CA(14)	AMA(0)

TABLE 13-3. WD90C24A/A2 MEMORY ORGANIZATION - 128K/PLANE - 512K TOTAL

Refer to notes following Table 13-4.

PR1(7) = 1, PR1(6) = 1						
ADDRESS FROM CPU OR CRTC						ADDRESS TO DISPLAY MEMORY
BYTE WIDE		WORD WIDE		DOUBLEWORD WIDE		
CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	CPU	CRT/ BITBLT	
A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)	AMA(17)
A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)	AMA(16)
A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)	AMA(15)
A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)	AMA(14)
A(13)	CA(13)	A(13)	CA(12)	A(13)	CA(11)	AMA(13)
---	---	---	---	---	---	---
A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)	AMA(2)
A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)	AMA(1)
A(0)	CA(0)	A(16) or3 XRN(5)	CA(15)	A(18)	CA(16)	AMA(0)

TABLE 13-4. WD90C24A/A2 MEMORY ORGANIZATION - 256K/PLANE - 1M TOTAL

NOTES FOR TABLES 13-1 THROUGH 13-4

1. A(19:0) are WD90C24A/A2 internally modified system addresses (CPU address plus offset address).
2. CA(17:0) are either CRT Character Address Counter bits or BITBLT generated counter bits
3. XRN(5) represents the inverted bit 5 or the Miscellaneous Output Register (3C2h). XRN(5) can be used to replace CPU address bits in order to select memory pages in word mode. For IBM compatible memory mapping, 3C5.4, bit 1 = 1 selects XRN(5) to replace CPU address bits.

   In other memory mapping schemes, PR1(7,6) are not set to 00. Registers 3C5.4, bit 1 = 1 and PR16 (2) = 1 will select XRN(5) to replace address bits.
4. CA(15) is selected as AMA(0) if CRTC Mode Register 17, bit 5 = 1 1 in word addressing modes.
5. PA is the memory plane select bit when the DRAM interface is set for 16 bits.

   PA = 0 selects Plane 1, 0

   PA = 1 selects Plane 3, 2
6. AMA(17:0) are divided into $\overline{RAS}$ and $\overline{CAS}$ addresses as follows:

MEMORY CONFIGURATION	MEMORY ADDRESS BITS	$\overline{RAS}$ OR $\overline{CAS}$ BITS
256K X 4 DRAM	AMA(16)-AMA(8)	$\overline{RAS}$(8)-$\overline{RAS}$(0)
	AMA(17), AMA(7)-AMA(0)	$\overline{CAS}$(8)-$\overline{CAS}$(0)
256K X 16 DRAM	AMA(16)-AMA(8)	$\overline{RAS}$(8)-$\overline{RAS}$(0)
	AMA(17), AMA(7)-AMA(0)	$\overline{CAS}$(8)-$\overline{CAS}$(0)
64K X 16 DRAM	AMA(15)-AMA(8)	$\overline{RAS}$(7)-$\overline{RAS}$(0)
	AMA(7)-AMA(0)	$\overline{CAS}$(7)-$\overline{CAS}$(0)
AMA(17,16)=00 AMA(17,16)=01 AMA(17,16)=10 AMA(17,16)=11	Select first 64K bank Select second 64K bank Select third 64K bank Select forth 64K bank	

PR1(5,4)

Memory Map Select

BIT 5	BIT 4	FUNCTION
0	0	IBM VGA Mapping, CPU addresses are decoded from 0A0000h-0BFFFFh from the lowest 1M byte CPU address space, (depending on 3CF.06 bits 2, & 3)
0	1	1st 256K byte in any 1M byte CPU addressing space, X00000h-X3FFFFh
1	0	1st 512K byte in any 1M byte CPU addressing space, X00000h-X7FFFFh)
1	1	In any 1M byte CPU address space, X00000h-XFFFFFh

NOTE

PR34A (3C5.14) bits 3:0 control which 1M byte of CPU address space the WD90C24A/A2 is mapped to.

Bit 3

Enable Alternate Address Offset Register PR0(B)

Bit 2

Enable 16 Bit CPU interface for display memory

When set to 1, $\overline{\text{MEMCS16}}$ is active low for all of the display memory cycles.

Bit 1

Reserved

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-down resistor on AMD(0) sets this bit to a 1 at power on reset.

13.3 PR2 - VIDEO SELECT REGISTER

Read/Write Port = 3CFh, Index 0Ch

BITS	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Reserved
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register & mode.

Bit 6

0 = VGA or EGA mode.
1 = Non-VGA (6845) mode.

Bit 5

Character Map Select. The following functions are overridden by setting PR15 (2). This bit in conjunction with PR2 (2) and bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected per the following table.

PR2(5)	PR2 (2)	ATT (4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE

Selecting page mode addressing (setting PR15 bit 2 to 1) overrides the plane selected in the previous table.

Bits 4:3

Character clock period control

BIT 4	BIT 3	FUNCTION
0	0	IBM VGA Character Clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	8 dots if PR17(5) = 0 10 dots if PR17(5) = 1

NOTE

The character clock period control functions have no effect in graphics modes (Graphics mode always uses eight dots).

Bit 2

Underline and Character Map Select.

Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 3, which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2 (5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2 (5) for details.

Bit 1

Reserved

Bit 0

Force VCLK (overrides SEQ1 bit 3)

Forces horizontal sync timing clock of the CRTC to VCLK.

Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

13.4 PR3 - CRT LOCK CONTROL REGISTER

Read/Write Port = 3CFh, Index 0Dh

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Bit 7

Lock VSYNC polarity, as programmed in 3C2 bit 7

Bit 6

Lock HSYNC polarity, as programmed in 3C2 bit 6

Bit 5

Lock Horizontal Timing.

Locks CRTC registers of Group 0 and 4. Prevents attempts by applications software to unlock Group 0 registers by setting 3?5.11h bit 7 = 0.

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0Ch, and bit 9 of Cursor Location High 3?5.0Eh. This bit corresponds to Character Address CA(17h).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0Ch, and bit 8 of Cursor Location High 3?5.0Eh. This bit corresponds to Character Address CA (16h).

Bit 2

Cursor Start, Stop, Preset Row Scan, and Maximum Scan Line Address registers values multiplied by two.

Bit 1

Lock Prevention.

1 = Prevents attempts by applications software to lock registers of Group 1 by its setting 3?5.11 bit 7 = 1.

Bit 0

Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempts by applications software to unlock Group 2 registers by its setting 3?5.11 bit 7 = 0.

CRT Controller Register Locking

Register locking is controlled by 4 bits. They are PR3 (5, 1, 0) and 3?5.11 (7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When 3?5.11 bit 7 is 1, CRT controller registers (R0 through R7) are write protected per VGA definition. For a list of the five locking groups, and their locking schemes, refer to the following table.

LOCKING GROUP 0		
Group 0 registers are locked if: Register PR3, bit 5 is set to 1 OR Register 3?5h, Index 11h, bit 7 is set to 1		
REGISTER	**INDEX**	**NAME**
3?5	00	Horizontal Total Characters per Scan
3?5	01	Horizontal Display Enable End
3?5	02	Start Horizontal Blanking
3?5	03	End Horizontal Blanking
3?5	04	Start Horizontal Retrace
3?5	05	End Horizontal Retrace

TABLE 13-5. CRT CONTROLLER REGISTER LOCKING

LOCKING GROUP 1		
Group 1 registers are locked if: Register PR3, bit 1 is set to 0 **AND** Register 3?5h, Index 11h, bit 7 is set to 1		
REGISTER	**INDEX**	**NAME**
3?5	07 Bit 1	Vertical Display Enable End, Bit 8
3?5	07 Bit 6	Vertical Display Enable End, Bit 9
LOCKING GROUP 2		
Group 2 registers are locked if: Register PR3, bit 1 is set to 0 **OR** Register 3?5h, Index 11h, bit 7 is set to 1		
REGISTER	**INDEX**	**NAME**
3?5	06	Vertical Total
3?5	07 Bit 7	Vertical Retrace Start Bit 9
3?5	07 Bit 5	Vertical Total Bit 9
3?5	07 Bit 3	Start Vertical Blank Bit 8
3?5	07 Bit 2	Vertical Retrace Start Bit 8
3?5	07 Bit 0	Vertical Total Bit 8
3?5	09 Bit 5	Start Vertical Blank Bit 9
LOCKING GROUP 3		
Group 3 registers are locked if: Register PR3, bit 0 is set to 1		
REGISTER	**INDEX**	**NAME**
3?5	10	Vertical Retrace Start
3?5	11 Bits 3:0	Vertical Retrace End
3?5	15	Start Vertical Blanking
3?5	16	End Vertical Blanking
LOCKING GROUP 4		

TABLE 13-5. CRT CONTROLLER REGISTER LOCKING (Continued)

Group 4 registers are locked if: Register PR3, bit 5 is set to 1		
REGISTER	**INDEX**	**NAME**
3?5	17 Bit 2	CRT Mode Control (Selects Vertical Timing as Horizontal Retrace or Horizontal Retrace divided by 2.)

TABLE 13-5. CRT CONTROLLER REGISTER LOCKING (Continued)

13.5 PR4 - VIDEO CONTROL REGISTER

Read/Write Port = 3CFh, Index 0Eh

The video monitor output control register (PR4) can be programmed to tristate the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK = VCLK
5	Tristate Video Outputs
4	Tristate Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Extended 256 color Shift Register Control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$. Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15 bit 1.

Bit 6

Select PCLK equal to VCLK.

0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tristates video outputs XSCLK, PCLK, $\overline{\text{RPTL}}$, $\overline{\text{WPTL}}$, UD[7:0], LD[7:0], FP, LP, and FR$\overline{\text{BLANK}}$. This bit is typically used for manufacturing test.

In the WD90C24A/A2 controller, these outputs are turned off.

0 = Normal Operation
1 = Enable Tristate

Bit 4

Tristate the memory control outputs. The memory address bus AMA(8:0), and all ten DRAM control signals are tristated when this bit is set to 1

Bit 3

Overrides CGA bit 3 (enable video) of mode register 3D8, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on or system reset do not cause override.

Bit 2

Set to 1 to lock Internal palette and overscan registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3C0/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1, disables reading PR0 through PR5, In VGA mode (PR4 bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definitions.

Bit 0

Extended Shift Register Control

These bits should be set to one for extended 256 color modes (IBM mode 13 is not included).

13.6 PR5 - GENERAL PURPOSE STATUS BITS/ UNLOCK PR0 THROUGH PR4

Read/Write Port = 3CFh, Index 0Fh

BIT	FUNCTION
7	Read CNF7 Status
6	Read CNF6 Status
5	Read CNF5 Status
4	Read CNF4 Status
3	Read CNF8 Status
2	PR0 through PR4 Unlock
1	PR0 through PR4 Unlock
0	PR0 through PR4 Unlock

Bits 2:0 are READ/WRITE bits and cleared to 0 by reset. This provides lock or unlock capability for PR registers PR0 through PR4. The PR0 through PR4 registers are unlocked when value X5h is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 through PR5.

PR5 REGISTER BIT	CNF REGISTER
7	7
6	6
5	5
4	4
3	8
NOTE: All CNF Registers listed are Read Only.	

Bits 2:0

READ/WRITE bits are cleared to 0 by reset. They control writing to PR registers PR0 through PR4 as follows:

PR5 BITS 2	1	0	REGISTERS PR0 THROUGH PR4
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected
1	0	1	Write enable

13.7 PR10 - UNLOCK PR11 THROUGH PR17

Read/Write Port = 3?5h, Index 29h
Read Unlock: PR10 (3?5.29h) = 1xxx0xxxb

This register is READ/WRITE and cleared to 0 by reset. PR11 through PR17 can be loaded if PR10 contains XXXXX101b, and can be read only if PR10 contains 1XXX0XXXb. Bit 7, bit 3, and bits 2:0 control access to PR registers PR11 through PR17. Bits 7 and 3 enable register read operations for PR11 through PR17. Bits 6:4 may be used as scratch pad bits. Bits 2:0 enable register write operations for PR11 through PR17.

BITS	FUNCTION
7	PR11 - PR17 - Read Enable Bit 1
6:4	Scratch Pad
3	PR11 - PR17 - Read Enable Bit 0
2:0	PR11 - PR17 - Write Enable

BIT 7	BIT 3	PR11 - PR17
0	X	Read Protected, read back data 00h
X	1	Read protected, read back data 00h
1	0	Read Enabled

BIT 2	BIT 1	BIT 0	PR11 - PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write enabled

BIT6	BIT 5	BIT 4	PR10 (6:4)
0	X	X	Scratch Pad
X	1	X	Scratch Pad
X	X	0	Scratch Pad
1	0	1	Reserved for manufacturing test.

13.8 PR11 - EGA SWITCHES

Read/Write Port = 3?5h, Index 2Ah

The EGA configuration bits are stored in the PR11 bits 7:4. PR11 bits 3:0 are read/write bits that are cleared to 0 at power-on or system reset.

BIT	FUNCTION
7	Memory Mode Configuration (CNF16)
6	Memory Mode Configuration (CNF14)
5	Memory Mode Configuration (CNF13)
4	Bus Architecture (CNF17)
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits 7:5

Configuration Bits CNF13, 14, and 16

Configuration bits CN13, CN14, and CNF16 are used to select the memory mode at power-on and reset as listed in Table 13-6. These bits are read/write and latched internally from corresponding memory data bus pins AMD[15:13] and BMD[15:0]. These bits can be read as bit 4 of port 3C2h if the EGA Compatibility bit [PR4, bit 1] has been set to 1. Selection of the bit to be read is determined by bits 3 and 2 of the Miscellaneous Output Register 3C2h, as listed in Table 13-7.

For additional information on configuration registers, refer to Section 24.

MEMORY					
MODE	DRAMS		CNF16 PR11[7]	CNF14 PR11[6]	CNF13 PR11[5]
	TYPE	QTY			
1	256Kx16	1	1	0	1
2[3]	256Kx16	2	1	0	0

NOTES:

1. With CNF[16] set to 0, display memory uses 256K by 16 DRAMs.
2. CNF(16), CNF(14), and CNF(13) are readable via PR 11 bits 7, 6, and 5, respectively (refer to Section 24).
3. Mode 2 has no frame buffer.

TABLE 13-6. MEMORY MODE SETUP

WRITE		READ
3C2h BIT 3	3C2h BIT 2	3C2h BIT 4
0	0	PR11, Bit 7 (CNF16)
0	1	PR11, Bit 6 (CNF14)
1	0	PR11, Bit 5 (CNF13)
1	1	PR11, Bit 4 (CNF17)

TABLE 13-7. READING MEMORY MODE AND BUS ACHITECTURE VIA REGISTER 3C2h

BIT 4

Bus Architecture (CNF17)

Configuration bit CNF17 works with bit CNF2 to select the bus architecture during power-on and reset as listed in Table 13-8.

CNF17	CNF2	HOST MODES
0	0	Reserved
0	1	ISA Bus
1	0	Reserved
1	1	Local Bus including VESA VL-Bus

TABLE 13-8. BUS ARCHITECTURE SELECTION

The bus architecture is selected during power-on and reset as described in Section 24 *WD90C24A/A2 Configuration Registers.*

Configuration bit CNF17 can be read as bit 4 of port 3C2h if the EGA Compatibility bit [PR4, bit 1] has been set to 1. Selection of the bit to be read is determined by bits 3 and 2 of the Miscellaneous Output Register 3C2h, as listed in Table 13-7

Bit 3

Select EGA emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2

Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1. (Refer to Section 22.)

Bit 1

Lock Graphics Controller/Sequencer screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller and Sequencer:

Graphics controller	3CFh, Index 05, bits 6:5
Sequencer	3C5h, Index 01, bits 5:2
Sequencer	3C5h, Index 03, bits 5:0

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

Bit 0

Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during reads.

13.9 PR12 - SCRATCH PAD/LP COUNTER

Read/Write Port = 3?5h, Index 2Bh

BITS	FUNCTION
7:0	Scratch Pad Bits 7:0

The data in this register is unaffected by hardware reset and undefined at power up.

When PR17 bit 6 is set to 1, this register is the LP Counter. The LP Counter is used to compensate the LP count for dual panel STN LCD operation.

13.10 PR13 - INTERLACE H/2 START

Read/Write port = 3?5h, Index 2Ch

BITS	FUNCTION
7:0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed into the Horizontal Retrace Start Register (3?5.04h) and Horizontal Total Register (3?5.00h):

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE

In the above expression, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

13.11 PR14 - INTERLACE H/2 END

Read/Write Port = 3?5h, Index 2Dh

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

BITS	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

Bit 7

Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0.

Bit 6

Vertical Double Scan. This bit should be set to 1 when emulating EGA on PS/2 display. Setting this bit to 1 causes the CRTC Vertical Displayed Line Counter and Row Scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 bit 7 = 0) is programmed to be positive. Therefore, the relationship between the actual number of line displayed [N] and the data [n] programmed in to the Vertical Display Enable End register is:

N = 2(n + 1)

There is a similar relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register. This bit is usually set to 1.

Bit 5

Interlaced mode.

Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.

Line compare and double scan are not supported.

Bits 4:0

Interlaced H/2 End bits 4:0. Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

13.12 PR15 - MISCELLANEOUS CONTROL 1

Read/Write Port = 3?5h, Index 2Eh

BIT	FUNCTION
7	Read 46E8h Enable
6	High VCLK
5	Reserved
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8h. This bit is functional only if AT BUS architecture [CNF2 = 1] is selected. Setting this bit to 1 enables I/O port 46E8h to be read, regardless of the state of its own bits 3 and 4 of port 102 bit 0 (sleep bit). Only bits 4:0 of port 46E8h are readable; bits (7:5) are 0.

Bit 6

Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much higher than the memory clock (MCLK) frequency. This bit should be set to 1 if (MCLK in MHz) / VCLK in MHz) = 1.5

This bit also should be set to 1 in all extended 256 color modes.

Bit 5

Reserved

Bit 4

Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.

Bit 3

Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated form the trailing edge of non-skewed horizontal sync. Instead of leading edge, as generated for VGA timing. Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than $\overline{RAS}$-$\overline{CAS}$ addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access display memory by 30 to 40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR2 (2). Setting this bit to one in any alpha mode overrides the character map select functions of PR2 (2) and PR2 (5). When this bit is set to 1, it redefines the Character Map Select Register (3C4.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits 2:0 of this register while the map selection is determined by the bits 4:3. A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

The character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the following table:

3C5.03 BIT 4	3C5.03 BIT 3	ATT BIT 3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE

These Character Map Select functions override the functions of PR2 bit 5.

This bit must be set to 1 before loading the character maps in the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select. This bit is used to select between two types of display enable timings available at output pin BLNKN if PR4 (7) = 1. If PR4 (7) = 0, this bit has no effect.

0 = BLNKN supplies Pre-Display enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

13.13 PR16 - MISCELLANEOUS CONTROL 2

Read/Write Port = 3?5h, Index 2Fh

BIT	FUNCTION
7	External register 46E8h lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7

Lock External 46E8h register.

Setting this bit to 1 causes $\overline{\text{EBROM}}$ output to be forced high (inactive) during I/O writes to port 46E8h. This bit has no effect on loading the internal port 46E8h.

Bits 6:5

CRTC Address Counter Width.

Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double Word). These bits may be used in virtual VGA applications containing 512KB or 1024KB of display memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16 (6) should be set to 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. The following table lists the appropriate bit settings.

PR16		
BIT 6	BIT 5	COUNT WIDTH
0	0	256K
0	1	128K
1	X	64K

Bits 4:3

CRTC Address Counter Offset

Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even

This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06h (1) to 1, setting 3C5.04h (3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2h (5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1 (7:6).

Bit 1

VGA Memory Mapping

1 = Selects 256KB IBM VGA Mapping, regardless of the Memory Size bits PR1 (7:6).

Bit 0

Lock RAMDAC write strobe (3C6h through 3C9h)

0 = Normal operation
1 = Output $\overline{\text{WPLT}}$ to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C24A/A2 is also protected from the modification but may still be read at the port 3C7h.

13.14 PR17 - MISCELLANEOUS CONTROL 3

Read/Write Port = 3?5h, Index 30h

BITS	FUNCTION
7	Reserved
6	Enable LP Counter Register PR12
5	Character clock period select
4	PCLK = $VCLK/_2$
3	Map out 4K of BIOS ROM
2	Enable 64K BIOS ROM
1	Hercules Compatibility
0	Map out 2K of BIOS ROM

Bits 7

Reserved

Bit 6

Enable LP Counter Register PR12

When this bit is set to 1, LP Counter Register PR12 is enabled.

Bit 5

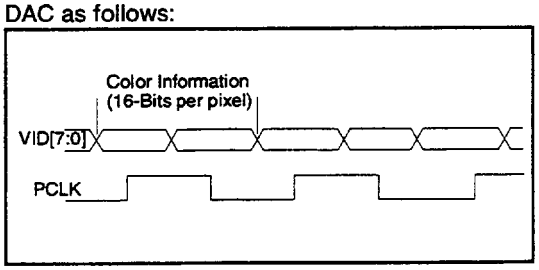
Character Clock Period Select.

When PR2 (3CF:0C) bits 4:3 = 11, then setting this bit to 0 selects the 6 dot font. Setting this bit to 1, selects the 10 dot font. Otherwise this bit has no effect.

Bit 4

PCLK = $VCLK/_2$

With this bit set to 1 it forces PCLK = $VCLK/_2$. This control is useful for interface with high color RAM-DAC as follows:



Bit 3

Map out 4K of BIOS ROM.

Setting this bit to 1 disables access to the BIOS ROM in the system address range of C000:0h through CFFF:Fh. Power-on or system reset sets this bit to 0.

Bit 2

Enable 64K BIOS ROM.

Setting this bit to 1 enables address of the BIOS ROM in the system address range C000:0h through CFFF:Fh. Power-on or system reset sets this bit to 0.

Bit 1

Setting this bit to a 1 locks Hercules compatibility register (I/O port 3BFh). Power on reset sets this bit to 0.

Bit 0

Map out 2K of BIOS ROM.

Setting this bit to 1 disables access of the BIOS ROM in the system address range C600:0h through C67F:Fh. Power-on or system reset sets this bit to 0.

13.15 PR18A - CRTC VERTICAL TIMING OVERFLOW

Read/Write Port = 3?5h, Index 3Dh

These bits combined with other vertical timing overflow bits in the CRTC provide an 11-bit vertical timing control. These bits are set to zero at power-on or system reset.

BITS	FUNCTION
7:5	Reserved
4	Line Compare Bit 10
3^1	Start Vertical Blank Bit 10
2^1	Start Vertical Retrace Bit 10
1^2	Vertical Display Enable End Bit 10
0^1	Vertical Total Bit 10

NOTES
1 This bit is locked if PR3 bit 0 = 1 OR 3?5, Index 11, bit 7 = 1
2 This bit is locked if PR3 bit 1 = 0 AND 3?5, Index 11, bit 7 = 1

14.0 PARADISE EXTENDED REGISTERS

This section contains complete descriptions of all Paradise Extended registers. The Regular Paradise Registers are described in Section 13. Refer to Section 6 for a summary of all registers.

14.1 PR20 - UNLOCK PARADISE EXTENDED REGISTERS

Read/Write Port = 3C5h, Index 06h
Reset State = Locked

BITS	FUNCTION
7:0	Unlock Paradise Extended Registers

A value of x1x01xxx (48h) must be loaded to allow read/write of the Paradise Extended Registers (refer to Table 6-8). When the extended registers are locked, then the Sequencer index is readable as three bits only. When unlocked, the Sequencer index read returns a 6-bit value.

14.2 PR21 - DISPLAY CONFIGURATION AND SCRATCH PAD

Read/Write Port = 3C5h, Index 07h

This register provides a convenient location for determining the current VGA configuration state. This information is needed for many of the BIOS calls.

BITS	FUNCTION
7:4	Scratch Pad Bits
3	Status of 3C2 Bit 0
2	Status of PR2 Bit 6
1	Status of PR4 Bit 1
0	Status of PR5 Bit 3

Bits 7:4

Read/Write scratch pad for any BIOS status data that may need to be saved.

Bit 3

Reflects the setting of the I/O address select bit in the Miscellaneous Output Register.

0 = MDA (3Bx) addresses have been picked.
1 = CGA (3Dx) addresses have been selected by this read-only bit

Bit 2

Reflects the setting of the VGA/6845 select bit in PR2 (3CF index C).

0 = VGA or EGA compatibility has been picked.
1 = 6845 compatibility has been selected by this read-only bit

Bit 1

Reflects the setting of the VGA/EGA select bit in PR4 (3CF index E).

0 = VGA was picked.
1 = EGA compatibility has been selected by this read-only bit.

Bit 0

Reflects the setting of the Analog/TTL status bit in PR5 (3CF index F).

0 = Analog monitor selected by this read-only bit.
1 = TTL-type monitor picked.

14.3 PR22 - SCRATCH PAD REGISTER

Read/Write Port = 3C5h, Index 08h

BITS	FUNCTION
7:0	Scratch Pad Bits

Bits 7:0

Scratch pad bits

14.4 PR23 - SCRATCH PAD REGISTER

Read/Write Port = 3C5h, Index 09h

BITS	FUNCTION
7:0	Scratch Pad Bits

Bits 7:0

Scratch pad bits

14.5 PR30A - WRITE BUFFER AND FIFO CONTROL REGISTER

Read/Write Port = 3C5h, Index 10h

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset.

BITS	FUNCTION
7:6	Write buffer control
5	32-Bit or 16-Bit Memory data path
4	Disable 16-Bit CPU interface
3	2-level FIFO
2	4-level or 8-level FIFO
1:0	Display FIFO control

Bits 7:6

Bits 6 and 7 control the depth of the write buffer.

BITS		FUNCTION
7	6	
0	0	Write buffer is one level deep
0	1	Write buffer is two levels deep
1	0	Write buffer is three levels deep
1	1	Write buffer is four levels deep

PR31 bit 2 must be set to 1 for these two bits to have any effect.

Bit 5

0 = Data Path is 32-bits wide
1 = Data Path is 16-bits wide

Bit 4

0 = Normal conditions
1 = 16-bit interface, unchained mode is disabled. This is for debug only.

Bit 3

0 = The FIFO is 4 or 8 levels deep depending on bit 2 of this register.
1 = The FIFO is 2 levels deep regardless of bit 2.

Bit 2

0 = FIFO set to 8 levels deep
1 = FIFO set to 4 levels deep.

Bits 1:0

Display FIFO Control

These two bits can be used to adjust the display memory bandwidth. It is recommended that these two bits be set to 01 to accommodate most applications. These bits have no effect in any text mode. They are locked into 00 internally when a text mode is set.

BITS		FUNCTION
1	**0**	**The FIFO will request a memory cycle when the FIFO status is:**
0	0	One level empty
0	1	Two levels empty
1	0	Three levels empty
1	1	Four levels empty

14.6 PR31 - SYSTEM INTERFACE CONTROL

Read/Write Port = 3C5h, Index 11h

(Reset State = 00h)

This register provides the control bits for the system interface. This register should be set during the Post initialization routines of the VGA BIOS. The reset state is 100% IBM VGA compatible. Bit 7 is used during some of the enhanced display modes.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY release Control 1
3	CPU Read RDY release Control 0
2	Enable Write Buffer
1	Enable 16-Bit Attribute Controller
0	Enable 16-Bit CRTC, Sequencer and GRC

Bit 7

0 = Normal (Refer to PR0(A) and PR0(B) definitions).
1 = The offset register PR0(A) is added to CPU address for read cycles, while PR0(B) is added for write cycles.

Bit 6

0 = Normal

1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.

Bit 5

0 = Normal

1 = Improve text mode performance

Bits 4:3

CPU Read RDY Release Controls 1,0. These two bits set the CPU RDY timing to be optimized for different system timing. For slower systems, the RDY line may be released earlier because it takes longer for the read cycle to be completed.

BITS		FUNCTION
4	3	
0	0	Power-on reset condition. RDY is inserted at the end of a CPU memory cycle. Use this setting for Local Bus mode operation.
0	1	RDY is inserted 1MCK before the end of a CPU memory cycle. Use this setting in ISA Bus mode for 10 MHz and slower systems
1	0	RDY is inserted 2MCK before the end of a CPU memory cycle.
1	1	RDY is inserted 1MCK after the end of a CPU memory cycle. Use this setting in ISA Bus mode for 12 MHz and faster systems

Bit 2

1 =Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.

0 = Write buffer disabled

Bit 1

If this bit and bit 0 are both set to 1, then the Attribute Controller (3C0/3C1) is configured for 16-bit access. The index is at 3C0, while the data is at 3C1, and the address toggle is disabled for 16-bit reads or writes. The address toggle functions in the standard way for 8-bit cycles. IOCS16 is asserted for all cycles to 3C0h or 3C1h.

Normally, this bit is set to 1.

Bit 0

1 = Enables 16-bit access to the CRTC (3?4/3?5), Sequencer (3C4/3C5), and Graphics Controller (3CE/3CF). The output IOCS16 is active for any I/O read or write to these addresses.

0 = The VGA I/O is all 8-bit.

14.7 PR32 - MISCELLANEOUS CONTROL 4

Read/Write Port = 3C5h, Index 12h
(Reset State = 00h)

This register provides control for several different features. Some of these features help to support Genlock of the WD90C24A/A2 to another display controller for overlay.

BIT	FUNCTION
7	Reserved
6	Disable Cursor Blink
5	FPUSR1 Function Select
4	FPUSR1 Control
3	FPUSR0 Function Select
2	FPUSR0 Control
1	Allow readback in backward compatible modes
0	Force standard CPU addressing in 132-column mode

Bit 7

Reserved

Bit 6

1 = The text cursor blink is disabled, and the cursor remains on. This option can be used if cursor blink is not desired.

0 = Blink is enabled.

Bit 5

0 = Causes the FPUSR1 output to echo the state of bit 4.

1 = The FPUSR1 output is selected by PR35A bits 5, 4, 3. See PR35A description.

Bit 4

Controls the FPUSR1 output when selected by bit 5.

Bit 3

0 = Causes the FPUSR0 output to echo the state of bit 2.

1 =The FPUSR0 output is selected by PR35A bits 2,1,0. See PR35A and PR73 descriptions.

Bit 2

Controls the FPUSR0 output when selected by bit 3.

Bit 1

1 = This bit allows reading the registers that are not readable in backward compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

1 = The special CPU address mapping for page mode font address in 132-column text is set for standard mapping without disturbing the display. This is used only for special virtual VGA applications.

14.8 PR33A - DRAM TIMING AND ZERO WAIT STATE CONTROL REGISTER.

Read/Write Port = 3C5h, Index 13h

BITS	FUNCTION
7:6	Zero Wait State Output Pin
5	Reserved
4:3	$\overline{CAS}$ Timing
2	Select $\overline{CAS}$ Cycle Start
1:0	$\overline{RAS}$ Precharge

Bits 7:6

These two bits control the operation of the $\overline{ZWST}$ output pin.

CAUTION

Do not set bits 7:6 to 00. Setting these bits to 00 may cause the system to hang and result in the loss of data.

BITS		FUNCTION
7	6	
0	0	Reserved, Do Not Use
0	1	$\overline{ZWST}$ = 0 if the internal write buffer is ready AND the memory address is decoded
1	0	$\overline{ZWST}$ = 0 if the internal write buffer is ready AND the memory address is decoded AND $\overline{MWR}$ = 0
1	1	$\overline{ZWST}$ = 0 if condition 1 0 is true OR an I/O write to WD90C24A/A2 is occurring

Bit 5

Reserved

Bits 4:3

These two bits control the $\overline{CAS}$ timing.

BITS		FUNCTION
4	3	
0	0	$\overline{CAS}$ cycle is 2 MCLK cycles. $\overline{CAS}$ low is 1 MCLK cycle + d. $\overline{CAS}$ high is 1 MCLK cycle - d.
0	1	$\overline{CAS}$ cycle is 2 MCLK cycles. $\overline{CAS}$ low is 1 MCLK cycle + 2d. $\overline{CAS}$ high is 1 MCLK cycle - 2d.
1	0	$\overline{CAS}$ cycle is 2 MCLK cycles. $\overline{CAS}$ low is 1.5 MCLK cycles. $\overline{CAS}$ high is 0.5 MCLK cycles.
1	1	Reserved.
Refer to the following note.		

NOTE

The time d = 5 to 10 ns for 3.3V VDD operation.

Bit 2

Select $\overline{CAS}$ Cycle Start

BIT 2	FUNCTION
0	$\overline{CAS}$ cycle starts 2.5 MCLK cycles after $\overline{RAS}$ low.
1	$\overline{CAS}$ cycle starts 1.5 MCLK cycles after $\overline{RAS}$ low.

Bits 1:0

These two bits control $\overline{RAS}$ precharge.

BITS		FUNCTION
1	0	
0	0	$\overline{RAS}$ high is 2.5 MCLK cycles + d wide.
0	1	$\overline{RAS}$ high is 3 MCLK cycles wide.
1	0	$\overline{RAS}$ high is 2 MCLK cycles wide.
1	1	$\overline{RAS}$ high is 2.5 MCLK cycles wide.
Refer to previous note.		

Refer to DRAM timing adjustments in Section 30.

14.9 PR34A - DISPLAY MEMORY MAPPING REGISTER

Read/Write Port = 3C5h, Index 14h

BITS	FUNCTION
7:4	Reserved
3:0	Display Memory Mapping

Bits 7:4

Reserved

Bits 3:0

Display Memory Mapping

The contents of these four bits are compared with the CPU address SLA[23:20] as part of the display memory address decoding. This allows the VGA to be mapped into any 1M CPU memory space. This register does not affect the $\overline{EBROM}$ decoding. $\overline{EBROM}$ can still decode at SLA[23:20] = 0h. When used with proper setting on PR1 bits 5:4, this register supports virtual VGA applications. These four bits are set to 0 at power -on and system reset.

14.10 PR35A - FPUSR0, FPUSR1 OUTPUT SELECT REGISTER

Read/Write Port = 3C5h, Index 15h

This register selects the internal signals that can be observed through the FPUSR0 and FPUSR1 output pins. This feature is used for debug purposes, and may be useful for using internal signals to control external functions, PR32 bit 5 and 3 must be set to 1 for this register to have any effect.

BITS	FUNCTION
7:6	Reserved
5:3	FPUSR1 Function Select
2:0	FPUSR0 Function Select

Bits 7:6

Reserved

Bits 5:3

FPUSR1 Function Select

Refer to the following table.

BITS			FUNCTION
5	4	3	
0	0	0	FPUSR1 = 1 if WD90C24A/A2 is fetching a font from DRAM
0	0	1	FPUSR1 = 1 if WD90C24A/A2 is fetching graphics data from DRAM
0	1	0	FPUSR1 = 1 if the internal write buffer is ready
0	1	1	FPUSR1 = 1 if CPU write cycle is occurring
1	0	0	FPUSR1 = 0 if a CPU write cycle is not caused by write buffer
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Bits 2:0

FPUSR0 Function Select

Refer to the following table and PR73 description.

BITS			FUNCTION
2	1	0	
0	0	0	FPUSR0 = 1 if I/O address is decoded
0	0	1	FPUSR0 = 1 if WD90C24A/A2 is fetching character attribute from DRAM
0	1	0	FPUSR0 = 0 if the internal write buffer is not empty
0	1	1	FPUSR0 = 1 if CPU read cycle is occurring
1	0	0	FPUSR0 = 0 if a write buffer cycle is occurring
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

14.11 PR45 - VIDEO SIGNATURE ANALYZER CONTROL REGISTER

Read/Write Port = 3C5, Index 16h
Unlock: PR20 (3C5.06h) = 48h

Bit	Function
7:4	Reserved
3	Unlock Signature Read Registers
2	Test Pattern
1	Initialize
0	Start

Bits 7:4

Reserved

Should be set to 0000 on writes to PR45. Undefined on reads.

Bit 3

Unlock Signature Read Registers

Setting this bit to 1 enables reading of PR45A and PR45B. The setting of this bit is readable.

Bit 2

Test Pattern

Setting this bit to 1 substitutes a fixed all zeros test pattern instead of the RAMDAC inputs into the signature analyzer. This all zeros test pattern is used, along with the capability of initializing the signature to 0001, to test the signature analyzer circuit. Setting of this bit is readable.

Bit 1

Initialize

Setting this bit to a 0 causes an initialization of the signature analyzer by preloading the signature to 0001h. This bit must be set to 1 before a video signature can be generated. The setting of this bit is readable.

Bit 0

Start

Setting this bit to a 1 causes the signature analyzer to generate a signature of a video frame.

This bit must be set to 0 and then back to 1 to restart generation of a new signature. The setting of this bit is readable.

14.11.1 PR45A - Signature Analyzer Data I

Read/Write Port = 3C5, Index 17h
Unlock: PR20 (3C5.06h) = 48h, PR45 Bit 3 = 1.
Value after Reset: 01h.

BITS	FUNCTION
7:0	Low Data Byte

14.11.2 PR45B - Signature Analyzer Data II

Read/Write Port = 3C5, Index 18h
Unlock: PR20 (3C5.06h) = 48h, PR45 bit 3 = 1.
Value after Reset: 00h.

BITS	FUNCTION
7:0	High Data Byte

14.12 PR57 - FEATURE REGISTER I

Read/Write Port = 3C5h, Index 19h.

BITS	FUNCTION
7	Reserved
6	Selects Source for DRAM refresh timing ($\overline{\text{REFLCL}}$) Input
5	Enable Self-Refresh (Write Only)
4:3	TFT Dithering Mode Select
2	Panel Power Control
1	Selects Source DRAM refresh timing ($\overline{\text{REFRESH}}$ or CKIN) input
0	Bank B Enable

Bit 7

Reserved

Should be set to 0.

DRAM Refresh Timing for ISA and Local Bus Modes During Power-down

PR57 bits 6, 5, and 1 control DRAM refresh timing functions for ISA and Local Bus modes during power-down. When bit 5 is set to 1, self-refresh is selected in either the Local or ISA bus mode, and bits 6 and 1 are not used (don't care). If bit 5 is set to 0, the DRAM refresh timing is selected by bits 6 and 1 (refer to the following table). The bit descriptions provide addition information.

BUS MODE	PR57 (BIT) 6	5	1	POWER-DOWN REFRESH TYPE
LOCAL BUS	X	1	X	Selects Self-refresh
	1	0	X	Selects $\overline{\text{REFLCL}}$ input
	0	0	1	Selects CKIN via PR71
ISA BUS	X	1	X	Selects Self-refresh
	0	0	0	Selects $\overline{\text{REFRESH}}$ input.
	0	0	1	Selects CKIN via PR71

Bits 6

Selects Source for DRAM Refresh Timing ($\overline{\text{REFLCL}}$) Input.

Bit 6 is used with bits 5 and 1 to select the source of DRAM refresh timing during power-down mode operation.

0 = Disable $\overline{\text{REFLCL}}$ as refresh source.

1 = $\overline{\text{REFLCL}}$ input (Pin 171) provides refresh clock source (typically 32 KHz). This setting overrides the settings of PR57 bit 1 and PR71.

NOTES

1. $\overline{\text{REFLCL}}$ is used in Local Bus Mode only.
2. Do not use the $\overline{\text{REFLCL}}$ input in Deep Sleep power-down mode.

Bit 5

Enable Self-Refresh (Write Only Bit)

Bit 5 is used with bits 6 and 1 to select the source of DRAM refresh timing during power-down mode operation.

This bit enables self-refresh operation when entering power-down mode. Refer to *AC Timing Characteristics* in Section 30.

0 = Disable self-refresh (refer to previous table).

1 = Enable self-refresh

Bits 4:3

TFT Dithering Mode Select

These bits are used with PR59 bit 4 and PR66 bits 2 and 6 to select the mode of operation and colors for the TFT dithering engine. Selection of modes depends upon the TFT interface (9, 12, or 18-bit) as listed in Tables 14-1 through 14-3.

PR57		PR66		
BIT 4	BIT 3	BIT 2	BIT 6	MODE
0	0	0	0	2-Frame Dithering, 27K Colors (Default)
0	0	1	0	2-Frame Dithering, 180K Colors
0	1	0	0	Invalid Setup
0	1	1	0	2 and 3 Frame Dithering, 256K Colors
1	0	0	0	No Dithering, 512 Colors
1	0	1	0	No Dithering, 512 Colors
1	1	0	0	Space Dithering, 27K Colors
1	1	1	0	Invalid Setup
NOTE: PR59 bit 4 must be set to 0 for all modes.				

TABLE 14-1. MODES FOR 9-BIT TFT

PR57		PR66		
BIT 4	BIT 3	BIT 2	BIT 6	MODE
0	0	X	1	2-Frame Dithering, 226K Colors (Default)
0	1	X	1	2-Frame Dithering, 226K Colors
1	0	X	1	No Dithering, 4K Colors
1	1	X	1	Space Dithering, 226K Colors
NOTE: PR59 bit 4 must be set to 0 for all modes.				

TABLE 14-2. MODES FOR 12-BIT TFT

PR57		PR66		
BIT 4	BIT 3	BIT 2	BIT 6	MODE
0	0	X	X	Invalid Setup
0	1	X	X	Invalid Setup
1	0	X	X	No Dithering, 256K Colors (Setup Only)
1	1	X	X	Invalid Setup
NOTE: PR59 bit 4 must be set to 1 for all modes.				

TABLE 14-3. MODES FOR 18-BIT TFT

Bit 2

Panel Power Control

0 = PNLOFF goes high and power to the panel is turned off. (default)

1 = PNLOFF goes low and power to the panel is turned on.

Refer to Section 26.11 for a description of panel power sequencing.

Bit 1

Selects Source for DRAM refresh Timing

Bit 1 is used with bits 6 and 5 to select the source of DRAM refresh timing during power-down mode operation (refer to the table preceding bit 6).

NOTE

$\overline{\text{REFRESH}}$ is used in ISA Bus Mode only.

0 = $\overline{\text{REFRESH}}$ pin input (pin 166)

1 = CKIN controlled by PR71

Bit 0

Bank B Enable

When this bit is set to 1, memory accesses and refresh operations to Bank B display memory are enabled. Bank B operation occurs as determined by the setting of bit 1 of this register.

When this bit is set to 0 all accesses and refresh operations to Bank B are halted. The Bank B address and control lines are static and the control lines at inactive levels. Bank B data lines are tristated, being pulled high or low by their power-on configuration pullup or pulldown resistors.

This bit is set to 1 at reset (default).

14.13 PR58 - FEATURE REGISTER II

Read/Write Port = 3C5h, Index 20h
Unlock: PR20 (3C5.06h) = 48h

BITS	FUNCTION
7:1	Reserved
0	Scratch Pad Bit

Bits 7:1

Reserved

Bit 0

Scratch Pad Bit

14.14 PR58A - MEMORY MAP TO I/O REGISTER FOR BLT ACCESS IN LOCAL BUS

Read/Write Port = 3C5h, Index 26h.

BITS	FUNCTION
7:5	Reserved
4	High Color Shift Control
3:2	Select High Color Modes (TRCLR[1:0])
1	Enable Mapping of Display Memory Addresses to I/O Port 23C4h
0	Enable Mapping of Display Memory Addresses to I/O Ports 23C0h through 23C5h

Bits 7:5

Reserved

Bit 4

High Color Shift Control

Used to control how data is shifted out of the video FIFO during high color mode operation.

0 = Normal data shift
1 = Data is shifted 16-bits at a time

Bits 3:2

Select True Color Modes (TRCLR[1:0])

True color mode uses 16 bits per pixel and is partitioned into red, green, and blue bits (with red at the MSB and blue at the LSB). For example, 6-5-5 would have 6 red bits, 5 green bits, and 5 blue bits.

BITS		FUNCTION
3	2	
0	0	Standard Color Palette Mode
0	1	5-6-5 64K True Color Mode
1	0	6-5-5 64K True Color Mode
1	1	5-5-5 32K True Color Mode

Bit 1

Enable Mapping of Display Memory Addresses to I/O Port 23C4h.

This bit works with the following bit 0 to enable I/O port mapping. The enabled I/O ports are selected by address bits SA2 through SA0.

Bit 0

Enable Mapping of Display Memory Addresses to I/O Ports 23C0h through 23C5h.

This bit works with the preceding bit 1 to enable I/O port mapping as follows:

BITS		FUNCTION
1	0	
0	0	No Memory Map to I/O Ports
0	1	Enable Memory Mapping to I/O Ports 23C0h through 23C5h
1	0	Reserved
1	1	Enable Memory Mapping to I/O Port 23C4h only

Address bits SA2 through SA0 are use to decode the selected I/O port as follows:

ADDRESS BITS			I/O PORT SELECTED
SA2	SA1	SA0	
0	0	0	23C0h
0	0	1	23C1h
0	1	0	23C2h
0	1	1	23C3h
1	0	0	23C4h
1	0	1	23C5h

To enhance the WD90C24A/A2 hardware BITBLT operations, I/O ports 23C0h through 23C7h can be mapped to system memory addresses for PR58A bits 1:0 = 01 and 11.

For bits 1:0 = 01, SA2:SA0 are mapped to ports 23C0h:23C5h.

For bits 1:0 = 11, SA2:SA0 = 100 or 101 for 23C4h and 23C5h are recognized, 23C0h:23C3h are ignored.

PR58A		MEMORY ADDRESS	I/O PORT
BIT 1	BIT 0		
0	1	A0000h	23C0h
0	1	A0002h	23C2h
0	1	A0004h	23C4h
0	1	A0008h	23C0h
⇓	⇓	⇓	⇓
0	1	AFFFCh	23C4h
1	1	A0000h	23C4h
1	1	A0002h	23C4h
1	1	A0004h	23C4h
1	1	A0008h	23C4h
⇓	⇓	⇓	⇓
1	1	AFFFEh	23C4h

This feature permits the use of fast string move instructions rather than the relatively slower I/O instructions for BITBLT.

14.15 PR59 - MEMORY ARBITRATION CYCLE SETUP REGISTER

This register works with PR57 to select the mode of operation and colors for the TFT dithering engine. It is also used to setup the total length of the frame buffer memory fixed arbitration cycle, as a method of adjusting arbitration cycle length to the speed of the memory and speed of the CRT and Flat Panel Displays.

Read/Write Port = 3C5h, Index 21h
Unlock: PR20 (3C5.06h) = 48h.

BITS	FUNCTION
7:6	Reserved
5	ENDATA Polarity
4	TFT Panel Interface Select
3	Mode 13 Space Dithering (Space Dithering is supported in Mode 13 Only)
2:0	Arbitration Cycle Select

Bits 7:6

Reserved

Bit 5

Selects ENDATA polarity as follows:

BIT 5	FUNCTION
0	ENDATA Active High (Default)
1	ENDATA Active Low

Bit 4

TFT Panel Interface Select

This bit works with PR18, bit 2 to provide color TFT enhancement as follows:

BIT 4	FUNCTION
0	Selects 9-Bit or 12-Bit TFT
1	Selects 18-Bit TFT

Bit 3

In color and monochrome STN LCD modes, the WD90C24A/A2 provides space dithering to enhance the low resolution mode (Mode 13).

Space dithering is selectable as follows:

BIT 3	FUNCTION
0	Disable space dithering in Mode 13
1	Enable space dithering in Mode 13 (Default)

Bits 2:0

Setting these bits adjusts the arbitration cycle length in increments of 160 ns. The default arbitration cycle at reset is the 101b setting, or 800 ns. Cycle increments are based on a VCLK rate of 25 MHz and should be scaled accordingly for differing VCLK values.

14.16 PR62 - FR TIMING REGISTER

Read/Write Port = 3C5h, Index 24h

BITS	FUNCTION
7:0	Programmable FR 8-Bit Divisor

For color flat panels, this register controls the period of the Frame Rate (FR) signal in relation to the refresh rate. For monochrome flat panels, the FR rate is fixed at 480 line intervals.

The FR signal appears at the FR/$\overline{\text{BLANK}}$ pin anytime that PR19 bit 4 is set to 1.

The default rate of the FR signal is once every 240 lines because PR62 defaults to 3Ch.

The rate of the FR signal may be adjusted faster or slower in increments of 4 lines.

The FR pulse rate is generated at a line count rate of 4 times the value stored in PR62.

For an FR pulse rate of once every 480 lines, set PR62 to 120d (78h)

The FR pulse is 50% duty cycle.

PR62 should not be set to 00h because this setting is reserved for test purposes.

14.17 PR63 - READ/WRITE FRAME BUFFER CONTROL REGISTER

Read/Write Port = 3C5h, Index 25h.

BITS	FUNCTION
7:2	Read/Write Frame Buffer Control
1	Control Read Frame Buffer Arbitration in Single Simultaneous Display Mode
0	Control Write Frame Buffer Arbitration in Single Simultaneous Display Mode

Bits 7:2

This 6-bit counter value determines the time that the frame buffer can be accessed as measured in MCLKs.

Bit 1

Controls read operations from the frame buffer.

0 = Disables reads
1 = Enable reads

Bit 0

Controls write operations from the frame buffer.

0 = Disables writes
1 = Enable writes

14.18 PR64 - CRT LOCK CONTROL II

Read/Write Port = 3C5h, Index 27h

BITS	FUNCTION
7	Reserved
6	Unlock the Vertical Display End CRT register
5	Reserved
4	Unlock the Horizontal Display End CRT register
3:2	Reserved
1:0	Enhanced Vertical Expansion Selection for Text mode.

Bits 7, 5

Reserved

Bits 6

Set bit 6 to 0 (default) to unlock the VDE (3?5h, Index 12h) register and Overflow (3?5h, Index 07h) bits 6 and 1.

Bits 4

Set bit 4 to 0 (default) to unlock the HDE (3?5h, Index 01h) register.

Bits 3:2

Reserved

Bits 1:0

PR64 bits 1:0 are functional in 400 line text modes only. When functional, these bits work with PR19 bits 3:2 to select vertical expansion.

BIT 1	BIT 0	Vertical Expansion Selected
X	0	No enhanced expansion selected.
0	1	Three lines repeated below character.
1	1	One line repeated above character, and two lines repeated below character.

14.19 PR65 - RESERVED FOR FUTURE NEED

Read/Write Port = 3C5h, Index 28h

BITS	FUNCTION
7:0	Reserved for future need

14.20 PR66 - FEATURE REGISTER III

Read/Write Port = 3C5h, Index 29h

BITS	FUNCTION
7	Enable Auxiliary Video Extender (AVE) Mode
6	TFT Dithering Mode Select
5	Force LP and FP to be the same as HSYNC and VSYNC, respectively
4	Disable PCLK, $\overline{\text{BLANK}}$, VID[7:0]
3	Disable VSYNC, HSYNC
2	TFT Dithering Mode Select
1:0	Reserved, set to 0

Bit 7

Enable Auxiliary Video Extender (AVE) Mode

The AVE mode allows the internal RAMDAC to be used by an external source. The PCLK, $\overline{\text{BLANK}}$, and VD[7:0] pins become inputs to give direct access to the RAMDAC.

0 = AVE not enabled
1 = AVE enabled

Bits 6

TFT Dithering Mode Select

This bit is used with bit 2 of this register, with PR57 bits 4:3, and with PR59 bit 4 to select the TFT Dithering mode. Refer to the description for PR57.

Bits 5

Force LP and FP to be the same as HSYNC and VSYNC, respectively.

0 = LP and FP normal
1 = LP is the same as HSYNC and FP is the same as VSYNC

Bits 4

Disable PCLK, $\overline{\text{BLANK}}$, VID[7:0]

0 = normal operation.
1 = PCLK forced to inactive low. $\overline{\text{BLANK}}$, VID[7:0] forced inactive low only in CRT-only mode.

Bits 3

Disable VSYNC, HSYNC

0 = normal operation.
1 = VSYNC, HSYNC forced to inactive low.

Bit 2

TFT Dithering Mode Select

This bit is used with bit 6 of this register, with PR57 bits 4:3, and with PR59 bit 4 to select the TFT Dithering mode. Refer to the description for PR57.

Bits 1:0

Reserved, must be set to 0.

14.21 PR68 - PROGAMMABLE CLOCK SELECTION REGISTER

Read/Write Port = 3C5h, Index 31h
Unlock: PR72 (3C5.35h) = 5xh

BITS	FUNCTION
7:5	Reserved
4:3	Video Dot Clock Select
2:0	Display Memory Clock Select

Bits 7:5

Reserved.

Bits 4:3

Video Dot Clock Select

Bits 4:3 are used with register 3C2h, bits 3:2 to select the VCLK frequency in internal PCLK mode. Refer to the description of the Embedded Clock Generator in Section 22.

Bits 2:0

Display Memory Clock Select]

Enables MSEL[2:0] of the internal clock. Refer to the description of the Embedded Clock Generator in Section 22.

14.22 PR69 - PROGAMMABLE VCLK FREQUENCY REGISTER

Read/Write Port = 3C5h, Index 32h.

BITS	FUNCTION
7:0	N-Value of user programmable VCLK frequency.

Bit 7

N-Value

Holds the N-value that defines the VCLK frequency and is enabled when VSEL[3:0] = 0010. For additional information, refer to the description of the *Embedded Clock Generator* in Section 22.

NOTE

The N-Value must be between 38h and BEh for proper clock operation.

14.23 PR70 - MIXED VOLTAGE OVERRIDE REGISTER

Read/Write Port = 3C5h, Index 33h.

BITS	FUNCTION
7:6	Reserved
5	Override Internal Voltage Detectors
4:0	Force Voltage Mode

Bits 7:6

Reserved

Bit 5

Override Internal Voltage Detectors

When set to 1, this bit enables bits 4:0 to override all five internal voltage detectors.

Bits 4:0

Force Voltage Mode

Independently sets five voltage mode latches for 3.3V or 5V. The detector output latches set by bits 4:0 are PVDD, BVDD, FPVDD, MVDD, and AVDD2, respectively.

Any bit set to 1 forces the voltage mode to 3.3 V operation.

14.24 PR71 - PROGRAMMABLE REFRESH TIMING REGISTER

Read/Write Port = 3C5h, Index 34h.

BITS	FUNCTION
7:0	Divide CKIN for Refresh

Bit 7:0

Divide CKIN for Refresh

Holds the value minus 1 (n-1)of the upper 8 bits of the 11-bit divisor, which is used to divide CKIN and generate a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. This register is enabled by setting PR57 bit 1 to 1. The width of the refresh cycle is the CKIN period multiplied by 8. If bit 0 is set to 0, the CKIN signal (32 KHz) is passed through to the refresh cycle.

For example:

1. If PR71 bit 0 = 1,
   then refresh rate = CKIN/(8*(PR71+1))
2. If PR71 bit 0 = 0,
   then refresh rate = CKIN

14.25 PR72 - PROGRAMMABLE CLOCK UNLOCK

Read/Write Port = 3C5h, Index 35h.

BITS	FUNCTION
7	Reserved
6:4	Unlock Programmable Clock Selection Register
3:0	Reserved

Bit 7

Reserved

Bits 6:4

Unlock Programmable Clock Selection Register

Set bits 6:4 to 101, respectively to unlock PR68; the Programmable Clock Selection register. For ISO Monitor support, this is used as an ISO register lock of PR68 register.

Bits 3:0

Reserved

14.26 PR73 - VGA STATUS DETECT

Read/Write Port = 3C5h, Index 36h.

BITS	FUNCTION
7	Enable/Disable Status Detect on FPUSR0
6:5	I/O and Memory Detect on FPUSR0
4	Select FPUSR0 Status Signal Polarity
3	Reserved
2:0	Read AVDD2, FPVDD, and PVDD Voltage Selection, Respectively

Bit 7

Enable/Disable Status Detect on FPUSR0

0 = Disable Status Detect
1 = Enable Status Detect

Bits 6:5

I/O and Memory Detect on FPUSR0

These bits select how the FPUSR0 output pin (167) is controlled.

BITS		SELECT FPUSR0 OUTPUT FUNCTION
6	5	
0	0	Reserved
0	1	I/O Detection
1	0	Memory Detection
1	1	Both I/O and Memory Detection

Bit 4

Select FPUSR0 Status Signal Polarity

0 = Status Signal from FPUSR0 is active high.
1 = Status Signal from FPUSR0 is active Low.

Bit 3

Reserved.

Bits 2:0

Read AVDD2, FPVDD, and PVDD Voltage Selection, Respectively

These are read-only bits that indicate the output of the voltage detector circuits as follows:

0 = AVDD2, FPVDD, or PVDD Voltage is set to 5 VDC.
1 = AVDD2, FPVDD, or PVDD Voltage is set to 3.3 VDC.

15.0 FLAT PANEL PARADISE REGISTERS

This section contains complete descriptions of all Flat Panel Paradise registers. Refer to Section 6 for a summary of all registers.

NOTE

Combinations of bits from Paradise registers PR18, PR19, PR1A, and PR39 are used to select the display type and operation. Table 15-1 provides a summary of the selections.

15.1 PR18 - FLAT PANEL STATUS REGISTER

Read/Write Port = 3?5h, Index 31h

BITS	FUNCTION
7	Select Internal/External RAMDAC Mode
6	Enable Free Running Clock for EL, Plasma, or TFT Panel
5	Enable 256K Colors for STN Dithering
4	Enable Reverse Video in Flat Panel Mode
3	Enable/Disable Monochrome TFT Interface
2	Enable/Disable Color TFT Interface
1:0	LCD Panel Select
NOTE: Bits 1:0 are used to select display type and operation. Refer to Table 15-1.	

Bit 7

Select Internal/External RAMDAC Mode

This bit is used to shut off the internal RAMDAC outputs. Usually, the RAMDAC is shut off whenever PR19 bit 5 is low. If an external RAMDAC is used, setting this bit keeps the internal RAMDAC disabled even when PR19 bit 5 is high.

0 = Internal RAMDAC mode is selected (default)
1 = External RAMDAC mode is selected (the internal RAMDAC is disabled).

Bit 6

Enable Free Running Clock for 4-bit Plasma, EL panel.

0 = Disable free running.
1 = Enable free running.

Bit 5

Enable 256K Colors for STN Dithering

This bit is used to select color palette size for color STN multiplexed panel support. Set this bit to 0 for a 4K color dithering palette only if the smaller dithering palette improves the appearance of the display.

0 = Select 4K color palette dithering (Usual setting)
1 = Select 256K color palette dithering

Bit 4

Enable Reverse Video in Flat Panel Mode.

This bit is used with PR39, bit 3 to reverse the polarity of video output data VUD(3:0) and VLD (3:0) in flat panel mode. For best viewing of a flat panel display, it is often desirable to have the panel display text in reverse video. The the setting of PR18 bit 4, along with PR39 bit 3, allow selection of conditions for text and graphics displays in reverse image on a panel as shown in the following table.

Normally, both bits are set to 1 for reverse image text and normal image graphics.

The settings of PR18 bit 4 and PR39 bit 3 do not affect CRT display.

PR18 BIT 4	PR39 BIT 3	PANEL DISPLAY POLARITY
0	0	Normal text and graphics
0	1	Reserved
1	0	Reverse image text and graphics
1	1	Reverse image text, and normal image graphics

NOTE

Reverse image settings are not recommended for color panels. PR18 bit 4 and PR39 bit 3 should both be set to 0 for color panel support.

Bit 3

Enable/Disable Monochrome TFT Interface

0 = Disable Monochrome TFT LCD panel interface (Default)
1 = Enable Monochrome TFT LCD panel interface.

Bit 2

Enable/Disable Color TFT Interface

This bit is not readable.

0 = Disable Color TFT LCD panel interface.
1 = Enable Color TFT LCD panel interface.

Bits 1:0

LCD Panel Select

These two bits are used with bit 3 to select different sets of parameters which are loaded into the CRT controller. The parameters should be locked after loading.

The panel type can be selected during power turn-on and system reset using the configuration registers CNF19 and CNF18 (refer to Section 24). PR18, bits 1 and 0 can override the Configuration bits CNF19 and CNF18, respectively

.

---	CNF19	CNF18	
PR18 BIT 3	PR18 BIT 1	PR18 BIT 0	PANEL TYPE
0	0	0	Dual Panel LCD Panel
0	0	1	Plasma/EL Panel
0	1	0	Reserved
0	1	1	Single Panel LCD Panel
1	0	1	Monochrome TFT Panel

CASE	DISPLAY MODE	CRT ENABLE	PANEL ENABLE	MONOCHROME OR COLOR	PANEL TYPE	STN INTERFACE	TFT INTERFACE	PLASMA INTERFACE	PANEL RESOLUTION	4-bit, 8-bit INTERFACE	
		PR19		PR39	PR18	PR1A	PR18/ PR59	PR19	PR1A	PR1A	PR83
		5	4	5	3,1,0	6,5	2/4	7	7,4	3	3
1	CRT	1	0	0	0,0,0	0,0	0/0	0	0,0		0
2	Panel-Mono-Dual-LCD-640	0	1	0	0,0,0	0,0	0/0	0	0,0	X	0
3	Panel-Mono-Single-LCD-640 4-Bit	0	1	0	0,1,1	0,0	0/0	0	0,0	1	0
4	Panel-Mono-Single-LCD-640 8-Bit	0	1	0	0,1,1	0,0	0/0	0	0,0	0	0
5	Panel-Color-Dual-STN 16-Bit-640	0	1	1	0,0,0	1,1	0/0	0	0,0	X	0
6	Panel-Color-Single-STN 16-Bit-640	0	1	1	0,1,1	1,1	0/0	0	0,0	X	0
7	Panel-Color-Single-STN 8-Bit-640	0	1	1	0,1,1	0,1	0/0	0	0,0	X	0
8	Panel-Color-Single-TFT 18-Bit-640	0	1	1	0,1,1	0,0	1/1	0	0,0	X	0
9	Panel-Color-Single-TFT 9 or 12-Bit-800	0	1	1	0,1,1	0,0	1/1	0	1,1	X	0
10	Panel-Color-Single-TFT 18-Bit-1024	0	1	1	0,1,1	0,0	1/1	0	1,0	X	0
11	Panel-Color-Single-TFT 9 or 12-Bit-640	0	1	1	0,1,1	0,0	1/0	0	0,0	X	0
12	Panel-Color-Single-TFT 9 or12-Bit-1024	0	1	1	0,1,1	0,0	1/0	0	1,0	X	0
13	Panel-Mono-Plasma-2 Pixel	0	1	0	0,0,1	0,0	0/0	0	0,0	X	0
14	Panel-Mono-Plasma-1 Pixel	0	1	0	0,0,1	0,0	0/0	0	0,0	X	0
15	Panel-Mono-EL	0	1	0	0,0,1	0,0	0/0	0	0,0	X	0
16	Panel-Mono-TFT 8-bits/2 pixels 680	0	1	0	1,0,1	0,0	1/0	0	0,0	X	0
17	Panel-Color-TFT18-bits, 9-bits per pixel 680	0	1	0	0,1,1	0,0	1/0	0	0,0	X	0
18	CRT & Panel-Mono-Dual-LCD 640	1	1	0	0,0,0	0,0	0/0	0	0,0	X	0
19	CRT & Panel-Mono-Single-LCD 640 4-Bit	1	1	0	0,1,1	0,0	0/0	0	0,0	1	0
20	CRT & Panel-Mono-Single-LCD 640 8-Bit	1	1	0	0,1,1	0,0	0/0	0	0,0	0	0
21	CRT & Panel-Color-Dual-STN 640 16-Bit	1	1	1	0,0,0	1,1	0/0	0	0,0	X	0
22	CRT & Panel-Color-Single-STN 64016-Bit	1	1	1	0,1,1	1,1	0/0	0	0,0	X	0
23	CRT & Panel-Color-Single-STN 640 8-Bit	1	1	1	0,1,1	0,1	0/0	0	0,0	X	0
24	CRT & Panel-Color-Single-TFT 640 18-Bit	1	1	1	0,1,1	0,0	1/1	0	0,0	X	0
25	CRT & Panel-Color-Single-TFT800 9 or 12-Bit	1	1	1	0,1,1	0,0	1/1	0	1,1	X	0
26	CRT & Panel-Color-Single-TFT 1024 18-Bit	1	1	1	0,1,1	0,0	1/1	0	1,0	X	0
27	CRT & Panel-Color-Single-TFT 640 9 or 12-Bit	1	1	1	0,1,1	0,0	1/0	0	0,0	X	0
28	CRT & Panel-Color-Single-TFT 1024 9 or 12-Bit	1	1	1	0,1,1	0,0	1/0	0	1,0	X	0
29	CRT & Panel-Mono-TFT 8-bits/2 pixels 680	1	1	0	1,0,1	0,0	1/0	0	0,0	X	0
30	CRT & Panel-Color TFT 18-bit 9-bits per pixel 680	1	1	0	0,1,1	0,0	1/0	0	0,0	X	1

TABLE 15-1. DISPLAY TYPE AND OPERATION SELECTION SUMMARY

15.2 PR19 - FLAT PANEL CONTROL I REGISTER

Read/Write Port = 3?5h, Index 32h

BITS	FUNCTION
7	Plasma Panel Interface and HSYNC Timing Select
6	Frame Pulse (FP) Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Auto-Centering/Vertical Expansion Select
2	Enable Auto Centering and Vertical Expansion
1:0	HSYNC Delay Adjustment
NOTE: Bit 7 is used to select display type and operation. Refer to Table 15-1.	

Bit 7

Plasma Panel Interface

This bit is used to select either of two plasma panels, and also selects the range of delay for HSYNC by setting bits 1:0.

0 = Select 4 data bits/1 pixel interface.
1 = Select 8 data bits/2 pixel interface (4 bits/pixel).

Bit 6

Frame Pulse (FP) Timing Select.

This bit is used to select two different frame pulse (FP) timings for different LCD panels.

0 = Select ON time during first horizontal line.
1 = Select ON time during second horizontal line.

Bit 5

CRT Display Enable.

This bit enables the CRT display.

0 = Disable CRT
1 = Enable CRT (default)

When the CRT is the only display selected, outputs VLD0 through VLD3 and VUD0 through VUD3 are active and can be used to drive the P7:P0 bus for an external RAMDAC.

Bit 4

Flat Panel Display Enable.

This bit selects the flat panel as the main display.

0 = Disable Flat Panel display (default).
1 = Enable Flat Panel display.

Bit 3

Screen Auto Centering/Vertical Expansion Select.

0 = Auto-centering (default).
1 = Vertical Expansion.

Bit 2

Enable Auto-Centering and Vertical Expansion.

0 = Disable (default).
1 = Enable.

Bits 1:0

HSYNC Delay Adjustment

Bits 1 and 0 are used with bit 7 to program a delay of HSYNC in one VCLK (one dot) increments. This delay is used to horizontally adjust the position of the picture displayed on flat panels. This HSYNC timing adjustment does not affect the delay of HSYNC signal to panels

PR19			Number of VCLK Delay of Hsync
BIT 7	BIT 1	BIT 0	
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

15.3 PR1A - FLAT PANEL CONTROL II REGISTER

Read/Write Port = 3?5h, Index 33h.

BITS	FUNCTION
7	Panel Resolution Select
6:5	STN Panel Select
4	Panel Resolution Select
3	Enable 4/8-Bit LCD
2	Shading Method Select
1	Select the Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit 7

Panel Resolution Select

This bit is used with bit 4 to select panel resolution as follows:

BITS		FUNCTION
7	4	
0	0	640 x 480 Panel Width
0	1	1280 x 1084 Panel Width (Reserved for future use.)
1	0	1024 x 768 Panel Width
1	1	800 x 600 Panel Width

Bits 6:5

STN Panel Select

Selects 8-bit and 16-bit STN type panels.

BITS		FUNCTION
6	5	
0	0	Not STN
0	1	8-Bit STN
1	1	16-Bit STN

Bit 4

Panel Resolution Select

Used with bit 7 to select panel width. Refer to the bit 7 description.

Bit 3

Enable 4/8-Bit LCD

0 = Enable 8-bit single LCD
1 = Enable 4-bit single LCD

Bit 2

Shading Method Select.

0 = Frame rate modulation (default).
1 = Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.

This bit is enabled by PR1A bit 0.

0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.

0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by bit 1.

15.4 PR1B - FLAT PANEL UNLOCK REGISTER

Write Only Port 3?5, Index 34h

BITS	FUNCTION
7:0	Flat Panel Unlock

This register is used to protect PR18, PR19, PR1A, PR36 through PR41, and PR44 from being read from or written to. In order to access PR18, PR19, and PR1A, PR1B must be loaded first with 101XXXXX. PR18, PR19, and PR1A, as well as PR36 through PR41 remain unlocked until another value is written to PR1B. PR1B is also used to lock all Shadow registers. To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

15.5 PR30 - MAPPING RAM UNLOCK REGISTER

Read/Write Port = 3?5H, Index 35h

BITS	FUNCTION
7:0	Mapping RAM Unlock

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with 30h. The mapping RAM registers remain unlocked until another value is written to the PR30 register.

15.6 PR33 - MAPPING RAM ADDRESS COUNTER REGISTER

Read/Write Port = 3?5h, Index 38h

BITS	FUNCTION
7:0	Mapping RAM Address Counter

This register can be accessed only in 8-bit I/O mode. It is used to select the Mapping RAM Address Counter register location. Refer to register PR34.

NOTE

Any I/O Read or Write to the I/O port 3?5.39h (Mapping RAM Data register) increments the Mapping RAM Address Counter by one.

15.7 PR34 - MAPPING RAM DATA REGISTER

Read/Write Port = 3?5h, Index 39h

BITS	FUNCTION
7:0	Mapping RAM Data

This register can be accessed only in 8-bit I/O mode. It is used to read data from or write data to the Mapping Ram location selected by setting register PR33.

15.8 PR35 - MAPPING RAM AND POWER-DOWN CONTROL REGISTER

Read/Write Port = 3?5h, Index 3Ah

BIT	FUNCTION
7	Select System Power-down Mode/Display Idle Mode
6	Select Internal Divided By 8 Clock to Control General Powerdown Mode
5	Host Release Control
4	Reserved
3	Mapping RAM Bypass
2	Reserved
1	Enable Weighting Equation
0	Reserved

Bit 7

Select System Power-down Mode/Display Idle Mode. Works with bit 6 of this register and register PR44, bit 7. Refer to the following table.

0 = Display Idle Mode (default).
1 = System Power-down mode; MCLK and VCLK turned off.

Bit 6

Select Internal Divided by 8 Clock to Control General Power-down Mode. This bit is active only when register PR44, bit 7 is set to 1.

0 = Disable internal clock divider
1 = Enable internal clock; clock is divided by 8

Bit 5

Host Release Control.

This bit will allow another VGA controller onto the I/O bus. When PR35(5) is set to 1 and $\overline{\text{PDOWN}}$ input is set to 0, the WD90C24A/A2 does not respond to any CPU memory or I/O accesses. All output buffers of the system interface are turned off (tristated). The default value of this bit after reset is 0.

Bit 4

Reserved

Bit 3

Mapping RAM Bypass

This bit is usually set to 0.

0 = Enables mapping RAM for programmable gray scale to gray shade mapping (default).
1 = Sets bypass mapping RAM for 1:1 gray scale to gray shade mapping for monochrome LCD panels only.

NOTE

Mapping RAM bypass can be set to 1 for LCD panels only.

Bit 2

Reserved

Bit 1

Enable Weighting Equation.

This bit is used to turn the following weighting equation (I= 0.3R + 0.59G = 0.11B) on and off in either color mode or monochrome mode.

0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved

15.9 PR36 - PANEL HEIGHT SELECT REGISTER

Read/Write Port = 3?5h, Index 3Bh

BITS	FUNCTION
7:0	Panel Height Select

This register is loaded with the height, less 1, of a single panel. This information is used to calculate auto-centering, vertical expansion, and related values.

- For a 640 by 480 dual panel display, this register should be loaded with EFh. (480/2)-1 = 239d = EFh.
- In a 640 by 400 dual panel display, the equation is: (400/2)-1 = 199d = C7h.

15.10 PR37 - FLAT PANEL BLINKING CONTROL

Read/Write Port = 3?5h, Index 3Ch

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

BITS	FUNCTION
7	LCD LP Signal Select
6	Shift-Clock Polarity Select
5:3	Character Blink-Rate Select
2:0	Cursor Blink-Rate Select

Bit 7

LCD LP Signal Select

Some panels require that the LP (Latch Pulse) signal be a constant free-running pulse while others require that LP stop at the last line at the bottom of the panel and start again at the first line on the top when the top line is refreshed. When this bit (PR37 bit 7) is set to 1, the LP signal on the WD90C24A/A2 panel interface free runs during retrace (blanking) intervals. This free run occurs from the last line pulse at the bottom to the first line pulse at the top of the panel.

BIT 7	FUNCTION
0	LP is disabled during vertical blanking period.
1	LP is generated continuously during vertical blanking period (XSCLK is turned off).

Bit 6

Shift Clock Polarity Select

NOTE

The shift clock polarity cannot be changed on plasma panels

Allows XSCLK polarity to be set so that it will make either a low-to-high or high-to-low transition at the time when panel data should be latched into the panel.

BIT 6	FUNCTION
0	Data changes with rising edge of XSCLK: data should be latched into panel by falling edge of XSCLK.
1	Data changes with falling edge of XSCLK: data should be latched into panel by rising edge of XSCLK.

Bits 5:3

Character Blink-Rate Select

Bits 5 through 3 select the character blink rate as given in the following list.

BITS			CHARACTER BLINK-RATE SELECT
5	4	3	
0	0	0	No character blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

Bits 2:0

Cursor Blink-Rate Select

Bits 2 through 0 select the cursor blink rate as given in the following list.

BITS			CURSOR BLINK-RATE SELECT
2	1	0	
0	0	0	No cursor blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

15.11 PR39 - COLOR LCD CONTROL REGISTER

Read/Write Port = 3?5h, Index 3Eh

This register is used to support color LCD panels.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Monochrome/Color Panel Select
4	Reserved
3	Enable Reverse Video
2	Enable CRT VSYNC and HSYNC
1	FP Polarity Select
0	LP Polarity Select

Bit 7

Enable Border LP Control

This bit is used to generate a special LP pulse to latch border information (black or white).

0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select

0 = Select black border.
1 = Select white border.

Bit 5

Monochrome/Color Panel Select

This bit is used to select monochrome or color LCD interface support (refer to Table 15-1). When set to 1, this bit selects color panel FP, LP, and FR timing, and selects color dithering.

0 = Monochrome LCD panel interface.
1 = Color LCD panel interface.

Bit 4

Reserved

Bit 3

Enable Reverse Video

This bit works with PR18 bit 4 refer to Section 15.1).

Bit 2

Enable CRT VSYNC and HSYNC.

PR39 BIT 2	VSYNC PIN 173	HSYNC PIN 174
0	Inactive High	Inactive High
1	CRT VSYNC	CRT HSYNC

At reset, PR39 bit 2 defaults to 0. Also, it may be set to 0 for power saving when CRT support is not needed.

Bit 1

FP Polarity Select

If PR39 (1)=0, then FP has normal polarity.
If PR39 (1)=1, then FP has reverse polarity.

Bit 0

LP Polarity Select

If PR39 (0)=0, then LP has normal polarity.
If PR39 (1)=1, then LP has reverse polarity.

15.12 PR41 - VERTICAL EXPANSION INITIAL VALUE REGISTER

Read/Write Port = 3?5h, Index 37h

BITS	FUNCTION
7:0	Vertical Expansion Initial Value

Bits 7:0

This register is used to decide which horizontal line is repeated in the very beginning when vertical expansion is enabled. It is very useful to implement smooth scrolling when 200, 350 or 400 line-modes are displayed on a 480-line panel.

15.13 PR44 - POWER-DOWN AND MEMORY REFRESH CONTROL REGISTER

Read/Write Port = 3?5h, Index 3Fh

This register controls two power saving features when in the general Powerdown modes. Bit 7 is used with PR35, bits 7:6 to select the Powerdown mode to be used (refer to Section 15.8). With some Powerdown modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. Bits 6:0 of this register are loaded with a value that modifies the display memory refresh period during Powerdown mode operations.

BITS	FUNCTION
7	General Powerdown Mode Enable
6:0	Memory Refresh Cycle Period

Bit 7

General Powerdown Mode Enable Bit (refer to Section 26).

This bit enables General Powerdown mode.

0 = Disables General Powerdown.
1 = Enables General Powerdown.

Bits 6:0 - Memory Refresh Cycle Period.

These bits are loaded with the value Z, which is used to determine the refresh period during General Powerdown mode operation (refer to Section 26.8).

16.0 COMPATIBILITY REGISTERS

This section contains complete descriptions of all Compatibility registers. Refer to Section 6 for a summary of all registers.

16.1 HERCULES/MDA MODE CONTROL REGISTER

Write Only Port = 3B8h

This register is accessible in Hercules and MDA modes with hardware emulation.

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BFh Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If bit 1 = 1 and Port 3BFh bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.

0 = Display memory page address starts at B000:0h.
1 = Display memory page address starts at B800:0h.

Bit 6

Reserved.

Bit 5

Enable Blink.

0 = Disable Blinking
1 = Enable Blinking

Bit 4

Reserved.

Bit 3

Video Enable.

0 = Video Disable
1 = Video activated

Bit 2

Reserved.

Bit 1

Port 3BFh enable.

0 = Prevents setting of Port 3BFh bit s 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode.

Should be 1.

0 = High resolution disabled.
1 = High resolution is enabled.

16.2 HERCULES MODE REGISTER

Write Only Port = 3BFh

BITS	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BFh. It affects the device operation only in the 6845 mode. The Hercules/MDA Mode Control register located at the address 3B8h overrides the write port 3BFh functions defined by its bits 0 and 1.

Bits 7:2

Reserved

No function is defined on writes to the Hercules Mode Register.

Bit 1

Upper Memory Page Address

Enable Mode Control Register (3B8h) bit 7 selects the displayed memory page address in graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B000:0h for the 32K Byte memory space.

0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics

Selects alpha or graphics mode. May be overridden by Hercules Enable Mode Register, bit 1.

0 = Alpha mode display.
1 = Graphics modes may be displayed.

16.3 COLOR CGA OPERATION REGISTER

Write Only Port = 3D8h

BITS	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W or Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bits 7:6

Reserved.

Bit 5

Enable Blink Function.

0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking

Bit 4

B/W Graphics Mode Enable.

0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.

0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Mode Select

0 = B/W Mode Enable.
1 = Color Mode Enable.

Bit 1

Text or Graphics Mode Selection.

0 = Alpha mode enable.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.

0 = 40 by 25 Alpha mode enabled.
1 = 80 by 25 Alpha mode activated.

16.4 CGA COLOR SELECT REGISTER

Write Only Port = 3D9h

BITS	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit s 7:6

Reserved.

Bit 5

Select 320 by 200 Color Set for the CGA at 2 bits per pixel.

0 = Background, Green, Red, Brown colors.
1 = Background, Cyan, Magenta, White colors.

Bit 4

Alternate Color Set Enable.

0 = Background color in Alpha mode.
1 = Enable alternate color set in Graphics mode.

Bit 3

Border Intensity.

Border color select in Text modes, and screen background color in 320 by 200 and 640 by 200 Graphics mode.

Alphanumeric Mode

1 = Selects intensified border color.

320 by 200 Graphics mode.

1 = Selects intensified background and border color (C0 through C1).

640 by 200 Graphics Mode.

1 = Selects red foreground color.

Bit 2

Red Border/Background

Border color select in Text modes, and screen background color in 320 by 200 and 640 by 200 Graphics modes.

Text mode:

1 = select red border color

320 by 200 Graphics mode:

1 = Select red background and border color

640 by 200 Graphics mode:

1 = select red foreground color.

Bit 1

Green border/Background.

Border Color select in Text modes, and screen background color in 320 by 200 and 640 by 200 Graphics mode.

Alphanumeric Mode.

1 = Selects green border color.

320 by 200 Graphics Mode.

1 = Selects green background and border color (C0 through C1).

640 by 200 Graphics Mode.

1 = Selects green foreground color.

Bit 0

Blue border/Background.

Border Color select in Text modes and screen background color in 320 by 200 and 640 by 200 Graphics mode.

Alphanumeric Mode.

1 = Selects Blue border color.

320 by 200 Graphics Mode.

1 = Selects Blue background and border color (C0 through C1).

640 by 200 Graphics Mode.

1 = Selects Blue foreground color.

16.5 CRT STATUS REGISTER MDA OPERATION

Read Only Port = 3BAh

BITS	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.

0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bits 6:4

Reserved.

Bit 3

B/W Video Status.

0 = B/W Video disabled.
1 = B/W Video enabled.

Bits 2:1

Reserved.

Bit 0

Display Enable.

0 = Display enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

16.6 CRT STATUS REGISTER CGA OPERATION

Read Only Port = 3DAh

BITS	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bits 7:4

Reserved.

Bit 3

Vertical Retrace.

0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode

Bit 2

Light Pen Switch Status.

0 = Light pen switch closed.
1 = Light pen switch open

Bit 1

Light Pen Latch.

0 = Light Pen Latch cleared.
1 = Light Pen Latch set.

Bit 0

Display Enable.

0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

16.7 AT&T/M24 REGISTER

Write Only Port = 3DEh

This is a write only, 8-bit register located at address 3DEh. It is used to control the 640 by 400 AT&T Graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in the Video Select register (PR2).

BITS	FUNCTION
7	Reserved
6	White/Blue Underline
5,4	Reserved
3	Memory Map display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.

Defines underline attribute according to the MDA display requirements.

0 = Underline attributes selects blue foreground in-color Text modes.
1 = Underline attribute selects white underlined foreground.

Bits 5:4

Reserved.

Bit 3

Page Select.

Selects between one or two 16 Kbyte RAM page for display in 200 line Graphics mode.

0 = Display memory address starts at B800:0h (16KB length).
1 = Display memory address starts at BC00:0h (16KB length).

Bit 2

Character Set Select.

Selects between two character font planes.

0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or non-IBM Graphics Mode. 400 line mode, (A 400 line monitor is required for this mode).

0 = 200-line graphics mode active using paired lines.
1 = AT&T mode enabled for 400-line graphics.

17.0 INDEXED REGISTER ACCESS FOR HARDWARE CURSOR, BITBLT, AND LINE DRAWING

All of the WD90C24A/A2 enhanced functions are controlled by one or more indexed registers, most of which are above and beyond standard VGA registers.

Enhanced functions are controlled by indexed register blocks. Each indexed register block can contain up to 16 12-bit indexed registers. The 4-bit register index is written, along with the 12-bit data field, to form a 16-bit word.

Access to VGA-type registers is described in Section 21. This section describes the access to indexed register blocks.

17.1 ACCESSING INDEXED REGISTERS

To write to one or more indexed registers within any register block, the register block must first be selected by loading its address into the Register Block Pointer fields of the Index Control Register. This causes the selected register block to appear at the Register Access port.

A 16-bit word is then written to the Register Access port. The 4 high-order bits specify the Index of the register to be written, while the 12 low-order bits are the data to be written. Then, additional registers within the same register block can be written without selecting the same register block again.

To read one or more indexed registers within a register block, first, the address of the register block is written to the Register Block Pointer Field bits [7:0], of the Index Control Register at port 23C0h/23C1h. Then, the desired starting register to be read within the block is written to the Register Index Field, bits [11:8]. Both fields are set with the same 16-bit write. This causes the selected register to appear at the Register Access Port located at 23C2h//23C3h.

A 16-bit word is then read from the Register Access port. When reading an indexed register, the four high-order bits of the value returned contain the index of the register.

If the Auto-increment Disable bit in the Index Control Register is reset, consecutive reads to the Register Access port will return consecutively indexed registers within the same register block. Registers are read in ascending order through register Fh (the sixteenth register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Addressing a non-existent register results in zeros being returned in the 12-bit data field.

If the Auto-increment Disable bit is set, consecutive reads return the same index register.

GLOBAL PORT MAP	
PORT	**DESCRIPTION**
23C0h	Index Control Register, Low Byte
23C1h	Index Control Register, High Byte
23C2h	Register Access Port, Low Byte
23C3h	Register Access Port, High Byte
23C4h	BITBLT I/O Port
23C5h	BITBLT I/O Port
23C6h	Reserved
23C7h	Reserved

17.2 INDEX CONTROL REGISTER - PORT 23C0h/23C1h

Except for bit 13, which is read-only, the Index Control Register is a read/write register that controls reads and writes to indexed register blocks.

BITS	FUNCTION
15:14	Reserved
13	Invalid Register Block (read-only bit)
12	Auto-increment Disable
11:8	Register Index (Used for Read Operations)
7:0	Register Block Pointer

Bits 15:14

Reserved

Bit 13

Invalid Register Block (Read Only)

0 = Currently addressed register block exists on this device.
1 = Currently addressed register block does not exist on this device.

Bit 12

Auto-increment Disable

0 = Consecutive Reads return consecutive indexed registers.
1 = Consecutive Reads return the same indexed register.

Bits 11:8

Register Index

The index of the desired starting register to be read within a block is written to these bits. When read, these bits return the index of the next register to be read.

Bits 7:0

Register Block Pointer

To read one or more indexed registers within a register block, the address of the register block is written to this field.

REGISTER BLOCK MAP	
POINTER	**REGISTER/PORT ACCESS**
00	System Control Registers
01	BITBLT Registers
02	Hardware Cursor Registers

17.3 INTERRUPT STATUS REGISTER, SYSTEM CONTROL REGISTERS BLOCK - INDEX 0

Interrupt Status information is provided by the Interrupt Status Register in the System Control Register Block. This register returns information regarding which part of the WD90C24A/A2 caused an interrupt.

Reading this register does not reset any interrupts. Resetting of each interrupt is handled independently.

17.3.1 Interrupt Status Register

Unassigned interrupts are returned as zeros.

BITS	FUNCTION
15:12	0000 (Index)
11	Interrupt 10 Active
⇓	⇓
8	Interrupt 7 Active
7	High when at least one of interrupts 10 through 7 is active.
6	Interrupt 6 Active
⇓	⇓
1	Interrupt 1 Active
0	Any Interrupt is Active

17.3.2 Global Interrupt Map

INTERRUPT	DESCRIPTION
1	VGA Interrupt
2	BITBLT Interrupt

18.0 HARDWARE CURSOR

NOTE

The Hardware Cursor Feature supports dual panel mode for the WD90C24A/A2 controller.

The hardware cursor supports a user-defined pattern of up to 64 by 64 pixels defined at 2-bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all packed and planar VGA graphics modes, as well as VGA text modes.

The Hardware Cursor is accessed at Port 23C2h/ 23C3h when the register block pointer at Port 23C0h is set to 02h. Each register is identified by the index number in bits [15:12].

INDEX	FUNCTION
0	Cursor Control
1	Cursor Pattern Address Low
2	Cursor Pattern Address High
3	Cursor Primary Color
4	Cursor Secondary Color
5	Cursor Origin
6	Cursor Display Position X
7	Cursor Display Position Y
8	Cursor Auxiliary Color

TABLE 18-1. CURSOR REGISTERS

18.1 CURSOR CONTROL REGISTER, INDEX 0

This register controls operation of the hardware cursor.

BIT	FUNCTION
15:12	0000 (Index)
11	Cursor Enable
10:9	Cursor Pattern type
8	Cursor Plane Protection
7:5	Cursor Color Mode
4:0	Reserved

NOTE

A write to either Cursor Pattern Address register or to the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the cursor control register. (In interlaced mode, it is the next video field.)

Bits 15:12

Index 0.

Bit 11

Cursor Enable

0 = Cursor is not displayed
1 = Cursor is displayed

Bits 10:9

Cursor Pattern Type

00 = Cursor is 2-bits per pixel, 32 by 32 pixels
01 = Cursor is 2-bits per pixel, 64 by 64 pixels
10 = Reserved
11 = Reserved

Bit 8

Cursor Plane Protection

0 = Cursor plane protection disabled
1 = Cursor plane protection enabled

Bits 7:5

Cursor Color Mode

BITS 7:5			FUNCTION
0	0	0	Straight monochrome (compatibility)
0	0	1	Two-color cursor with inversion
0	1	0	Two-color cursor with special inversion
0	1	1	Three-color cursor
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Bits 4:0

Reserved

18.2 CURSOR PATTERN ADDRESS

The two cursor pattern address registers form a 20-bit address which specifies the location in the non-visible portion of display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin.

Generally, this address represents the CPU address at which the pattern begins minus the CPU address of the top-left corner of the screen, in whatever VGA mode is currently in use. All addresses are not valid in all modes. Refer to the Cursor Location High and Low registers in Sections 9.16 and 9.17, respectively.

NOTE

A write to either Cursor Pattern Address register or to the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the cursor control register. (In interlaced mode, it is the next video field.)

18.2.1 Cursor Pattern Address Low, Index 1

The lower order twelve bits of the 20-bit cursor pattern address.

BIT	FUNCTION
15:12	0001 (Index)
11:0	Cursor Pattern Address Bits [11:0]

18.2.2 Cursor Pattern Address High, Index 2

The high order eight bits of the 20-bit cursor pattern address.

BIT	FUNCTION
15:12	0010 (Index)
11:8	Reserved
7:0	Cursor Pattern Address Bits [19:12]

18.3 CURSOR ORIGIN, INDEX 5

The cursor origin register specifies the offset from the top-left corner of the pattern which is displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

For 32 by 32 cursor patterns each field is restricted to the values 31 through 0.

BIT	FUNCTION
15:12	0101 (Index)
11:6	Cursor Origin Y Bits [63:0]
5:0	Cursor Origin X Bits [63:0]

18.4 CURSOR DISPLAY POSITION

The cursor display position X and Y registers specify the location on the screen at which the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels, not characters. The cursor can be displayed at any position on the screen, including between characters.

NOTE

A write to the cursor display position X or Y register does not take effect until the beginning of the next video frame. (In interlaced mode, it is the next video field.)

18.4.1 Cursor Display Position X, Index 6

BIT	FUNCTION
15:12	0110 (Index)
11	Reserved
10:0	Cursor Display Position X

18.4.2 Cursor Display Position Y, Index 7

BIT	FUNCTION
15:12	0111 (Index)
11	Reserved
10:0	Cursor Display Position Y

18.5 CURSOR COLOR REGISTERS

The cursor color resisters control display of 2-bit per pixel cursor patterns.

The cursor primary color, cursor secondary color, and cursor auxiliary color registers specify 8-bit colors to be displayed for different parts of the cursor pattern.

NOTE

Even in planar mode, with 4-bits per pixel, these colors are 8-bits per pixel

18.5.1 Cursor Primary Color, Index 3

BIT	FUNCTION
15:12	0011 (Index)
11:8	Reserved
7:0	Cursor Primary Color

18.5.2 Cursor Secondary Color, Index 4

BIT	FUNCTION
15:12	0100 (Index)
11:8	Reserved
7:0	Cursor Secondary Color

18.5.3 Cursor Auxiliary Color, Index 8

BIT	FUNCTION
15:12	1000 (Index)
11:8	Reserved
7:0	Cursor Auxiliary Color

18.6 CURSOR REGISTER UPDATES

When a new cursor pattern is selected, up to four different registers must be updated. If a new video frame were to begin before all registers were updated, a single frame could be displayed with incorrect cursor data. While the display would recover within one video frame, the results would be visually annoying. Therefore, the WD90C24A/A2 holds off use of updated register data until all of the associated registers have been updated.

Writing to either the Cursor Pattern Address register or the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the Cursor Control register. Therefore, the Cursor Control register must be written to after updating either of these registers, even if the data in the Cursor Control register is to remain unchanged. However, reading any of these registers always returns the data last written to the register, whether or not such data has already taken effect.

A write to either Cursor Display Position X or Y register does not take effect until the beginning of the next video frame. In interlaced mode, updates occur at the beginning of the next video field.

18.6.1 Cursor Address Mapping

Cursor patterns are always stored in contiguous locations in display memory, usually in a non-visible portion, and always across all four maps. The definition of contiguous locations differs slightly by mode, as defined in Tables 18-2, 3 and 4.

Each mode has restrictions on where a cursor pattern may begin and how such a pattern must be stored. The location where the currently required cursor pattern is stored in display memory is loaded by the host into the Cursor Pattern Address registers, as defined in Tables 18-2, 3, and 4.

The Cursor Pattern Address registers point to the doubleword starting region of the cursor pattern. They are not byte addresses and consecutive register values generally do not point to consecutive memory bytes. However, the cursor pattern must use all of the consecutive memory bytes (1K or 256 bytes) assigned to it starting from the byte pointed to.

CPU ADDRESS	CURSOR PATTERN ADDRESS
Bank 0	
A0000[1]	
Map 0	0 If pattern starts here...
Map 1	2 then the next byte is here...
Map 2	2 then here...
Map 3	2 then here...
A0001	
Map 0	1 and the fifth byte is here
⇓	
AFFFF	
Map 0	FFFF
Bank 1	
A0000	
Map 0	10000
⇓	
AFFFF[3]	
⇓	
Map 3	1FFFF (Theoretical maximum for 1K X 1K display memory.)
Refer to the following notes.	

TABLE 18-2. PLANAR MODES

NOTES FOR TABLES 18-2 THROUGH 18-4

1. These locations are usually visible. In practice, cursor pattern is usually stored in non-visible memory.
2. Cursor pattern must start in map 0 but pattern is stored on all maps.
3. Some modes and/or boards may not support CPU addresses up to this level. Since up to 1K consecutive locations are required for the pattern, the pattern cannot actually start at the highest locations.
4. In mode 7, CPU addresses are B0000-B7FFE.

CPU ADDRESS	CURSOR PATTERN ADDRESS
Bank 0	
A0000[1]	0 If pattern starts here . . .
A0001	2 then next byte is here . . .
A0002	2 then here . . .
A0003	2 then here . . .
A0004	1 and the fifth byte is here
⇓	
AFFFC	3FFF
Bank 1	
A0000	4000
⇓	
Bank 0F	
⇓	
AFFFC[3]	3FFFF (Theoretical maximum for 1K X 1K display memory.)
Refer to the previous notes.	

TABLE 18-3. PACKED MODES

CPU ADDRESS	CURSOR PATTERN ADDRESS
Maps 0:1	
B80001	0 If pattern starts here . . .
B8001	2 then next byte is here . . .
Maps 2:3	
B8000	2 then here . . .
B8001	2 then here . . .
Maps 0:1	
B8002	1 and the fifth byte is here
B8003	
⇓	⇓
BFFFE	3FFF
BFFFF	
Refer to the previous notes.	

TABLE 18-4. TEXT MODES

18.6.2 Two-Bit Cursor Pattern Format

The cursor pattern pointed to by the Cursor Pattern Address registers for two-bit cursor patterns is stored in either 1K or 256 consecutive memory byte locations. The cursor pattern data is stored for 64 by 64 and 32 by 32 cursors as follows:

18. 6.2.1 Cursor Pattern - 2-Bit, 64 by 64 Cursors

OFFSET 1	MAP 2	CURSOR PATTERN3,4
0	0	AND plane, row 0, col 0-7
	1	XOR plane, row 0, col 0-7
	2	AND plane, row 0, col 8-15
	3	XOR plane, row 0, col 8-15
1	0	AND plane, row 0, col 16-23
	1	XOR plane, row 0, col 16-23
	2	AND plane, row 0, col 24-31
	3	XOR plane, row 0, col 24-31
2	0	AND plane, row 0, col 32-39
	1	XOR plane, row 0, col 32-39
	2	AND plane, row 0, col 40-47
	3	XOR plane, row 0, col 40-47
3	0	AND plane, row 0, col 48-55
	1	XOR plane, row 0, col 48-55
	2	AND plane, row 0, col 56-63
	3	XOR plane, row 0, col 56-63
4	0	AND plane, row 1, col 0-7
	1	XOR plane, row 1, col 0-7
	2	AND plane, row 1, col 8-15
	3	XOR plane, row 1, col 8-15
	⇩	
255	0	AND plane, row 63, col 48-55
	1	XOR plane, row 63, col 48-55
	2	AND plane, row 63, col 56-63
	3	XOR plane, row 63, col 56-63
Refer to the following notes.		

NOTES

1. Offset is relative to the value in the Cursor Pattern Address register.
2. In packed mode, Map is selected by the two low-order CPU address bits.
3. Cursor pattern must start in map 0 but pattern is stored on all maps.
4. Within each byte, the high-order bit represents the left most column.

18. 6.2.2 Cursor Pattern - 2-Bit, 32 by 32 Cursors

OFFSET 1	MAP 2	CURSOR PATTERN3,4
0	0	AND plane, row 0, col 0-7
	1	XOR plane, row 0, col 0-7
	2	AND plane, row 0, col 8-15
	3	XOR plane, row 0, col 8-15
1	0	AND plane, row 0, col 16-23
	1	XOR plane, row 0, col 16-23
	2	AND plane, row 0, col 24-31
	3	XOR plane, row 0, col 24-31
2	0	AND plane, row 1, col 0-7
	1	XOR plane, row 1, col 0-7
	2	AND plane, row 1, col 8-15
	3	XOR plane, row 1, col 8-15
3	0	AND plane, row 1, col 16-23
	1	XOR plane, row 1, col 16-23
	2	AND plane, row 1, col 24-31
	3	XOR plane, row 1, col 24-31
	⇩	
63	0	AND plane, row 31, col 16-23
	1	XOR plane, row 31, col 16-23
	2	AND plane, row 31, col 24-31
	3	XOR plane, row 31, col 24-31
Refer to the previous notes.		

18.6.3 Loading The Cursor Pattern

Loading a cursor pattern requires writing the pattern to a non-visible portion of display memory, then pointing to the pattern with the Cursor Pattern Address registers (Index 1, 2). A cursor pattern already in display memory can be selected simply by loading these registers.

In some VGA modes, certain maps are not defined but the physical RAM connected to those maps appears at higher memory locations in the maps that are defined. For instance, the first byte of map 2 may appear as the 64th Kbyte in map 0. Therefore a cursor pattern that occupies contiguous locations in one mode may appear fragmented in other modes. It is the responsibility of the software to track these fragments and assure that no part of the pattern will be accidentally overwritten.

18.6.4 Cursor Color Modes

A cursor may be displayed using any of four color modes selected by the Cursor Color Mode field of the Cursor Control Register (Index 0).

Depending on the color mode selected, each 2-bit pixel of the cursor pattern will be displayed against the background as described in Table 18-5.

The "special" color generates the exclusive-NOR (XNOR) of the background and the Auxiliary Color Register (Index 9, A, or B). This retains the "different from background" color property of inversion while adding the ability to specify one preferred "special inversion" from a background color to any desired color.

To use this feature, the Cursor Color Mode field must be set to "special", and the Cursor Auxiliary Color should be loaded with the exclusive NOR (XNOR) of the background color to be translated and the desired color to be displayed. When set in this manner, any screen pixel of the former color covered by an inverting cursor pattern pixel will be "inverted" into the auxiliary color.

CURSOR PATTERN1	COLOR MODE 0	COLOR MODE 1	COLOR MODE 2	COLOR MODE 3
00	All 0s	Secondary	Secondary	Secondary
01	All 1s	Primary	Primary	Primary
10	Transparent	Transparent	Transparent	Transparent
11	Inverted	Inverted	Special2	Auxiliary

NOTES:

1. The high-order bit of each 2-bit pattern is the AND mask, and the low-order bit is the XOR mask.
2. The result is Background XNORd with the auxiliary color.

TABLE 18-5. CURSOR COLOR MODES

18.6.5 Compatibility Differences Between Hardware And Software Cursor

Some cursor colors may display differently using the hardware cursor than when using a software cursor. This can happen in Planar Modes, because a software cursor modifies memory data that is then passed through the Attribute Controller's Palette registers, while the hardware cursor operates on data at the output of the Attribute Controller's Palette registers. The following section on Cursor Plane Protection explains how to minimize these incompatibilities.

18.6.6 Cursor Plane Protection

In 256-color modes, a background pixel covered by the cursor is either replaced by a specified 8-bit color or is inverted. For other modes, cursor plane protection is available.

When the Cursor Plane Protection bit of the Cursor Control register is set, some bits of the background are handled differently. In these cases the two or four high-order bits of the background are replaced with the corresponding bits of the Cursor Auxiliary Color register (Index 9, A, or B).

When bit 7 of the VGA Attribute Mode Control register (Port 3C0h/3C1h, Index 10h) is reset, cursor plane protection applies to the two high-order bits of the background. When this bit is set, protection applies to the four high-order bits.

This feature is designed to provide as much flexibility and compatibility with a software cursor as possible, due to the processing done by the VGA attribute controller.

19.0 HARDWARE BITBLT

The BITBLT hardware supports accelerated data transfers between regions of display memory. Display memory regions may be rectangular or linear.

A full complement of raster operations are available. Color expansion and transparency, useful for accelerating text modes as well as plane masking, are also supported.

This same hardware can be used to rapidly copy 8 by 8 patterns and fill rectangles.

The BITBLT hardware supports text modes and monochrome, 4-bit and 8-bit color modes, as well as the 16-bit color mode. The BITBLT registers are listed by their index number in Table 19-1.

INDEX NUMBER	REGISTER NAME
0	BITBLT Control - Part 1[1]
1	BITBLT Control - Part 2
2	BITBLT Source Low/XSTEP
3	BITBLT Source High/RSTEP
4	BITBLT Destination Low[1]
5	BITBLT Destination High[1]
6	BITBLT Dimension X/Delta-X
7	BITBLT Dimension Y/Delta-Y
8	BITBLT Row Pitch
9	BITBLT Raster Operation
A	BITBLT Foreground Color
B	BITBLT Background Color
C	BITBLT Transparency Color
D	BITBLT Transparency Mask
E	BITBLT Map and Plane Mask

1. All or part of these registers can change automatically.
2. The BITBLT ports (23C4 and 23C5) are accessed as extended registers. Refer to Extended Register Access, Section 17.

TABLE 19-1. BITBLT REGISTERS

19.1 CONTROL AND STATUS

19.1.1 BITBLT Control - Part 1, Index 0

BITS	FUNCTION
15:12	0000 (Index)
11	BITBLT Activation/Status*
10	BITBLT Direction
9:8	BITBLT Addressing Mode
7:6	BITBLT Destination/Source Linearity
5:4	BITBLT Destination Select
3:2	BITBLT Source Format
1:0	BITBLT Source Select

* Bit 11 is automatically reset when BITBLT is complete.

Bits 15:12

Index 0.

Bit 11

BITBLT Activation Status

Writing a one to this bit starts a BITBLT operation using the currently loaded register values. This bit is reset automatically when the BITBLT operation is complete. Therefore, reading a 1 from this bit indicates that a BITBLT operation is in progress.

Writing a 0 to this bit will not start a BITBLT operation but may be useful in "quick start" mode to set the other bits in the register for the coming series of quick-start operations.

CAUTION

Writing a 0 to this bit while a BITBLT operation is in progress may cause unexpected and unrecoverable results.

0 = Do not start BITBLT (write), BITBLT complete (read).
1 = Start BITBLT (write), BITBLT in progress (read).

Bit 10

BITBLT Direction

0 = BITBLT direction is top to bottom and left to right.
1 = BITBLT direction is bottom to top and right to left.

Bits 9:8

BITBLT Address Mode

00 = Planar Mode (includes monochrome modes).
01 = Packed mode (includes text and 256-color modes).
1x = Reserved for future expansion.

Bits 7:6

BITBLT Destination/Source Linearity

When the Destination or Source region of a BITBLT operation is specified as linear, each row of that region is considered to begin at the doubleword immediately following the doubleword containing the last pixel of the preceding row. The alignment of the first pixel in each line is the same. No doubleword will straddle two lines and there may be gaps at unused pixels between adjacent lines.

Bit 7 controls the destination region and bit 6 controls the source region.

0 = Region is rectangular.
1 = Region is linear.

Bits 5:4

BITBLT Destination Select

00 = Destination is screen memory.
10 = Destination is system I/O location.
x1 = Reserved for future expansion.

Bits 3:2

BITBLT Source Format

00 = Source format is color.
01 = Source format is monochrome from color comparators.
10 = Source format is fixed color (filled rectangle).
11 = Source format is monochrome from host.

Bits 1:0

BITBLT Source Select

00 = Source is screen memory.
10 = Source is system I/O location, 32-bits.
x1= Reserved for future expansion.

19.1.2 BITBLT Control - Part 2, Index 1

BITS	FUNCTION
15:12	0001(Index)
11	Enable Line Drawing
10	BITBLT Interrupt Enable
9	X or Y Major
8	Y Direction
7	BITBLT Quick Start
6	BITBLT Update Destination
5:4	BITBLT Pattern Select
3	BITBLT Monochrome Transparency
2	BITBLT Transparency Polarity
1	Reserved, must be 0
0	BITBLT Transparency Enable

Bits 15:12

Index 1

Bit 11

Enable Line Drawing

0 = Enable another BITBLT function
1 = Enable Line Drawing

Bit 10

BITBLT Interrupt Enable

0 = Do not interrupt on completion of BITBLT.
1 = Interrupt on completion of BITBLT.

Bits 9

X or Y Major (Valid only when bit 11 is set to 1)

0 = X Major (Slope is less than 1)
1 = Y Major (Slope is greater than 1)

Bits 8

Y direction (Valid only when bit 11 is set to 1)

0 = Top to Bottom
1 = Bottom to Top

Bit 7

BITBLT Quick Start

When bit 7 is set, BITBLT starts automatically as soon as the BITBLT Destination Low register (Index 4) is written unless automatic destination update is enabled for BITBLT. If automatic BITBLT update destination (bit 6) is enabled, BITBLT starts automatically when the BITBLT Source Low Register (Index 2) is written.

Quick Start permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control Register operate as they were last written, and the BITBLT activation bit is physically set and can be read back normally.

0 = BITBLT starts only when explicitly enabled.
1 = BITBLT starts automatically when the destination register is written or when the source register is written if destination update is enabled.

Bit 6

BITBLT Update Destination

A host doing multiple BITBLT operations only needs to update the registers that change from one BITBLT to the next. Most BITBLT registers do not change unless written to by the host. The exceptions are the two BITBLT Destination Registers (Index 4 and 5) and the status bit in the BITBLT Control Register (Index 0).

When bit 6 of this register is set, the BITBLT Destination Registers are automatically updated at the end of each BITBLT operation. When updated, the registers point to the rectangular region immediately to the right of the previous destination region. When the destination region is specified as linear rather than rectangular, the destination registers point to the location immediately past the previous destination region. This feature specifically improves text output operations.

0 = Do not update destination on completion of BITBLT operation.
1 = Update destination on completion of BITBLT operation.

Bits 5:4

BITBLT Pattern Select

00 = Patterns are not used.
01 = 8 by 8 patterns are used for source.
1x = Reserved for future expansion.

Bit 3

BITBLT Monochrome Transparency

0 = Monochrome transparency is not enabled.
1 = Monochrome transparency is enabled.

Bit 2

BITBLT Transparency Polarity

0 = Matching pixels are transparent.
1 = Matching pixels are opaque.

Bit 1

Reserved, must be set to 0.

Bit 0

BITBLT Transparency Enable

0 = Destination transparency is not enabled.
1 = Destination transparency is enabled.

19.2 SOURCE AND DESTINATION

The BITBLT Source Low and BITBLT Source High registers specify the source address for BITBLT operations. The BITBLT Destination Low and BITBLT Destination High registers specify the destination address for BITBLT operations. The high and low fields of each register pair are concatenated to form a 21-bit address pointing to the starting corner of the source or destination region.

The starting corner for the source and destination will be either the top-left or bottom-right corner. The corner specified must be coordinated with the BITBLT Direction bit of the BITBLT Control Register.

When the source and destination regions do not overlap, BITBLT can be started in either corner. When these regions do overlap, the corner and direction must be selected to prevent parts of the source region from being overwritten by the destination array before they are copied.

When the BITBLT Update Destination bit in the BITBLT Control Register is set, the host should not read the BITBLT Destination Registers while a BITBLT operation is in progress. This is because the BITBLT Destination Registers will change just before the end of the operation.

When the BITBLT Quick Start bit in the BITBLT Control Register is set, writing to the BITBLT Destination Registers may automatically start BITBLT operations.

19.2.1 BITBLT Source Low, Index 2

BITS	FUNCTION
15:12	0010 (Index)
11:0	BITBLT Source Position, Bits [11:0]
NOTE: For Line Drawing, XSTEP uses bits [9:0] only.	

19.2.2 BITBLT Source High, Index 3

BITS	FUNCTION
15:12	0011 (Index)
11:9	Reserved, must be 0
8:0	BITBLT Source Position, Bits [20:12]
NOTE: For Line Drawing, RSTEP uses bits [9:0] only.	

19.2.3 BITBLT Destination Low, Index 4

BITS	FUNCTION
15:12	0100 (Index)
11:0	BITBLT Destination Position, Bits [11:0]

19.2.4 BITBLT Destination High, Index 5

BITS	FUNCTION
15:12	0101 (Index)
11:9	Reserved, must be 0
8:0	BITBLT Destination Position, Bits [20:12]

19.3 ADDRESS MAPPING

The source and destination addresses are partially mode dependent. Addresses represent the character or pixel at the starting corner of the move, which may be the top-left or bottom-right corner.

19.3.1 Monochrome and Planar Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Location 0, Bit 7 (left most pixel).
	1	Location 0, Bit 6
	⇓	
	7	Location 0 Bit 0 (right most pixel)
A0001	8	Location 1, Bit 7
⇓		
AFFFF[2]	2M-1	Location 256K -1 Bit 0[1]

[1]Last location in a 1 MB system. Smaller system memory configurations have fewer display memory locations.

[2]The address has wrapped around four times.

19.3.2 Packed Modes

CPU ADDRESS	BITBLT REGISTER ADDRESS	DISPLAY MEMORY LOCATION (ALL MAPS)
A0000	0	Map 0, Location 0 (left most pixel)
A0001	1	Map 1, Location 0
A0002	2	Map 2, Location 0
A0003	3	Map 3, Location 0
A0004	4	Map 0, Location 1 (left most pixel)
⇓	⇓	⇓
A0007	7	Map 3, Location 1 (right most pixel)
	⇓	
AFFFF[2]	1M-1	Map 3, Location 256K -1[1]

[1]Last location in a 1 MB system. Smaller system memory configurations have fewer display memory locations.

[2]The address has wrapped around 16 times.

The locations referred to in the previous lists are the CPU address offsets in bytes from the top of display memory for any given mode. For example, where display memory starts at CPU address A0000h, location 123h would correspond to CPU address A0123h. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64 Kbytes, location 10123h would correspond to CPU address A0123h in the second page of the display memory.

When the source or destination of a BITBLT operation is not a memory location, the corresponding pair of position registers are unused and may contain any value, except that the two or three low order bits of the BITBLT Source Low Register are still used to specify a source alignment of the data.

19.4 DIMENSIONS AND ROW PITCH

19.4.1 BITBLT Dimension X, Index 6

BITS	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension X[1]/Delta -X[2]

NOTES:

1. For BITBLT Dimension X, the legal range is 1 to 2K pixels
2. For Line Drawing, Delta -X uses bits [9:0] only.

The BITBLT Dimension X register specifies the width of the rectangular region to be copied.

In Line Drawing mode, this register specifies the length of the line in the X- coordinate.

In Graphics Modes, this value is expressed in pixels.

In Text Modes, this value is expressed in the number of characters multiplied by eight (even though each character is stored using only two bytes).

19.4.2 BITBLT Dimension Y, Index 7

BITS	FUNCTION
15:12	0110 (Index)
11:0	BITBLT Dimension Y[1]/Delta -Y[2]

NOTES:

1. For BITBLT Dimension Y, the legal range is 1 to 2K pixels
2. For Line Drawing, Delta -Y uses bits [9:0] only.

The BITBLT Dimension Y register specifies the width of the rectangular region to be copied.

In Line Drawing mode, this register specifies the length of the line in the Y- coordinate.

In Graphics Modes, this value is the height of the rectangular region expressed in pixels.

In Text Modes, this value is the height of the region expressed in character rows.

19.4.3 BITBLT Row Pitch, Index 8

BITS	FUNCTION
15:12	1000 (Index)
11:0	BITBLT Row Pitch*
* In Packed Mode, the two low order bits of this field must be zero. In Planar Mode, the three low order bits of this field must be zero.	

The BITBLT Row Pitch Register specifies the linear offset from any location in a given row to the same location in the next row. This offset is in the same units as the source and destination fields to which it applies.

When both the source and destination are rectangular regions, the BITBLT Row Pitch value applies to both regions. When either or both are not rectangular, the offset does not apply to that range.

19.5 FOREGROUND AND BACKGROUND COLORS

The BITBLT Foreground and Background registers specify 8-bit or 4-bit digital colors to be used when expanding monochrome source areas. Also, the foreground color can be specified as the source of a BITBLT to produce a filled rectangle.

19.5.1 BITBLT Foreground Color, Index A

BITS	FUNCTION
15:12	1010 (Index)
11:8	Reserved
7:0	BITBLT Foreground Color*
* In Planar Mode, only bits [3:0] are used to specify color.	

19.5.2 BITBLT Background Color, Index B

BITS	FUNCTION
15:12	1011 (Index)
11:8	Reserved
7:0	BITBLT Background Color*
* In Planar Mode, only bits [3:0] are used to specify color.	

19.6 MAP AND PLANE MASK

The BITBLT Mask Register controls both the plane and map masks used in BITBLT.

19.6.1 BITBLT Map Mask

The BITBLT Map Mask field specifies a 4-bit mask that prevents data in the specified maps from being updated. This mask is needed for BITBLT in all text modes to prevent font data from being overwritten in a character-attribute move and vice versa. This also applies to VGA mode F, and it can be used in VGA modes 4, 5, and 6 for partial hardware support. In addition, it can be used in VGA modes D, E, 10, 11, and 12 and extended Planar modes as a Plane Mask.

19.6.2 BITBLT Plane Mask

The BITBLT Plane Mask field specifies an 8-bit mask that prevents data in the specified planes from being updated. This is useful in VGA mode 13 and in extended Packed modes when Plane masking is desired.

19.6.3 BITBLT Mask - VGA, Index E

BITS	FUNCTION
15:12	1110 (Index)
11:8	Reserved
7:0	BITBLT Plane Map Mask Mode*
* In Planar Mode, only bits [3:0] are used.	

BITS 3:0	BITBLT MAP MASK
XXX0	Map 0 Disabled
XXX1	Map 0 Enabled
⇓	⇓
0XXX	Map 3 Disabled
1XXX	Map 3 Enabled

BITS 7:0	BITBLT PLANE MASK
XXXX XXX0	Plane 0 Disabled
XXXX XXX1	Plane 0 Enabled
⇓	⇓
0XXX XXXX	Plane 7 Disabled
1XXX XXXX	Plane 7 Enabled

19.7 RASTER OPERATIONS

The BITBLT Raster Operation Register specifies a logical operation to be performed on the source and destination fields. These fields are always active and must be loaded with the appropriate value even when a simple source copy is to be performed.

19.7.1 BITBLT Raster Operation, Index 9

BITS	FUNCTION
15:12	1001 (Index)
11:8	BITBLT Raster Operation Code (abcd in Table 19-3).
7:0	Reserved

All BITBLT operations apply a source color, pattern, or area to a destination region. The result, which is written to the destination, is a logical function of the source and destination pixels for each location.

19.7.2 Raster Operation Code

The Raster Operation code is defined as follows:

The source (S) and Destination (D) form a 2-bit value. Table 19-2 lists the logical results of these combined Source and Destination values.

The four 1-bit results from Table 19-2 form the Raster Operation code (abcd). The 'a' in the code is defined as the high order bit.

While the Raster Operation code represents a two-input operation (any two results form one code), both inputs are not always relevant to the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination value.

NOTE

Arithmetic operations are not supported.

S	D	RESULT
0	0	a
0	1	b
1	0	c
1	1	d

TABLE 19-2. RESULTS OF COMBINED SOURCE AND DESTINATION VALUES

RASTER OP CODE (abcd)	FUNCTION	RASTER OP CODE (abcd)	FUNCTION
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	$S \bullet \overline{D}$	1010	Inverted Destination
0011	Source	1011	$S+\overline{D}$
0100	$\overline{S} \bullet D$	1100	Inverted Source
0101	Destination	1101	$\overline{S}+D$
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 19-3. RASTER OPERATION CODE FUNCTIONS

19.8 PATTERNS

The WD90C24A/A2 has a special mode to accelerate the copying of 8 by 8 source patterns. In this mode, an 8 by 8 full-color or monochrome pattern can be repetitively applied to a large destination region in an efficient manner.

To perform a pattern copy, the host first writes the 8 by 8 pattern to display memory in a linear fashion, usually in a non-visible location, depending on the current addressing mode as described in the following paragraphs. The host then loads the BITBLT Source Registers with the location of the pixel within the pattern corresponding to the top-

left corner of the destination region. The BITBLT Pattern Select field of the BITBLT Control Part 2 Register must be set to 8 by 8 patterns.

To specify a monochrome pattern, the host must write a color pattern in the current mode, planar or packed, and then use the control registers to specify a single plane of the source to be used.

19.8.1 BITBLT Pattern Storage - Monochrome and Planar Modes

In planar mode, the 8 by 8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data
n* to n+7	All maps, top row of 8 by 8 pattern
n+8 to n+15	All maps, second row of 8 by 8 pattern
⇓	
n+56 to n+63	All maps, bottom row of 8 by 8 pattern
n+64 to...	Any data
*n must be a multiple of 64	

19.8.2 BITBLT Pattern Storage - Packed Modes

In packed mode, the 8 by 8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

REGISTER ADDRESS	DISPLAY MEMORY CONTENTS
⇓	
n - 1	Any data
n*	Top row of 8 by 8 pattern, left most pixel
n+1	Top row of 8 by 8 pattern, Second Pixel
⇓	
n+7	Top row of 8 by 8 pattern, Right Most Pixel
n+8	Second row of 8 by 8 pattern, Left Most Pixel
⇓	
n+63	Bottom row of 8 by 8 pattern, right most pixel
n+64	Any data
*n must be a multiple of 64	

19.9 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each 0 in the source region is replaced with the specific background color, while each 1 is replaced with the foreground color. All other processing options, including mask and raster operations, remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination will be filled with the foreground color, subject to masks, raster operations, and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available since the transparency color registers are in use.

19.10 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data extracted in this manner is replicated to each plane or map as if it had been read from memory.

Also, monochrome data can be extracted from host data when the BITBLT source is the I/O port. In this case, each 32-bit word written to the I/O port is treat in the same manner as if it was read from display memory. Alternately, the host may send monochrome data through the I/O port that does not require extraction (refer to Section 19.14).

To extract a single plane from a color source field, the BITBLT Transparency Color Register should be loaded with FFh (all ones), while the BITBLT Transparency Mask Register should be loaded with a 0 in the map or plane position to be extracted, and with a 1 in all other positions.

Monochrome data is usually extracted as a specific bit of each 4-bit or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color 1, with all other colors returning a monochrome 0.

When the Monochrome Transparency bit is set in the BITBLT Control Register, monochrome source pixels of 0 do not modify the destination, regardless of any selected raster operation.

The Transparency Enable and Polarity bits in this register have no effect on the monochrome data extraction.

19.11 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually transparent, with the rest being opaque. Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of the source and destination, in which the source field of zero is effectively a transparent color, since when ORed with the destination, it does not change.

Color destination transparency is supported by the WD90C24A/A2, in addition to the more limited monochrome transparency described elsewhere.

19.11.1 BITBLT Transparency Color, Index C

The BITBLT Transparency Color Register specifies an 8-bit or 4-bit color to be used as the transparency color.

BITS	FUNCTION
15:12	1100 (Index)
11:8	Reserved
7:0	BITBLT Transparency Color*
* In Planar Mode, only the four low order bits [3:0] are used.	

19.11.2 BITBLT Transparency Mask, Index D

The BITBLT Transparency Mask Register specifies an 8-bit or 4-bit mask for use in comparison with the transparency color.

BITS	FUNCTION
15:12	1101 (Index)
11:8	Reserved
7:0	BITBLT Transparency Mask*
* In Planar Mode, only the four low order bits [3:0] are used.	

The pixels of the destination are compared with the transparency color under control of the transparency mask. Each bit of the Transparency Mask Register that is set to 1 makes the corresponding bit of the Transparency Color Register a "don't care."

The BITBLT Transparency Enable bit of the BITBLT Control Register, Index 1 specifies whether color transparency is enabled or disabled. The BITBLT transparency polarity bit specifies whether the pixels matching the transparency color are considered transparent. In this case, only destination pixels matching the transparent color can be overwritten, or transparent, and only non-matching pixels cannot be overwritten.

19.12 FILLED RECTANGLES

Filled rectangles can be drawn efficiently by the BITBLT hardware. A filled rectangle is a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the Source Format field in the BITBLT Control Register (Index 0) to "fixed color" and the Foreground Color Register (Index A) to the desired fill color. A source address is not required. All other BITBLT options are available in a normal manner.

20.0 HARDWARE LINE DRAWING

This section describes hardware line drawing, which is used to generate Microsoft Windows compatible Strip line drawings.

20.1 CONDITIONS

The following conditions must be met for strip line drawing to function properly.

- The line drawing must always start from left to right, regardless of other parameters such as top to bottom, bottom to top, Y-major, or X-major.
- The software must set up the BLT registers as if it were performing a rectangular fill.
- Software must also provide information concerning XSTEP, RSTEP, DELTA X, DELTA Y, X-DIRECTION, Y-DIRECTION, X-MAJOR, AND Y-MAJOR.

20.2 ALTERED BLT REGISTER FUNCTIONS

Some BLT register functions are altered during line draw. The altered register functions are given in the following list:

BLT INDEX	BLT FUNCTION	LINE DRAW FUNCTION
1.11	Reserved	0 = other BLT function 1 = Line Draw
1.9	Reserved	0 = X-Major (slope is less than 1) 1 = Y-Major (slope is greater than 1)
1.8	Reserved	Y-Direction 0 = Top to bottom 1 = Bottom to top
2	Source Low	XSTEP [9:0]
3	Source High	RSTEP [9:0]
6	Dimension X	Delta-X
7	Dimension Y	Delta-Y

TABLE 20-1. BLT FUNCTIONS ALTERED BY LINE DRAW

20.3 LINE DRAW OPERATION

At the start of a Line Draw operation, the software must set up all necessary BITBLT registers for proper operation.

After completion of a Line Draw operation, BITBLT Register Index 1, bit 11 must be set to 0 before the next BITBLT operation.

(All data previously on this page has been deleted.. The page remains in place to preserve page numbering in the rest of the document.)

21.0 APPLICATIONS AND PROGRAMMING NOTES

This section contains descriptions of the different applications and how to program the WD90C24A/A2. The following subjects are included:

- Using the Hardware Cursor in 16-bit per Color Mode
- BITBLT Operations in VGA Modes 4, 5, and 6
- BITBLT Operations in Text Mode
- Using BITBLT in 16-bit Per Color Mode
- Patterns
- Support for Kanji Characters
- Reading and Writing the VGA Readback Latches
- Changing Monochrome Sources to Color
- Extracting Monochrome Data
- Color Transparency
- Drawing Filled Rectangles
- System Memory to Display Memory Operations
- Display Memory to System Memory Operations
- System Memory to Display Memory Transfers with Color Expansion
- Control and Status
- Automatic Destination Update
- Quick Start Mode
- Aborted BITBLT
- Register Access

21.1 USING THE HARDWARE CURSOR IN 16-BIT PER COLOR MODE

The hardware cursor, while not specifically designed for "high-color" mode operation, can still be used, with certain limitations in that mode.

The hardware cursor is unaware of the existence of high-color mode, but can still be used by specifying two adjacent 2-bit pixel codes for each high-color cursor pixel. A "transparent" high-color pixel would be specified using two adjacent transparency codes, ("1010"), while a "color" high-color pixel would usually be specified using adjacent primary and secondary color codes, such as "0100". The desired 16-bit cursor color would then be split between the 8-bit primary and 8-bit secondary color registers. Inversion is also available as "1111" but the results might not be visually desirable.

Note that this limits the effective maximum cursor width in high-color mode to 32 pixels. Further, the cursor origin and position are defined in terms of 8-bit, not the displayed 16-bit, pixels. Therefore, these values should be horizontal multiples of two.

A developer could use the secondary and auxiliary color registers to create additional cursor colors by mixing cursor codes within a 16-bit pixel region. However, the developer should be aware of the effects of inversion in systems that use one bit to switch between false color and high-color modes on a pixel-by-pixel basis.

21.2 BITBLT OPERATIONS IN VGA MODES 4, 5, AND 6

VGA modes 4, 5, and 6 are partially supported on the WD90C24A/A2. Since these modes are not commonly used in Windows™, the additional hardware required to support the even/odd scan line offset technique employed in these modes is not supported.

However, a BITBLT operation in these VGA modes can often be broken up into two or three BLT operations, each of which operates on a contiguous area of memory.

When the vertical offset between source and destination is an even number of rows, the desired operation can be broken into two BITBLTs, one for the even rows and one for the odd rows. This requires careful consideration of the register parameters, especially the BITBLT Dimension Y register.

Where the offset is an odd number of rows, it may still be possible to break up the operation into only two BITBLTs, providing that there is no overlap between the source and destination regions. This is because information is being "swapped" between the even and odd scan line regions.

Where source and destination do overlap, it may be possible to use a scratch space in off-screen memory and break up the operation into three BITBLTs.

Another possibility is to break up a BITBLT into a series of one-line high operations that might be referred to as Line-BLTs. In this manner, a BITBLT may be simulated by the driver as a series of Line-BLTs.

21.3 BITBLT OPERATIONS IN TEXT MODE

BITBLT acceleration is available in VGA text modes, Text mode BITBLTs generally consist of moving only character and attribute data (in maps 0 and 1), while leaving the font data (in maps 2 and 3) alone. The BITBLT mask is set to prevent update to those maps. For this reason, planar (not packed) mode must be used, Similarly, the BITBLT mask can be set to move only character data, or only font data.

Each display memory location consists of four bytes: one character, one attribute, and two font plane bytes that are not part of the character but happen to fall in the same location as the character, but on maps 2 and 3. In planar mode, this is a space of eight pixels. Therefore, the source and destination of a character BLT must be multiples of 8. The X dimension is the number of character columns to be copied times 8, but the Y dimension is simply the number of character rows with no multiplying. The row pitch is set to the CPU address offset between character rows times 8.

21.4 USING BITBLT IN 16-BIT PER COLOR MODE

The BITBLT hardware can be used in 16-bit per color "High-color" mode with a few changes and a few limitations.

High-color BITBLTs should be performed in packed mode, remembering that each high-color pixel takes up two adjacent normal packed pixels. The BITBLT Source and Destination registers should point to the first byte of the respective regions. Generally, the values in these register pairs is double the corresponding values for normal packed mode.

In a right-to-left BITBLT in high-color mode, the source and destination values must point to the second byte of each region.

The BITBLT dimensions are twice the number of pixel columns, but the correct number of pixel rows. The Row Pitch Register contains eight times the number of bytes between rows on the screen. Linear source and destination operate normally.

Monochrome to color expansion is not, as a rule, usable. Neither is plane masking. Raster operations are available but often produce undesired results. Similarly, color transparency is rarely usable.

Pattern fills are available, however, the effective pattern is only 4 by 8 pixels. This may be usable where an 8 by 8 pattern is identical in the left and right halves.

Filled rectangles are available in two ways. First, where the desired fill color is the same in the high and low bytes (generally meaning all black or all white), rectangle fill can be used normally.

In the more general case of filling a rectangle with an arbitrary 16-bit color, the host should create a 4 by 8 pattern of the fill color and use pattern fills to create the rectangle.

Host I/O BITBLTs can operate normally by treating each 16-bit high-color pixel as two adjacent, aligned 8-bit packed mode pixels.

The user is cautioned regarding implementations that use one of the 16-bits in a high-color pixel as a switch between false color and high-color, as no mask exists to protect this flag bit during operations.

21.5 PATTERNS

The device has a special mode to accelerate the copying of 8 by 8 source patterns. In this mode, an 8 by 8 full-color or monochrome pattern can be repetitively applied to a large destination area in an efficient manner.

To perform a pattern copy, the host writes the 8 by 8 pattern to display memory in a linear fashion, depending on the current addressing mode, as defined below. The host then loads the *BITBLT Source* registers with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The *BITBLT Source Select* field of the BITBLT *Control* register must be set to source pattern.

To specify a monochrome pattern, the host must write a color pattern in the current (planar or packed) mode, and then use the control registers to specify a single plane of the source to be used.

In planar mode, the 8 by 8 source pattern must be stored in display memory in a 32-byte aligned area. It is stored as 64 consecutive pixels, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point

In packed mode, the 8 by 8 source pattern must be stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

BITBLT PATTERN STORAGE - MONOCHROME AND PLANAR MODES	
ADDRESS	**DISPLAY MEMORY CONTENTS**
	⇓
n- 8	(any data)
n* to n+7	All maps, top row of 8 by 8 pattern
n+ 8 to n+15	All maps, second row of 8 by 8 pattern
	⇓
n+ 56 to n+63	All maps, bottom row of 8 by 8 pattern
n+ 64	(any data)
	⇓
*'n' *must be a multiple of* 64	

BITBLT PATTERN STORAGE - PACKED MODES	
ADDRESS	**DISPLAY MEMORY CONTENTS**
	⇓
n-1	(any data)
n*	Top row of 8 by 8 pattern, left most pixel
n+1	Top row of 8 by 8 pattern, second pixel
	⇓
n+7	Top row of 8 by 8 pattern, right most pixel
n+8	Second row of 8 by 8 pattern, left most pixel
	⇓
n+63	Bottom row of 8 by 8 pattern, right most pixel
n+64	(any data)
*'n' *must be a multiple of 64*	

21.5.1 Using BITBLT For Arbitrary Sized Patterns

While the BITBLT hardware specifically accelerates 8 by 8 patterns, patterns of arbitrary size can be accelerated by use of the BITBLT, albeit to a lesser degree.

To copy an arbitrary size pattern to a destination region, the pattern should be stored in non-visible memory as a rectangular region, not a linear strip. With destination update enabled, one copy of the pattern should be BLTed to the top-left corner of the destination. The BITBLT source is then set to point to the pattern now in the destination region.

A series of BLTs is then performed, each doubling the width of the patterned area, simply by adjusting the X dimensions register. (The last of this series of BLTs fill out the destination region.)

A new series of BLTs is then performed, taking the horizontally complete pattern and doubling it in height each time. Note that destination update should be turned off, and the destination must be

set for each new BLT. (Again, the final BLT is probably not a double of the last one as it fills out the region.)

21.5.2 Patterns Built On-Screen

Normally, a pattern to be used in BITBLT is stored in a non-visible portion of display memory. This requires an aligned strip of 32 or 64 bytes to be available.

Where this is not available, it is often possible to still perform a pattern BLT by placing the pattern in the last line of the destination region. This can be done if the raster operation is a source copy (or source inversion), and if the destination region can accommodate the specified aligned strip on a single line. This technique works because each row of the pattern is read at the beginning of the row in which it is used, and the pattern wont be overwritten until it after it has been read for the last time.

Where a full strip is unavailable, the destination can be broken up into a series of line-BLTs, with a one line pattern, requiring only 4 or 8 aligned bytes, placed on each destination line before the BLT is started for that line. This method is substantially slower than other pattern BLTs.

An acceptable alternative might be to write the pattern in a visible portion of memory, first saving the underlying area and restoring it after the BLT. This momentary "borrowing" of a visible region might be visible to the user. This might be lessened by using the last line of the destination and saving and restoring only those regions that overhang the destination.

21.5.3 Use Of Patterns In Text Mode

Patterns may be in text mode to quickly set character and/or attribute bytes in a rectangular area to a common value. A pattern space must be created containing eight consecutive copies of the four-byte area consisting of the character, the attribute, and two "font map" bytes, all aligned to a 64-pixel boundary. The BITBLT map mask is then used to protect the font maps. This pattern should be created in off-screen memory.

If an off-screen pattern space is not available, one may be created on screen by loading an aligned group of 8 character/attribute pairs within the destination area, then pointing to that as the pattern source.

If the first character of the destination space happens to be on an 8-byte boundary (such as the conventional top of screen) then, as long as the destination is at least 8 characters wide, only the first character/attribute pair must be loaded, and the BITBLT operation "creates its own pattern" as it goes along. This also works if the destination is less than 8 characters wide, but is still wider than it is high.

If this is not possible, then the operation can be performed one character row at a time, loading the first character of each row to be used as an on-screen pattern.

Filled rectangles have a very limited application in text mode, but could be used to clear out a section of a font map or to set a section of a character or attribute map to all zeroes or all ones. Different values are not easily set in this manner because, in order to protect the font maps, planar mode, rather than packed mode, must be used.

21.6 SUPPORT FOR KANJI CHARACTERS

The BITBLT hardware can support generation of Kanji characters very efficiently. The common implementation of Kanji characters calls for a character box of 28 by 28 pixels with five possible scoring lines for each character box.

Kanji characters are best drawn in two passes. The first pass draws the characters while erasing any old ones. The second pass adds the score lines.

The Kanji font should be stored in non-visible display memory. Since the font is monochrome, multiple characters can be stored one per plane, one under the other. The color compare registers are used to switch between banks of characters stored on different planes.

A group of 32 special characters is generated along with the font, consisting of all possible combinations of scoring lines.

The dimension registers are loaded with the size of the character box. Foreground and background

colors are set as desired. Destination update and quick BLTs are enabled.

For each character row, the source destination registers are set to the beginning of the row, and monochrome expansion is enabled. A series of quick BLTs is performed, one per character, by loading the source address of each desired character. If a font-plane change is required, this is done before loading the source registers, which start the BLT automatically.

After the character row is complete, the destination registers are reset to the beginning of the row. Monochrome transparency is enabled, and a second pass is done over the character drawn to add score lines as needed, one special score-line character per Kanji character.

Where a Kanji character requires no score lines, either a BLT of a special "blank" score-line character is performed, or the destination registers may simply be updated to skip the position. The driver may add additional intelligence to skip entire character rows or parts where score lines are not required.

21.7 READING AND WRITING THE VGA READBACK LATCHES

The 32-bit VGA readback latches may be written and read by the host. This ability is primarily useful in context switching.

To write the contents of the VGA readback latches, the host may set up a system-to-display memory transfer with a width and height of 1 pixel. The BITBLT Mask is then set to all zeroes to prevent destination update. The host then starts the operation and word pointer is reset on power-up and whenever a BITBLT operation begins or ends.

This technique is guaranteed only for this revision of the device, and may or may not work on future revisions.

21.8 CHANGING MONOCHROME SOURCES TO COLOR

When the source of a BITBLT operation is monochrome, each'0' in the source region is replaced with the specified background color, while each'1' is replaced with the foreground color. All other processing options, including masks and raster operations remain active and operate on the expanded colors.

When the source is specified as a fixed color, the entire destination is filled with the foreground color, subject to masks, raster operations, and destination transparency. Filled rectangles are generated in this manner.

When a monochrome source is generated by the color comparators, color destination transparency is generally not available, since the transparency color registers are in use.

21.9 EXTRACTING MONOCHROME DATA

Monochrome data can be extracted from color data read from display memory by the color comparators. Data so extracted is replicated to each plane or map as if it was so read from the memory.

When extracted, monochrome data is usually extracted from color data in display memory. However, when the BITBLT source is the system I/O location, monochrome data can be extracted in the same way.

To extract a single plane from a color source field, load the *BITBLT Transparency Color* register with 'FFF' (all ones), and load the *BITBLT Transparency Mask* register with a '0' in the map or plane position to be extracted, and load a '1' in all other positions. (As described in the section on color transparency, one of the two fields of each of these registers is actually a don't care at any given time.)

Monochrome data is usually extracted as a specific bit of each 4- or 8-bit pixel. However, the color comparators can be used to extract any color, or any maskable group of colors, into the monochrome color '1', with all other colors returning a monochrome '0'.

When the *Monochrome Transparency* bit is set in the *BITBLT Control* register, monochrome source pixels of '0' do not affect the background, regardless of the selected raster operation.

The *Transparency Enable* and *Polarity* bits in this register have no effect on monochrome data extraction.

21.10 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually "transparent", with the rest being "opaque". Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color since it does not change the destination when ORed with it.

21.11 DRAWING FILLED RECTANGLES

Color destination transparency is supported on this device, in addition to the more limited monochrome transparency described elsewhere.

Filled rectangles can be drawn very efficiently by the BITBLT hardware. A filled rectangle is simply a BITBLT with a source of a fixed color. To draw a filled rectangle, the host sets the *Source Format* field in the *BITBLT Control* register to "fixed color", and the *Foreground Color* register to the desired fill color. A source address is not required. All other BITBLT options are available normally.

21.12 SYSTEM MEMORY TO DISPLAY MEMORY OPERATION

To copy data from system memory to display memory, the host may specify the source of a BITBLT as a system I/O location rather than display memory. In this case, display memory reads come from the 32-bit readback latch written by the host.

After starting the BITBLT operation, the host writes a series of doublewords to the readback latch. The 32-bit register is accessed by two consecutive writes to the 16-bit BITBLT I/O port, with the low order word of this register written first. Also, this port may be accessed by two 8-bit writes as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a source read is required and data from the host is unavailable, the WD90C24A/A2 suspends the BITBLT operation until the data becomes available. Similarly, when the host attempts to write the register before the previous data in it has been processed, the WD90C24A/A2 holds off the host.

Conceptually, the 32-bits written by the host exactly replace the 32-bits that would have been read from display memory. Just like the destination, the source may have any alignment. The two or three low-order bits (Packed or Planar Mode) of the BITBLT Source Low Register (Index 2) specify the alignment of the source region. The other bit of the BITBLT Source Low Register may have any value. That is, the pixel of the source word pointed to by those low-order bits corresponds to the first pixel of the destination.

NOTE

Source writes from the host are always performed in 32-bit groups. However, the data are written to a 16-bit port. Therefore, the host must always perform two consecutive 16-bit I/O writes to the port even when the remaining width is less than 4 or 8 bits.

Similar to display memory, no source doubleword from the host may straddle two lines of the destination.

21.13 DISPLAY MEMORY TO SYSTEM MEMORY OPERATIONS

To copy data from display memory to system memory, the host may specify the destination of a BITBLT as a system I/O location rather than display memory. In this case, display memory writes are replaced by writes to a 32-bit register read by the host.

This 32-bit register is accessed by two consecutive reads of the 16-bit BITBLT I/O port. The low-order word of this register id read first. Also, this port may be accessed by two 8-bit reads, as long as the even port is accessed first. At the beginning of each BITBLT operation, the internal pointer is reset to the low-order word.

When a destination write is required and the host has not read data from the previous write, the WD90C24A/A2 suspends the BITBLT operation until the host catches up. Similarly, when the host attempts to read the register before data are available, the WD90C24A/A2 holds off the host.

Conceptually, the 32-bits read by the host exactly match the 32-bits that would have been written to the display memory. Unlike outputting to display memory, the destination is always doubleword aligned. That is, the first pixel of the source corresponds to the first pixel of the destination.

NOTE

Source reads by the host are always performed in 32-bit groups. However, the data are read from a 16-bit port. Therefore, the host must always perform two consecutive 16-bit I/O reads from the port, even when less that 32-bits remain on the current line.

Similar to display memory, no destination doubleword to the host may straddle two lines of the source.

21.14 SYSTEM MEMORY TO DISPLAY MEMORY TRANSFERS WITH COLOR EXPANSION

The host may transfer monochrome data from system memory to display memory and, in the process, expand it to any two colors or any one color plus transparent.

To accomplish this, the host set the BITBLT Source Select field in the BITBLT Control Register (Index 0) to "System I/O Location" and the BITBLT Source Format field to "Monochrome From Host." If transparency is desired, the Monochrome Transparency bit is also set. Also, the BITBLT Foreground and Background Color Registers (Index A and B) may be set.

The host then issues a series of 16-bit I/O writes to the BITBLT I/O port which are expanded to eight 4-bit pixels. The remaining eight high-order bits are ignored. In Packed Mode, the four low-order bits are expanded to four 8-bit pixels and the remaining 12-bits are ignored.

The low-order bits of the BITBLT Source Register (Index 2) work as any other system-to- display memory transfers.

No source word may straddle two lines of the destination. All other BITBLT options work normally in this mode.

21.15 BITBLT CONTROL AND STATUS

21.15.1 BITBLT Control, Part 1, Index 0

INDEX NUMBER	BITBLT REGISTER NAME
0	Control - Part 1
1	Control - Part 2
2	Source Low/XSTEP
3	Source High/RSTEP
4	Destination Low1
5	Destination High1
6	Dimension X/Delta-X
7	Dimension Y/Delta-Y
8	Row Pitch
9	Raster Operation
A	Foreground Color
B	Background Color
C	Transparency Color
D	Transparency Mask
E	Map and Plane Mask

1. All or part of these registers can change automatically.
2. The BITBLT ports (23C4 and 23C5) are accessed as extended registers. Refer to Extended Register Access, Section 17.

BIT D11	BITBLT ACTIVATION STATUS
0	Abort BITBLT/ BITBLT completed
1	Begin BITBLT / BITBLT in progress

Bit 11 is reset automatically when BITBLT is completed. Writing a '0' to this bit aborts a BITBLT operation in progress

BIT D10	BITBLT DIRECTION
0	BITBLT direction is top to bottom and left to right

BIT D10	BITBLT DIRECTION
1	BITBLT direction is bottom to top and right to left

BITS		BITBLT ADDRESS MODE
D9	D8	
0	0	Planar mode (includes mono-chrome modes)
0	1	Packed mode (includes text and 256-color modes)
1	0	Reserved for future expansion
1	1	Reserved for adder test

BIT D7	BITBLT DESTINATION LINEARITY
0	Destination area is rectangular
1	Destination area is linear

BIT D6	BITBLT SOURCE LINEARITY
0	Source area is rectangular
1	Source area is linear

BITS		BITBLT DESTINATION SELECT
D5	D4	
0	0	Destination is screen memory
0	1	Destination is system memory
1	0	Destination is system I/O location
1	1	Reserved for future expansion

BITS		BITBLT SOURCE FORMAT
D3	D2	
0	0	Source format is color
0	1	Source format is monochrome from color comparators
1	0	Source format is fixed color (filled rectangle)

BITS		BITBLT SOURCE FORMAT
D3	D2	
1	1	Source format is monochrome from host

BITS		BITBLT SOURCE SELECT
D1	D0*	
0	0	Source is screen memory
0	1	Source is system memory
1	0	Source is system I/O location, 32-bits
1	1	Reserved for future expansion

21.15.2 BITBLT Control, Part 2, Index 1

BITS	FUNCTION
15:12	0001(Index)
11	Enable Line Drawing
10	BITBLT Interrupt Enable
9	X or Y Major
8	Y Direction
7	BITBLT Quick Start
6	BITBLT Update Destination
5:4	BITBLT Pattern Select
3	BITBLT Monochrome Transparency
2	BITBLT Transparency Polarity
1	Reserved, must be 0
0	BITBLT Transparency Enable

BIT D11	BITBLT ENABLE LINE DRAWING
0	Enable Another BITBLT Function
1	Enable Line Drawing

BIT D10	BITBLT INTERRUPT ENABLE
0	Do not interrupt on completion of BIT-BLT

BIT D10	BITBLT INTERRUPT ENABLE
1	Interrupt on completion of BITBLT

BIT D9	BITBLT X OR Y MAJOR*
0	X Major (Slope is less than 1)
1	Y Major (Slope is greater than 1)
*This bit is valid only when bit 11 is set to 1.	

BIT D8	BITBLT Y DIRECTION*
0	Top to Bottom
1	Bottom to Top
*This bit is valid only when bit 11 is set to 1.	

BIT D7	BITBLT QUICK START
0	BITBLT starts only when explicitly enabled
1	BITBLT starts automatically when destination* register is written
*or source register, if destination update is enabled	

BIT D6	BITBLT UPDATE DESTINATION
0	Do not update destination on completion of BITBLT
1	Update destination on completion of BITBLT

BITS		BITBLT PATTERN SELECT
D5	D4	
0	0	Patterns are not used
0	1	8 by 8 patterns are used for source
1	0	Reserved for future use
1	1	Reserved for future use

BIT D3	BITBLT MONOCHROME TRANSPARENCY
0	Monochrome transparency is not enabled
1	Monochrome transparency is enabled

BIT D2	BITBLT TRANSPARENCY POLARITY
0	Matching pixels are transparent
1	Matching pixels are opaque

BIT D1	BITBLT TRANSPARENCY SELECT
0	Destination pixels control transparency
1	Source pixels control transparency

BIT D0	BITBLT TRANSPARENCY ENABLE
0	Transparency is not enabled
1	Transparency is enabled

21.16 AUTOMATIC DESTINATION UPDATE

A host doing multiple BITBLTs need only update those registers that change from one BITBLT to the next. Most BITBLT registers never change unless written by the host. The exceptions to this rule are the two BITBLT Destination registers and the status bit in the BITBLT Control register.

When the BITBLT Update Destination bit in the BITBLT Control register is set, the BITBLT Destination registers are automatically updated at the end of each BITBLT operation to point to the rectangular region immediately to the right of the previous destination region. This is specifically aimed at improving text output operations. When the destination area is specified as linear rather than rectangular, the destination registers points to the location immediately past the previous destination area.

21.17 QUICK START MODE

When the BITBLT Quick Start bit is set in the BITBLT Control register, then BITBLT starts automatically as soon as the BITBLT Destination Low register is written, unless automatic destination update is enabled for BITBLT, in which case the BITBLT starts automatically when the BITBLT Source Low register is written.

This mode permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control register operates as they were last written, and the BITBLT Activation bit is physically set and can be read back normally.

21.18 ABORTED BITBLT

The host may abort a BITBLT in progress by resetting the BITBLT Activation bit in the BITBLT Control register. The operation then terminates within a few memory clocks.

When a BITBLT is aborted, the destination registers are generally unchanged, unless the operation was coincidentally aborted near the very end.

Aborted BITBLTs cannot generally be continued, since it is unknown what remains to be copied, and even if it were known, the region remaining to be copied might not be rectangular. Further, BITBLTs that use certain logical operations or transparency settings might not produce correct results if simply repeated with the original parameters.

21.19 REGISTER ACCESS

If the Auto-Increment Disable bit in the Index Control register is reset, consecutive reads to the Register Access port return consecutively indexed registers within the same register block. Registers are read in ascending order through register F (the 16th register in the block), followed by register 0 and cycling indefinitely as long as reads continue. Registers that do not exist return unknown data when read.

If the Auto-Increment Disable bit is set, consecutive reads return the same indexed register.

22.0 EMBEDDED CLOCK GENERATOR

This section describes the Embedded Clock Generator that is capable of providing various display memory clock (MCLK) and video dot clock (VCLK) frequencies.

22.1 FEATURES

The main features of the Embedded Clock Generator are:

- Dual clock generator based on the Western Digital WD90C65 VGA Clock Generator
- Generates 15 preprogrammed video clock frequencies (including 25.175 MHz and 28.322 MHz) that are derived from a 14.31818 MHz system clock reference frequency
- Generates 8 preprogrammed memory clock frequencies
- External PCLK mode allows users to bypass the internal PCLK to input a video clock and memory clock (EXCKEN = 1)
- With the WD90C24A/A2 in System Powerdown mode, the clock generator is placed in a low-current state
- The AVDD1 analog power supply to the clock generator can be powered off when the system is in Deep Sleep mode

22.2 DESCRIPTION

The Embedded Clock Generator is a dual clock synthesizer capable of generating two different internal clock frequencies under firmware control. One clock frequency is for the display memory clock, and the other frequency is for the video dot clock. The operating frequencies are derived from a 14.31818 MHz system clock input available in IBM PC/XT/AT and Personal System/2 computers.

The VCLK may be one of 15 internally generated frequencies as shown in Table 22-1. The VCLK frequency is selected via Paradise Extended Register PR68 (3C5h, index 31h) bits [4:3] and VGA Miscellaneous Output Register 3C2h bits [3:2] (Write Only).

NOTE

In order to change the setting of PR68, it must be unlocked by setting PR72 (3C5.35h) to 5xh and PR11 (3?5.2Ah) bit 2 to 0.

The VCLK is also user-programmable in a range from 25.057 MHz to 85.014 MHz, in 447.443 KHz increments. The user can also enter an external PCLK mode that bypasses the clock generator by generating VCLK and MCLK from primary chip inputs. The embedded clock generator is held in low-current mode during external clock mode.

VSEL				FREQUENCY CODE[1]	VCLK FREQUENCY (MHz)
PR68		3C2h			
BIT 4	BIT 3	BIT 3	BIT 2		
0	0	0	0	67	29.979
0	0	0	1	173	77.408
0	0	1	0	N	See Note 2
0	0	1	1	179	80.092
0	1	0	0	n/a	25.175
0	1	0	1	n/a	28.322
0	1	1	0	n/a	65.000
0	1	1	1	n/a	36.000
1	0	0	0	89	39.822
1	0	0	1	112	50.114
1	0	1	0	94	42.060
1	0	1	1	99	44.297
1	1	0	0	n/a	31.500
1	1	0	1	n/a	35.501
1	1	1	0	168	75.166
1	1	1	1	112	50.114

NOTES:

1. Refer to Section 22.2.2.
2. Selects programmable frequency via PR69.

TABLE 22-1. VCLK SELECTION

The MCLK may be one of 8 internally generated frequencies, which are selected via PR68 (3C5h, index 31h) bits [2:0] as shown in Table 22-2.

MSEL			FREQUENCY CODE[1]	MCLK FREQUENCY (MHz)
PR68				
BIT 2	BIT 1	BIT 0		
0	0	0	123	55.035
0	0	1	74	33.111
0	1	0	134	59.957
0	1	1	84	37.585
1	0	0	89	39.822
1	0	1	99	44.297
1	1	0	106	47.429
1	1	1	110	49.219

NOTE:
1. Refer to Section 22.2.2.

TABLE 22-2. MCLK SELECTION

The various VCLK and MCLK operating frequencies are achieved by multiplying the 14.31818 MHz input frequency by a factor of N/32. External filter components are attached to the VCAP and MCAP pins for the internal phase lock loops.

22.2.1 System Bus Interface

The only system bus interface used by the clock generator is the CKIN pin (14.31818 MHz).

22.2.2 Firmware Interface

The clock generator receives inputs from three internal registers. VGA register 3C2h bits [3:2] hold the VSEL[1:0] bits. These bits allow for compatibility in switching between standard frequencies. Paradise Register (PR68) 3C5h, index 31h, bits [4:3] hold the VSEL[3:2] bits. The MSEL[2:0] bits are held by the same 3C5h, index 31h register in bits [2:0].

NOTE

In order to change the setting of PR68, it must be unlocked by setting PR72 (3C5.35h) to 5xh and PR11 (3?5.2Ah) bit 2 to 0..

Paradise Register PR69 (3C5h, index 32h) holds the 8-bit N value of the user-programmable VCLK. The N value is calculated by dividing the desired frequency (in MHz) by 0.447443 MHz. The resulting value must be rounded to give an integer value, which is loaded into Paradise Register PR69. At reset the default frequencies are 25.175 Mhz for VCLK and 44.297 Mhz for MCLK.

22.2.3 Analog Interface

MCAP and VCAP are analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. Figure 22-1 shows the filter circuit. The capacitor tolerances are ±20%. The resistor tolerance is ±2%.

22.2.4 External Clock Mode

Setting EXCKEN high enables the external clock mode, which allows the user the option to bypass the internal clock generator. The following list defines the signal function for internal and external clock modes.

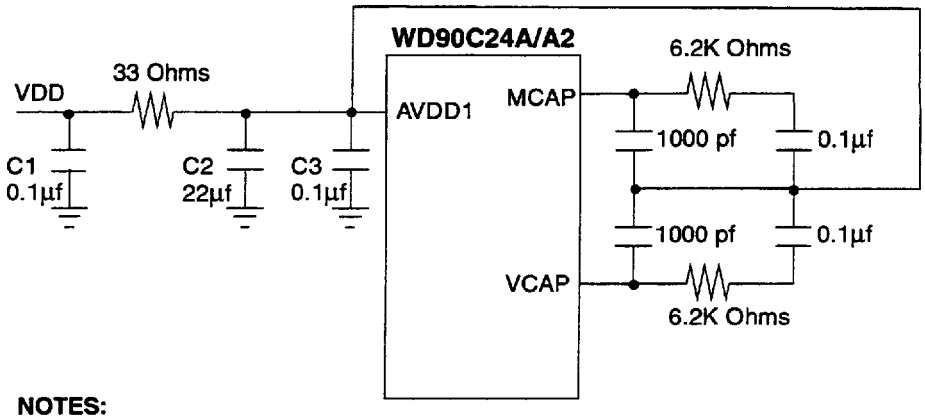
SIGNAL		CLOCK MODES	
PIN NO.	NAME	INTERNAL PCLK	EXTERNAL PCLK
161	EXCKEN	Set to 0	Set to 1
103	XMCLK	Not Used	MCLK
170	CKIN	Reference Clock (14.318Mhz)	VCLK
168	VCLK1	FPUSR1	VCLK1
106	VCLK2	Not Used	VCLK2

TABLE 22-3. SIGNAL FUNCTIONS FOR INTERNAL AND EXTERNAL CLOCK MODES

22.2.5 ISO Support

For ISO monitor operation, unlock PR68 (3C5h, index 31h) by writing 5xh to PR72 (3C5h, index 35h), and then write 11b to PR68 bits [4:3].

Relock PR68 by setting PR72 to any value other than 5xh.



NOTES:
1. C3 should be placed as close as possible to the AVDD1 pin.
2. The 33 Ohm resistor in the power supply filter can be replaced with a ferrite bead.
3. Place the two 1000 pf capacitors as close as possible to the WD90C24A/A2.

FIGURE 22-1. CLOCK GENERATOR CONNECTIONS

23.0 INTERNAL RAMDAC

The WD90C24A/A2 supports an internal RAMDAC (Random Access Memory Digital to Analog Converter) for CRT display. Figure 23-1 shows how the WD90C24A/A2 is connected to a CRT. External components required to connect the internal RAMDAC are listed in Table 23-1.

DESIGNATOR	DESCRIPTION
C1, C5	0.1 µF Ceramic Capacitor
C6	10 µF Tantalum Capacitor
L1	Ferrite Bead
R1-R3	150 Ohm 1% Metal Film Resistor
R4	1 Kohm 5% Resistor
RSET	~11 Kohm 1% Metal Film Resistor (Refer to Section 26.2)
Z1	Voltage Reference (1.235V)

TABLE 23-1. RAMDAC EXTERNAL COMPONETS

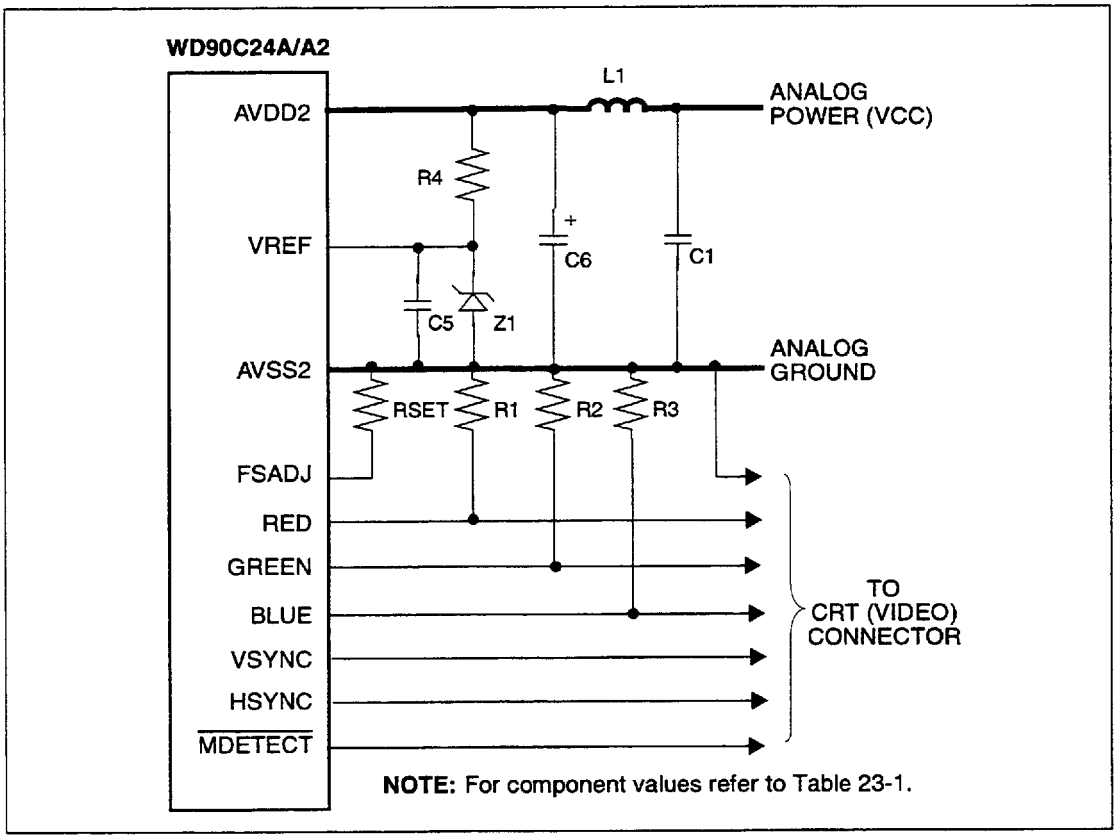


FIGURE 23-1. INTERNAL RAMDAC CONNECTIONS TO A CRT

24.0 WD90C24A/A2 CONFIGURATION REGISTERS

Memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data, CNF[31:0], at system power-on or reset. External pull-down resistors are used to set the state of the internal configuration registers. The resistors cause bits to be set in internal registers, which then establish the operating configuration at start up. Some configuration bits are contained in non-writable registers while others can be modified after start up. The non-writable bits set features such as bus architecture that are not modified after start up. Configuration bits CNF[15:12], CNF10, and CNF0 can be changed by software after power-up. The memory data lines, AMD[15:0] and BMD[15:0], are all internally pulled up by 100 Kohm resistors.

Table 24-1 lists the WD90C24A/A2 Configuration Registers by the register number, and then provides the signal pin name and the CNF register function. Table 24-2 lists the register bit functions.

CONFIGURATION (CNF) REGISTER	SIGNAL NAME	REGISTER FUNCTION
0	AMD0	BIOS ROM Mapping
1	AMD1	Reserved
2	AMD2	Works with CNF17 to determine the bus architecture, refer to Table 3-1.
3	AMD3	Video Clock Source Control
7:4	AMD7:AMD4	General Purpose Status
8	AMD11	General Purpose
9	AMD9	46E8h/3C3h Select I/O Port for Wake-up
10	AMD10	Reserved
11	AMD8	Select Operating Voltage
12	AMD12	Reserved
13	AMD13	Used with CNF14 and CNF 16 to determine the memory mode configuration, refer to Table 4-1.
14	AMD14	Used with CNF13 and CNF 16 to determine the memory mode configuration, refer to Table 4-1.
15	AMD15	486 Host Indicator Bit
16	BMD0	Used with CNF13 and CNF 14 to determine the memory mode configuration, refer to Table 4-1.
17	BMD1	Works with CNF2 to determine the architecture, refer to Table 3-1.
18	BMD2	LCD Panel Select, Refer to PR18, Bit 0
19	BMD3	LCD Panel Select, Refer to PR18, Bit 1
20	BMD4	Local Bus: Select 2x clock to support Intel S-series 486 processor
21	BMD5	Reserved
27:22	BMD[11:6]	Configuration Bits for VLBI Register 2DF1h [5:0]
31:28	BMD[15:12]	Configuration Bits for VLBI Register 2DF0h [7:4]

TABLE 24-1. CONFIGURATION REGISTERS

SIGNAL NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD0	R/W	0*	PR1[0]	0 = (No Pulldown) Enable BIOS ROM
				1 = (Pulldown) BIOS ROM is Mapped Out
AMD1	R	1*	PR1[1]	0 = (No Pulldown) Reserved
				1 = (Pulldown) Reserved
AMD2	---	2	---	0 = (Pulldown) Works with CNF17 to determine the bus architecture, refer to Table 3-1.
				1 = (No Pulldown) Works with CNF17 to determine the bus architecture, refer to Table 3-1.
AMD3	---	3	---	0 = (Pulldown) Select VCLK1 and VCLK2 as Input
				1 = (No Pulldown) Select VCLK1 and VCLK2 as Output
AMD4	R	4	PR5[4]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD5	R	5*	PR5[5]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD6	R	6*	PR5[6]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD7	R	7*	PR5[7]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD8	---	11	---	0 = (Pulldown) Force All Voltage Detectors to the value of the contents in PR70[4:0], regardless of the setting of PR70 Bit 5. This value is 5 VDC at power-on and reset.
				1 = (No Pulldown) Allow Automatic Voltage Detect
AMD9	---	9	---	0 = (Pulldown) 3C3h I/O Port. VGA wake-up is enabled by setting Port 3C3h Bit 0 to 1.
				1 = (No Pulldown) 46E8h I/O Port. VGA wake-up is enabled by using I/O Ports x102h and 46E8h.
AMD10	---	10	---	Reserved
AMD11	R	8*	PR5[3]	0 = (No Pulldown) General Purpose Status Bit
AMD12	---	12	---	Reserved
AMD13	R/W	13	PR11[5]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1.

TABLE 24-2. CONFIGURATION REGISTER BITS, CNF[31:0]

SIGNAL NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD14	R/W	14	PR11[6]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1.
AMD15	---	15	---	0 = (Pulldown) Select 16-Bit Host Processor
				1 = (No Pulldown) Select 32-Bit Host Processor
BMD0	R	16	PR11[7]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1
BMD1	R	17	PR11[4]	0 = (Pulldown) Works with CNF2 to determine the bus architecture, refer to Table 3-1.
				1 = (No Pulldown) Works with CNF2 to determine the bus architecture, refer to Table 3-1.
BMD2	R/W	18	PR18[0]	0 = (Pulldown)
				1 = (No Pulldown) LCD Panel Select, refer to PR18, Bit 0
BMD3	R/W	19	PR18[1]	0 = (Pulldown)
				1 = (No Pulldown) LCD Panel Select, refer to PR18, Bit 1
BMD4	---	20	---	0 = (Pulldown) Select 2x Local Bus Clock
				1 = (No Pulldown) Select 1x Local Bus Clock
BMD5	---	21	---	Reserved
BMD[11:6]	---	27:22	2DF1[5:0]	0 = (Pulldown)
				1 = (No Pulldown) Configuration Bits for VLBI Register 2DF1[5:0]
BMD[15:12]	---	31:28	2DF0[7:4]	0 = (Pulldown)
				1 = (No Pulldown) Configuration Bits for VLBI Register 2DF0[7:4]
NOTES: * A pulldown resistor sets these bits to 1.				

TABLE 24-2. CONFIGURATION REGISTER BITS, CNF[31:0] (Continued)

25.0 I/O MAPPING

This section provides the following information:

- A Description of WD90C24A/A2 I/O Mapping
- A list of I/O Mapping groups (Table 25-1)
- An I/O Mapping Group Diagram (Figure 25-2)

The I/O Mapping allows the WD90C24A/A2 to enter a test mode where all of its pins are divided into groups with inputs and outputs. The path for each group goes from the input pin(s), through the WD90C24A/A2, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table 25-1 lists each group (path) with its corresponding input and output pins.

The WD90C24A/A2 must meet the following requirements in order to enter the I/O Mapping test mode.

- $\overline{\text{MEMR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CNF(2) is HIGH
- RESET is ACTIVE HIGH then goes LOW
- $\overline{\text{PDOWN}}$ is HIGH

If both $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in ISA(AT) machines and a reserved condition in the PS/2 machines. AMD2 high ensures that WD90C24A/A2 is in ISA(AT) mode.

Reset controls a transparent latch as shown in Figure 25-1.

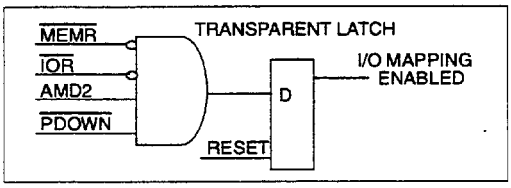


FIGURE 25-1. ENABLING I/O MAPPING ON THE WD90C24A/A2

Figure 25-2 provides a diagram of the I/O mapping groups (paths).

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
1, 16	BMD0, BMD9	201	AMA0
3, 14	BMD1, BMD10	203	AMA1
8, 12	BM3, BMD11	205	AMA2
6, 9	BMD2, BMD12	207	AMA3
7, 11	BMD13, BMD4	208	AMA4
4, 13	BMD14, BMD5	206	AMA5
2, 15	BMD15, BMD6	204	AMA6
17, 52	BMD7, PD16	202	AMA7
18, 51	BMD8, PD17	200	AMA8
42, 47	PD24, PD20	198	$\overline{\text{ARAS}}$
41, 46	PD25, PD21	196	$\overline{\text{AWE}}$
40, 45	PD26, PD22	24	$\overline{\text{BRAS}}$
39, 44	PD27, PD23	22	$\overline{\text{BWE}}$
20, 23	$\overline{\text{BCASL}}$, $\overline{\text{BCASH}}$	25	$\overline{\text{BOE}}$
38	PD28	172	VLBICS
37	PD29	165	PNLOFF
53, 115	SD15, SD5	123	STN13
54, 114	SD14, SD4	124	STN12
55, 112	SD13, SD3	126	STN11
56, 111	SD12, SD2	127	STN10

TABLE 25-1. I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
58, 110	SD11, SD1	128	STN9
59, 109	SD10, SD0	129	STN8
71, 75, 78	$\overline{\text{IOCS16}}$, IRQ, $\overline{\text{ZWST}}$	119	XSCLK
61, 74	SD8, ALE	120	$\overline{\text{WPLT}}$
63, 85, 151	SLA17, SA5, SA29	137	VLD1
64, 86, 152	SLA18, SA6, SA30	136	VLD2
65, 87, 153	SLA19, SA7, SA31	135	VLD3
66, 89, 99	SLA20, SA8, $\overline{\text{IOW}}$	134	VUD0
67, 90, 98	SLA21, SA9, $\overline{\text{IOR}}$	133	VUD1
68, 91, 101	SLA22, SA10, $\overline{\text{MEMW}}$	132	VUD2
69, 92, 100	SLA23, SA11, $\overline{\text{MEMR}}$	131	VUD3
60, 70, 72	SD9, CLK486, $\overline{\text{MEMCS16}}$	77	$\overline{\text{IOCHRDY}}$
73, 117	$\overline{\text{SBHE}}$, SD7	121	$\overline{\text{RPLT}}$
76, 116	$\overline{\text{EIO}}$, SD6	122	STN14
80, 93, 146	SA0, SA12, SA24	144	FR

TABLE 25-1. I/O MAPPING GROUPS (Continued)

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
81, 94, 147	SA1, SA13, SA25	143	FP
82, 95, 148	SA2, SA14, SA26	142	LP
83, 95, 149	SA3, SA15, SA27	140	XSCLK
84, 97, 150	SA4, SA16, SA28	139	VLD0
161	EXCKEN	173	VSYNC
166	$\overline{\text{REFRESH}}$	168	FPUSR1, VCLK1
170	CKIN	167	FPUSR0
171	$\overline{\text{EBROM}}$, $\overline{\text{REFLCL}}$	172, 174	$\overline{\text{LCDENA}}$, HSYNC
175	PCLK	106	VCLK2
177, 190	AMD0, AMD9	28	BMA0
179, 188	AMD1, AMD10	30	BMA1
183, 186	AMD3, AMD11	32	BMA2
181, 184	AMD2, AMD12	34	BMA3
182, 185	AMD13, AMD4	35	BMA4
180, 187	AND14, AMD5	33	BMA5
178, 189	AMD15, AMD6	31	BMA6
50, 191	PD18, AMD7	29	BMA7
49, 192	PD19, AMD8	27	BMA8
194, 197	$\overline{\text{ACASL}}$, ACASH	199	$\overline{\text{AOE}}$

TABLE 25-1. I/O MAPPING GROUPS (Continued)

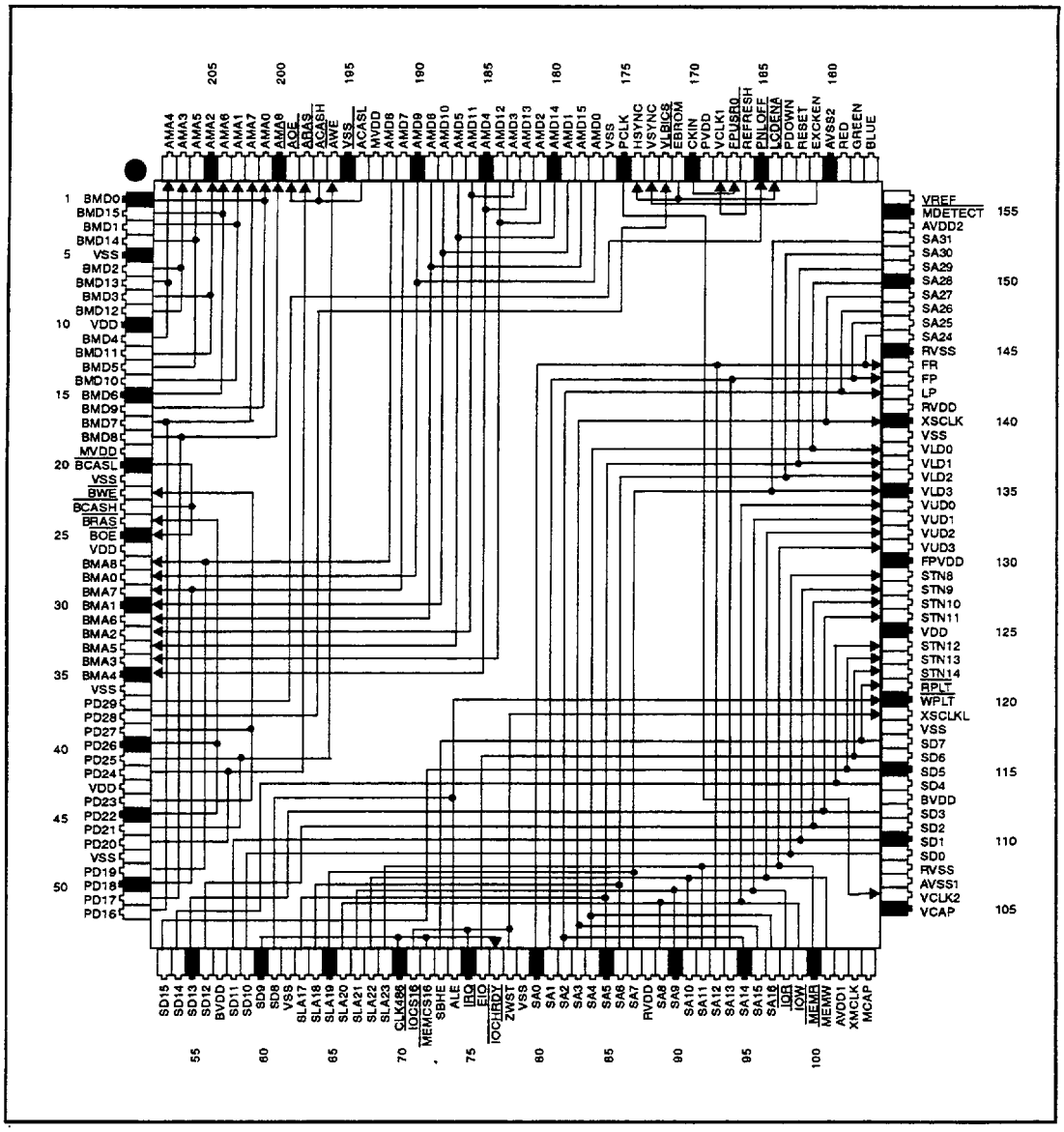


FIGURE 25-2. I/O MAPPING GROUP DIAGRAM

26.0 USE OF FEATURES

The section describes how to use the following WD90C24A/A2 features:

- Panel Connections
- CRT Connections
- Mapping RAM Programming
- External RAMDAC Connections
- Video Signature Analyzer
- Auxiliary Video Extender (AVE) Mode
- Power-down Management
- Power Distribution
- Recommended Power Supply Isolation and Decoupling
- Panel Protection
- Register Shadowing
- Activating CRT and Flat Panel Displays

26.1 PANEL CONNECTIONS

The WD90C24A/A2 supports several different types of flat panel designs. A combination of Paradise Register and configuration bit settings are used to connect the WD90C24A/A2 to each flat panel type (refer to Tables 14-1 and 23-2).

The following figures are included in this section:

- Simultaneous CRT and Monochrome LCD Panel Interface (Figure 26-1)
- Multiplexed Color STN 8/16-Bit Panel Interface (Figure 26-2)
- Simultaneous CRT and 9-Bit Color TFT LCD Panel Interface (Figure 26-3)
- Simultaneous CRT and 12-Bit Color TFT LCD Panel Interface (Figure 26-4)
- Simultaneous CRT and 18-Bit Color TFT LCD Panel Interface (Figure 26-5)
- Monochrome Dual Panel LCD Data Organization (Figure 26-6)
- Single-Panel Multiplexed Color STN LCD Data Organization (Figure 26-7)
- Example of CRT Connections showing VREF and FSADJ Circuits (Figure 26-8)
- Monitor Detection Circuit for Internal RAMDAC (Figure 26-9)
- Power Distribution Block Diagram (Figure 26-11)

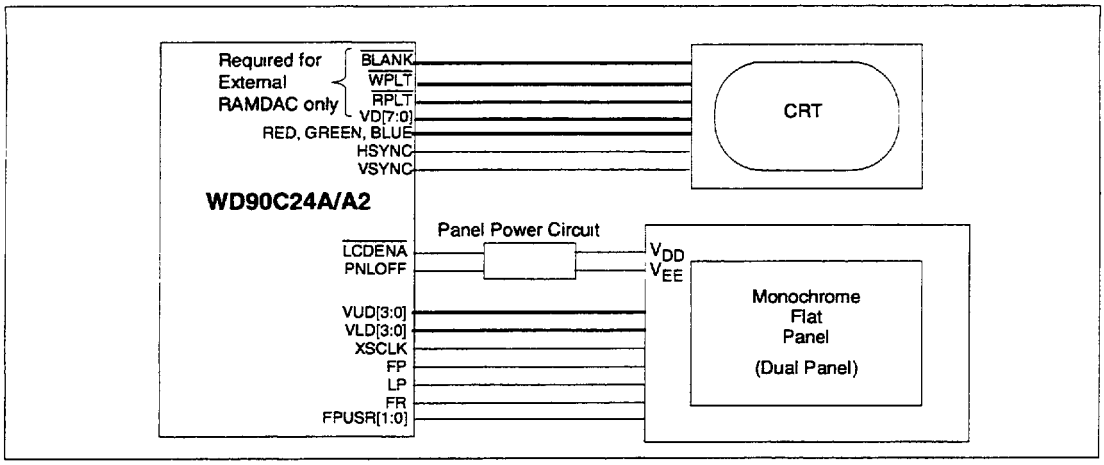


FIGURE 26-1. SIMULTANEOUS CRT AND MONOCHROME LCD PANEL INTERFACE

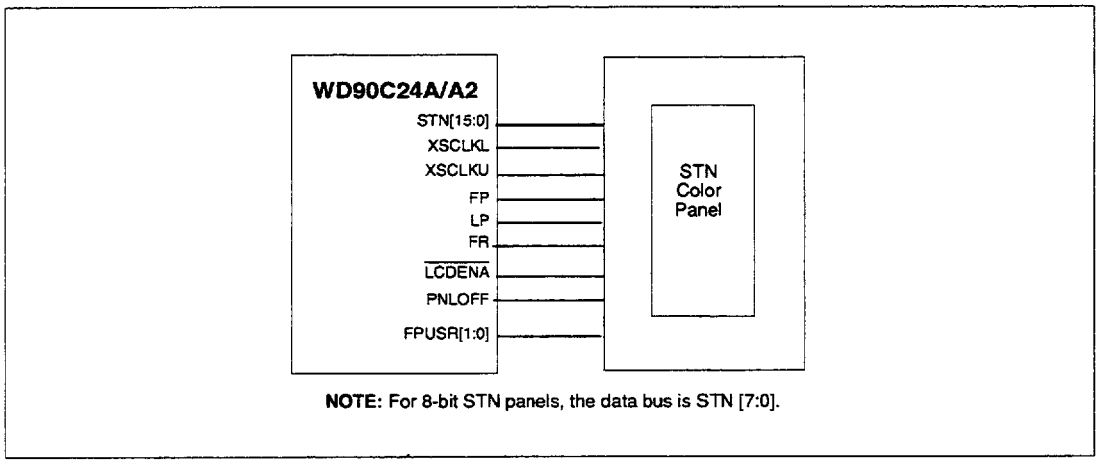


FIGURE 26-2. MULTIPLEXED COLOR STN 8/16-BIT PANEL INTERFACE

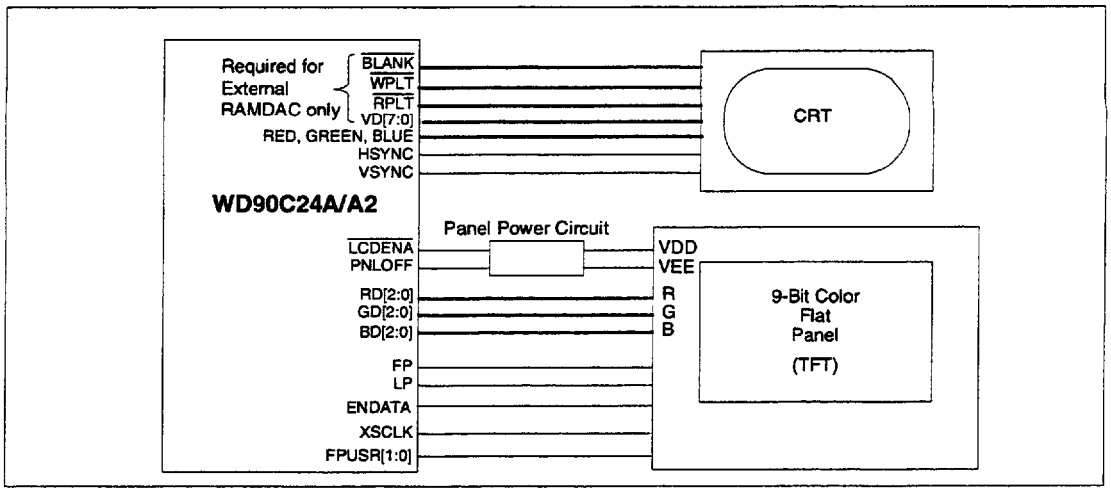


FIGURE 26-3. SIMULTANEOUS CRT AND 9-BIT COLOR TFT LCD PANEL INTERFACE

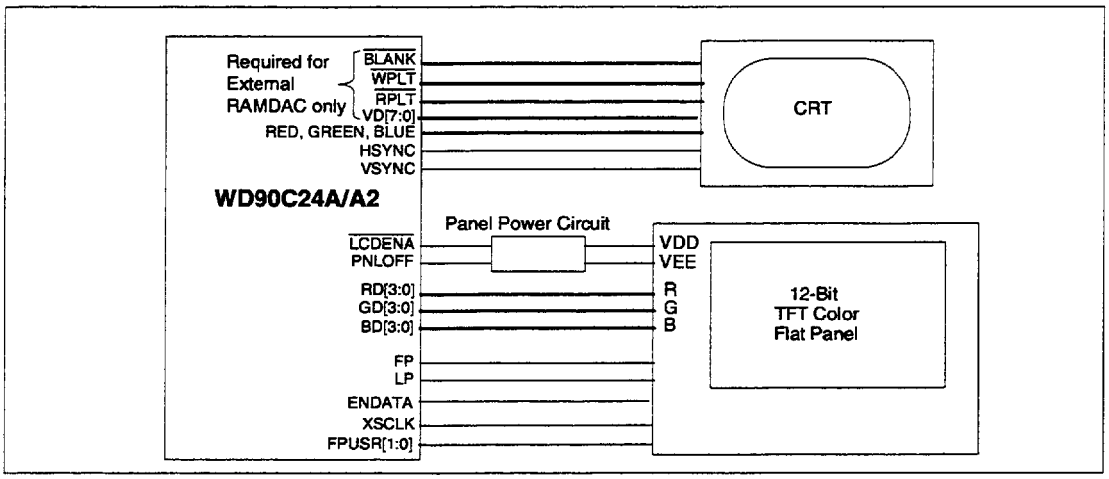


FIGURE 26-4. SIMULTANEOUS CRT AND 12-BIT COLOR TFT LCD PANEL INTERFACE

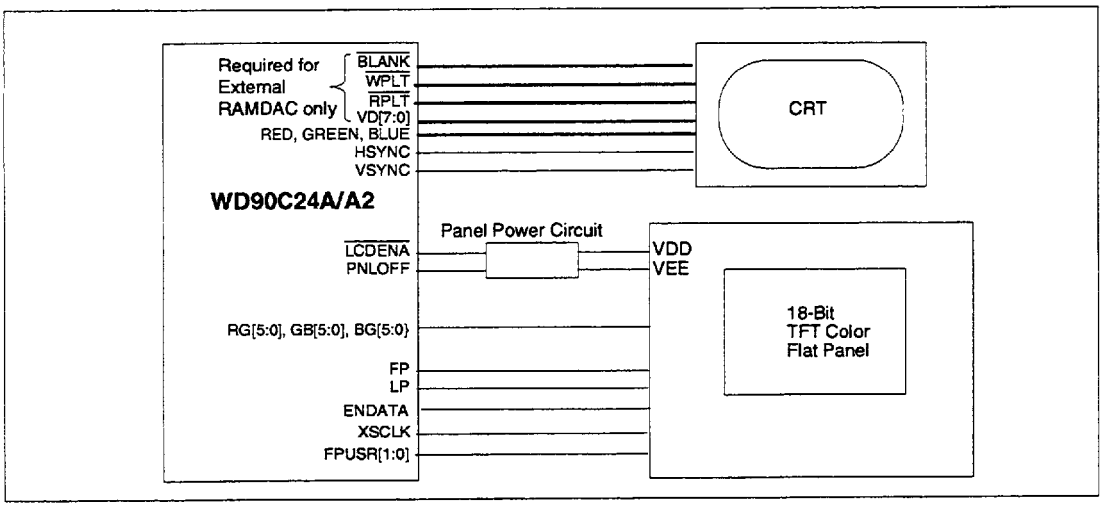


FIGURE 26-5. SIMULTANEOUS CRT AND 18-BIT COLOR TFT LCD PANEL INTERFACE

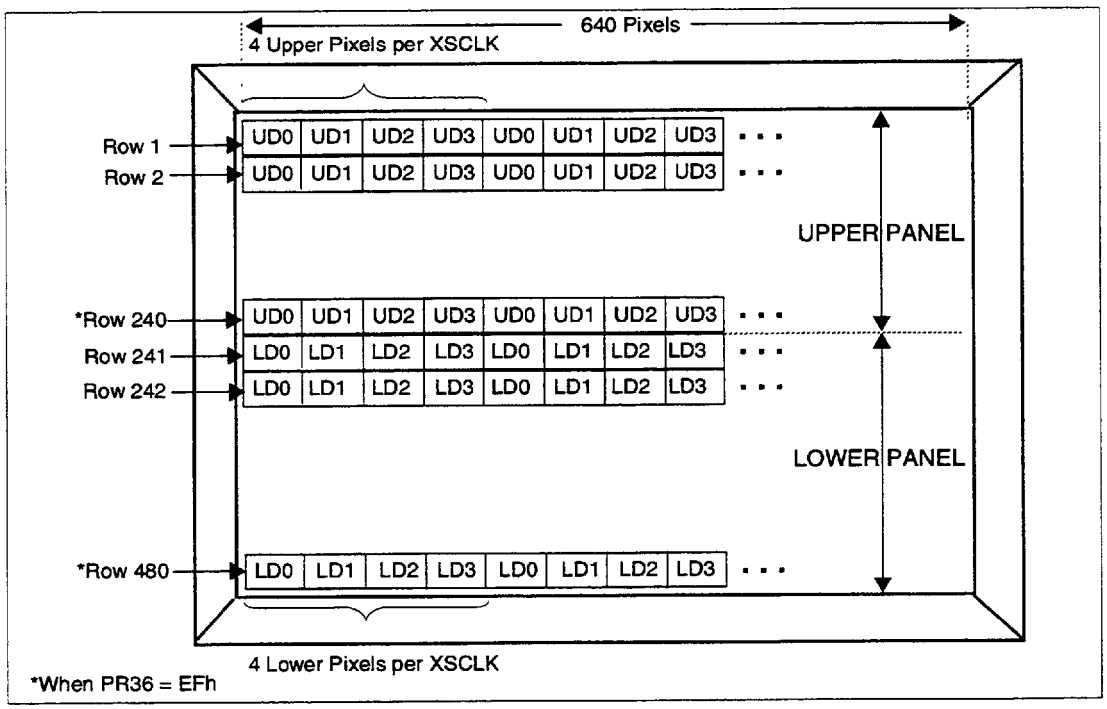


FIGURE 26-6. MONOCHROME DUAL PANEL LCD DATA ORGANIZATION

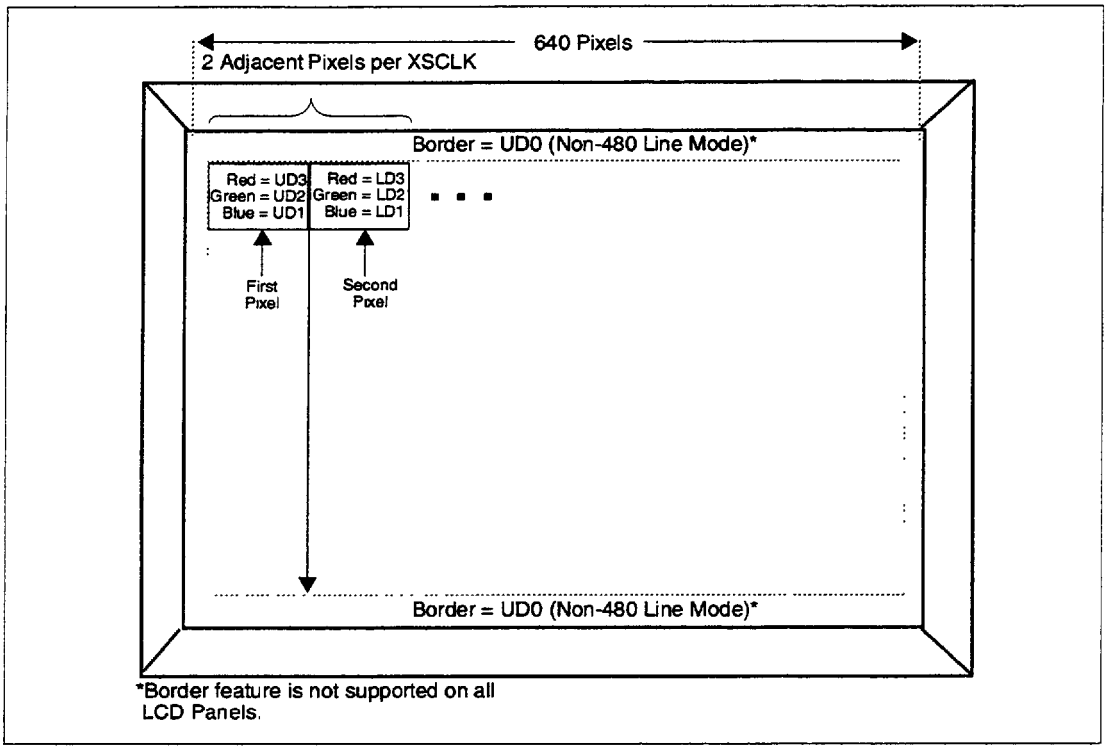


FIGURE 26-7. SINGLE-PANEL MULTIPLEXED COLOR STN LCD DATA ORGANIZATION

26.2 CRT CONNECTIONS

26.2.1 Introduction

This section provides the following information:

- Calculating the RSET Value (Figure 26-7)
- Internal RAMDAC Monitor Detection (Figure 26-8)
- Internal RAMDAC Outputs
- VSYNC and HSYNC Connections
- Selecting the CRT Interface

26.2.2 Calculating RSET Value

The I_{DAC} output currents I_{RED}, I_{GREEN}, and I_{BLUE} develop a voltage across the load resistance R_{LD}. These voltages are compared against a voltage derived from the external voltage reference V_{REF}.

The output current (I_{DAC}) is determined with the following formula:

$$I_{DAC} = \frac{V_{REF} \times 1.979 \times code}{RSET}$$

where the code range from 0 to 63 (0h to 3Fh) is for 6-bit DACs. Using the full-scale code of 63 and an RSET value of 11K ohms in the formula yields a full-scale I_{DAC} value of 14 mA for each DAC output.

NOTE:

RSET values must be selected that do not violate the maximum full scale current limits.

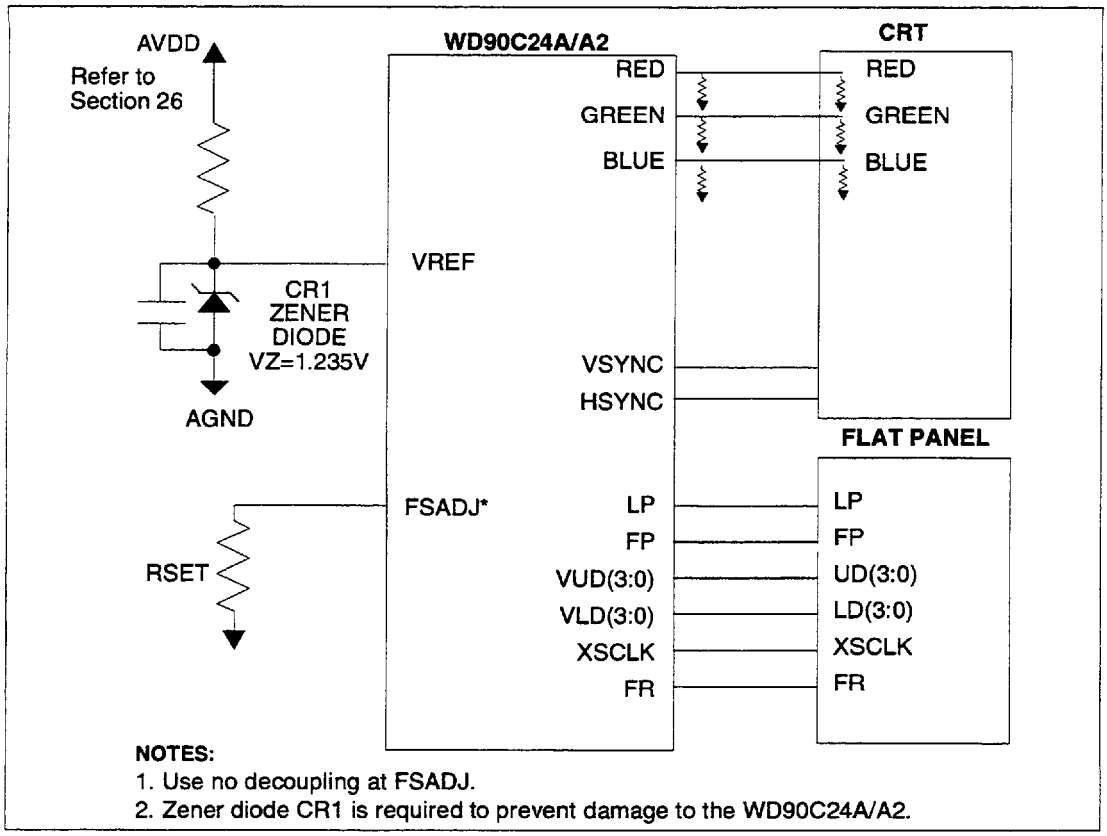


FIGURE 26-8. EXAMPLE OF CRT CONNECTIONS SHOWING VREF AND FSADJ CIRCUITS

26.2.3 Internal RAMDAC Monitor Detection

Figure 26-9 shows the monitor detection connections for the internal RAMDAC.

The output signal $\overline{\text{MDETECT}}$ is readable at port 3C2h bit 4 (VGA Input Status Register 0).

NOTE

It is important to read $\overline{\text{MDETECT}}$ during active video output. Do not read $\overline{\text{MDETECT}}$ during retrace or any other blanking period.

The internal monitor detection circuit of the WD90C24A/A2 is designed to allow detection of whether or not a monitor is connected to CRT outputs and also if that monitor is monochrome or color. The monitor detection circuit relies on differences in voltages at DAC outputs depending on whether a CRT is attached that has internal RGB termination resistors.

Voltages generated at DAC outputs are compared against an internal reference that is approximately the half-scale voltage if a monitor were attached. If voltages on all three DAC outputs are below this internal reference voltage, then the $\overline{\text{MDETECT}}$ signal goes active. The active $\overline{\text{MDETECT}}$ can be read as bit 4 high in VGA Input Status Register 0 (I/O address 3C2h).

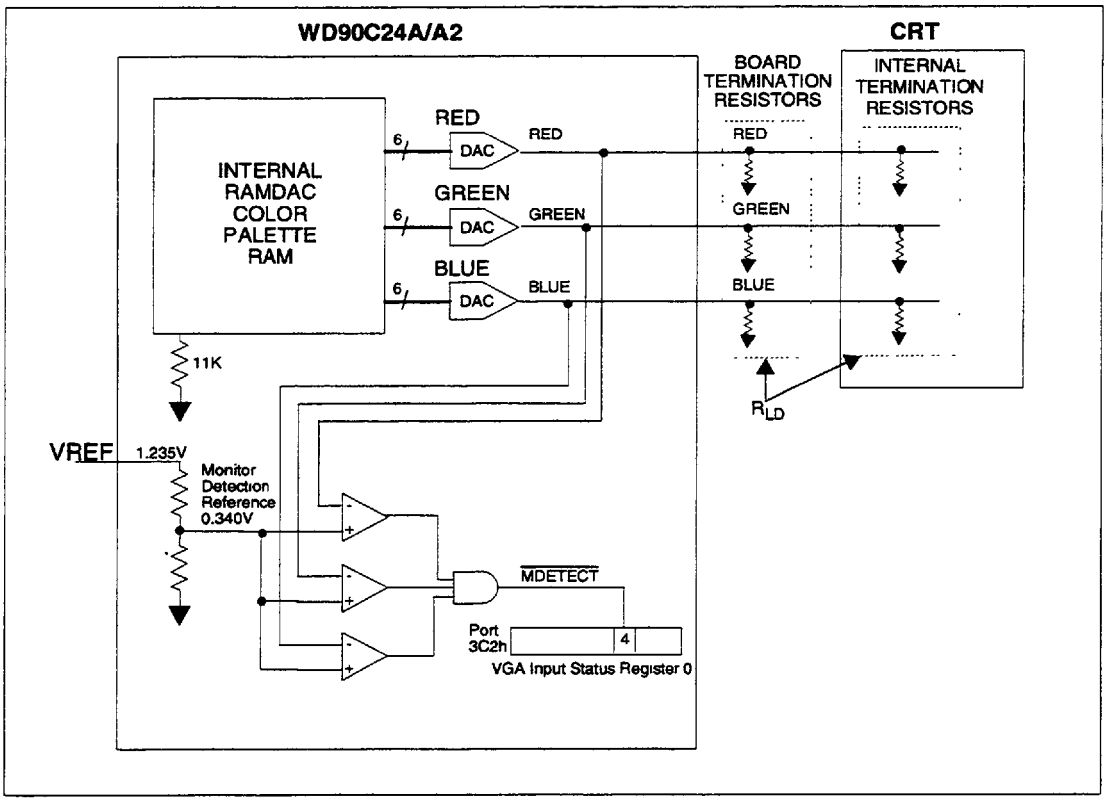


FIGURE 26-9. MONITOR DETECTION CIRCUIT FOR INTERNAL RAMDAC

Typically monitors have a 75 Ohm internal termination and boards have a 150 Ohm source termination. From the source termination value and 75 Ohm monitor termination an R_{LD} value can be calculated, and from that the relationship between DAC output voltage, R_{LD}, and DAC input code can be determined by using the equation in the previous section. Then, DAC codes can be supplied to each of the three internal DACs that should cause the generated voltages at the DAC outputs to be below the monitor detect reference voltage if a monitor is attached, or above the monitor detect voltage if no monitor is attached.

By separately programming each DAC code so that only one of the comparators would change output based on the monitor connection the red, green, and blue monitor connections can be separately sensed. This allows the detection of whether a monochrome-only monitor is attached by looking for green monitor connection, with red and blue monitor connections missing.

DAC codes are controlled by reprogramming the color palette RAM of the internal RAMDAC during monitor detect functions. It is recommended that monitor detect operations be done at power-up to avoid the need to save and restore RAMDAC palette contents required by an application.

The monitor detection comparators require stable DAC output voltages for a minimum of 300 nanoseconds in order to correctly indicate monitor detect status at 3C2h bit 4. To allow DAC outputs to remain stable for this minimum period and to allow reading of the results of monitor detect, it is recommended that the CRT parameters be adjusted during the test to eliminate blanking periods that would disable DAC outputs. After monitor detect functions have completed, the CRT parameters should be returned to their normal values.

26.2.4 Internal RAMDAC Outputs

Pins 157 through 159 are the analog, PS/2 monitor compatible, video outputs. They are active when the WD90C24A/A2 has been configured to drive a CRT monitor. Otherwise, Pins 156 through 158 are zero-current outputs because the DAC portion of the WD90C24A/A2 is only operational when an external CRT is being driven from the internal RAMDAC.

In most applications, Pins 157 through 159 are doubly terminated with 150 Ohm loads (on the PC board) from each pin to ground, and also within a PS/2-compatible monitor from each signal to ground.

Pins 157 through 159 are zero-current outputs when the WD90C24A/A2 is not enabled or when it is in powerdown modes where screen display does not occur. These pins are also shut off when the WD90C24A/A2 is performing retrace activities.

26.2.5 VSYNC and HSYNC Connections

NOTE

VGA monitors that are fully IBM compatible can be driven directly by the VSYNC and HSYNC pins. Older, noncomplying monitor designs may require external buffering.

For VGA compatible monitor connections, VSYNC and HSYNC polarity settings are used by some monitors to adjust screen resolution. Standard VGA monitor resolution selection is shown in the following table. These bits determine the vertical size of the vertical frame by the monitor. Their encoding is also shown in the table.

HSYNC PULSE LEVEL	VSYNC PULSE LEVEL	Vertical Frames
+	+	Reserved
+	-	350 Lines/Frame
-	+	400 Lines/Frame
-	-	480 lines/Frame

The WD90C24A/A2 allows control of VSYNC and HSYNC polarity selection as well as allowing locking of selected polarities.

NOTE

For Simultaneous Display Mode operation, VSYNC and HSYNC pulse polarities are set and locked to 480 lines per frame.

26.2.6 Selecting the CRT Interface

The CRT is enabled by setting PR19 bit 5 to 1.

NOTE

For simultaneous display, PR19 bits 4 and 5 are both set to 1.

26.3 MAPPING RAM PROGRAMMING

The 64 by 6 mapping RAM is designed for dithering pattern selection. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM is read from or written to by the CPU. The outputs from the weighting equation (6 bits) are connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (6 bits) are connected to the dithering logic. For plasma display support, the lower four bits of mapping RAM output are connected to the panel interface circuit.

NOTE

To program mapping RAM, PR19 bit 4 must be set to 1 and no Power-down modes can be active.

Before accessing the mapping RAM, PR31 bit 0 should be set to 0. The following procedure describes a write access to the mapping RAM. A similar procedure is followed to read mapping RAM values.

NOTE

In ISA Mode, the internal mapping RAM is an 8-bit I/O device.

1. Examine port 3CCh to determine is the system is running in color or monochrome mode. Color mode is selected when the least significant bit (LSB) is set to 1. The base address for color is 3D4h, and for monochrome is 3B4h.
2. Load PR1B with A6h to unlock the Flat Panel Registers.
3. Save the value in PR19 bit 4 and then set the bit to 1 to enable the flat panel display.
4. Save the contents of the Sequencer Index Register Port (3C4h).
5. Save the value of PR20 and then load PR20 with 48h.
6. Save the value of PR31 and then set PR31 bits 1 and 0 to 00 to disable $\overline{\text{IOCS16}}$.
7. Save the value of PR30A and then set PR30 bit 4 to 1 to disable the 16-bit system interface.
8. Use assembly instructions "pushf" and "cli" to disable system interrupts and prevent undesired access to the mapping RAM.
9. Test port 3DAh (color) or 3BAh (monochrome) bit 3 for 0 to determine when vertical retrace becomes inactive. To find the correct port address, add 6 to the base address determined in step 1.
10. Test port 3DAh (color) or 3BAh (monochrome) bit 3 for 1 to determine when vertical retrace becomes active.
11. Load PR30 with 30h to unlock the mapping RAM. **(Beginning of loop.)**
12. Load PR33 with the desired mapping RAM address(00-3Fh)
13. Do a "dummy" read to a CRTC index other than PR34.
14. Read (or write) the mapping RAM value from PR34.
15. Wait the minimum of 4 VLCK and 4 MCLK cycles. The following assembly code will provide the proper waiting time:

```
        push  cx
        mov   cx, 10
SMALL_LOOP: jmp   WAITING : (NOTE)
WAITING:  loop  SMALL_LOOP
        pop   cx
```

NOTE

In the above routine, jumping forward flushes the cache.

16. Repeat steps 11 through 15 to read (or write) more registers. **(End of loop.)**
17. Restore the interrupt state ("popf")
18. Restore the saved values in PR30A and then PR31.
19. Restore the lock state of PR20.
20. Restore the saved contents of port 3C4h.
21. Restore the saved value in PR19.
22. Restore the lock state of PR1B.

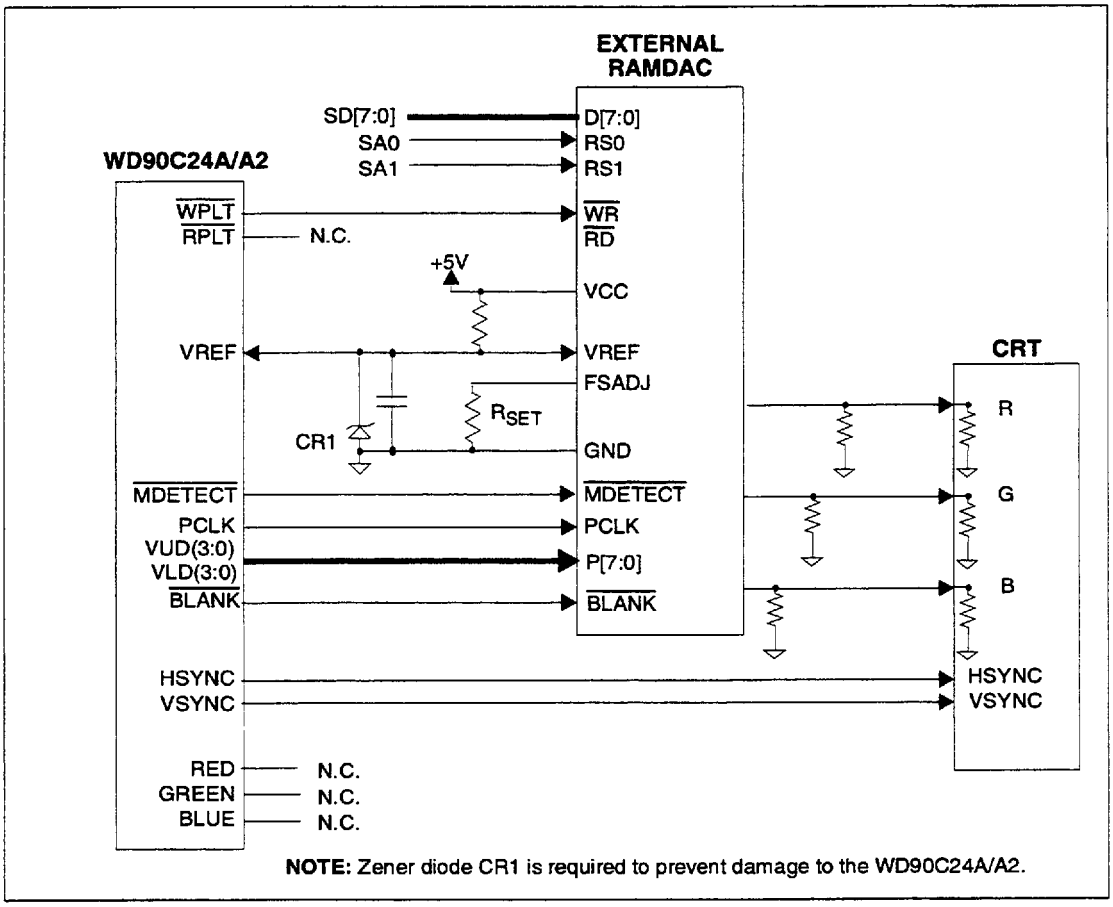
26.4 EXTERNAL RAMDAC CONNECTIONS

The WD90C24A/A2 is used with an external RAMDAC when special color modes are required and are not available with the VGA compatible internal RAMDAC.

Figure 26-10 shows a typical connection for an external RAMDAC.

NOTE

The $\overline{\text{RPLT}}$ signal should not be used to strobe data out of an external DAC onto the SD bus. Palette reads in the WD90C24A/A2 always access the internal RAMDAC.



NOTE: Zener diode CR1 is required to prevent damage to the WD90C24A/A2.

FIGURE 26-10. WD90C24A/A2 WITH EXTERNAL RAMDAC INTERFACE

26.5 VIDEO SIGNATURE ANALYZER

The WD90C24A/A2 contains a signature analyzer circuit that records 16-bit digital signatures of video frames, previous to their conversion to analog colors by the internal RAMDAC. A unique 16-bit signature can be generated for a given frame of video data. Then, the generated signature can be used to verify correctness of the video output and system function.

The basis of the signature analyzer is a linear feedback shift register, or LFSR. The LFSR implements the CCITT CRC16 polynomial of $x_{16}+x_{12}+x_5+1$, adapted from serial implementation to one accepting the 8-bits of RAMDAC input. The inputs to the LFSR are connected to the 8-bit internal RAMDAC inputs which represent the video data previous to RAMDAC color lookup, weighting, gray scale mapping, dithering, etc.

For non-interlaced video modes, the signature analyzer samples video data over single frame intervals. For interlaced video modes, the video signature is generated over an odd and even pair of frames.

When the signature analyzer is enabled it begins shifting in the video signature at the falling edge of the internal VSYNC signal. Video signal generation is complete at the rising edge of the internal VSYNC so that the signature represents an entire display screen of video information.

For interlaced video modes, signal generation is complete at the rising edge of the internal VSYNC following the second frame of the odd and even pair of frames.

The signature analyzer is controlled by its own register at PR45. This register cannot be accessed for reads or writes until the general read/write locks of PR20 are removed. The setting of PR20 (3?5.06h) to 48h allows signature analyzer registers to be accessed. PR45 bit 3 must also be set to 1 to allow reading of the low and high bytes of the signature from PR45A and PR45B, respectively.

The sequence of operations required for the LFSR to capture a video frame signature is as follows:

1. Set PR20 to 48h, which enables read/write of signature analyzer registers.
2. Set PR45 bit 3 to 1, which enables reading of the signature from PR45A and PR45B.
3. Set PR45 bit 0 to 0 to disable signature generation.
4. Set PR45 bit 1 to 0 and then set it back to 1, which initializes the signature to 0001h.
5. Verify that the signature is initialized by checking the contents of PR45A and PR45B as follows:

   PR45A = 01h
   PR45B = 00h

6. Set PR45 bit 0 to 1, to enable the capturing of a frame signature.
7. Wait for a minimum of two VSYNC intervals before reading the video signature.
8. Read low and high bytes of the captured signature from PR45A and PR45B.
9. Compare the captured signature against the expected values for a given screen display.
10. Change PR20 settings to lock the signature analyzer control register and stop signature analyzer functions.

26.6 AUXILIARY VIDEO EXTENDER (AVE) MODE

The AVE mode allows an external controller to drive the internal RAMDAC. This mode is for use in CRT-only display mode. AVE mode is entered by setting PR66 bit 7 to a high, which causes the following actions to occur:

1. The VUD[3:0] and VLD[3:0] pins become inputs, for use as the RAMDAC pixel data bus.
2. The PCLK pin switches to the input mode, for use as the Pixel Clock input.
3. The FR pin switches to input, for use as the $\overline{\text{BLANK}}$ signal.
4. The VSYNC and HSYNC pins tristate to allow the external controller to drive these signals directly to the CRT.

26.7 POWER-DOWN MANAGEMENT

The WD90C24A/A2 provides four major Power-down modes:

- Suspend/Resume Mode (a.k.a Sleep mode or System Power-down mode)
- Deep Sleep Mode
- Display Idle
- General Power-down Mode

Each mode is described in the following paragraphs.

26.7.1 Suspend/Resume Mode (System Power-down Mode)

Suspend/Resume mode (also called System Power-down Mode or Sleep Mode) is used when a display is not required but minimum access to the display registers is required. In this mode, all supply voltages (VDD) remain active, but both the DAC and Clock Synthesizer are shut down. For this mode, the current consumption is less than 5 mA. Since the contents of all display registers and RAM is retained, a minimum of software control is required. The following conditions apply:

- The CPU cannot access the registers, the palette RAM, the mapping RAM, nor the video display memory. (The exceptions being PR4 bit 5, PR57, and PR71).
- Display memory refresh ($\overline{CAS}$-before-$\overline{RAS}$) is generated by the $\overline{REFRESH}$ input, by the CKIN input (at 14.318 Mhz) divided down by a programmable counter through PR71, by the CKIN input (at 32 Khz) pass-through, or by the $\overline{REFLCL}$ input (at 32 KHz) pass-through.
- Most outputs are tri-stated.
- All inputs are required to be in a known state and stable.
- The suspend and resume sequences described in the following paragraphs assume PNLOFF is used to control the VDD of the LCD panel, and $\overline{LCDENA}$ is used to control the VLCD of the panel.

To Enter Suspend/Resume Mode:

- The CPU must set PR44 bit 7 to 0, and set PR35 bit 7 to 1.
- The Power-down control manager drives the $\overline{PDOWN}$ signal low.
- $\overline{LCDENA}$ goes inactive high, and the DAC shuts off.
- After 2-3 horizontal retrace cycles and 2-3 refresh cycles, the MCLK and VCLK frequencies are turned off, the Clock Synthesizer is disabled, and the source of refresh switches to the alternate source.
- After 1 to 5 ms, set PR4 bit 5 to 1, thereby tristating the flat panel control and data signals.
- Set PR57 bit 2 to 0, which drives PNLOFF high.
- The WD90C24A/A2 has entered Suspend/Resume Mode.

To Leave Suspend/Resume Mode:

- The power-down control manager ensures that the 14.318 MHz clock is stable.
- Set PR57 bit 2 to 1, which drives PNLOFF low.
- Set PR4 bit 5 to 0, which drives the flat panel control and data signals from tristate to low.
- The power-down control manager drives $\overline{PDOWN}$ high.
- The rising edge of $\overline{PDOWN}$ wakes up the Clock Synthesizer and re-activates MCLK and VCLK.
- After 2-3 refresh cycles and 2-3 horizontal retrace cycles, the flat panel control and data signals resume operation.
- After 2 FP pulses, $\overline{LCDENA}$ goes active low.

26.7.2 Deep Sleep Mode

Deep Sleep Mode is used when the entire display subsystem can be turned off. This mode is designed to conserve the most power and also requires the most system overhead. In this mode, current consumption is less than 1 mA. When entering Deep Sleep Mode, most of the VDD power is shutdown, and the contents of all display registers will be lost. Therefore, a software routine is required to preserve and restore the contents of the registers, palette RAM, and mapping RAM. It is necessary to provide power (PVDD, MVDD A, and MVDD B) to the logic that generates memory refresh signals.The following conditions apply:

- Display memory refresh ($\overline{CAS}$-before-$\overline{RAS}$) is generated by the $\overline{REFRESH}$ input, by the CKIN input (at 14.318 Mhz) divided down by a programmable counter through PR71, or by the CKIN input (at 32 Khz) pass-through.

To Enter Deep Sleep Mode:

- Execute a power-down software routine that collects data from all the display registers and palette RAM, then stores the data in system main memory.
- The CPU must set PR44 bit 7 to 0, and set PR35 bit 7 to 1.
- The Power-down control manager drives the PDOWN signal low.
- LCDENA goes inactive high, and the DAC shuts off.
- After 2-3 horizontal retrace cycles and 2-3 refresh cycles, the MCLK and VCLK frequencies are turned off, the Clock Synthesizer is disabled, and the source of refresh switches to the alternate source.
- After 1 to 5 ms, set PR4 bit 5 to 1, thereby tristating the flat panel control and data signals.
- Set PR57 bit 2 to 0, which drives PNLOFF high.
- After 300 ms, the Power-down control manager drives the RESET signal high.
- After another 300 ms, the Power-down control manager shuts off all the VDD pins except PVDD, MVDD A, and MVDD B power.
- While in Deep Sleep Mode, the logic remaining powered generates the CAS-before-RAS memory refresh cycles.

To Leave Deep Sleep Mode:

- The Power-down control manager turns on all VDD supply pins.
- After 300 ms, the Power-down control manager drives the RESET signal low. The falling edge RESET wakes up the Clock Synthesizer and the WD90C24A/A2 enters Display Idle Mode. The 14.318 MHz system clock must be stablized befire RESET is allowed to go high.
- After another 100 ms, The Clock Synthesizer generates the default MCLK and VCLK signals.
- The WD90C24A/A2 is then initialized. First, it is awakened via either VGA wake-up port (3C3h or 46E8h). Then the CRTC registers, followed by the other registers, are restored by a software restore routine. The Palette RAM and Mapping RAM are not restored.
- Set PR57 bit 2 to 1, which drives PNLOFF low.
- Set PR4 bit 5 to 0, which drives the flat panel control and data signals from tristate to low.
- After another 100 ms, the power-down control manager drives the PDOWN signal high.
- Finally, the power-down control manager restores Palette RAM and Mapping RAM.
- After 2-3 refresh cycles , the flat panel control and data signals will resume operation.
- After 2 FP pulses, LCDENA goes active low.

26.7.3 Display Idle Mode

Display Idle Mode is used to turn off the display when the keyboard has been idle for a preset time interval. In this mode all the supply voltages (VDD) and the Clock Synthesizer remain on. The MCLK and VCLK clock rates are slowed down to 1/8 of their normal frequency. The following conditions apply:

- The CPU can access the registers, but cannot access the palette RAM, the mapping RAM, or the video display memory.
- Display memory refresh (CAS-before-RAS) is generated by the REFRESH input.
- The DAC and the LCD panel interfaces are turned off.

To Enter Display Idle Mode:

- The CPU must set PR44 bit 7 to 0, and set PR35 bit 7 to 0.
- The Power-down control manager drives the PDOWN signal low.
- LCDENA goes inactive high, and the DAC shuts off.
- After 2-3 horizontal retrace cycles and 2-3 refresh cycles, the MCLK and VCLK frequencies switch to 1/8 of normal frequency and the source of refresh switches to the alternate source.
- After 1 to 5 ms, set PR4 bit 5 to 1, thereby tristating the flat panel control and data signals.
- Set PR57 bit 2 to 0, which drives PNLOFF high.

To Leave Display Idle Mode:

- Set PR57 bit 2 to 1, which drives PNLOFF low.
- Set PR4 bit 5 to 0, which drives the flat panel control and data signals from tristate to low.
- The Power-down control manager drives the PDOWN signal inactive high.

- The rising edge of $\overline{\text{PDOWN}}$ causes the MCLK and VCLK frequencies to switch back to normal frequency.
- After 2-3 refresh cycles and 2-3 horizontal retrace cycles, the flat panel control and data signals will resume operation.
- After 2 FP pulses, $\overline{\text{LCDENA}}$ goes active low.

26.7.4 General Power-down Mode

General Power-down Mode is used to turn off the display when the keyboard has been idle for a preset time interval. In this mode all the supply voltages (VDD) and the Clock Synthesizer remain on. The MCLK and VCLK clock rates are slowed down to 1/8 of their normal frequency. If it is desired to keep the clock rate at full value, PR35 bit 6 disables the divide-by-8 feature. The following conditions apply:

- The CPU can access the registers and the video display memory, but cannot access the palette RAM or the mapping RAM.
- Display memory refresh ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$) is generated by the internal horizontal counter which is programmable through PR44.
- The DAC and the LCD panel interfaces are turned off.

The memory refresh cycle is generated by the same logic for normal display mode but with slower MCLK and VCLK clock rates. By using PR44 to program the memory refresh period and memory refresh cycles per horizontal line, the user-defined memory refresh cycle can be achieved. In this mode, PR44 overrides the horizontal total register. Refer to the PR44 register description for an example of how to calculate the value for PR44 bits 6 through 0.

Entering General Power-down Mode:

- The CPU must set PR44 bit 7 to 1.
- To enable the internal clock divide, if desired, set PR35 bit 6 to 1.
- The Power-down control manager drives the $\overline{\text{PDOWN}}$ signal low.
- $\overline{\text{LCDENA}}$ goes inactive high, and the DAC shuts off.
- After 2-3 horizontal retrace cycles and 2-3 refresh cycles, the MCLK and VCLK frequencies switch to 1/8 of normal frequency and the source of refresh switches to the alternate source.
- After 1 to 5 ms, set PR4 bit 5 to 1, thereby tristating the flat panel control and data signals.
- Set PR57 bit 2 to 0, which drives PNLOFF high.

Leaving General Power-down Mode:

- Set PR57 bit 2 to 1, which drives PNLOFF low.
- Set PR4 bit 5 to 0, which drives the flat panel control and data signals from tristate to low.
- The Power-down manager drives the $\overline{\text{PDOWN}}$ signal inactive high.
- The rising edge of $\overline{\text{PDOWN}}$ causes the MCLK and VCLK frequencies to switch back to normal frequency.
- After 2-3 refresh cycles and 2-3 horizontal retrace cycles, the flat panel control and data signals will resume operation.
- After 2 FP pulses, $\overline{\text{LCDENA}}$ goes active low.

26.8 CALCULATION OF GENERAL POWER-DOWN MODE REFRESH TIMING

In General Power-down Modes, the WD90C24A/A2 internally generates the necessary refresh cycles to maintain DRAM contents and allow access to display memory. This is performed by internal refresh circuits that time refresh operations based on the value in PR44[6:0]. For correct refresh operation during General Power-down modes it is necessary to program an appropriate value into PR44. The actions required to determine the appropriate value to program into PR44 are described in the following paragraphs.

26.8.1 Understanding DRAM Requirements

In order to calculate the appropriate values for PR44 when in General Power-down Modes, it is first necessary to understand DRAM parameters that determine its refresh needs. The WD90C24A/A2 supports DRAM that requires 512 refresh cycles for a complete refresh operation. Therefore, all DRAM used with the WD90C24A/A2 requires 512 refresh cycles over a maximum refresh peri-

od referred to as t_{REF}. Typical t_{REF} values range from 8 to 64 ms. Another DRAM requirement which needs to be understood before calculating PR44 values is the random cycle time required to do one refresh cycle, referred to as t_{rc}. For 100 nsec DRAM, t_{rc} is typically 180 ns, and for 70 nsec DRAM t_{rc} is typically 130 ns.

26.8.2 Determining Number of Refresh Cycles Per Refresh Operation

The values in PR1A[1:0] and the Vertical Retrace End Register bit 6 determine whether 1, 2, 3 or 5 refresh cycles will occur per refresh operation.

26.8.3 MCLK Frequency Requirements During General Power-down Modes

Each refresh cycle requires 6 MCLK periods, plus a setup of a maximum of 6 MCLK periods before refresh operations begin. Each system access during General Power-down modes requires 6 MCLK periods as well. Thus the required MCLK frequency during General Power-down is calculated by determining the total number of MCLK cycles required during the refresh operation.

The total number of MCLK cycles required per refresh operation is represented as...

6(1 + #system accesses + #refresh cycles)

26.8.4 VCLK Frequency Requirements and PR44[6:0]

In General Power-down modes, the internal VCLK frequency and PR44[6:0] value have the following relationship:

Refresh Operation Period (ROP) = VCLK period x Dots per Char x (Value in PR44[6:0]+5)

Of that value, the portion of the period dedicated to DRAM refresh is determined by using the above equation except with the PR44+5 value divided by two and the fraction discarded. The difference between the amount used for refresh and the total refresh operation period is the amount used for system access of video DRAM during power-down refresh cycles.

26.8.5 Example

This example assumes the following conditions:

A. DRAM has 190 ns t_{rc} and 8 msec t_{REF}
B. Internal VCLK and MCLK frequencies of 5 MHz during the selected General Power-down mode.
C. PR44 bits 6:0 set to 14d

With these conditions, calculate the refresh operation period as follows:

ROP = 1/(5 MHz)(8 dots/char)(14+5) = 30.4 µsec

Refresh time per ROP = 1/(5 MHz)(8dots/char)(9)=14.4 µsec

Assuming a trc of 200 nsec for a margin of safety and a 5 MHz MCLK, we get one refresh cycle per 1.2 µsec plus a 1.2 µsec setup. Therefore, there is enough margin to program PR1A[1:0] and the Vertical Retrace End Register bit 6 for 1-5 refresh cycles per refresh operation.

For this example we will select two refresh cycles.

Since we need a total of 512 refresh cycles to completely refresh the DRAM and we are doing 2 refresh cycles per refresh operation, we need 256(30.4 µsec)=7.78 msec to completely refresh the DRAM. This figure is within the 8 msec t_{REF} specified and will work.

From this example it can be seen that values of PR44, VCLK, and MCLK can be further optimized if additional reductions in clock frequencies are desired.

26.9 POWER DISTRIBUTION

Power distribution for the WD90C24A/A2 is shown in Figure 26-11.

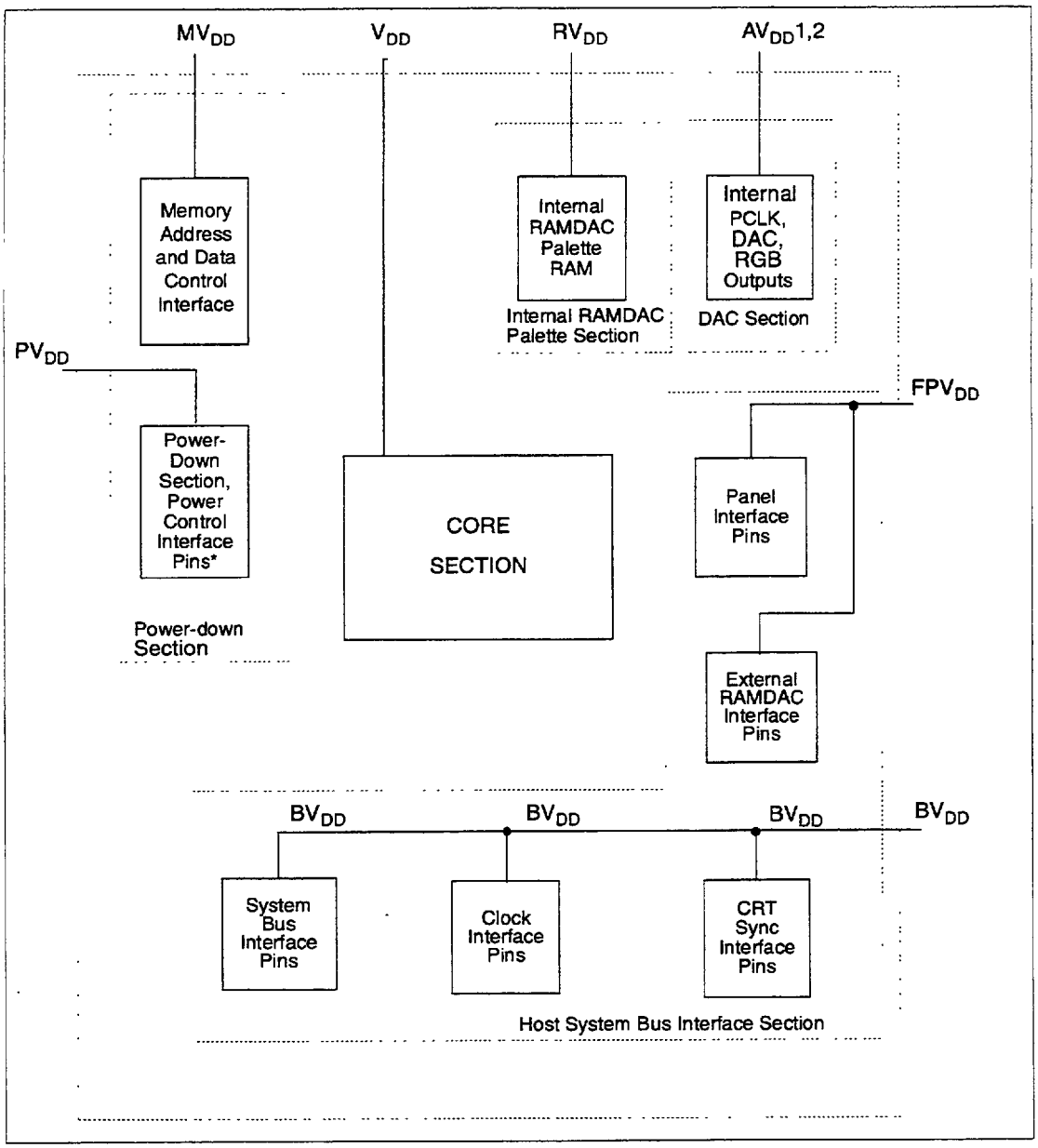
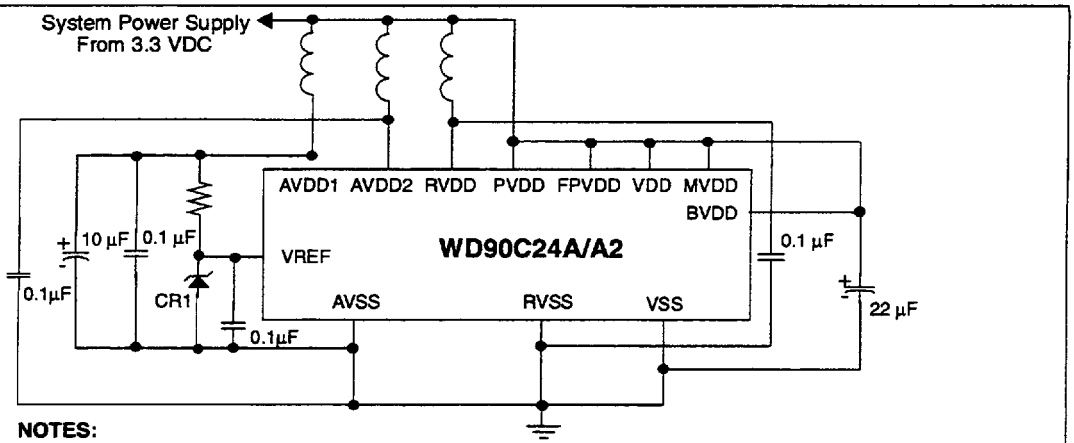


FIGURE 26-11. POWER DISTRIBUTION BLOCK DIAGRAM

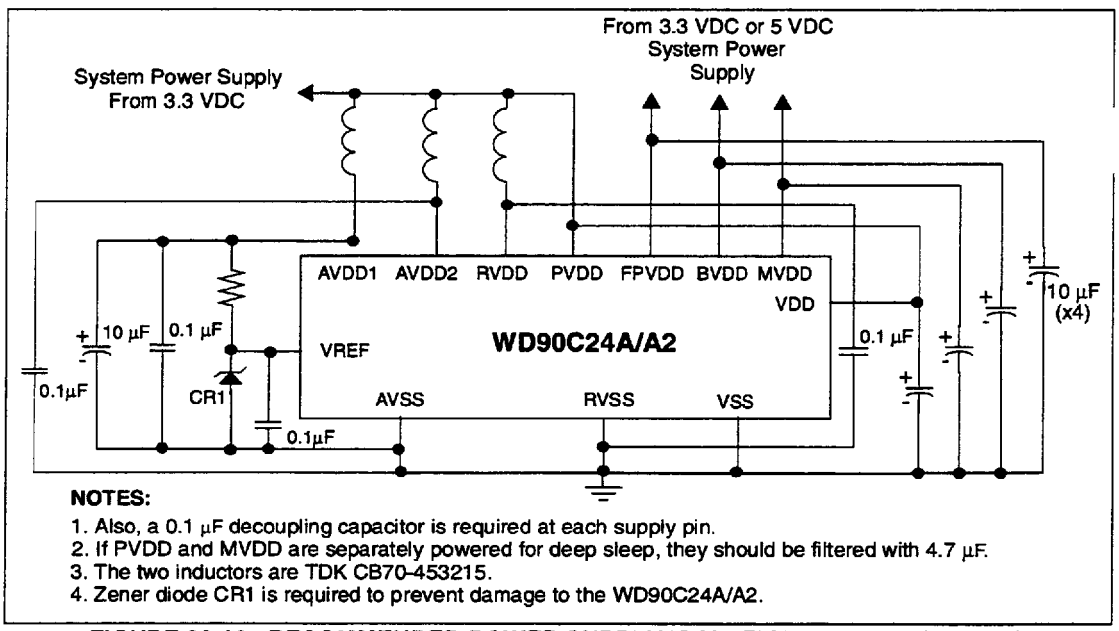
26.10 RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING

The recommended power supply connections for isolation and decoupling are shown in the following figures. The first figure shows the recommended connections for single voltage operation, while the second shows the setup for mixed voltage operation.



NOTES:
1. Also, a 0.1 µF decoupling capacitor is required at each supply pin.
2. If PVDD and MVDD are separately powered for deep sleep, they should be filtered with 4.7 µF.
3. The two inductors are TDK CB70-453215.
4. Zener diode CR1 is required to prevent damage to the WD90C24A/A2.

FIGURE 26-12. RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING FOR SINGLE VOLTAGE OPERATION



NOTES:
1. Also, a 0.1 µF decoupling capacitor is required at each supply pin.
2. If PVDD and MVDD are separately powered for deep sleep, they should be filtered with 4.7 µF.
3. The two inductors are TDK CB70-453215.
4. Zener diode CR1 is required to prevent damage to the WD90C24A/A2.

FIGURE 26-13. RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING FOR MIXED VOLTAGE OPERATION

PR44	PR35		MODE ENTERED AT POWER-DOWN	CRT I/F	PANEL I/F	DISPLAY MEMORY CONTENTS	VIDEO DRAM REFRESH	REGISTER CONTENTS	MAPPING RAM TABLE	INTERNAL PALETTE RAM	CLOCK INPUTS	NECESSARY POWER CONNECT-IONS	TO RETURN TO NORMAL OPERATION
7	7	6											
0	1	X	Suspend/ Resume (System Power-down or Sleep Mode)	Disabled	Disabled	Retained, not accessible[2]	1) Self-refresh 2) AC-Timed $\overline{CAS}$ before $\overline{RAS}$ refresh (Refer to Note 4)	[1,3]Retained, not accessible	[1]Retained, not accessible	[1]Retained, not accessible	None, unless CKIN is used to generate refresh cycles. (PCLK shut off)	All required.	Restore CKIN, and set $\overline{PDOWN}$ high.
0	1	X	Deep Sleep Reset Activated	Disabled	Disabled	Retained, not accessible[2]	1) Self-refresh 2) AC-Timed $\overline{CAS}$ before $\overline{RAS}$ refresh (Refer to Note 4)	Not retained if V_{DD} is removed	Not retained if RV_{DD} is removed	Not retained if RV_{DD} is removed	None, unless CKIN is used to generate refresh cycles. (PCLK shut off)	PV_{DD} and MV_{DD} are required, all others may be disconnected	Connect power, restore CKIN, deactivate RESET and $\overline{PDOWN}$; and restore all registers, mapping RAM, and internal palette RAM
0	0	X	Display Idle	Disabled	Disabled	Retained, not accessible[2]	1) Self-refresh 2) AC-Timed $\overline{CAS}$ before $\overline{RAS}$/each $\overline{REFRESH}$.	Accessible	[1]Retained, not accessible	[1]Retained, not accessible	CKIN (14.3 Mhz) must be main-tained. VCLK and MCLK internally divided by 8	All required.	Set $\overline{PDOWN}$ high
1	X	1	General Power-down, with Internal Clock Divide	Disabled	Disabled	Retained, not accessible[2]	$\overline{CAS}$ before $\overline{RAS}$ refresh according to PR44 (6:0) interval and PR1A(1:0).	Accessible	[1]Retained, not accessible	[1]Retained, not accessible	CKIN (14.3 Mhz) must be main-tained. VCLK and MCLK internally divided by 8	All required.	Set $\overline{PDOWN}$ high
1	X	0	General Power-down, without internal clock divide	Disabled	Disabled	Accessible	$\overline{CAS}$ before $\overline{RAS}$ refresh according to PR44 (6:0) interval and PR1A(1:0).	Accessible	[1]Retained, not accessible	[1]Retained, not accessible	CKIN (14.3 Mhz) must be maintained.	All required.	Set $\overline{PDOWN}$ high

TABLE 26-1. POWER-DOWN MODES

NOTES FOR TABLE 26-1

1. Should not be accessed in sleep mode. Access is disabled if the host release bit (PR35 bit 5) is set to 1.
2. An alternate source of refresh cycles is required to maintain display memory contents.
3. PR4 bit 5, PR57 bits 2 and 5, and PR71 are accessible
4. Video DRAM refresh can be enabled in several ways:
   A. Self-refresh
   B. AC-timed $\overline{CAS}$-before-$\overline{RAS}$ refresh with $\overline{REFRESH}$ pulse.
   C. AC-timed $\overline{CAS}$-before-$\overline{RAS}$ refresh using one of the following refresh sources:
      a. The CKIN input (at 14.318 KHz) divided by a programmable counter through PR71.
      b. The CKIN input (at 32KHz) pass-through.
      c. The $\overline{REFLCL}$ input (at 32 KHz) pass-through

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE AEN ACTIVE HIGH	STATE WHILE INTERNAL $\overline{REFRESH}$ ACTIVE	STATE WHILE $\overline{REFRESH}$ ACTIVE LOW	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES
$\overline{IOCS16}$	Z	Z	Z	N	N	N	Z	N	N
$\overline{MEMCS16}$	Z	Z	Z	N	N	Z	Z	N	Z
IRQ	Z	Z	Z	N	N	N	Z	N	N
$\overline{IOCHRDY}$	Z	Z	Z	Z	N	N	Z	N	N
$\overline{0WS}$	Z	Z	Z	N	N	P	Z	P	P
SD(15:0)	Z	Z	Z	N	N	N	Z	N	N
NOTE: Refer to key and notes on the following page.									

TABLE 26-2. RESET AND POWERDOWN STATES OF THE SYSTEM BUS INTERFACE --- ISA BUS MODE

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE INTERNAL $\overline{REFRESH}$ ACTIVE	STATE WHILE $\overline{REFRESH}$ ACTIVE LOW	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES	HOST RELEASE DURING SLEEP MODE
$\overline{CPURDY}$	Z	Z	Z	Z	Z	Z	Z	Z	Z
$\overline{VLBICS}$	Z	Z	Z	Z	Z	Z	Z	Z	Z
PD(31:0)	I	I	I	I	I	I	I	I	I
NOTE: Refer to key and notes on the following page.									

TABLE 26-3. RESET AND POWERDOWN STATES OF THE SYSTEM BUS INTERFACE --- LOCAL BUS MODE

KEY FOR TABLES 26-2 THROUGH 26-4

H = pin in output high mode
I = pin in input mode
L = pin in output low
N = normal operation state
N÷8 = Normal frequency divided by 8
P = previous state held
Z = pin in high-impedance output mode
U = undetermined

NOTES FOR TABLES 26-2 THROUGH 26-4

1. For internal PCLK mode, XMCLK and VCLK2 default to tristate, unless CNF(3)=1 which enables the VCLK2 output buffer. For external PCLK mode, these pins serve as the Memory and VCLK2 clock inputs.
2. $\overline{RAS}$ and $\overline{CAS}$ outputs are high except during refresh functions, where they operate as normal for the duration of the refresh cycle. If self-refresh is activated, $\overline{RAS}$ and $\overline{CAS}$ are sequenced low during power-down modes.
3. When in external clock mode, this pin is input or output as determined by CNF(3) [AMD(3) high or low at reset].
4. Low if configured as an $\overline{FR}$ output, otherwise this is the normal $\overline{BLANK}$ signal to the external RAMDAC.
5. HSYNC and VSYNC are affected by programmable polarity options, and can be set static high with PR39 bit 2 = 0, or can be set static low by setting PR66 bit 3 = 1.
6. Output enable is usually low and write enable usually high to allow read cycles from display memory for screen updating.
7. This pin can be tristated by setting PR4, bit 5 to 1.
8. This pin can be toggled using PR57, bit 2.
9. This pin can be held static low by setting PR66, bit 4 = 1.

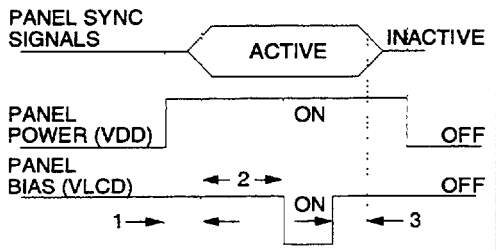
I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE $\overline{\text{REFRESH}}$ ACTIVE LOW	CRT MODE	LCD MODE	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES
$\overline{\text{EBROM}}$	H	H	H	N	N	N	N	N	N
AMD(15:0)	I	N	N	Z	Z	Z	Z	Z	Z
AMA(8:0)	L	N	N	N	N	N	H	H	N
$\overline{\text{ARAS}}$	H	N	N	L	L	L	N	N^2	N^2
$\overline{\text{ACASL/H}}$	H	N	N	L	L	L	N	N^2	N^2
$\overline{\text{AOE}}$	H	N^7	N^7	L	L	L	L	L	L
$\overline{\text{AWE}}$	H	N^7	N^7	H	H	H	H	H	N
BMD(15:0)	I	N	N	Z	Z	Z	Z	Z	Z
BMA(8:0)	L	N	N	N	N	N	H	H	N
$\overline{\text{BRAS}}$	H	N	N	L	L	L	N	N^2	N^2
$\overline{\text{BCASL/H}}$	H	N	N	L	L	L	N	N^2	N^2
$\overline{\text{BOE}}$	H	N^7	N^7	L	L	L	L	L	L
$\overline{\text{BWE}}$	H	N^7	N^7	H	H	H	H	H	N
RED/ GREEN/ BLUE	U	U	N	N	N	L	L	L	L
HSYNC	L	L	L	N^6	N^6	$L/H/N^6$	L	L	L
VSYNC	L	L	L	N^6	N^6	$L/H/N^6$	L	L	L
PCLK	N^{10}	N^{10}	N^{10}	N^{10}	N^{10}	N^{10}	L	L	L
XMCLK[1]	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N
VCLK2[1,4]	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N
FPUSR1/ VCLK1[4]	L/N	L/N	L/N	N	N	N	P/N	N	N
FPUSR0	L	L	L	N	N	N	P	N	N
$\overline{\text{LCDENA}}$	H	H	H	N	H	L	H	H	H
PNLOFF	H	H	H	N^9	H^9	L^9	H^9	H^9	H^9
VUD(3:0), VLD(3:0)	L	L	L	N	N^{10}	N	L/Z^8	L/Z^8	L/Z^8
STN(14:8)	L	L	L	N	L	N	L/Z^8	L/Z^8	L/Z^8
STN15/ $\overline{\text{RPLT}}$	H	H	H	N	N	N	L/Z^8	L/Z^8	L/Z^8
$\overline{\text{WPLT}}$/ RGB4	H	H	H	N	N	N	L/Z^8	L/Z^8	L/Z^8
XSCLKL/ RGB5	L	L	L	N	L	N	L/Z^8	L/Z^8	L/Z^8
XSCLK	L	L	L	N	L	N	L/Z^8	L/Z^8	L/Z^8
FR/ $\overline{\text{BLANK}}$/ ENDATA	N	N	N	N	N^{10}	N	L/Z^8	L/Z^8	L/Z^8
LP	L	L	L	N	L	N	L/Z^8	L/Z^8	L/Z^8
FP	L	L	L	N	L	N	L/Z^8	L/Z^8	L/Z^8

NOTE: Refer to key and notes on the previous page.

TABLE 26-4. RESET AND POWERDOWN STATES OF DISPLAY MEMORY AND VIDEO/PANEL INTERFACES

26.11 PANEL PROTECTION

The WD90C24A/A2 is designed to ensure proper control of LCDENA and PNLOFF signals during cycling of system power and entering or exiting power-down modes. This is done to allow these signals to be used as controls for power to LCD or other technology panels that require power sequencing to prevent damage. The PNLOFF signal is intended for connection to the primary power control and LCDENA to the negative bias. Typically, these two biases have particular sequencing requirements, as shown below.



NOTES: Typical panel specifications may list the following parameters:

1. Power should be applied to the panel for some time before the sync signals become active.
2. Sync signal should be active and panel power on for some minimum time before the panel bias is turned on.
3. To prevent panel damage at power off, the panel bias should be turned off first, followed by the panel sync signals, and then the panel power.

FIGURE 26-14. TYPICAL PANEL SEQUENCING REQUIREMENTS

26.11.1 Panel Protection During System Power-On

If the system power-on reset signal ensures that RESET is active low until system power meets WD90C24A/A2 minimums, the WD90C24A/A2 will hold LCDENA inactive high and PNLOFF active high until software activates these signals.

After system power stabilizes and RESET goes inactive, LCDENA remains inactive and PNLOFF remains active, holding an attached panel in a powered-off state until software actions cause their state to change.

26.11.2 Panel Protection and Enabling during Power-Up and Switching from CRT to LCD

During power-on-reset, PR19 bit 4 and PR57 bit 2 default low, causing both PNLOFF and LCDENA to be driven high, i.e. both panel VDD and VLCD are turned off. In addition, PR4 bit 5 defaults 'high' which keeps the flat panel interface pins tri-stated. The panel power-up sequence is as follows:

1. Initialize LCD mode by programming the proper flat panel timing.
2. Set PR57 bit 2 to 1, which drives PNLOFF low, activating panel power.
3. Set PR4 bit 5 to 0, driving the flat panel interface pins low.
4. Set PR19 bit 4 to 1, entering LCD display mode. LCDENA will be driven low 2 FP pulses later, activating panel bias.

26.11.3 Panel Protection when Switching from LCD to CRT.

When panel support is no longer needed the panel power control signals are returned to their power-up state using the following procedure:

1. Set PR19 bit 4 to 0, exiting LCD mode. LCDENA will be driven high (inactive).
2. Wait 20ms before initializing CRT mode.
3. Set PR4 bit 5 to 1, tri-stating the flat panel interface pins.
4. Set PR57 bit 2 to 0, driving PNLOFF high.

26.11.4 Panel Protection During Power-Off

When main power is turned off, the system RESET signal is expected to cause the RESET input to go active high. This causes the WD90C24A/A2 to force $\overline{\text{LCDENA}}$ and PNLOFF high, disabling panel power).

While RESET or $\overline{\text{PDOWN}}$ are active, $\overline{\text{LCDENA}}$ and PNLOFF remain high until PV_{DD} drops below 2.0V, below which time they become undefined.

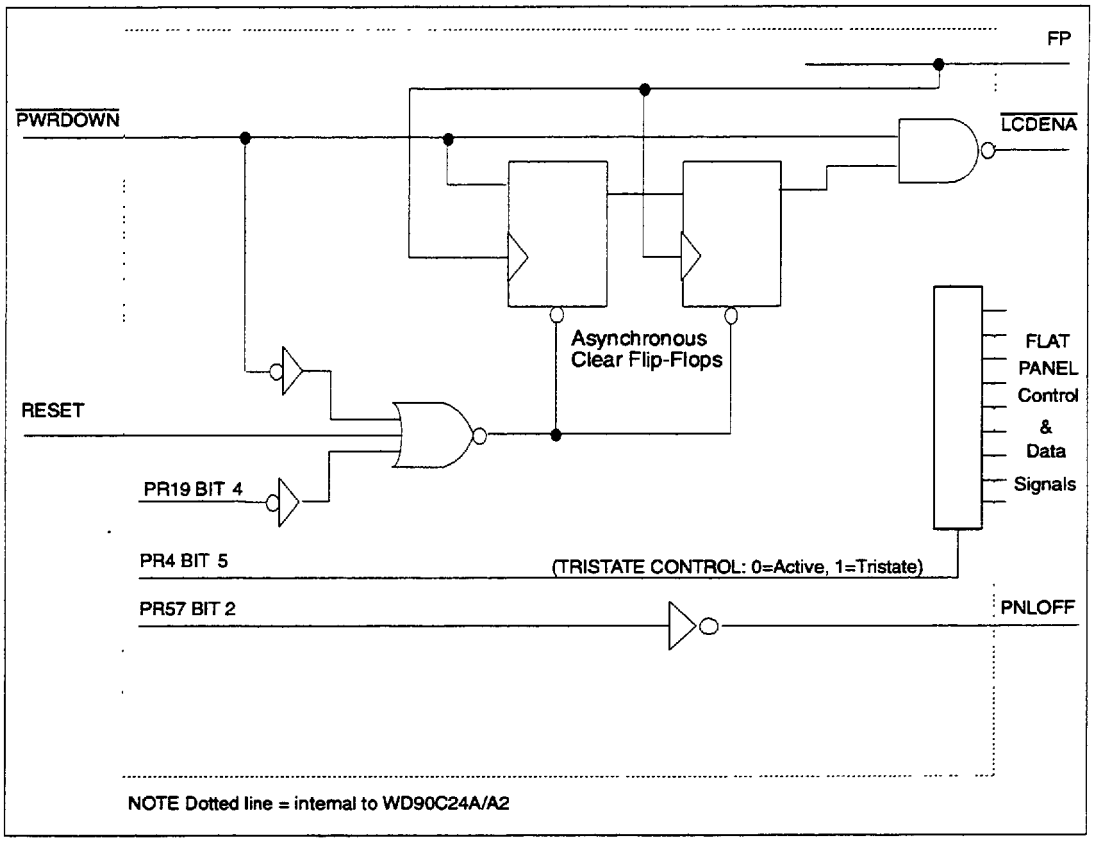


FIGURE 26-15. $\overline{\text{LCDENA}}$ AND PNLOFF PANEL PROTECTION SIGNALS

26.12 REGISTER SHADOWING

The shadowing feature allows certain key registers affecting screen timing and resolution to be locked (once properly programmed) and then overlaid with a base register with the same read/write characteristics. This register shadowing capability allows the CRT controller to be set for a screen resolution compatible with its flat-panel resolution. Then, system applications can modify the CRTC registers without affecting flat-panel display operation. Other circuits in the CRT controller compensate for the fixed-display resolution on panel displays by using hardware algorithms to adjust displayed information to its intended size.

The CRTC Shadow registers control flat panel and CRT timing. When the regular CRTC registers are written to, the shadow timing registers, if unlocked, receive the same data. Locking the shadow timing registers is controlled by PR1B.

In Flat Panel and in Simultaneous Display mode, the shadow timing registers should be loaded once and then locked by PR1B. Once they are locked, data written to the base registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

In CRT only modes, shadow registers should remain unlocked.

There are eleven sets of registers which have this base/shadow register pair function. All are indexed in port 3?5h.

The typical shadow values are for a monochrome dual panel LCD with 640 by 480 pixels when in LCD only mode.

NAME	INDEX	BITS SHADOWED	TYPICAL SHADOW VALUES
Horizontal Total	00h	7:0	5Fh
Horizontal Display End	01h	7:0	4Fh
Start Horizontal Blanking	02h	7:0	50h
End Horizontal Blanking	03h	6:0	82h
Start Horizontal Retrace	04h	7:0	54h
End Horizontal Retrace	05h	7:0	80h
Vertical Total	06h	7:0	F2h
Overflow	07h	7-5,3-0	10h
Vertical Retrace Start	10h	7:0	EFh
Vertical Retrace End	11h	3:0	F2h
Vertical Display End	12h	7:0	EFh
Start Vertical Blank	15h	7:0	EAh
End Vertical Blank	16h	7:0	02h

TABLE 26-5. SHADOWED CRTC REGISTERS

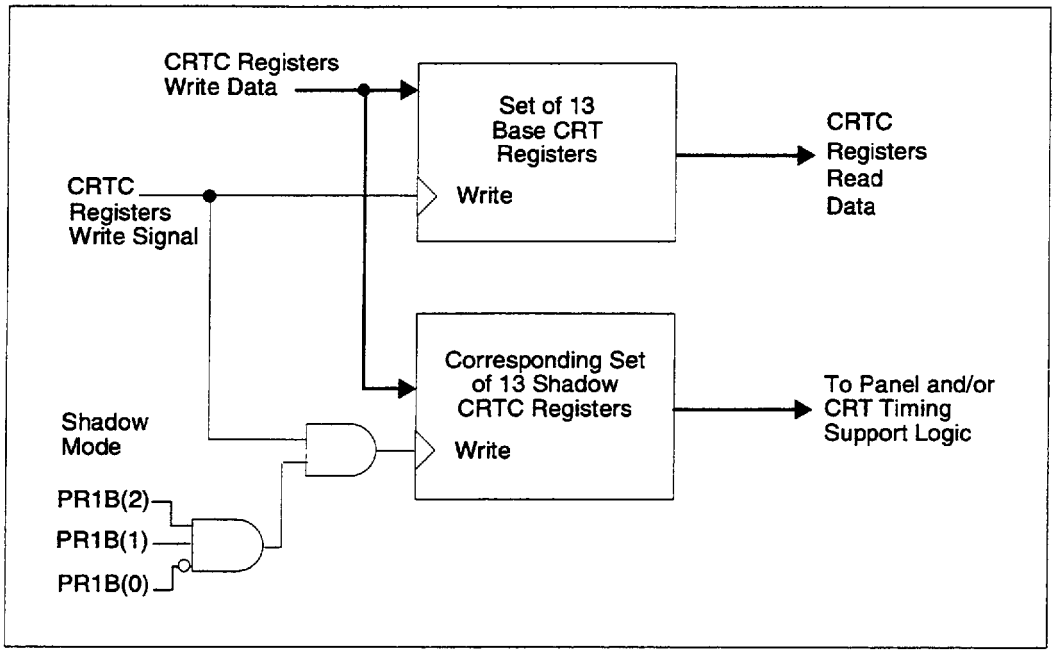


FIGURE 26-16. RELATIONSHIP BETWEEN SHADOW AND BASE CRTC REGISTERS

26.13 ACTIVATING CRT AND FLAT PANEL DISPLAYS

This section describes how to do the following operations:

- Set up the WD90C24A/A2 for flat panel only display mode
- Set up the WD90C24A/A2 for CRT only display mode
- Set up the WD90C24A/A2 for simultaneous display mode with the video image displayed on both a flat panel and a CRT
- Switch from one mode of operation to any other

The WD90C24A/A2 supports flat panel displays using paired CRTC registers that are accessible at the same I/O address. The paired CRTC registers are referred to as:

- Shadow CRTC register
- Base CRTC register

Base registers are used as a method of making the CRTC settings appear unaltered to the system interface when CRTC register settings need to be modified to fit the timing needs of flat panel displays.

Base CRTC registers are mapped to the I/O address of their equivalent Shadow CRTC registers. Base CRTC registers are read on I/O reads. However, Base CRTC registers do not affect CRTC or flat panel timing.

Shadow CRTC registers have direct control over CRTC operation but are not accessed by system reads of the CRTC registers. Writing to the Shadow CRTC registers is enabled by entering shadow mode.

After the shadow CRTC registers are configured for flat panel operation, there values are locked in by exiting shadow mode. Then, any modifications to the CRTC register values that cause video mode changes will not cause corresponding changes to the flat panel configuration. This ensures that flat panel timing remains unchanged.

26.13.1 Flat Panel Only Display

The procedure for configuring the WD90C24A/A2 to support flat panel only display is the same under any of the following circumstances:

- The WD90C24A/A2 is being brought up in Flat-Panel Only Display Mode
- The configuration is being switched from CRTC Only to Flat-Panel Only Display Mode
- The configuration is being switched from simultaneous Display to Flat-Panel Only Mode

Use the following procedure to configure the WD90C24A/A2 to operate in flat-panel only display mode.

NOTE

Perform this procedure outside of any active application.

1. Ensure that a video mode is programmed into the CRTC registers. If a mode is not programmed, the panel power control pins will not be activated by step 9 until panel synchronizing signals are received.
2. Disable both CRT only and flat-panel only display modes by setting PR19 bits 4 and 5 to 0.
3. Configure the Paradise Registers for the particular panel type.
4. Save the current Base CRTC register values.
5. Set PR1B to XXXXX110b to enter shadow mode.
6. Load the Base and Shadow CRTC registers with values appropriate to the panel type.
7. Set PR1B to other than XXXXX110b to exit shadow mode.
8. Reload the saved Base CRTC Register values.
9. Enable flat panel display mode by setting PR19 bit 4 to 1.
10. Sequence flat panel power on after a delay for sync signals to activate.

26.13.2 CRT Only Display

The procedure for configuring the WD90C24A/A2 to support CRT Only Display is the same under any of the following circumstances:

- The WD90C24A/A2 is being brought up in CRT Only Display Mode
- The configuration is being switched from Flat-Panel Only Display Mode to CRT Only display mode.
- The configuration being switched from simultaneous Display Mode to CRT Only Display Mode

Use the following procedure to configure the WD90C24A/A2 to operate in CRT only display mode.

NOTE

Perform this procedure outside of any active application.

1. Sequence panel power off.
2. Disable both CRT and flat panel display modes by setting PR19 bits 4 and 5 to "0".
3. Configure the Paradise Registers for the particular CRT type.
4. Set PR1B to XXXXX110b to enable write to Shadow CRTC Registers.
5. Load the Base and Shadow CRTC registers with values appropriate to the video mode.
6. Enable CRT display mode by setting PR19 bit 5 to 1.

26.13.3 Simultaneous Display Mode

The procedure for configuring the WD90C24A/A2 to support Simultaneous Display Mode is the same under any of the following circumstances:

- The WD90C24A/A2 is being brought up in Simultaneous Display Mode.
- The configuration is being switched from CRTC Only or Flat-Panel Only Display Mode to the Simultaneous Display Mode.

Use the following procedure to configure the WD90C24A/A2 to operate in Simultaneous display mode.

NOTE

Perform this procedure during power-on initialization routines where no previous video mode is being preserved.

1. Sequence panel power off.
2. Disable both CRT and flat-panel display modes by setting PR19 bits 4 and 5 to 0.
3. Configure the Paradise Registers for the particular CRT and panel types.
4. Save the current Base CRTC Register values.
5. Set PR1B to XXXXX110b to enable write to Shadow CRTC Registers.
6. Load the Base and Shadow CRTC registers with simultaneous display values appropriate to the panel type.
7. Set PR1B to other than XXXXX110b to disable write to Shadow CRTC Registers.
8. Restore the Base CRTC Register values appropriate to the video mode.
9. Enable panel and CRT simultaneous display mode by setting PR19 bits 4 and 5 to 1.
10. Sequence the flat panel power on after a delay for sync signals to activate.

NOTE

For dual-panel type flat panel displays, display memory use changes when switching back and forth from single display to simultaneous display operation. Changing to or from simultaneous display mode from within applications is not recommended because the video image is not preserved when switching to or from simultaneous display modes.

27.0 SPECIFICATIONS

The following table lists the specifications for the WD90C24A/A2 controller.

Package Dimensions	Refer to Section 31.
Package temperature range (operating)	$0^{o}C$ to $80^{o}C$ (Refer to note.)
Storage Temperature	$-40^{o}C$ to $125^{o}C$
Power Supply Voltage	6.0 Volts
Voltage on all inputs and outputs with respect to V_{SS}	V_{SS} -0.3 to 7 Volts
Power Dissipation	1 Watt maximum
Electrostatic Discharge (ESD)	**REFER TO NOTE 3** All Pins except those listed below will withstand 1200V Human Body Model (HBM). The following pins will withstand 1000V HBM: CKIN, IOCS16, PDOWN, REFRESH, RESET, SD9 The following pins will withstand 800V HBM: PD[29:16], IRQ,
Latch up Threshold	+/- 100 mA
Input Current	+/– 20 mA

NOTE:

1. The package temperature of $80^{o}C$ corresponds approximately to a $70^{o}C$ ambient temperature when the WD90C24A/A2 is mounted on FR4 or equivalent PC board material.
2. Unless otherwise specified, the values given in this table are absolute maximum ratings.
3. The ESD listed above is for the WD90C24A Controller. ESD for the WD90C24A2 Controller is listed in Appendix C.

TABLE 27-1. SPECIFICATIONS

CAUTION

Stresses above those listed in the table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

28.0 DC ELECTRICAL SPECIFICATIONS

This section provides the DC electrical specifications for the WD90C24A/A2 controller. The following information is contained in this section:

- DC Power Distribution
- Internal Clock DC Characteristics
- DC Electrical Specifications for Mixed DC Voltage Operation
- DC Electrical Specifications for 3.3 VDC Operation
- Pin Capacitance

28.1 DC POWER DISTRIBUTION

The WD90C24A/A2 Controller supports a supply voltage of 3.3 VDC, or a mix of 3.3 VDC and 5.0 VDC supply voltages. This allows the WD90C24A/A2 to be used in situations where portions of the design operate at 3.3 VDC for power savings, while other portions operate at the traditional 5.0 VDC for interface compatibility. Table 28-1 lists the power level required for each power designator depending upon which power configuration is used. Table 28-2 lists each WD90C24A/A2 pin with its associated power designator and signal name mnemonic. Table 28-3 lists the Internal Clock DC characteristics.

When operating in the mixed voltage configuration, the following 3.3 VDC-powered buffers can be driven with 5.0 VDC signals:

RESET	$\overline{\text{REFRESH}}$
CKIN	$\overline{\text{PDOWN}}$

The following pins have internal pullup resistors (minimum value = 75K ohms):

AMD[15:0]	BMD[15:0]
SA[31:24]	

The following pins have internal pulldown resistors (minimum value = 75K ohms):

CLK486 CKIN

POWER DESIGNATOR	OPERATING DC VOLTAGE		DEEP SLEEP POWER DOWN DC VOLTAGE	
	3.3V ONLY	MIXED	3.3V ONLY	MIXED
VDD (Core)	3.3	3.3	0	0
PVDD	3.3	3.3	3.3	3.3
BVDD	3.3	Refer to Note 1	0	0
MVDD	3.3	Refer to Note 1	3.3	Refer to Note 1
FPVDD	3.3	Refer to Note 1	0	0
RVDD	3.3 Refer to Note 2	3.3 Refer to Note 2	0	0
AVDD1	3.3	Refer to Note 1	0	0
AVDD2	3.3	3.3	0	0

NOTES:

1. For mixed voltage operation, this voltage can be either 3.3 VDC or 5.0 VDC, regardless of any other operating voltage.
2. For operation at 3.3 VDC, the minimum (MIN) VDC tolerance is -5% and the maximum (MAX) VDC tolerance is +10%. For operation at 5 VDC, the minimum and maximum VDC tolerances are ±5%, respectively.
3. For the WD90C24A2, RVDD must be 4.3 VDC ±5% to support the 65 MHz clock required for 1024 by 768 non-interlaced mode at a 60 Hz refresh rate.

TABLE 28-1. WD90C24A/A2 POWER DISTRIBUTION

PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR	PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR
1	BMD0	MVDD	36	VSS	---
2	BMD15	MVDD	37	PD29	BVDD
3	BMD1	MVDD	38	PD28	BVDD
4	BMD14	MVDD	39	PD27	BVDD
5	VSS	---	40	PD26	BVDD
6	BMD2	MVDD	41	PD25	BVDD
7	BMD13	MVDD	42	PD24	BVDD
8	BMD3	MVDD	43	VDD	---
9	BMD12	MVDD	44	PD23	BVDD
10	VDD	---	45	PD22	BVDD
11	BMD4	MVDD	46	PD21	BVDD
12	BMD11	MVDD	47	PD20	BVDD
13	BMD5	MVDD	48	VSS	BVDD
14	BMD10	MVDD	49	PD19	BVDD
15	BMD6	MVDD	50	PD18	BVDD
16	BMD9	MVDD	51	PD17	BVDD
17	BMD7	MVDD	52	PD16	BVDD
18	BMD8	MVDD	53	SD15	BVDD
19	MVDD	---	54	SD14	BVDD
20	$\overline{\text{BCASL}}$	MVDD	55	SD13	BVDD
21	VSS	---	56	SD12	BVDD
22	$\overline{\text{BWE}}$	MVDD	57	BVDD	---
23	$\overline{\text{BCASH}}$	MVDD	58	SD11	BVDD
24	$\overline{\text{BRAS}}$	MVDD	59	SD10	BVDD
25	$\overline{\text{BOE}}$	MVDD	60	SD9	BVDD
26	VDD	---	61	SD8	BVDD
27	BMA8	MVDD	62	VSS	---
28	BMA0	MVDD	63	SLA17	BVDD
29	BMA7	MVDD	64	SLA18	BVDD
30	BMA1	MVDD	65	SLA19	BVDD
31	BMA6	MVDD	66	SLA20	BVDD
32	BMA2	MVDD	67	SLA21	BVDD
33	BMA5	MVDD	68	SLA22	BVDD
34	BMA3	MVDD	69	SLA23	BVDD
35	BMA4	MVDD	70	CLK486	BVDD

TABLE 28-2. DC POWER DISTRIBUTION

PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR	PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR
71	IOCS16I BOFF	BVDD	99	IOWI BE1	BVDD
72	MEMCS16I PD31	BVDD	100	MEMRI M/IO	BVDD
73	SBHEI CPURESET	BVDD	101	MEMWI W/R	BVDD
74	ALEI ADS	BVDD	102	AVDD1	---
75	IRQI PD30	BVDD	103	XMCLK	RVDD
76	EIOI BE0	BVDD	104	MCAP	AVDD1
77	IOCHRDYI CPURDY	BVDD	105	VCAP	AVDD1
78	ZWSTI VLBI BUSY	BVDD	106	VCLK2	RVDD
79	VSS	---	107	AVSS1	---
80	SA0I BE3	BVDD	108	RVSS	---
81	SA1I BE2	BVDD	109	SD0	BVDD
82	SA2	BVDD	110	SD1	BVDD
83	SA3	BVDD	111	SD2	BVDD
84	SA4	BVDD	112	SD3	BVDD
85	SA5	BVDD	113	BVDD	---
86	SA6	BVDD	114	SD4	BVDD
87	SA7	BVDD	115	SD5	BVDD
88	RVDD	---	116	SD6	BVDD
89	SA8	BVDD	117	SD7	BVDD
90	SA9	BVDD	118	VSS	---
91	SA10	BVDD	119	XSCLKLI XSCLKUI BD5	FPVDD
92	SA11	BVDD	120	WPLT/BD4	FPVDD
93	SA12	BVDD	121	RPLTI BD3I STN15I BD3I VD7	FPVDD
94	SA13	BVDD	122	STN14I BD2I BD2I VD6	FPVDD
95	SA14	BVDD	123	STN13I BD1I BD1I VD5	FPVDD
96	SA15	BVDD	124	STN12I BD0I BD0I VD4	FPVDD
97	SA16	BVDD	125	VDD	---
98	IORI D/C	BVDD	126	STN11I GD5I VD3	FPVDD

TABLE 28-2. DC POWER DISTRIBUTION (Continued)

PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR	PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR
127	STN10|GD4|VD2	FPVDD	156	VREF	AVDD2
128	STN9|RD5|VD1	FPVDD	157	BLUE	AVDD2
129	STN8|RD4|VD0	FPVDD	158	GREEN	AVDD2
130	FPVDD	---	159	RED	AVDD2
131	VUD3|RD3|RD3| STN7|LD7|VD7	FPVDD	160	AVSS2	---
132	VUD2|RD2|RD2| STN6|LD6|VD6	FPVDD	161	EXCKEN	PVDD
133	VUD1|RD1|RD1| STN5|LD5|VD5	FPVDD	162	RESET|SYSRES	PVDD
134	VUD0|RD0|RD0| STN4|LD4|VD4	FPVDD	163	$\overline{\text{PDOWN}}$	PVDD
135	VLD3|GD3| STN3|LD3|VD3	FPVDD	164	$\overline{\text{LCDENA}}$	PVDD
136	VLD2|GD2| STN2|LD2|VD2	FPVDD	165	PNLOFF	PVDD
137	VLD1|$\overline{\text{GD1}}$| STN1|LD1|VD1	FPVDD	166	$\overline{\text{REFRESH}}$|$\overline{\text{RDYIN}}$	PVDD
138	VLD0|GD0| STN0|LD0|VD0	FPVDD	167	FPUSR0	PVDD
139	VSS	---	168	VCLK|FPUSR1	PVDD
140	XSCLK| XSCLKL| XSCLKU	FPVDD	169	PVDD	---
141	RVDD	---	170	CKIN|VCLK	PVDD
142	LP	FPVDD	171	$\overline{\text{EBROM}}$|$\overline{\text{REFLCL}}$	BVDD
143	FP	FPVDD	172	$\overline{\text{VLBICS}}$	BVDD
144	FR|$\overline{\text{BLANK}}$|ENDATA	FPVDD	173	VSYNC	BVDD
145	RVSS	---	174	HSYNC	BVDD
146	SA24	BVDD	175	PCLK	BVDD
147	SA25	BVDD	176	VSS	---
148	SA26	BVDD	177	AMD0	MVDD
149	SA27	BVDD	178	AMD15	MVDD
150	SA28	BVDD	179	AMD1	MVDD
151	SA29	BVDD	180	AMD14	MVDD
152	SA30	BVDD	181	AMD2	MVDD
153	SA31	BVDD	182	AMD13	MVDD
154	AVDD2	---	183	AMD3	MVDD
155	$\overline{\text{MDETECT}}$|FSADJ	AVDD2	184	AMD12	MVDD

TABLE 28-2. DC POWER DISTRIBUTION (Continued)

PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR	PIN NO.	SIGNAL MNEMONIC	POWER DESIGNATOR
185	AMD4	MVDD	197	$\overline{\text{ACASH}}$	MVDD
186	AMD11	MVDD	198	$\overline{\text{ARAS}}$	MVDD
187	AMD5	MVDD	199	$\overline{\text{AOE}}$	MVDD
188	AMD10	MVDD	200	AMA8	MVDD
189	AMD6	MVDD	201	AMA0	MVDD
190	AMD9	MVDD	202	AMA7	MVDD
191	AMD7	MVDD	203	AMA1	MVDD
192	AMD8	MVDD	204	AMA6	MVDD
193	MVDD	---	205	AMA2	MVDD
194	$\overline{\text{ACASL}}$	MVDD	206	AMA5	MVDD
195	VSS	---	207	AMA3	MVDD
196	$\overline{\text{AWE}}$	MVDD	208	AMA4	MVDD

TABLE 28-2. DC POWER DISTRIBUTION (Continued)

28.2 INTERNAL CLOCK DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
Vil	Input Low Voltage	VSS	0.8	V	
Vih	Input High Voltage	2.0	VDD	V	
Iil	Input Leakage Current	--	±10	µA	VSS < Vin < VDD
Cin	Input Pin Capacitance	--	8	pF	Fc = 1 MHz
Idd	Current Consumption in Normal Operation	--	278	mA	VDD = 3.3 V

TABLE 28-3. INTERNAL CLOCK DC CHARACTERISTICS

28. 3 DC ELECTRICAL SPECIFICATION

This subsection contains the following tables:

- Power Supply Voltage for Mixed DC Voltage Operation
- Power Supply Voltage for 3.3 VDC Operation
- Typical Current/Power Consumption for 3.3 VDC Operation
- Input Pin Characteristics
- Output Pin Characteristics
- I/O Pin Characteristics
- Pin Capacitance

28.3.1 Power Supply Voltage for Mixed DC Voltage Operation

The following DC electrical specifications apply to the WD90C24A/A2 operating in a mixed DC voltage environment. Refer to Tables 28-2 and 28-4 for information on which pins operate at 3.3 VDC in a mixed voltage environment.

SUPPLY	MIN (VDC)	MAX (VDC)	PINS	COMMENTS
VDD	3.135	3.6	10, 26, 43, 125	Power for core logic
AVDD1	3.135/ 4.75	3.6/5.25	102	PCLK Analog Input and Clock Power
AVDD2	3.135	3.6	154	Analog Power for Internal RAMDAC
BVDD	3.135/ 4.75	3.6/5.25	57, 113	Bus Power for System Clock and CRT sync Interfaces
MVDD	3.135/ 4.75	3.6/5.25	19, 193	Power for Display Memory Interface
FPVDD	3.135/ 4.75	3.6/5.25	8, 132, 130	Power for Flat Panel Interface
PVDD	3.135	3.6	169	Power-Down Power
RVDD	3.135 Refer to Note 3	3.6 Refer to Note 3	88, 141	RAM Filtered Palette Power
VSS, AVSS1, AVSS2, RVSS	0.0	0.0	5, 36, 62, 79, 107, 108, 118, 139, 145, 176, 195	Grounds

NOTES:

1. Where two values are listed:
   a. The lesser value applies to operation at 3.3 VDC and the greater value applies to operation at 5.0 VDC.
   b. Any multivoltage pin can operate at either value without regard to the value applied to other pins.
2. For operation at 3.3 VDC, the minimum (MIN) VDC tolerance is -5% and the maximum (MAX) VDC tolerance is +10%. For operation at 5 VDC, the minimum and maximum VDC tolerances are ±5%, respectively.
3. For the WD90C24A2, RVDD must be 4.3 VDC ±5% to support the 65 MHz clock required for 1024 by 768 non-interlaced mode at a 60 Hz refresh rate.

TABLE 28-4. POWER SUPPLY VOLTAGE FOR MIXED DC VOLTAGE OPERATION

28.3.2 Power Supply Voltage for 3.3 VDC Operation

The following DC electrical specifications apply to the WD90C24A/A2 operating at 3.3 VDC. Refer to the previous section for DC electrical specifications when the WD90C24A/A2 is operating in a Mixed DC voltage environment. When a WD90C24A/A2 is used in mixed voltage applications, the specifications in this section apply to those pins powered by a 3.3 VDC supply. Refer to Tables 28-1 and 28-2 for information on which pins operate at 5 VDC in a mixed voltage environment

SUPPLY	MIN (VDC)	MAX (VDC)	PINS	COMMENTS
VDD	3.135	3.6	10, 26, 43, 125	Power for core logic
AVDD1	3.135	3.6	102	PCLK Analog Input and Clock Power
AVDD2	3.135	3.6	154	Analog Power for Internal RAMDAC
BVDD	3.135	3.6	57, 113	Bus Power for System Clock and CRT sync Interfaces
MVDD	3.135	3.6	19, 193	Power for Display Memory Interface
FPVDD	3.135	3.6	8, 132, 130	Power for Flat Panel Interface
PVDD	3.135	3.6	169	Power-Down Power
RVDD	3.135 Refer to Note 2	3.6 Refer to Note 2	88, 141	RAM Filtered Palette Power
VSS, AVSS1, AVSS2, RVSS	0.0	0.0	5, 36, 62, 79, 107, 108, 118, 139, 145, 176, 195	Grounds

NOTES:

1. For operation at 3.3 VDC, the minimum (MIN) VDC tolerance is -5% and the maximum (MAX) VDC tolerance is +10%.
2. For the WD90C24A2, RVDD must be 4.3 VDC ±5% to support the 65 MHz clock required for 1024 by 768 non-interlaced mode at a 60 Hz refresh rate.

TABLE 28-5. POWER SUPPLY VOLTAGE FOR 3.3 VDC OPERATION

28.3.3 Typical Current/Power Consumption For 3.3 VDC Operation

Table 28-6 lists the typical current and power consumption for operation at 3.3 VDC.

MODE	CRT/PANEL FREQUENCY				
	25 MHZ	28 MHZ	32MHZ	36 MHZ	45MHZ
Display Active, LCD Only	125 mA 412 mW	132 mA 435 mW	140 mA 462 mW	149 mA 491 mW	160 mA 528 mW
Display Active, CRT Only	160 mA 528 mW	170 mA 561 mW	180 mA 594 mW	195 mA 643 mW	215 mA 709 mW
Display Active, Single Panel Simultaneous Display	170 mA 561 mW	180 mA 594 mW	190 mA 627 mW	205 mA 676 mW	225 mA 742 mW
Display Active, Dual Panel Simultaneous Display	180 mA 594 mW	190 mA 627 mW	200 mA 660 mW	215 mA 709 mW	235 mA 775 mW
System Power Down[1]	5 mA 25 mW	5 mA 25 mW	5 mA 25 mW	5 mA 25 mW	5 mA 25 mW
Display Idle	30 mA 99 mW	33 mA 110 mW	39 mA --- mW	42 mA --- mW	50 mA 165 mW
General Power-Down with Internal Clock Control[2]	30 mA 99 mW	33 mA 110 mW	39 mA --- mW	42 mA --- mW	50 mA 165 mW

NOTES

Conditions: V_{DD}=BV_{DD}=PV_{DD}=RV_{DD}=3.3V, AV_{DD}=3.3V. Typical windowed application displayed. VCLK = CRT/Panel Frequency (unless otherwise noted). MCLK = 44.3 MHz (unless otherwise noted). System configured with 256K x 8 70 nsec display memory.

[1]VCLK = MCLK = 0 Hz.

[2]All power except MVDD and PVDD is disconnected.

TABLE 28-6. TYPICAL CURRENT/POWER CONSUMPTION FOR 3.3 VDC OPERATION

28.3.4 Internal Voltage Detector Operation

Table 28-7 lists the internal voltage detector minimum and maximum values.

VOLTAGE MODE	MINIMUM	MAXIMUM
3.3 VDC Detection	---	3.8
5.0 VDC Detection	4.2	---

TABLE 28-7. INTERNAL VOLTAGE DETECTOR OPERATION

28.3.5 Input Pin Characteristics

NOTE

Refer to Tables 28-2 and 28-4 for signal pin numbers and the minimum and maximum voltage values to reference for each signal.

Table 28-8 provides the DC input characteristics for the following signals:

PDOWN	REFRESH/RDYIN	REFLCL
MEMW/W/R	MEMR/M/IO	CLK486
ALE/ADS	IOR/D/C	IOW/BE1
EIO/BE0	VCLK/CKIN	XMCLK
SA0/BE3	SA1/BE2	SA[16:2]
SLA23-SLA17	SA24	SA[31:25]
SBHE/CPURESET	EXCKEN	MCAP
VCAP		

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.5	$VDD_{MIN} < VDD < VDD_{MAX}$
I_{IL}	-10 µA	+10 µA	V_{IN} = 0V to VDD

TABLE 28-8. INPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-9 provides the DC input characteristics for the following signals:

RESETI/SYSRES MDETECT/IFSADJ

PARAMETER	MINIMUM	MAXIMUM	CONDITIONS
V_{IL}	-0.5V	0.5V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	VDD-0.5V	VDD+0.5	$VDD_{MIN} < VDD < VDD_{MAX}$
I_{IL}	-10 µA	+10 µA	V_{IN} = 0V to VDD

TABLE 28-9. INPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

28.3.6 Output Pin Characteristics

NOTE

Refer to Tables 28-2 and 28-4 for signal pin numbers and the minimum and maximum voltage values to reference for each signal.

Table 28-10 provides the DC output pin voltage/current characteristics for the following signals:

AMA8	AMA[7:0]	$\overline{AOE}$
BMA8	BMA[7:0]	$\overline{BOE}$
	$\overline{WPLT}$IBD4	$\overline{ACASH}$
$\overline{ACASL}$	$\overline{ARAS}$	$\overline{AWE}$
$\overline{BCASH}$	$\overline{BCASL}$I	$\overline{BRAS}$
$\overline{BWE}$	$\overline{RPLT}$STN15IBD3IUD7I	STN14IBD2IUD6
STN13IBD1IUD5	STN12IBD0IUD4I	STN11IGD5IUD3
STN10IGD4IUD2	STN9IGD5IUD1I	STN8IRD4IUD0
FPUSR0	XSCLKIXSCLKLIXSCLKUIBD5	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 3.0 mA VDD_{MIN} < VDD < VDD_{MAX}
V_{OH}	2.4V		I_{OH} = 3.0 mA VDD_{MIN} < VDD < VDD_{MAX}
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD

TABLE 28-10. OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-11 provides the DC output pin voltage/current characteristics for the following signals:

$\overline{LCDENA}$	LP	FP
XSCLKIXSCLKLIXSCLKU	PNLOFF	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 5.0 mA VDD_{MIN} < VDD < VDD_{MAX}
V_{OH}	2.4V		I_{OH} = 5.0 mA VDD_{MIN} < VDD < VDD_{MAX}
I_{OZ} (Where Applicable)	-10 µA	+10 µA	V_{OUT} = 0V to VDD

TABLE 28-11. OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-12 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Tables 28-2 and 28-4 for signal pin numbers and the minimum and maximum voltage values to reference for each signal.

$\overline{IOCS16}$|$\overline{BOFF}$ $\overline{IOCHRDY}$|$\overline{CPURDY}$

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 16.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH} (Where Applicable)	2.4V		I_{OH} = 8.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ}		10 µA	V_{OUT} = 0V to VDD

TABLE 28-12. OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-13 provides the DC output pin voltage/current characteristics for the following signals:

HSYNC VSYNC FRI$\overline{BLANK}$|ENDATA

FPUSR1|VCLK1

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 5.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 3.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$

TABLE 28-13. OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-14 provides the DC output pin voltage/current characteristics for the following signal:

$\overline{VLBICS}$

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 8.0 mA (Refer to Note) $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 5.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
NOTE: I_{OL} is listed for WD90C24A. For WD90C24A2, I_{OL} = 16 mA.			

TABLE 28-14. OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS

28.3.7 I/O Pin Characteristics

NOTE

Refer to Tables 28-2 and 28-4 for signal pin numbers and the minimum and maximum voltage values to reference for each signal.

Table 28-15 provides the DC input/output pin voltage and current characteristics for the following signals:

AMD[15:0] PD[29:16] BMD[15:0]I
IRQ/PD30

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	I_{OL} = 3.0 mA (Refer to Note) $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 3.0 mA (Refer to Note) $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD
NOTE: This note applies to the PD[30:16] lines only: The I_{OL}/I_{OH} for WD90C24A is listed. For the WD90C24A2, I_{OL}/I_{OH} = 8 mA			

TABLE 28-15. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-16 provides the DC input/output pin voltage and current characteristics for the following signals:

VUD[3:0] VLD[3:0] VCLK2

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	I_{OL} = 5.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 5.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD

TABLE 28-16. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-17 provides the DC input/output pin voltage and current characteristics for the following signals:

SD[15:0]

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	IOL =8.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		IOH = 7.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	VOUT = 0V to VDD

TABLE 28-17. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-18 provides the DC input/output pin voltage and current characteristics for the following signals:

$\overline{BOFF}$ $\overline{ZWST}$ $\overline{MEMCS16}$/PD31

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	I_{OL} = 16.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 8.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD

TABLE 28-18. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-19 provides the DC input/output pin voltage and current characteristics for the following signals:

PCLK

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	I_{OL} = 5.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} =3.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD

TABLE 28-19. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

Table 28-20 provides the DC input/output pin voltage and current characteristics for the following signals:

$\overline{EBROM}$

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{IH}	2.0V	VDD+0.6	$VDD_{MIN} < VDD < VDD_{MAX}$
V_{OL}		0.4 V	I_{OL} = 2.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
V_{OH}	2.4V		I_{OH} = 2.0 mA $VDD_{MIN} < VDD < VDD_{MAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to VDD

TABLE 28-20. I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS

28.4 PIN CAPACITANCE

This section lists the pin capacitance for all of the WD90C24A/A2 input, output and I/O pins. This capacitance does not change significantly between 5 VDC and 3.3 VDC operation.

Table 28-21 lists the capacitance for all pins with output only signals:

ALL OUTPUT ONLY PINS		
PINS	**MAX**	**CONDITIONS**
C_{OUT}	20 pF	F_C = 1 MHz

TABLE 28-21. CAPACITANCE FOR OUTPUT ONLY PINS

Table 28-22 lists the capacitance for all pins with input only signals:

ALL INPUT ONLY PINS		
PINS	**MAX**	**CONDITIONS**
C_{IN}	7 pF	F_C = 1 MHz

TABLE 28-22. CAPACITANCE FOR INPUT ONLY PINS

Table 28-23 lists the capacitance for all pins that provide both input and output paths for signals:

ALL INPUT/OUTPUT PINS		
PINS	**MAX**	**CONDITIONS**
C_{OUT}	20 pF	F_C = 1 MHz
C_{IN}	7 pF	F_C = 1 MHz

TABLE 28-23. CAPACITANCE FOR INPUT/OUTPUT (I/O) PINS

29.0 INTERNAL DAC SPECIFICATIONS

Table 29-1 lists the specifications for the RED, GREEN, and BLUE DACs from the internal RAMDAC of the WD90C24A/A2 controller (see Figure 23-1).

PARAMETER	MIN	TYP	MAX	CONDITIONS
DAC Resolution	6 Bits per Output			
Integral Linearity Error			1/2 LSB	Least Squares Fit
Differential Linearity Error			1/2 LSB	Least Squares Fit
White Level	13.3 mA	14.0 mA	14.7 mA	VREF = 1.235V, RSET = 11.0K Ω
Black Level	-20 µA		+20 µA	
Gray Scale Current Range			17 mA	
LSB Size		222 µA		V_{REF} = 1.235V, R_{SET} = 11.0K Ω
Gray Scale Error			5%	
Glitch Energy			50 pJ	
Settling Time			20 ns	100 pF Load
Clock Feed Through			20 pC	
DAC to DAC Matching			5%	
Output Compliance Current Tolerance	-5%		+5%	
Output Compliance Voltage Range	-0.25V		+1.5V	
Voltage Reference (VREF) Range	1.14V	1.235V	1.26V	**NOTE:** Do not ground the VREF input pin at any time.
Voltage Reference Input Current (VREF) Refer to NOTE			10 µA	
RSET Value, FSADJ Input		11.0K		50 Ω Load
Input Current, $\overline{\text{MDETECT}}$			10 µA	External RAMDAC Mode, PR18 bit 7 = 1
DAC Power-on Time			70 µs	Measured from RESET high-to-low or $\overline{\text{PDOWN}}$ low-to-high
DAC Power-off Time			20 µs	Measured from RESET low-to-high or $\overline{\text{PDOWN}}$ high-to-low

TABLE 29-1. DAC SPECIFICATIONS

30.0 AC TIMING CHARACTERISTICS

30.1 INTRODUCTION

This section describes the WD90C24A/A2 timing characteristics. It contains the following tables and their corresponding diagrams where applicable.

- Internal Clock AC Characteristics
- Clock and External RAMDAC Timing
- Reset Timing
- I/O and Memory Read/Write Timing in ISA(AT) Bus Mode
- VESA VL-Bus Interface Timing
- DRAM Timing
- Dual-Panel Monochrome LCD Functional Timing, Panel Only Mode (No CRT)
- Color STN LCD Interface Functional Timing
- TFT Panel AC Timing
- TFT Panel Functional Timing
- RAMDAC Timing
- $\overline{CAS}$-Before-$\overline{RAS}$ DRAM Refresh Timing
- Display Idle/Sleep Mode AC-Timed $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Timing
- Self-Refresh Timing, Sleep/Display Modes
- Timing Parameter Measurement Information

NOTE

Unless otherwise specified, AC Timing is with respect to Vil/Vih = 0.4/2.4 and Vol/Voh = 0.8/2.0.

30.2 INTERNAL CLOCK AC CHARACTERISTICS

The following conditions apply to all of the AC parameters presented in this section:

- CKIN = 14.31818 MHz
- All units are in nanoseconds (ns) unless otherwise specified.
- Maximum jitter measurements were taken within a range of 30 µs after triggering on a 400 MHz scope.
- Internal CLK rise and fall time between 0.8 and 2.0V at the output of the PCLK.
- External Clock Mode rise and fall time between 0.8 and 2.0V.
- Internal duty cycle measured at 1.4V, at the output of the PCLK.
- External Clock Mode duty cycle measured at 1.4V.

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
Reference Input Clock				
tr	Rise Time	--	10	0.8 to 2.0 VDC
tf	Fall Time	--	10	2.0 to 0.8 VDC
tj	Phase Jitter	--	1	
--	Duty Cycle	42.5%	57.5%	Measured at 1.4 V.
External Input Clock				
tr	Rise Time	--	3	0.8 to 2.0 VDC
tf	Fall Time	--	3	2.0 to 0.8 VDC
tjv	VCLK Jitter	--	3	
tjm	MCLK Jitter	--	5	
--	Duty Cycle	40%	60%	Measured at 1.4 V.
Internal MCLK & VCLK Timing				
tr	Rise Time	--	3	
tf	Fall Time	--	3	
tjv	VCLK Jitter	0	3	
tjm	MCLK Jitter	0	5	
--	Duty Cycle	40%	60%	Measured at 1.4 V.
--	Frequency Error	--	±0.5%	
--	Frequency Range	25	65	MHz
PCLK Specification				
---	Power-on Time	---	50 ms	
	Power-off Time	---	50 ns	
	Settling Time	---	20 ms	

TABLE 30-1. AC TIMING CHARACTERISTICS

30.3 CLOCK AND EXTERNAL RAMDAC TIMING

The clock and external RAMDAC timing is listed in Table 30-2 and shown in Figure 30-1.

NO.	SYMBOL/PARAMETER	MIN[4]	MAX[4]	CONDITIONS
1	VCLK Period[1, 2]	12.5[3]	72.5	13.8 to 65 MHz
2	VCLK High Duty Cycle [1]	40%	60%	% of period
3	VCLK Low Duty Cycle[1]	40%	60%	% of period
4	VCLK, MCLK Clock Rise Time[1]	-	3	0.8 to 2.0V
5	VCLK, MCLK Clock Fall Time[1]	-	3	2.0 to 0.8V
6	VCLK High to PCLK low Delay[1,5]	8	45	max @ 120 pF load
7a	VCLK High to HSYNC active Delay[1]	8	35	
7b	VCLK High to VSYNC active Delay[1]	8	35	
7c	VCLK High to $\overline{\text{BLANK}}$ active Delay[1]	8	30	
7d	VCLK High to VD[7:0], LD[7:0] Delay[1]	8	30	45ns max @120 pF load up to 45 MHz data rate
8	MCLK Period[3,2]	20	25	40 to 50 MHz
9	MCLK High Duty Cycle	40%	60%	
10	MCLK Low Duty Cycle	40%	60%	
11	VD[7:0], LD[7:0] setup to PCLK	3		
12	VD[7:0], LD[7:0] hold from PCLK	3		

NOTES

TA = 25°C, at V_{DD} pins = 3.3 VDC.

Timing specifications for 3.3 VDC operation are measured from a 1.4V switch point unless otherwise noted.

[1]VCLK = Selected VCLK source: VCLK, VCLK1, VCLK2, or MCLK, or selected frequency applied to CKIN.

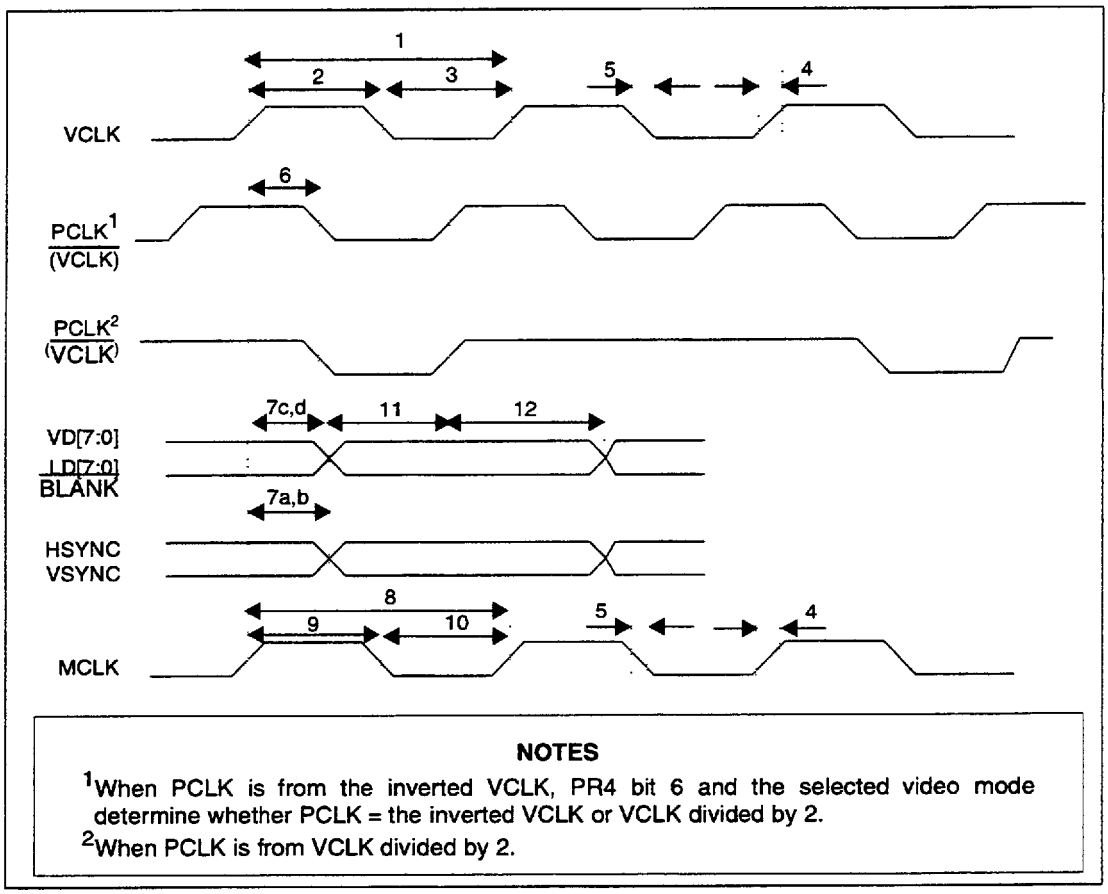
[2]Operational. Clocks may be stopped or slowed down further for power reduction purposes with limited operation.

[3]$VCLK_{max}$ = 65 MHz for 3.3 VDC operation, CRT only display. $VCLK_{max}$ = 65 MHz for flat panel only operation or for simultaneous display with single-panel type flat panels. $VCLK_{max}$ = 45 MHz for simultaneous display when using a dual panel-type flat panel.

[4]Numbers listed are in nanoseconds unless other units are given.

[5]Maximum delay is the same for PCLK = inverted VCLK or PCLK = VCLK divided by 2.

TABLE 30-2. CLOCK AND EXTERNAL RAMDAC TIMING



NOTES

[1]When PCLK is from the inverted VCLK, PR4 bit 6 and the selected video mode determine whether PCLK = the inverted VCLK or VCLK divided by 2.

[2]When PCLK is from VCLK divided by 2.

FIGURE 30-1. CLOCK AND EXTERNAL RAMDAC TIMING

30.4 RESET TIMING

The reset timing is listed in Table 30-3 and shown in Figure 30-2.

NO.	SYMBOL/PARAMETER	MIN[1]	MAX[1]	CONDITIONS
1	Reset Pulse Width	600		≥10t where t = $^1/_{MCLK}$
2	AMD[15:0], BMD[15:0] Setup to RESET low		50	For hardware configuration options
3	AMD[15:0], BMD[15:0] Hold from RESET low		30	For hardware configuration options
4	RESET low to first $\overline{IOW}$		600	≥10t where t = $^1/_{MCLK}$
[1]Values listed are in nanoseconds unless otherwise noted.				

TABLE 30-3. RESET TIMING

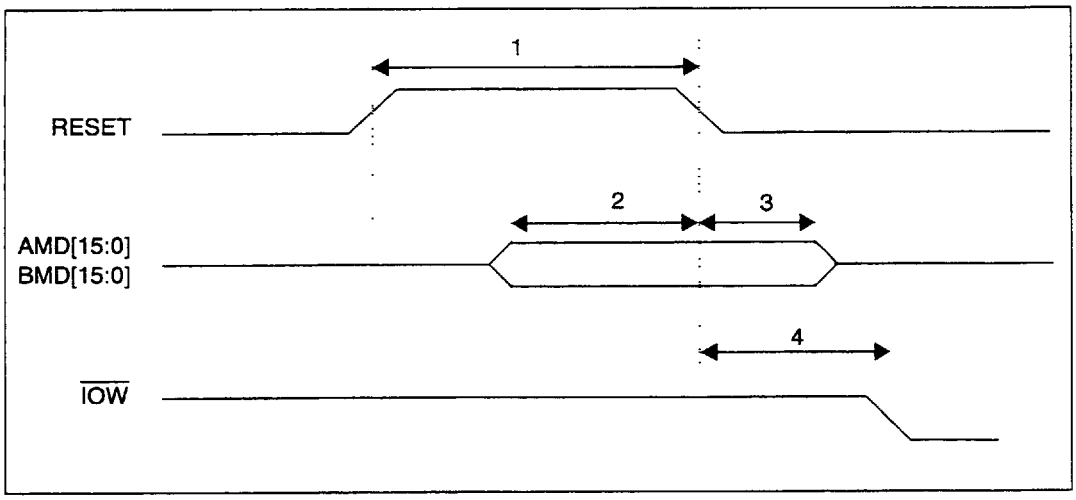


FIGURE 30-2. RESET TIMING

30.5 I/O AND MEMORY READ/WRITE TIMING IN ISA (AT) MODE

The I/O and memory read/write timing in ISA (AT) bus mode is listed in Table 30-4 and shown in Figure 30-3.

NO.	SYMBOL / PARAMETER	MIN	MAX	CONDITIONS
1	$\overline{SBHE}$, SA[16:0] setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ low	20		
2	$\overline{SBHE}$, SA[16:0] hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$,$\overline{MEMW}$ low	15		
3	SLA[23:17] setup to ALE low	20		
4	SLA[23:17] hold from ALE low	10		
5	$\overline{EIO}$ setup to $\overline{IOR}$ / $\overline{IOW}$ low	20		
6	$\overline{EIO}$ hold from $\overline{IOR}$ / $\overline{IOW}$ high	10		
7	SD[15:0] write data setup before $\overline{IOW}$, $\overline{MEMW}$ high	20		Write buffer on and not full.
7A	SD[15:0] write data valid after $\overline{MEMW}$ low		3t	Write buffer off or full.
8	SD[15:0] write data hold from $\overline{IOW}$ or $\overline{MEMW}$ high	10		
10	SD[15:0] read data valid from $\overline{IOR}$ low	20	2t + 20	See note 1.
10A	SD[15:0] read data valid from $\overline{IOR}$ low (For mapping RAM, t = 1/VCLK		2t + 50	
10B	SD[15:0] read data hold from $\overline{IOR}$, $\overline{MEMR}$ high	5	20	
11	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ high Cycle Recovery Time	2t + 20		
12	$\overline{IOCHRDY}$ high from $\overline{MEMR}$, $\overline{MEMW}$ low		2.67 µs	See note 2.
13	Memory read data valid from $\overline{IOCHRDY}$ high		40	
14	$\overline{ZWST}$, low from $\overline{IOW}$, $\overline{MEMW}$ low		40	
15	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ low pulse width	2t + 20		
15A	$\overline{IOW}$ low pulse width (I/O Port 3C2h)	2t + 50		
16	$\overline{ZWST}$, tristate after $\overline{IOW}$, $\overline{MEMW}$ high		20	
17	$\overline{IOCHRDY}$ low from $\overline{MEMW}$ / $\overline{MEMR}$ low	0	30	
17A	$\overline{IOCHRDY}$ low from $\overline{IOW}$ low	10	30	
18	$\overline{IOCHRDY}$ tristate from $\overline{MEMW}$ / $\overline{MEMR}$ high	0	30	
18A	$\overline{IOCHRDY}$ tristate from $\overline{IOW}$ high	10	30	
19	$\overline{EBROM}$ low from valid SLA[23:17] and SA[16:0]		40	
20	$\overline{EBROM}$ hold from $\overline{MEMR}$ high		45	
20A	$\overline{EBROM}$ low from $\overline{IOW}$ low (46E8h port)		1.5t + 40	
20B	$\overline{EBROM}$ high from $\overline{IOW}$ high (46E8h port)		45	
21	$\overline{WPLT}$ low from $\overline{IOW}$ low		60	

TABLE 30-4. I/O AND MEMORY READ / WRITE TIMING IN ISA(AT) MODE

NO.	SYMBOL / PARAMETER	MIN	MAX	CONDITIONS
22	$\overline{\text{RPLT}}$ low from $\overline{\text{IOR}}$ low		50	
23	$\overline{\text{WPLT}}$ high from $\overline{\text{IOW}}$ high		45	
24	$\overline{\text{RPLT}}$ high from $\overline{\text{IOR}}$ high		45	
25	$\overline{\text{VCLK1}}$ low from $\overline{\text{IOW}}$ low (3C2h port)		1t + 70	
26	$\overline{\text{VCLK1}}$ high from $\overline{\text{IOW}}$ high (3C2h port)		1t + 40	
27	SA[16:0] valid to $\overline{\text{IOCS16}}$ low		35	
28	$\overline{\text{IOCS16}}$ hold from $\overline{\text{IOW}}$ high		30	
29	ALE rising edge to $\overline{\text{MEMCS16}}$		36	SLA[23:17] valid
30	$\overline{\text{MEMCS16}}$ hold from $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$ low		40	From next ALE
30A	ALE pulse width	30		

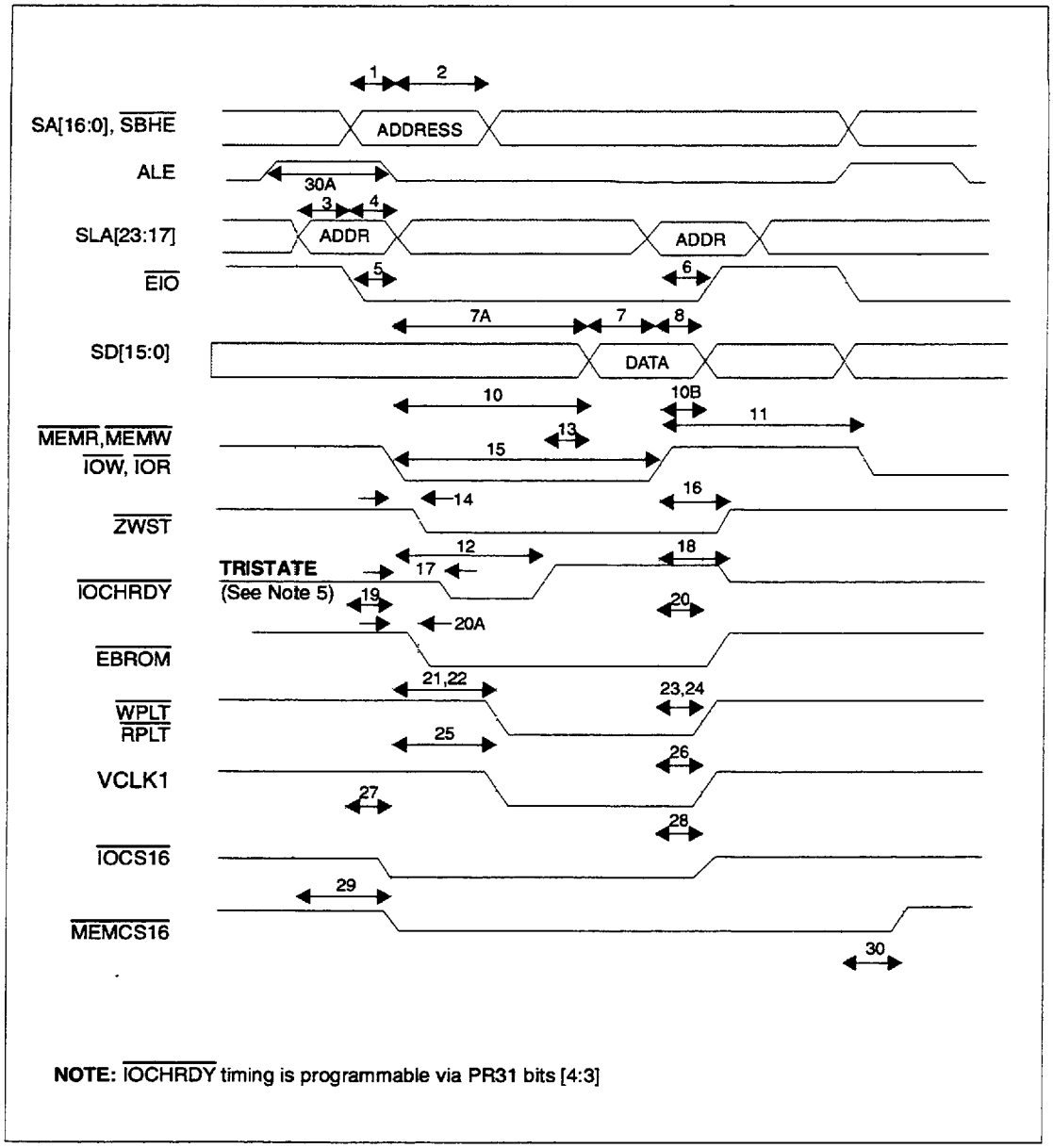
TABLE 30-4. I/O AND MEMORY READ / WRITE TIMING IN ISA(AT) MODE (Continued)

NOTES FOR TABLE 30-4

1. Memory map reads require a 130 nsec delay before data is valid.
2. Maximum value listed is for standard VGA modes. Other values may be used by setting PR31(3C5, index 11) bit 4,3 as follows:

BIT 4	BIT 3	MAX $\overline{\text{IOCHRDY}}$ FROM $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$ LOW
0	0	40 (default)
0	1	40 + 1*t*
1	0	40 + 2*t*
1	1	40- 1*t*

3. $t = {}^{1}/_{\text{MCLK}}$
4. Minimum and maximum values are given in nanoseconds (ns) unless otherwise specified.
5. $\overline{\text{IOCHRDY}}$ is a totem-pole high or low output when $\overline{\text{MEMW}}$ is active. Otherwise, IOCHRDY is a tristate (open collector) signal.
6. The asterisk (*) indicates that the timing has not been specified.



NOTE: $\overline{\text{IOCHRDY}}$ timing is programmable via PR31 bits [4:3]

FIGURE 30-3. I/O AND MEMORY READ/WRITE ISA (AT) MODE TIMING

30.6 VESA VL-BUS INTERFACE TIMING

Timing for the VESA VL-bus interface is listed in Table 30-5 and shown in Figure 30-4

.

NO.	SYMBOL / PARAMETER	MIN	MAX	CONDITIONS
1	CLK486 Period	30	---	BVDD/2 Threshold
2	CLK486 Low Time	11	---	BVDD/2 Threshold
3	CLK486 High Time	11	---	BVDD/2 Threshold
4a	SA[31:2], $\overline{BE}$[3:0], M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ to $\overline{VLBICS}$ Low	5	25	CL = 100 pF
4b	SA[31:2], $\overline{BE}$[3:0], M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ to $\overline{VLBICS}$ High	5	28	
5a	SA[31:2], $\overline{BE}$[3:0], M/$\overline{IO}$, W/$\overline{R}$, Setup to CLK486	0	---	
5b	$\overline{ADS}$, D/$\overline{C}$ Setup to CLK486	10	---	
6	SA[31:2], $\overline{BE}$[3:0], M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Hold from CLK486	3	---	
7	CLK486 to PD[31:16], SD[15:0] Vaild	3	20	CL = 100 pF
8	CLK486 to PD[31:16], SD[15:0] Tristate	3	20	CL = 100 pF
9	CLK486 of $\overline{ADS}$ Low to $\overline{CPURDY}$ Low	t + 14a	2.5 µs	t = CLK486 Period CL = 100 pF
10	PD[31:16], SD[15:0] Setup to CLK486	11	---	
11	PD[31:16], SD[15:0] Hold from CLK486	5	---	
12	$\overline{RDYIN}$ Setup to CLK486	7	---	
13	$\overline{RDYIN}$ Hold from CLK486	3	---	
14a	CLK486 to $\overline{CPURDY}$ Low	2	20	
14b	CLK486 to $\overline{CPURDY}$ High	2	20	
14c	CLK486 to $\overline{CPURDY}$ Tristate	3	25	CL = 100 pF

TABLE 30-5. VESA VL-BUS INTERFACE TIMING

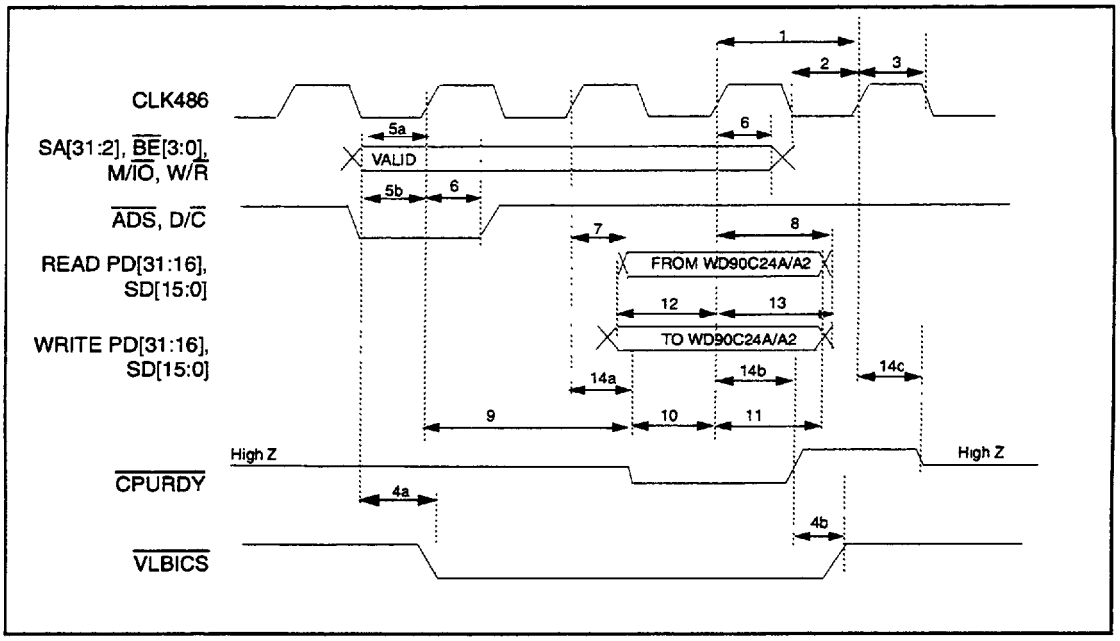


FIGURE 30-4. VL-BUS INTERFACE TIMING

30.7 DRAM TIMING

This section provides the following DRAM timing information:

- DRAM Timing (Table 30-6)
- DRAM Timing (Figure 30-5)
- DRAM Timing Adjustment (Figure 30-6)

NOTE

To determine the specific DRAM address and control lines used for each display memory configuration, refer to Table 5-10.

NO.	SYMBOL /PARAMETER	MIN	MAX	NOMINAL AT 44.3 MHz	CONDITIONS
1	$\overline{ARAS}$, $\overline{BRAS}$ cycle time	6t - 2		134	Note 4
2	$\overline{ARAS}$, $\overline{BRAS}$ pulse width low	3t + 9		78	Note 4
3	$\overline{ARAS}$ high time (precharge)	2.5t + 5		56	Note 4
4	$\overline{ARAS}$ low to $\overline{ACASL}$, $\overline{ACASH}$ low, $\overline{BRAS}$ low to $\overline{BCASL}$, $\overline{BCASH}$ low	2.5t - 25		57	Note 4
5	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ cycle time	2t - 2		44	
6	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ pulse width low	1t + 2		30	Note 4
7	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high time (precharge)	1t - 10		14	Note 4
8	Row address setup to $\overline{ARAS}$, $\overline{BRAS}$ low	1t - 5		26	
9	Row address hold time from $\overline{ARAS}$, $\overline{BRAS}$ low	1t - 10		22	
10	Column address setup to $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 2		27	
11	Column address hold from $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 12		17	
12	Read Data valid before $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high	3		---	
13	Read data hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high	13		---	
14	Write Data setup to $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	3t - 20		17.6	
15	Write Data hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	2t		68	
16	$\overline{AWE}$, $\overline{BWE}$ low setup before $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 5	1t + 3	25	

TABLE 30-6. DRAM TIMING

NO.	SYMBOL /PARAMETER	MIN	MAX	NOMINAL AT 44.3 MHz	CONDITIONS
17	$\overline{AWE}$, $\overline{BWE}$ low hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 5	1t + 12	30	
18	$\overline{AOE}$, $\overline{BOE}$ high before $\overline{AWE}$, $\overline{BWE}$ low	2t - 8		44	
19	$\overline{AOE}$ low after $\overline{AWE}$ high, $\overline{BOE}$ low after $\overline{BWE}$ high	1t -10		12	
20	$\overline{ACAS}$, $\overline{BCAS}$ high for $\overline{CAS}$-before-$\overline{RAS}$ refresh	0.5t		42	
21	$\overline{ARAS}$, $\overline{BRAS}$ low from $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low for $\overline{CAS}$-before-$\overline{RAS}$ refresh	1.5t		42	

TABLE 30-6. DRAM TIMING (Continued)

NOTES FOR TABLE 30-6

[1]All values are given in nanoseconds (ns) unless otherwise specified.

[2]MCLK edge respective to $\overline{ARAS}$, $\overline{BRAS}$, $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, and $\overline{BCASH}$, MA[8:0] edge delay may be up to 40 ns

[3]The timing is the result of setting PR33A (3C5, Index = 13) = XXX00000

[4]Timing is adjustable by PR33A.

[5]Memory write uses fast page early write, while keeping $\overline{AOE}$, $\overline{BOE}$ = 1

[6]Memory read uses fast page read, while keeping $\overline{AOE}$, $\overline{BOE}$ = 1

[7]$t = {}^{1}/_{MCLK}$

[8]The maximum MCLK frequency is dependent on DRAM speed as follows:
MCLK = 37.5 MHz for 80 ns DRAM
MCLK = 39.8 MHZ for some faster 80ns DRAM
MCLK = 44.3 MHZ for 70 ns DRAM
MCLK = 49.5 MHZ for 60 ns DRAM

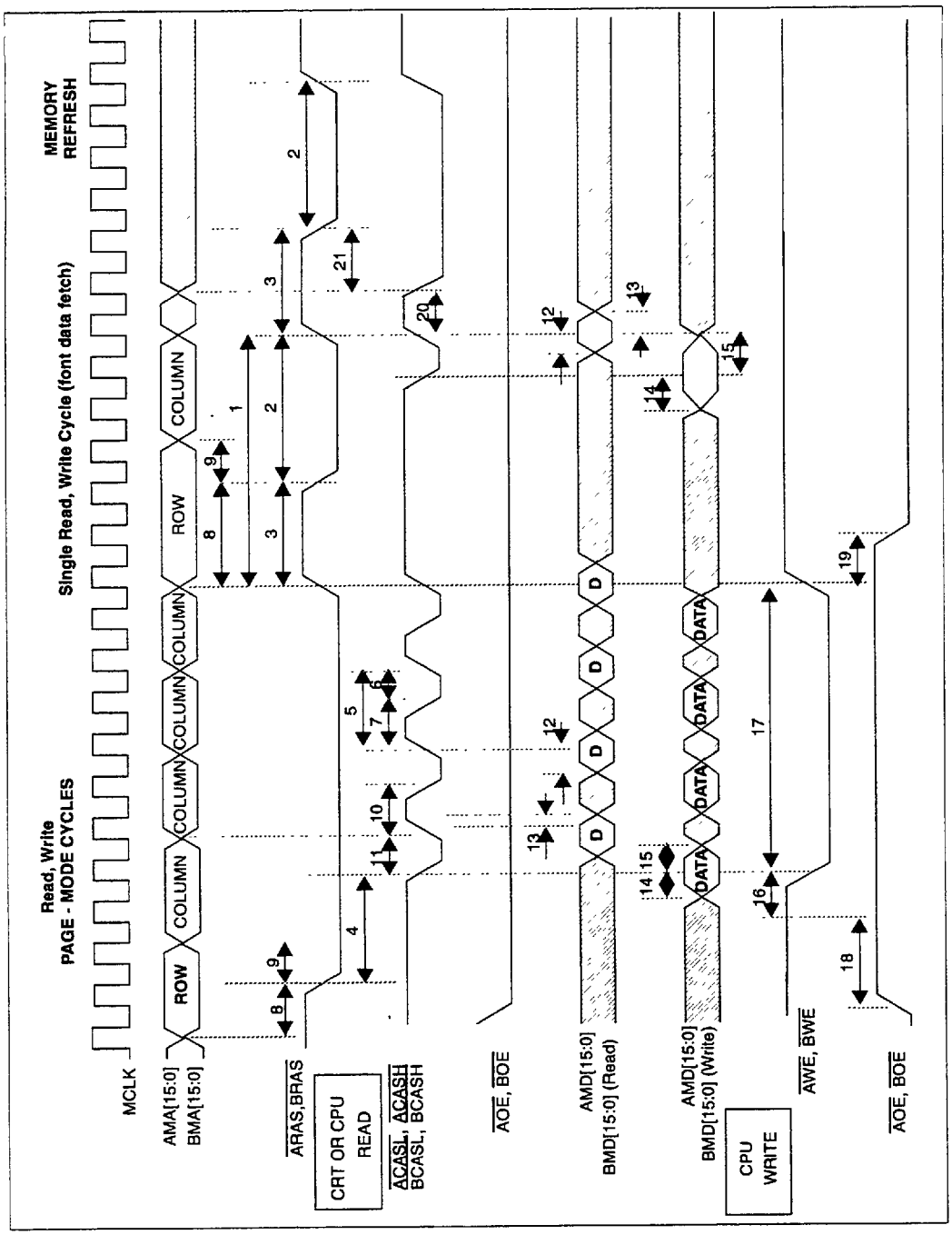
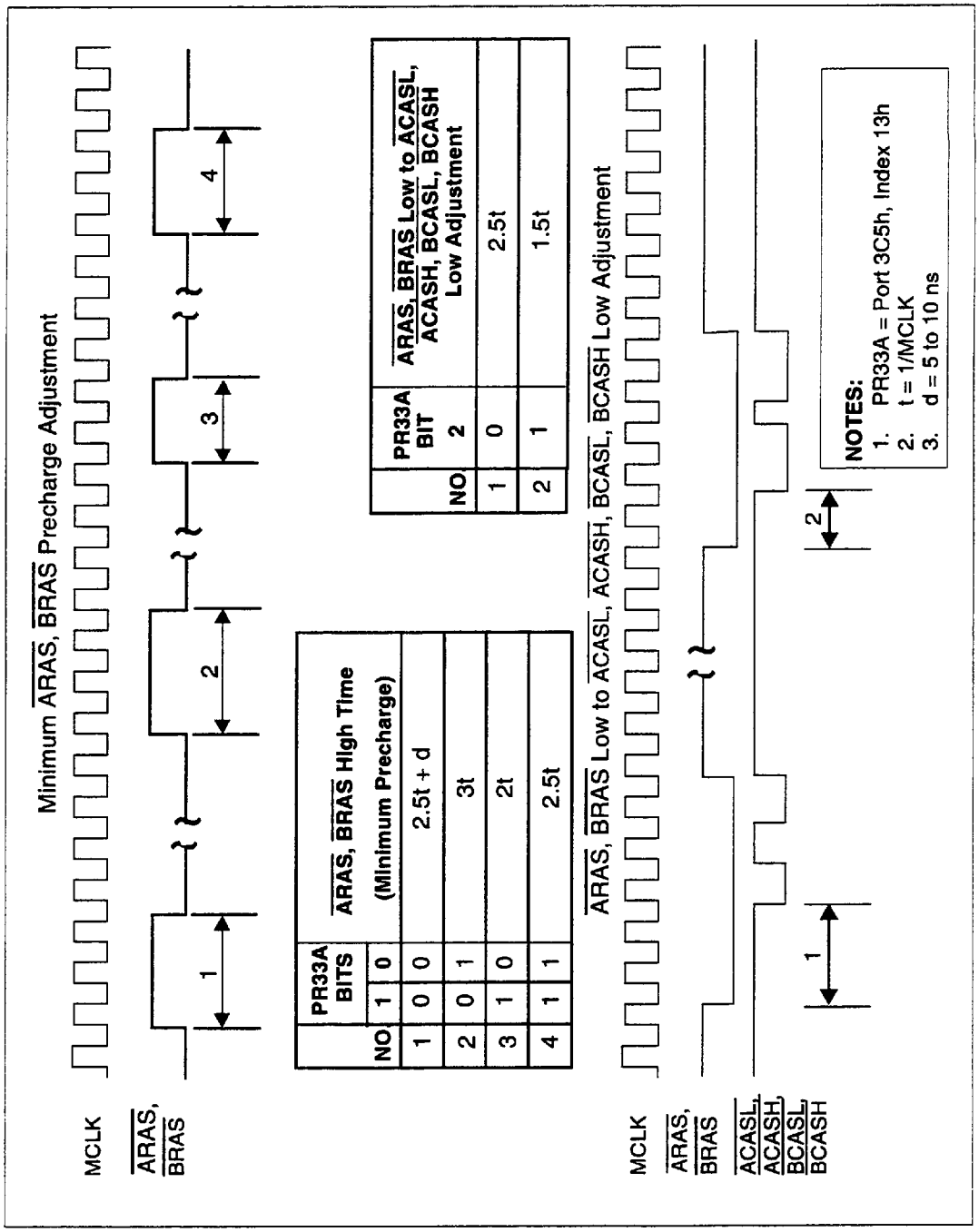


FIGURE 30-5. DRAM TIMING



NO	PR33A BITS 1	PR33A BITS 0	ARAS, BRAS High Time (Minimum Precharge)
1	0	0	2.5t + d
2	0	1	3t
3	1	0	2t
4	1	1	2.5t

NO	PR33A BIT 2	ARAS, BRAS Low to ACASL, ACASH, BCASL, BCASH Low Adjustment
1	0	2.5t
2	1	1.5t

FIGURE 30-6. DRAM TIMING ADJUSTMENT

30.8 DUAL-PANEL MONOCHROME LCD FUNCTIONAL TIMING, PANEL ONLY MODE

Dual-panel monochrome LCD functional timing is shown in Figure 30-7.

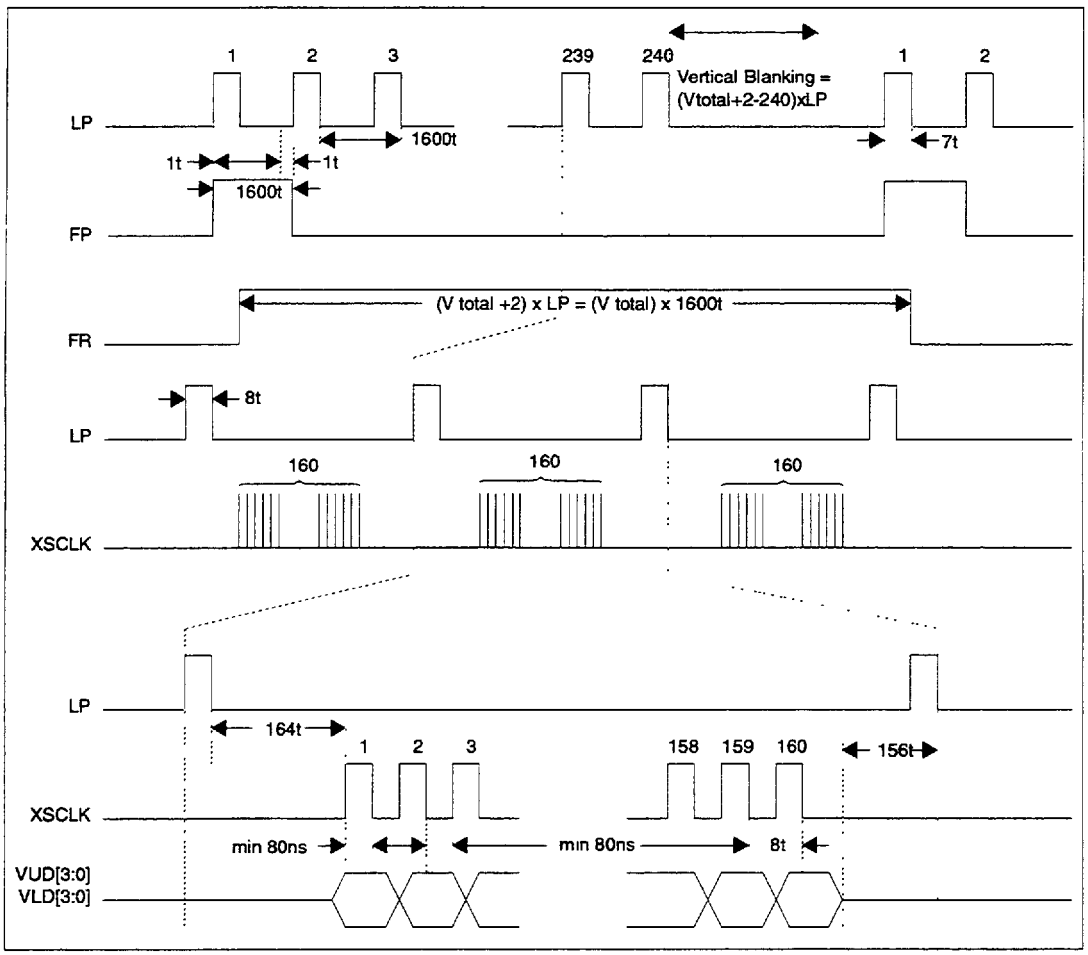


FIGURE 30-7. DUAL-PANEL MONOCHROME LCD FUNCTIONAL TIMING, PANEL ONLY MODE (NO CRT)

30.9 COLOR STN LCD INTERFACE FUNCTIONAL TIMING

The color STN LCD interface functional timing is shown in Figure 30-8.

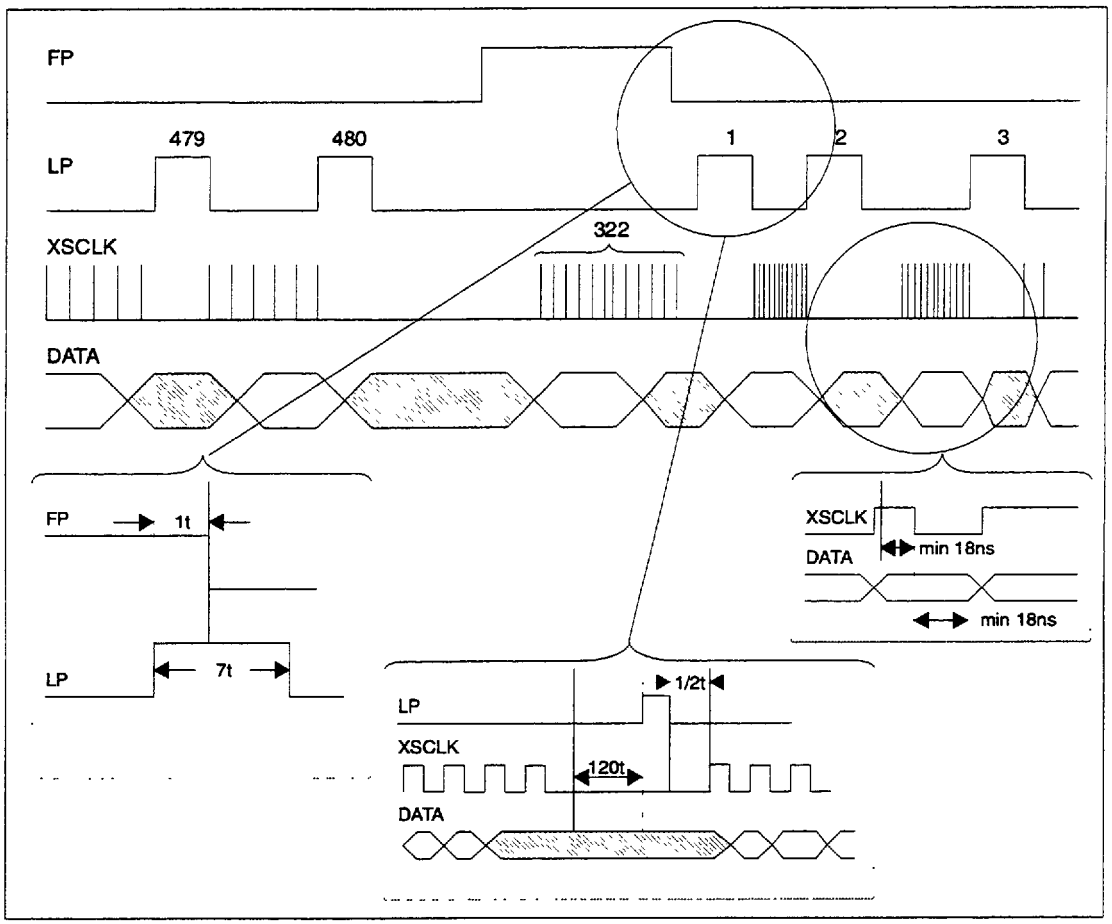


FIGURE 30-8. COLOR STN LCD INTERFACE FUNCTIONAL TIMING

30.10 DUAL-PANEL COLOR STN FUNCTIONAL TIMING (SIMULTANEOUSE DISPLAY MODE

The dual-panel color STN functional timing for simultaneous display mode is shown in Figure 30-9.

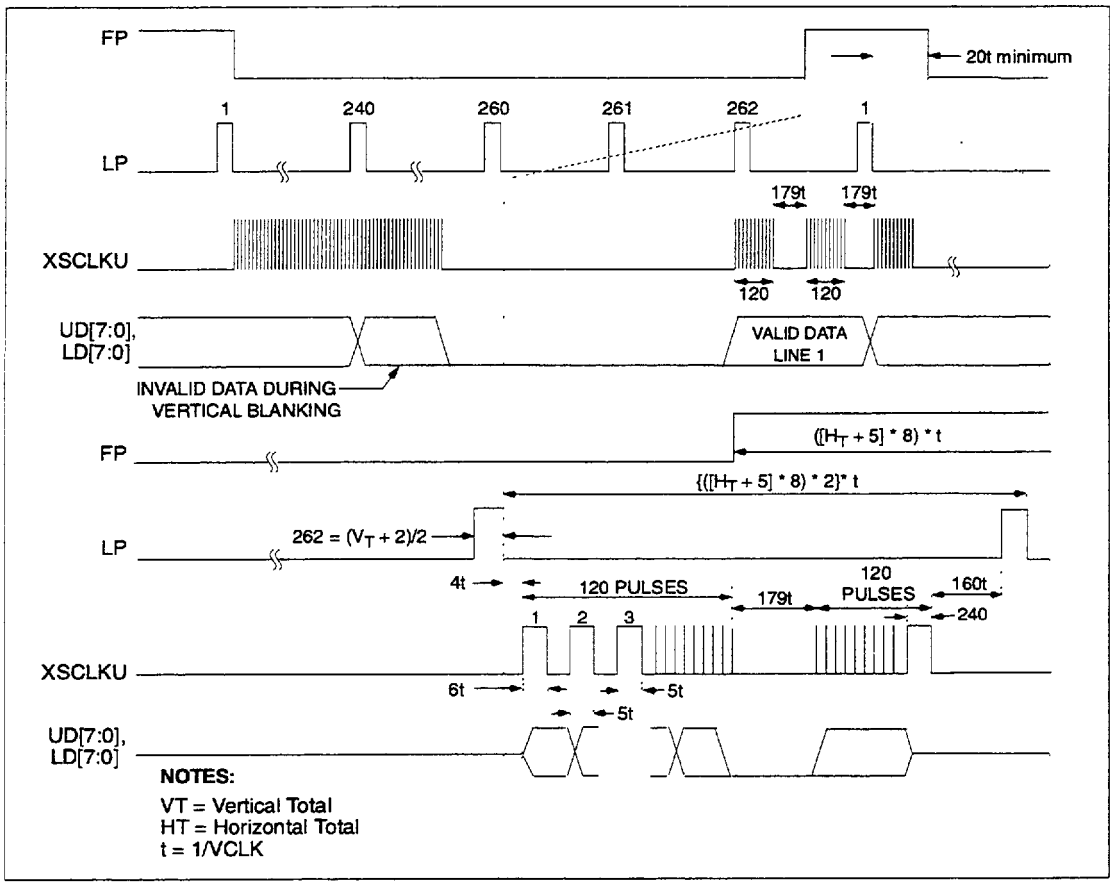
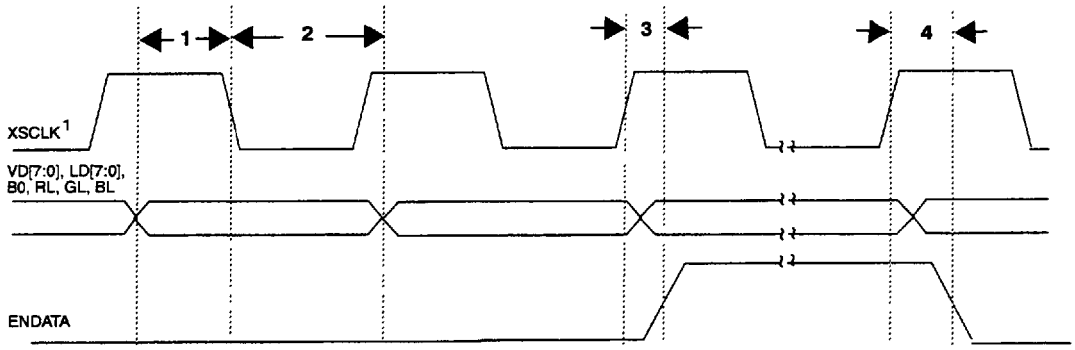


FIGURE 30-9. DUAL-PANEL COLOR STN FUNCTIONAL TIMING IN SIMULTANEOUS DISPLAY MODE

30.11 TFT PANEL AC TIMING

TFT panel AC timing is shown in Figure 30-10. For TFT functional timing, refer to Section 30.12.



ITEM NO.	DESCRIPTION	MIN.	TYPICAL[2]	MAX.
1	Panel data setup time before the fall of XSCLK		15 ns	
2	Panel data hold time after fall of XSCLK.		21 ns	
3	Rising edge of XSCLK to ENDATA active high		16 ns	
4	Rising edge of XSCLK to ENDATA low.		18 ns	

NOTES:
1. The XSCLK signal is set for normal polarity.
2. Values shown are for VCLK = 28 MHz.

FIGURE 30-10. TFT PANEL AC TIMING

30.12 TFT PANEL FUNCTIONAL TIMING

TFT panel functional timing is shown in Figure 30-11. For TFT panel AC timing, refer to Section 30.11.

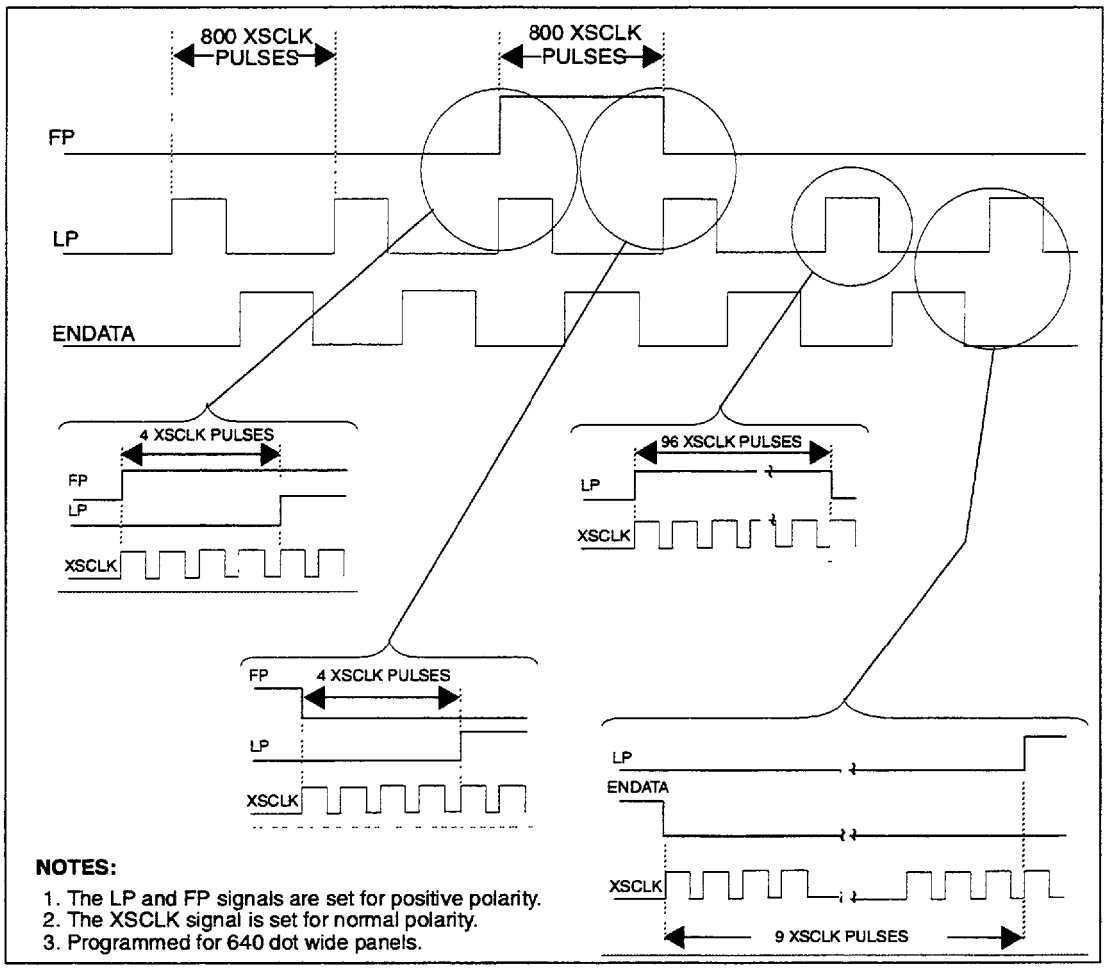


FIGURE 30-11. TFT PANEL FUNCTIONAL TIMING

30.13 RAMDAC TIMING

RAMDAC Timing is listed is Table 30-7 and shown in Figure 30-12.

NO.	PARAMETER	MIN	MAX	TYPICAL	UNITS
1	Analog Output Delay		25		ns
2	Analog Output Rise/Fall Time[1]			3	ns
3	Analog Output Settling Time[2]			20	ns
4	Blanking Delay Time from $\overline{\text{BLANK}}$		45		ns

NOTES:

1. Defined as 10% to 90% of final value.
2. Defined as the time from when the DAC output begins to change until the time overshoot/ undershoot falls below clock feed-through.

TABLE 30-7. RAMDAC TIMING

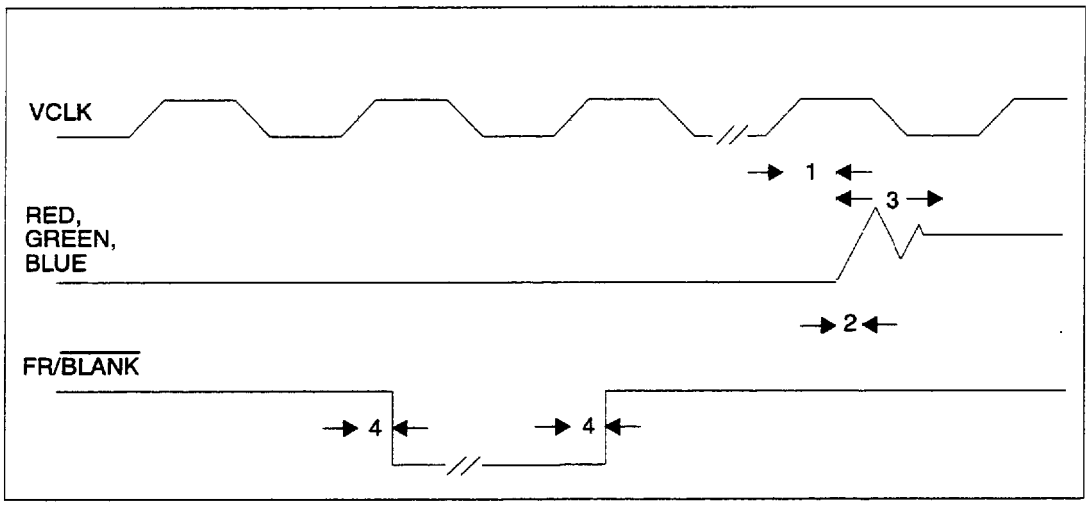


FIGURE 30-12. RAMDAC TIMING

30.14 $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ DRAM REFRESH TIMING

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ DRAM refresh timing for normal operation and Power Down modes is listed in Table 30-8 and shown in Figure 30-13.

NO	PARAMETER	MIN	MAX
1A 1B	$\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$, pulse width low ARAS,BRAS pulse width high	2.5t-10 2.5t-10	5t+10 5t+10
2A 2B	$\overline{\text{ACAS}}$,$\overline{\text{BCAS}}$ pulse width low ACAS,BCAS pulse width high	5t-5 t-20	4t+5 6t+5
3	$\overline{\text{ACAS}}$,$\overline{\text{BCAS}}$ low to $\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$ low	1.5t-10	
4	$\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$ low to $\overline{\text{ACAS}}$,$\overline{\text{BCAS}}$ high	2t-10	
5	$\overline{\text{AOE}}$,$\overline{\text{BOE}}$ high to $\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$ high	4t-8	5t+8
6	$\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$ low to $\overline{\text{AOE}}$,$\overline{\text{BOE}}$ low	30t	
7	$\overline{\text{ARAS}}$,$\overline{\text{BRAS}}$ high (precharge) to $\overline{\text{ACAS}}$,$\overline{\text{BCAS}}$ low	t-5	

TABLE 30-8. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ DRAM REFRESH TIMING

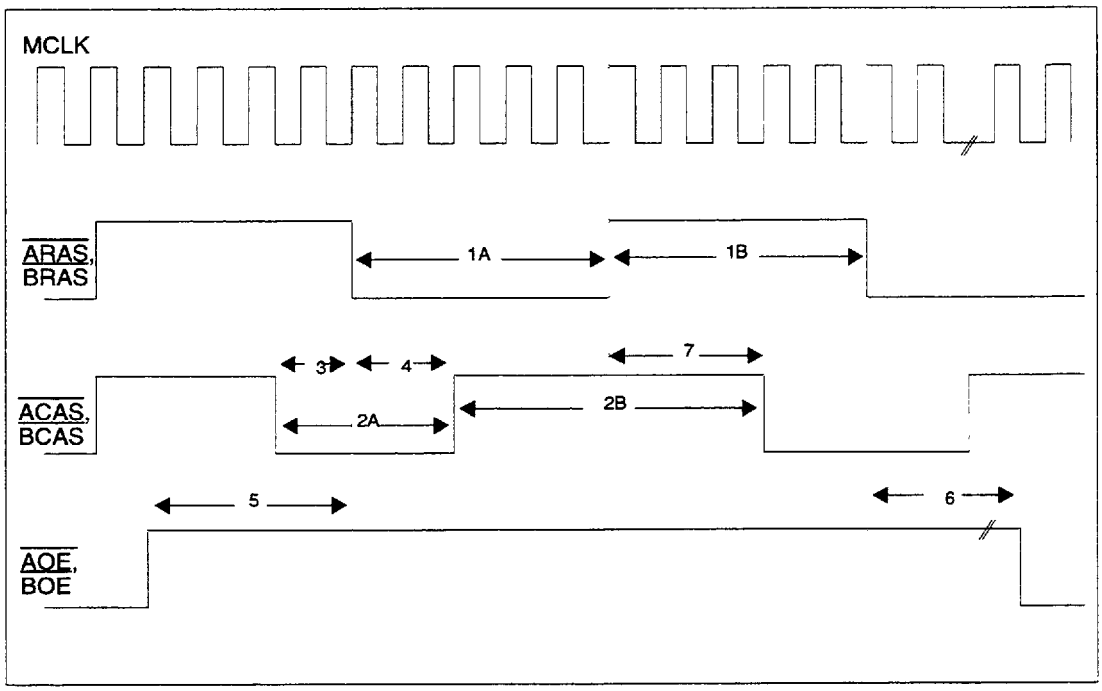


FIGURE 30-13. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ DRAM REFRESH TIMING, NORMAL OPERATION

30.15 DISPLAY IDLE/SLEEP MODE AC-TIMED $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH TIMING

The display idle/sleep mode AC-timed $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh timing is listed in Table 30-9 and shown in Figure 30-14.

NO	PARAMETER	MIN	MAX
1	$\overline{\text{CAS}}$ Low from $\overline{\text{REFRESH}}$ Low	10	
2	$\overline{\text{RAS}}$ Low from $\overline{\text{CAS}}$ Low	10	
3	$\overline{\text{CAS}}$ High from $\overline{\text{REFRESH}}$	10	
4	$\overline{\text{RAS}}$ High from $\overline{\text{CAS}}$ High	10	

TABLE 30-9. DISPLAY IDLE/SLEEP MODE AC-TIMED $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH TIMING

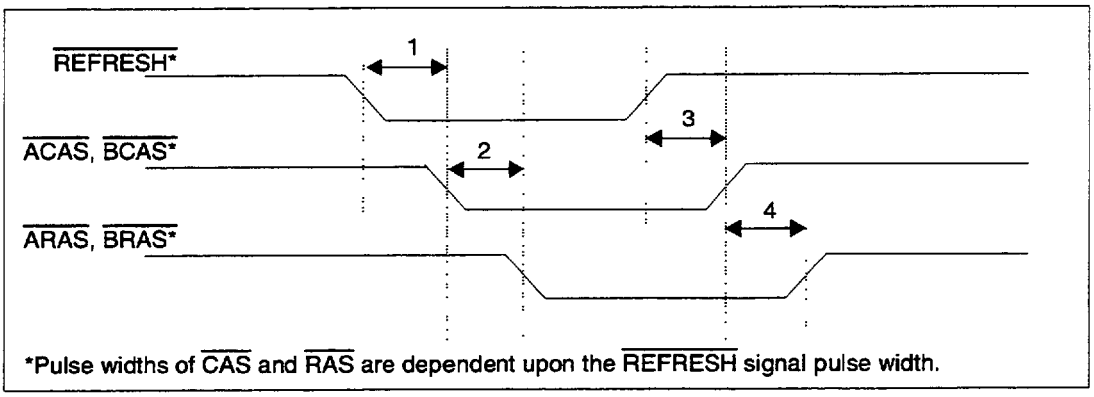


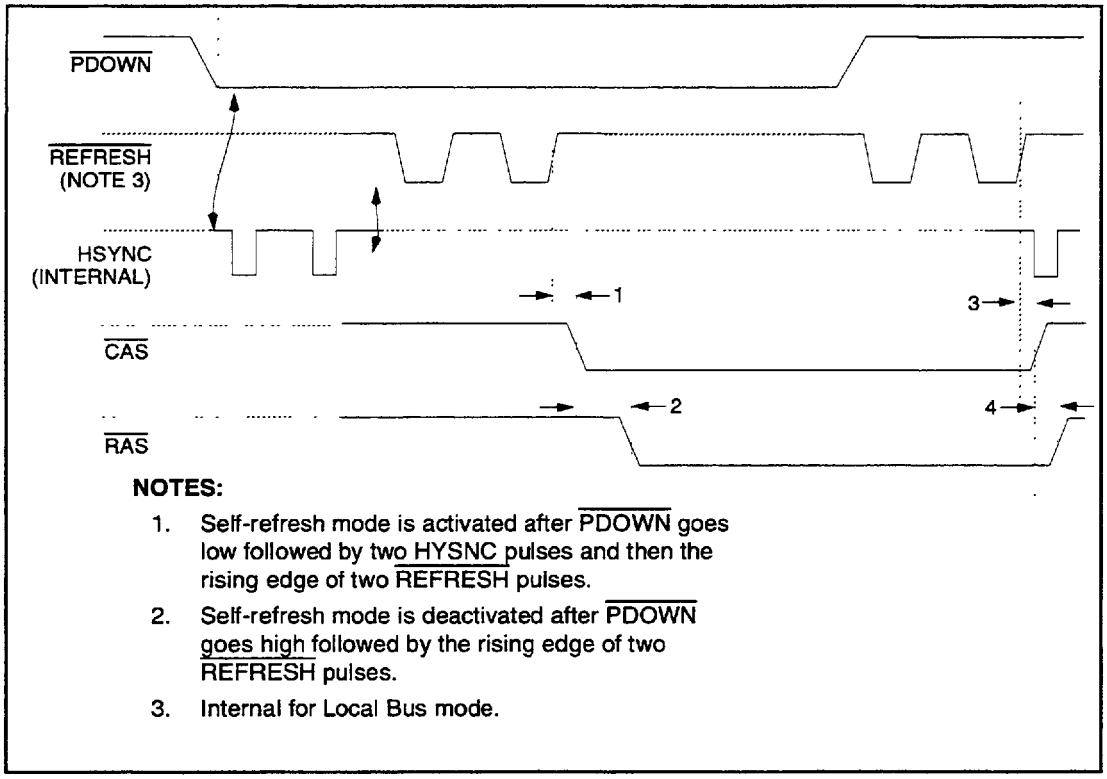
FIGURE 30-14. DISPLAY IDLE/SLEEP MODE AC-TIMED $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH TIMING

30.16 SELF-REFRESH TIMING, SLEEP/DISPLAY IDLE MODES

The self-refresh timing for sleep/display idle modes is listed in Table 30-10 and shown in Figure 30-15.

NO	PARAMETER	MIN	MAX
1	$\overline{CAS}$ Low from $\overline{REFRESH}$ High	10	
2	$\overline{RAS}$ Low from $\overline{CAS}$ Low	10	
3	$\overline{CAS}$ High from $\overline{REFRESH}$ High	10	
4	$\overline{RAS}$ High from $\overline{CAS}$ High	10	

TABLE 30-10. SELF-REFRESH TIMING, SLEEP/DISPLAY IDLE MODES



NOTES:

1. Self-refresh mode is activated after $\overline{PDOWN}$ goes low followed by two HYSNC pulses and then the rising edge of two $\overline{REFRESH}$ pulses.
2. Self-refresh mode is deactivated after $\overline{PDOWN}$ goes high followed by the rising edge of two $\overline{REFRESH}$ pulses.
3. Internal for Local Bus mode.

FIGURE 30-15. SELF-REFRESH TIMING, SLEEP/DISPLAY IDLE MODES

30.17 TIMING PARAMETER MEASUREMENT INFORMATION

Figure 30-16 shows the test setup for timing parameter measurements and Table 30-11 lists the timing parameter measurement information.

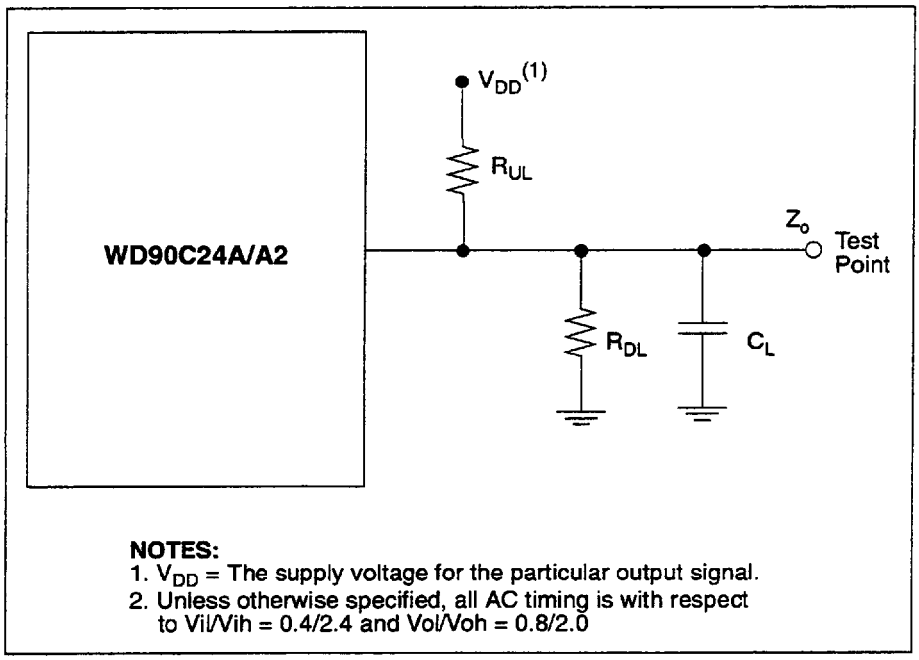


FIGURE 30-16. SETUP FOR TIMING PARAMETER MEASUREMENTS

SIGNAL NAME	C_{L1}	R_{UL}	R_{DL}	NOTES
EBROM|REFLCL	50 pF			
IOCS16|IBOFF	70 pF	300 Ω		
MEMCS16|IPD31	70 pF	300 Ω		
IRQ|PD30	70 pF	1K Ω[2]		Notes 2
IOCHRDY|CPURDY	100 pF	1K Ω		
ZWST|CSFB|VLBIBUSY	70 pF	300 Ω		
SD[15:0]	70 pF			
PD[29:16}	70 pF			
SLA[23:17]	50 pF			
ARAS, ACASH, ACASL, AOE, AWE, BRAS, BCASH, BCASL, BOE, BWE	50pF			
AMA8	50pF			
AMA[7:0]	50pF			
BMA8	50pF			
BMA[7:0]	50pF			
AMD[15:0]	50pF			
BMD[15:0]	50pF			
RED, GREEN, BLUE	40 pF		50 Ω	Z_0=75Ω @65 MHz
RPLT|STN15|BD3|VD7	50 pF			
WPLT|BD4	50 pF			
HSYNC, VSYNC	70 pF			
VCLK1|FPUSR1	50 pF			
VCLK2	50 pF			
LCDENA	50 pF			
PNLOFF	50 pF			
PCLK	30 pF			
FR/BLANK|ENDATA	50 pF			
VD[7:0], LD[7:0], STN[14:0], BD[5:0], GD[5:0], RD[5:0]	50 pF			
IXSCLK|XSCLKL|XSCLKU	50 pF			
FP, LP	50 pF			
VREF		4.32		

NOTES:

1. The values listed for C_L were used for the AC timing specified in this data sheet, unless otherwise indicated in the specific timing diagram.
2. VDD = The supply voltage for the particular output signal. Figure 30-16 shows the setup for timing parameter measurements.

TABLE 30-11. TIMING PARAMETER MEASUREMENT INFORMATION

31.0 PACKAGE DIMENSIONS

Figure 31-1 illustrates the 208-pin MQFP package showing the dimensions in millimeters and inches.

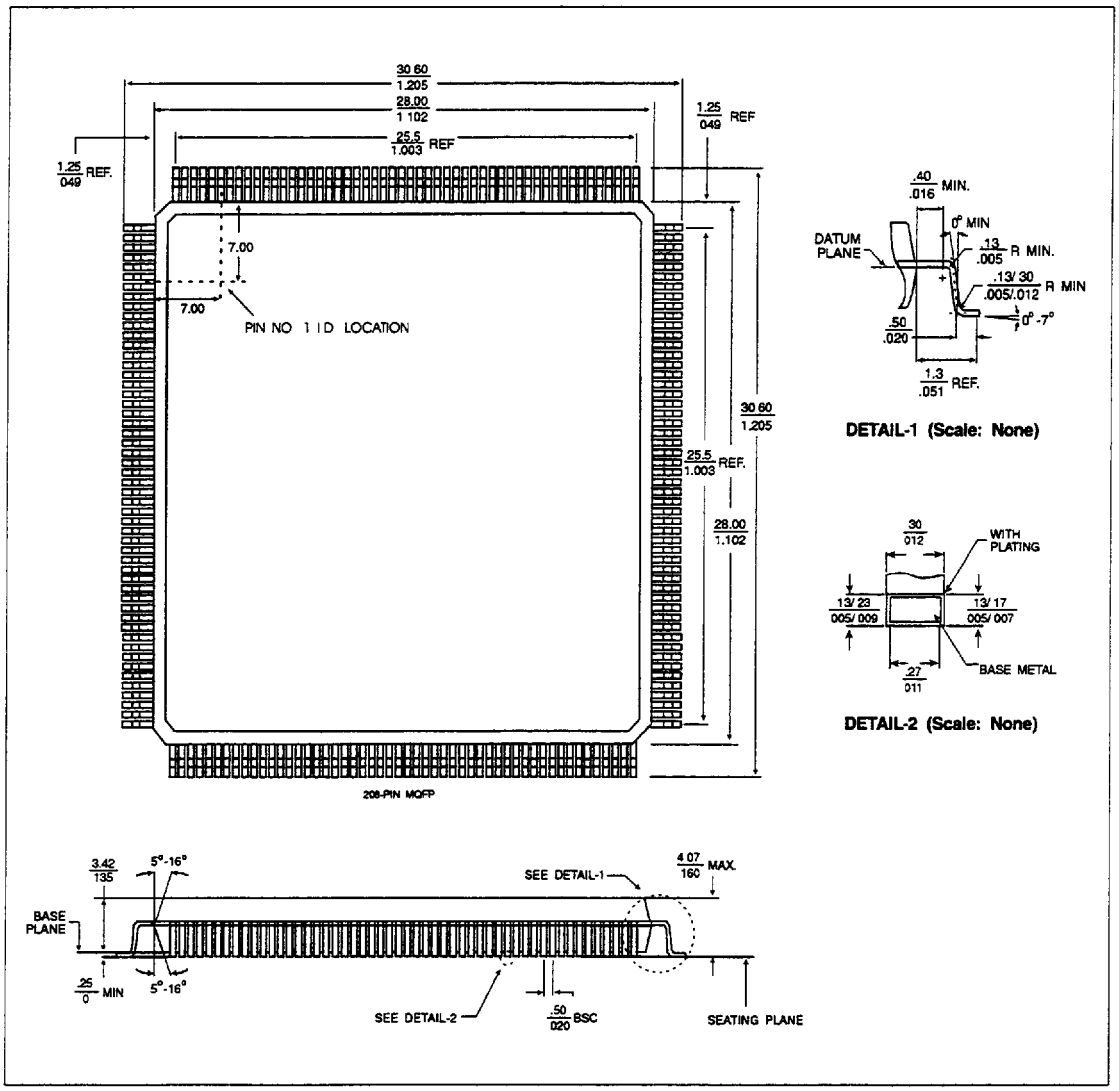


FIGURE 31-1. 208-PIN MQFP PACKAGE DIMENSIONS

A.0 APPENDIX A - REFERENCE DOCUMENTS

For further information on Personal Computer (PC) video display applications, refer to the manuals in the following list.

- IBM PC Hardware User Guide (IBM # 6322510)
- IBM PC XT Hardware User Guide (IBM # 6322511)
- IBM PC AT Hardware User Guide (IBM # 6280066)
- IBM PS/2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM PC AT Technical Reference Manual (IBM # 6280070)
- IBM PS/2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM PS/2 BIOS Reference Manual (IBM # 68x2260)
- IBM PC Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual

B.0 APPENDIX B - WD90C24 TO WD90C24A DIFFERENCE DATA

B.1 INTRODUCTION

This appendix describes the design and operational differences between the WD90C24 Controller and the WD90C24A Controller. Each of the controllers is thoroughly described in its respective data sheet. This appendix uses information contained in both data sheets to describe specific features and characteristics of the WD90C24A Controller that are not supported by the WD90C24 Controller.

B.1.1 PURPOSE

The information contained in the appendix is useful to electronic designers or developers who are already familiar with the WD90C24 Controller, and are now working with the WD90C24A Controller. The information in the appendix identifies the design differences to ease the transition to the newer controller.

B.1.2 GENERAL DESCRIPTION

The Western Digital WD90C24A2 is a 0.9 micron CMOS VLSI device with the capability to drive flat panel displays and standard CRTs. The WD90C24A2 allows simultaneous display for a CRT and a monochrome dual-panel, or a CRT and a color panel. The device is backwards compatible with previous video standards including MDA, EGA, and CGA.

B.1.3 ORDERING INFORMATION

Use the following number to order the WD90C24A controller:

90C24AZZ00

B.1.4 ADDITIONAL FEATURES OF THE WD90C24A CONTROLLER

The following paragraphs describe additional features and characteristics of the WD90C24A controller. Unless otherwise stated, the following features and characteristics apply only to the WD90C24A controller.

- Supports Dual-panel (1/240) color STN LCD interface.
- Supports Programmable Hardware Cursor in Dual-panel (1/240) STN LCD panels as well as single-panel applications.
- Supports 16-Bit High-Color capability in 320 by 200, 640 by 400, 640 by 480 and 800 by 600 modes.
- Supports an algorithm enhancement for vertical screen expansion in text mode. Raster lines are duplicated above or below the character block (either 1 above and 2 below, or 0 above and 3 below). These algorithms maintain the character font size, and are programmable with PR64 bits 1,0.
- The Microsoft Strip Line Draw algorithm has been implemented in hardware to further improve Windows performance. With this algorithm, the line draw engine interacts with software to determine the slope of the line and the number of pixels to be turned on.
- Supports TFT 800 by 600 color panel via register PR1A, Bits 7,4. This is in addition to 1024 by 768 and 640 by 480 support.
- Provides configuration bit CNF15 to directly accept the 2X clock from the new Intel S-series 486 microprocessors.
- Supports Single-panel (1/480) monochrome 640 by 480 STN LCD interface. Either 4-bit or 8-bit interface is selectable with PR1A, Bit 3.
- Allows CRT control signals to be forced static low. The PCLK output can be held static low using PR66, Bit 4 to reduce EMI emissions. VSYNC and HSYNC can be held static low using PR66, Bit 3. In addition, when in CRT-only mode, the VID[15:0] and $\overline{\text{BLANK}}$ signals are output on the flat-panel interface and can be forced inactive low with PR66, Bit 4.
- In Power-down mode, **all** CRT and panel interface pins, regardless of display type, are held static low. In addition, PR4, Bit 5 can continue to be used to tristate the panel data and control pins regardless of display type (SCLK, $\overline{\text{WPLT}}$/RGB4, XSCLK/RGB5, UD(7:0), LD(7:0), FP, LP and FR).
- In CRT-only mode, all panel control pins are held static low (SCLK, XSCLK, FP and LP). The panel data pins are controlled with PR66, Bit 4.

- The HDE (Horizontal Display End) and VDE (Vertical Display End) registers are now locked independently. PR64, Bit 6 locks the VDE, and PR64, Bit 4 locks the HDE register.
- The 18-bit TFT interface now operates in reverse video mode to support negative logic panels. This feature is programmable with PR18, Bit 4.
- I/O pins have been remapped to improve the ICT (In-Circuit Test) of the WD90C24A. Because there are more input pins than output pins, pairs of input pins had to be ORed to each output. There was a conflict in 3 pairs of pins in that they were next to each other, which would not allow for a "short test" on those pins. These 3 pairs of pins were AMD3 and AMD12 (pins 183 and 184), BMD3 and BMD12 (pins 8 and 9), and EBROM and VLBICS (pins 171 and 172).
- The PR62 register that programs the FR panel control signal now defaults to the value 3Ch at reset, which translates into a 480-line pulse rate.

B.2 INTERFACE CONNECTIONS

B.2.1 HOST INTERFACE

The Host Interface Signal Pin Definitions listed in Table 5-2 lists signal mnemonics PD29:PD16 on connector pins 37 through 52, respectfully. For the WD90C24A2, the source/sink drive capability of these pins is 8 mA.

B.2.2 TFT PANELS

Tables B-1 through B-3 each list the interface connections for a general panel type (refer to the table tile) as they apply to specific LCD panels (refer to column headings).

NOTE

In Tables B-1 through B-3, the shaded columns denote new operations of the WD90C24A controller.

B.2.3 TFT PANEL INTERFACE

WD90C24A		SHARP			HITACHI			NEC	TOSHIIBA	MATSUSHITA
PIN NO.	SIGNAL	LQ9D011 (9 BIT), LQ10D011 (9 BIT), LQ10D311 (9 BIT)	LQ10D311 (18 BIT)	LQ12D011 (9BIT)* x 2PIXELS	TX24D55VCICAA (12 BIT)	TX26D51VCIAA (9 BIT)	TX26A02VC (9 BIT)	NL6448AC30-03 (12 BIT)	LTM10C015K (9 BIT)	AA95VA3D (9 BIT)
128	RD5		R5	REQUIRES EXTERNAL LOGIC						
129	RD4		R4							
131	RD3	---	R3		R3	---	---	R3	---	---
132	RD2	R2	R2		R2	R2	R5	R2	R2	R3
133	RD1	R1	R1		R1	R1	R4	R1	R1	R2
134	RD0	R0	R0		R0	R0	R3	R0	R0	R1
126	GD5		G5							
127	GD4		G4							
135	GD3	---	G3		G3	---	---	G3	---	---
136	GD2	G2	G2		G2	G2	G5	G2	G2	G3
137	GD1	G1	G1		G1	G1	G4	G1	G1	G2
138	GD0	G0	G0		G0	G0	G3	G0	G0	G1

TABLE B-1. INTERFACE PIN CONNECTIONS FOR TFT LCD PANELS

	WD90C24A	SHARP			HITACHI			NEC	TOSHIBA	MATSUSHITA
PIN NO.	SIGNAL	LQ9D011 (9 BIT), LQ10D011 (9 BIT), LQ10D311 (9 BIT)	LQ10D311 (18 BIT)	LQ12D011 (9BIT)* x 2PIXELS	TX24D55VCICAA (12 BIT)	TX26D51VCIAA (9 BIT)	TX26A02VC (9 BIT)	NL6448AC30-03 (12 BIT)	LTM10C015K (9 BIT)	AA95VA3D (9 BIT)
119	BD5		B5	REQUIRES EXTERNAL LOGIC						
120	BD4		B4							
121	BD3	---	B3		B3	---	--	B3	---	---
122	BD2	B2	B2		B2	B2	B5	B2	B2	B3
123	BD1	B1	B1		B1	B1	B4	B1	B1	B2
124	BD0	B0	B0		B0	B0	B3	B0	B0	B1
140	XSCLK	CK	CK		DCLK	DCLK	DCLK	CLK	NCLK	DCLK
142	LP	HSYNC	HSYNC		HSYNC	HSYNC	HSYNC	HSYNC	---	HD
143	FP	VSYNC	VSYNC		VSYNC	VSYNC	VSYNC	VSYNC	---	VD
144	ENDATA	ENAB	ENA		DTMG	DTMG	DTMG	DE	ENAB	DENA

NOTE:
*The panel resolution for this column only is 1024 by 768 (2 pixels with 9 Bits per pixel). The resolution for all other columns is 640 by 480.

TABLE B-1. INTERFACE PIN CONNECTIONS FOR TFT LCD PANELS (Continued)

B.2.4 MONOCHROME STN PANEL INTERFACES

WD90C24A		SANYO	MATSUSHITA	TOSHIIBA	HITACHI			SHARP	EPSON			
PIN NO.	SIGNAL	LM-KE55-22NEZ, LCM-5505-22NTK	EDMGPN5WIF	TLX-5152S-C3M1, TLX-1832S-C3M1	LM8373DX	LM65160XUFC, LM65360XUFC, LM65262XUFC, LM65268XUFC	LMG9060ZZFC[1]	LM64P80, LM64148Z, LM64P10	EG9011D	TCM-A0610, EG9007	ECM-A9071[1]	EG9013[2]
131	VUD3/LD7	UD0	D0U	UD0	UD0	UD0	LD0	DU0	DU0	UD0	LD0	D7
132	VUD2/LD6	UD1	D1U	UD1	UD1	UD1	LD1	DU1	DU1	UD1	LD1	D6
133	VUD1/LD5	UD2	D2U	UD2	UD2	UD2	LD2	DU2	DU2	UD2	LD2	D5
134	VUD0/LD4	UD3	D3U	UD3	UD3	UD3	LD3	DU3	DU3	UD3	LD3	D4
135	VLD3/LD3	LD0	D0L	LD0	LD0	LD0	LD4	DL0	DL0	LD0	LD4	D3
136	VLD2/LD2	LD1	D1L	LD1	LD1	LD1	LD5	DL1	DL1	LD1	LD5	D2
137	VLD1/LD1	LD2	D2L	LD2	LD2	LD2	LD6	DL2	DL2	LD2	LD6	D1
138	VLD0/LD0	LD3	D3L	LD3	LD3	LD3	LD7	DL3	DL3	LD3	LD7	D0
121	UD7	---	---	---	---	---	UD0	---	---	---	UD0	---
122	UD6	---	---	---	---	---	UD1	---	---	---	UD1	---
123	UD5	---	---	---	---	---	UD2	---	---	---	UD2	---
124	UD4	---	---	---	---	---	UD3	---	---	---	UD3	---
126	UD3	---	---	---	---	---	UD4	---	---	---	UD4	---
127	UD2	---	---	---	---	---	UD5	---	---	---	UD5	---
128	UD1	---	---	---	---	---	UD6	---	---	---	UD6	---
129	UD0	---	---	---	---	---	UD7	---	---	---	UD7	---
140	XSCLK	CL2	CPX	SCP	CL2	CP	CL2	CP2	CP2	XSCL	XSCL	XSCL
143	FP	FLM	FRM	FP	FLM	FRAME	FLM	S	S	DIN	DIN	DIN
142	LP	CLI	LOAD	LP	CLI	LOAD	CL1	CP1	CP1	LP	LP	LP
144	FR	---	---	---	---	---	M	---	---	---	---	---

NOTE:

1. The resolution for these dual panels is 1024 by 768 (1 by 386 duty cycle).
2. This panel is single (1 by 480 duty cycle) with 640 by 480 resolution. All other panels listed are dual panels.
3. Resolution is 640 by 480 for all panels listed unless otherwise described in 1 or 2 above.

TABLE B-2. INTERFACE PIN CONNECTIONS FOR MONOCHROME LCD PANELS

WD90C24A		SANYO (16-BIT)		SHARP (8-BIT)	SHARP (16-BIT)	EPSON (8-BIT)	MATSUSHITA (16-BITS)	TOSHIIBA (8-BIT)	HITACHI (16-BIT)		CITIZEN, (16-BIT)	KYOCERA (16-BIT)
PIN NO.	SIGNAL	LCM-5330-22NTK, LCM-5327-24NAK, LCM-5313-22NAK	LCM-5331-22NTK, 1/240 DUTY CYCLE	LM64C05P, LM64C031	LM64C08P 1/240 DUTY CYCLE)			TLX-8052S-C3X	LMG9710VUFC	LMG972XUFC 1/240 DUTY CYCLE	1/240 DUTY CYCLE	KCL6448HSTT 1/240 DUTY CYCLE
121	STN15	UD7	UD7	---	DU7		DU7	---	UD7	UD7	UD0	HD0
122	STN14	UD6	UD6	---	DU6		DU6	---	UD6	UD6	UD1	HD1
123	STN13	UD5	UD5	---	DU5		DU5	---	UD5	UD5	UD2	HD2
124	STN12	UD4	UD4	---	DU4		DU4	---	UD4	UD4	UD3	HD3
126	STN11	UD3	UD3	---	DU3		DU3	---	UD3	UD3	UD4	HD4
127	STN10	UD2	UD2	---	DU2		DU2	---	UD2	UD2	UD5	HD5
128	STN9	UD1	UD1	---	DU1		DU1	---	UD1	UD1	UD6	HD6
129	STN8	UD0	UD0	---	DU0		DU0	---	UD0	UD0	UD7	HD7
131	STN7	LD7	LD7	D7	DL7	D0	DL7	D7	LD7	LD7	LD0	LD7
132	STN6	LD6	LD6	D6	DL6	D1	DL6	D6	LD6	LD6	LD1	LD6
133	STN5	LD5	LD5	D5	DL5	D2	DL5	D5	LD5	LD5	LD2	LD5
134	STN4	LD4	LD4	D4	DL4	D3	DL4	D4	LD4	LD4	LD3	LD4
135	STN3	LD3	LD3	D3	DL3	D4	DL3	D3	LD3	LD3	LD4	LD3
136	STN2	LD2	LD2	D2	DL2	D5	DL2	D2	LD2	LD2	LD5	LD2
137	STN1	LD1	LD1	D1	DL1	D6	DL1	D1	LD1	LD1	LD6	LD1
138	STN0	LD0	LD0	D0	DL0	D7	DL0	D0	LD0	LD0	LD7	LD0
119	XSCLK/ XSCLKL	CL2	CL2	XCKU	XSCK	XSCLL	LCK	XCKU	CL2	CP	CL2	CP
140	XSCLKU	---	---	XCKL	---	XSCLU	---	XCKL	---	---	---	---
143	FP	FLM	FLM	YD	YD	DIN	LVS	FP	FLM	FRAM E	FLM	FLM
142	LP	CLI	CLI	LP	LP	LP	LHS	LP	CLI	LOAD	CLI	LOAD
144	FR	M	M	---	---	---	M	---	M	---	--	---

TABLE B-3. INTERFACE PIN CONNECTIONS FOR COLOR STN LCD PANEL WITH 640 BY 480 RESOLUTION

B.3.0 REGISTER DESCRIPTIONS

B.3.1 PR62 - FR TIMING REGISTER

Read/Write Port = 3C5h, Index 24h

Read/Write Port = 3C5h, Index 24h

BITS	FUNCTION
7:0	Programmable FR 8-Bit Divisor

For color flat panels, this register controls the period of the Frame Rate (FR) signal in relation to the refresh rate. For monochrome flat panels, the FR rate is fixed at 480 line intervals.

The FR signal appears at the FR/$\overline{\text{BLANK}}$ pin anytime that PR19 register Bit 4 is set to 1.

The default rate of the FR signal is once every 240 lines because PR62 defaults to 3Ch.

The rate of the FR signal may be adjusted faster or slower in increments of 4 lines.

The FR pulse rate is generated at a line count rate of 4 times the value stored in PR62.

For an FR pulse rate of once every 480 lines, set PR62 to 120d (78h)

The FR pulse is 50% duty cycle.

PR62 should not be set to 00h because this setting is reserved for test purposes.

B.3.2 PR64 - CRT LOCK CONTROL II

Read/Write Port = 3C5h, Index 27h

BITS	FUNCTION
7	Reserved
6	Unlock the Vertical Display End CRT register
5	Reserved
4	Unlock the Horizontal Display End CRT register
3:2	Reserved
1:0	Enhanced Vertical Expansion Selection for Text mode.

Bits 7, 5

Reserved

Bits 6

Set bit 6 to 0 (default) to unlock the VDE (3?5h, Index 12h) register and Overflow (3?5h, Index 07h) bits 6 and 1.

Bits 4

Set bit 4 to 0 (default) to unlock the HDE (3?5h, Index 01h) register.

Bits 3:2

Reserved

Bits 1:0

PR64 Bits 1:0 are functional in 400 line text modes only. When functional, these bits work with PR19 Bits 3:2 to select vertical expansion.

BIT 1	BIT 0	Vertical Expansion Selected
X	0	No enhanced expansion selected.
0	1	Three lines repeated below character.
1	1	One line repeated above character, and two lines repeated below character.

B.3.3 PR66 - FEATURE REGISTER III

Read/Write Port = 3C5h, Index 29h

BITS	FUNCTION
7	Enable Auxiliary Video Extender (AVE) Mode
6	TFT Dithering Mode Select
5	Force LP and FP to be the same as HSYNC and VSYNC, respectively
4	Disable PCLK, $\overline{\text{BLANK}}$, VID[7:0]
3	Disable VSYNC, HSYNC
2	TFT Dithering Mode Select
1:0	Reserved, set to 0

Bit 7

Enable Auxiliary Video Extender (AVE) Mode

The AVE mode allows the internal RAMDAC to be used by an external source. The PCLK, $\overline{\text{BLANK}}$, and VD[7:0] pins become inputs to give direct access to the RAMDAC.

0 = AVE not enabled
1 = AVE enabled

Bits 6

TFT Dithering Mode Select

This bit is used with Bit 2 of this register, with PR57 Bits 4:3, and with PR59 Bit 4 to select the TFT Dithering mode. Refer to the description for PR57.

Bits 5

Force LP and FP to be the same as HSYNC and VSYNC, respectively.

0 = LP and FP normal
1 = LP is the same as HSYNC and FP is the same as VSYNC

Bits 4

Disable PCLK, $\overline{\text{BLANK}}$, VID[7:0]

0 = normal operation.
1 = PCLK forced to inactive low. $\overline{\text{BLANK}}$, VID[7:0] forced inactive low only in CRT-only mode.

Bits 3

Disable VSYNC, HSYNC

0 = normal operation.
1 = VSYNC, HSYNC forced to inactive low.

Bit 2

TFT Dithering Mode Select

This bit is used with bit 6 of this register, with PR57, bits 4:3, and with PR59 bit 4 to select the TFT Dithering mode. Refer to the description for PR57 in Section 14.12.

Bits 1:0

Reserved, must be set to 0.

B.3.4 PR1A - FLAT PANEL CONTROL II REGISTER

Read/Write Port = 3?5h, Index 33h.

BITS	FUNCTION
7	Panel Resolution Select
6:5	STN Panel Select
4	Panel Resolution Select
3	Enable 4/8-bit LCD
2	Shading Method Select
1	Select the Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit 7

Panel Resolution Select

This bit is used with bit 4 to select panel resolution as follows:

BITS		
7	4	FUNCTION
0	0	640 x 480 Panel Width
0	1	1280 x 1084 Panel Width (Reserved for future use.)
1	0	1024 x 768 Panel Width
1	1	800 x 600 Panel Width

Bits 6:5

STN Panel Select

Selects 8-bit and 16-bit STN type panels.

BITS		
6	5	FUNCTION
0	0	Not STN
0	1	8-bit STN
1	1	16-bit STN

Bit 4

Panel Resolution Select

Used with Bit 7 to select panel width. Refer to the bit 7 description.

Bit 3

Enable 4/8-bit LCD

0 = Enable 8-bit single LCD
1 = Enable 4-bit single LCD

Bit 2

Shading Method Select.

0 = Frame rate modulation (default).
1 = Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.

This bit is enabled by PR1A bit 0.

0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.

0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by bit 1.

CASE	DISPLAY MODE	CRT ENABLE	PANEL ENABLE	MONOCHROME OR COLOR	PANEL TYPE	STN INTERFACE	TFT INTERFACE	PLASMA INTERFACE	PANEL RESOLUTION	4-bit, 8-bit INTERFACE
		PR19		PR39	PR18	PR1A	PR18/ PR59	PR19	PR1A	PR1A
		5	4	5	1:0	6,5	2/4	7	7,4	3
1	CRT	1	0	0	0:0	0,0	0/0	0	0,0	
2	Panel-Mono-Dual-LCD-640	0	1	0	0:0	0,0	0/0	0	0,0	X
3	Panel-Mono-Single-LCD-640, 4-Bit	0	1	0	1:1	0,0	0/0	0	0,0	1
4	Panel-Mono-Single-LCD-640, 8-Bit	0	1	0	1:1	0,0	0/0	0	0,0	0
5	Panel-Color-Dual-STN 16-Bit-640	0	1	1	0:0	1,1	0/0	0	0,0	X
6	Panel-Color-Single-STN 16-Bit-640	0	1	1	1:1	1,1	0/0	0	0,0	X
7	Panel-Color-Single-STN 8-Bit-640	0	1	1	1:1	0,1	0/0	0	0,0	X
8	Panel-Color-Single-TFT 18-Bit-640	0	1	1	1:1	0,0	1/1	0	0,0	X
9	Panel-Color-Single-TFT 9 or 12-Bit-800	0	1	1	1:1	0,0	1/1	0	1,1	X
10	Panel-Color-Single-TFT 18-Bit-1024	0	1	1	1:1	0,0	1/1	0	1,0	X
11	Panel-Color-Single-TFT 9 or 12-Bit-640	0	1	1	1:1	0,0	1/0	0	0,0	X
12	Panel-Color-Single-TFT 9 or 12-Bit-1024	0	1	1	1:1	0,0	1/0	0	1,0	X
13	Panel-Mono-Plasma-2 Pixel	0	1	0	0:1	0,0	0/0	0	0,0	X
14	Panel-Mono-Plasma-1 Pixel	0	1	0	0:1	0,0	0/0	0	0,0	X
15	Panel-Mono-EL	0	1	0	0:1	0,0	0/0	0	0,0	X
16	CRT & Panel-Mono-Dual-LCD-640	1	1	0	0:0	0,0	0/0	0	0,0	X
17	CRT &Panel-Mono-Single-LCD-640,4-Bit	1	1	0	1:1	0,0	0/0	0	0,0	1
18	CRT &Panel-Mono-Single-LCD-640,8-Bit	1	1	0	1:1	0,0	0/0	0	0,0	0
19	CRT & Panel-Color-Dual-STN 16-Bit-640	1	1	1	0:0	1,1	0/0	0	0,0	X
20	CRT &Panel-Color-Single-STN 16-Bit-640	1	1	1	1:1	1,1	0/0	0	0,0	X
21	CRT &Panel-Color-Single-STN 8-Bit-640	1	1	1	1:1	0,1	0/0	0	0,0	X
22	CRT &Panel-Color-Single-TFT 18-Bit-640	1	1	1	1:1	0,0	1/1	0	0,0	X
23	CRT & Panel-Color-Single-TFT 9 or 12-Bit-800	1	1	1	1:1	0,0	1/1	0	1,1	X
24	CRT & Panel-Color-Single-TFT 18-Bit-1024	1	1	1	1:1	0,0	1/1	0	1,0	X
25	CRT & Panel-Color-Single-TFT 9 or 12-Bit-640	1	1	1	1:1	0,0	1/0	0	0,0	X
26	CRT & Panel-Color-Single-TFT 9 or 12-Bit-1024	1	1	1	1:1	0,0	1/0	0	1,0	X

NOTE: Shaded rows and columns indicate new operations supported by the WD90C24A controller.

TABLE B-4. DISPLAY TYPE AND OPERATION SELECTION SUMMARY

B.4.0 HARDWARE LINE DRAWING

NOTE

The Hardware Line Drawing feature is supported for the WD90C24A controller only.

B.4.1 STRIP LINE DRAWING

Strip line drawing is Microsoft Windows compatible.

B.4.1.1 Conditions

The following conditions must be met for strip line drawing to function properly.

- The line drawing must always start from left to right, regardless of other parameters such as top to bottom, bottom to top, Y-major, or X-major.
- The software must set up the BLT registers as if it were performing a rectangular fill.
- Software must also provide information concerning XSTEP, RSTEP, DELTA X, DELTA Y, X-DIRECTION, Y-DIRECTION, X-MAJOR, AND Y-MAJOR.

B.4.1.2 Altered BLT Register Functions

Some BLT register functions are altered during line draw. The altered register functions are given in the following list:

BLT INDEX	BLT FUNCTION	LINE DRAW FUNCTION
1.11	Reserved	0 = other BLT function 1 = Line Draw
1.9	Reserved	0 = X-Major (slope is less than 1) 1 = Y-Major (slope is greater than 1)
1.8	Reserved	Y-Direction 0 = Top to bottom 1 = Bottom to top
2	Source Low	XSTEP [9:0]
3	Source High	RSTEP [9:0]
6	Dimension X	Delta-X
7	Dimension Y	Delta-Y

TABLE B-5. BLT FUNCTIONS ALTERED BY LINE DRAW

B.4.1.3 Line Draw Operation

NOTE

The Line Drawing operation is supported for the WD90C24A controller only.

At the start of a Line Draw operation, the software must set up all necessary BITBLT registers for proper operation.

After completion of a Line Draw operation, BITBLT Register Index 1, bit 11 must be set to 0 before the next BITBLT operation.

B.5.0 WD90C24A CONFIGURATION REGISTER DESCRIPTION

Memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data, CNF[31:0], at system power-on or reset. External pull-down resistors are used to set the state of the internal configuration registers. The resistors cause bits to be set in internal registers, which then establish the operating configuration at start up. Some configuration bits are contained in non-writable registers while others can be modified after start up.

The non-writable bits set features such as bus architecture that are not modified after start up. Configuration bits CNF[15:12], CNF10, and CNF0 can be changed by software after power-up. The memory data lines, AMD[15:0] and BMD[15:0], are all internally pulled up by 75Kohm resistors.

Table B-6 lists the WD90C24 Configuration Registers by the register number, and then provides the signal pin name and the CNF register function. Table B-7 lists the register bit functions.

NOTE

Shaded areas in the table indicate new operations supported by the WD90C24A controller.

CONFIGURATION (CNF) REGISTER	SIGNAL NAME	REGISTER FUNCTION
0	AMD0	BIOS ROM Mapping
1	AMD1	Reserved
2	AMD2	Works with CNF17 to determine the bus architecture, refer to Table 3-1 in the applicable data sheet.
3	AMD3	Video Clock Source Control
7:4	AMD7:AMD4	General Purpose Status
8	AMD11	General Purpose
9	AMD9	46E8h/3C3h Select I/O Port for Wake-up
10	AMD10	Reserved
11	AMD8	Select Operating Voltage
12	AMD12	General Purpose
13	AMD13	Used with CNF14 and CNF 16 to determine the memory mode configuration, refer to Table 4-1 in the applicable data sheet.
14	AMD14	Used with CNF13 and CNF 16 to determine the memory mode configuration, refer to Table 4-1 in the applicable data sheet.
15	AMD15	486 Host Indicator Bit
16	BMD0	Used with CNF13 and CNF 14 to determine the memory mode configuration, refer to Table 4-1 in the applicable data sheet.
17	BMD1	Works with CNF2 to determine the architecture, refer to Table 3-1 in the applicable data sheet.
18	BMD2	LCD Panel Select, refer to PR18, bit 0
19	BMD3	LCD Panel Select, refer to PR18, bit 1
20	BMD4	Local Bus: Select 2X clock to support Intel S-series 486 processor
21	BMD5	Reserved
27:22	BMD[11:6]	Configuration bits for VLBI Register 2DF1[5:0]
31:28	BMD[15:12]	Configuration bits for VLBI Register 2DF0[7:4]

TABLE B-6. CONFIGURATION REGISTERS

SIGNAL NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD0	R/W	0*	PR1[0]	0 = (No Pulldown) Enable BIOS ROM
				1 = (Pulldown) BIOS ROM is Mapped Out
AMD1	R	1*	PR1[1]	0 = (No Pulldown) Reserved
				1 = (Pulldown) Reserved
AMD2	---	2	---	0 = (Pulldown) Works with CNF17 to determine the bus architecture, refer to Table 3-1.
				1 = (No Pulldown) Works with CNF17 to determine the bus architecture, refer to Table 3-1.
AMD3	---	3	---	0 = (Pulldown) Select VCLK1 and VCLK2 as Input
				1 = (No Pulldown) Select VCLK1 and VCLK2 as Output
AMD4	R	4	PR5[4]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD5	R	5*	PR5[5]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD6	R	6*	PR5[6]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD7	R	7*	PR5[7]	0 = (No Pulldown) General Purpose Status Bit
				1 = (Pulldown) General Purpose Status Bit
AMD8	---	11	---	0 = (Pulldown) Force All Voltage Detectors to the value of the contents in PR70[4:0], regardless of the setting of PR70 Bit 5. This value is 5 VDC at power-on and reset.
				1 = (No Pulldown) Allow Automatic Voltage Detect
AMD9	---	9	---	0 = (Pulldown) 3C3h I/O Port. VGA wake-up is enabled by setting Port 3C3h Bit 0 to 1.
				1 = (No Pulldown) 46E8h I/O Port. VGA wake-up is enabled by using I/O Ports x102h and 46E8h.
AMD10	---	10	---	Reserved
AMD11	R	8*	PR5[3]	0 = (No Pulldown) General Purpose Status Bit
AMD12	---	12	---	Reserved
AMD13	R/W	13	PR11[5]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1.

TABLE B-7. CONFIGURATION REGISTER BITS, CNF[31:0]

SIGNAL NAME	READ/ WRITE	CNF	REGISTER [BITS]	DESCRIPTION
AMD14	R/W	14	PR11[6]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1.
AMD15	---	15	---	0 = (Pulldown) Select 16-Bit Host Processor
				1 = (No Pulldown) Select 32-Bit Host Processor
BMD0	R	16	PR11[7]	0 = (Pulldown) Select Memory Mode Configuration
				1 = (No Pulldown) Select Memory Mode Configuration, refer to Table 4-1
BMD1	R	17	PR11[4]	0 = (Pulldown) Works with CNF2 to determine the bus architecture, refer to Table 3-1.
				1 = (No Pulldown) Works with CNF2 to determine the bus architecture, refer to Table 3-1.
BMD2	R/W	18	PR18[0]	0 = (Pulldown)
				1 = (No Pulldown) LCD Panel Select, refer to PR18, Bit 0
BMD3	R/W	19	PR18[1]	0 = (Pulldown)
				1 = (No Pulldown) LCD Panel Select, refer to PR18, Bit 1
BMD4	---	20	---	0 = (Pulldown) Select 2x Local Bus Clock
				1 = (No Pulldown) Select 1x Local Bus Clock
BMD5	---	21	---	Reserved
BMD[11:6]	---	27:22	2DF1[5:0]	0 = (Pulldown)
				1 = (No Pulldown) Configuration Bits for VLBI Register 2DF1[5:0]
BMD[15:12]	---	31:28	2DF0[7:4]	0 = (Pulldown)
				1 = (No Pulldown) Configuration Bits for VLBI Register 2DF0[7:4]

NOTES:

* A pulldown resistor sets these Bits to 1.

TABLE B-7. CONFIGURATION REGISTER BITS, CNF[31:0] (Continued)

B.6.0 I/O MAPPING

This section provides the following information:

- A Description of WD90C24 I/O Mapping
- A list of I/O Mapping groups (Table B-8)

B.6.1 DESCRIPTION

The I/O Mapping allows the WD90C24 to enter a test mode where all of its pins are divided into groups with inputs and outputs. The path for each group goes from the input pin(s), through the WD90C24, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table B-8 lists each group (path) with its corresponding input and output pins.

The WD90C24 must meet the following requirements in order to enter the I/O Mapping test mode.

- $\overline{\text{MEMR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CNF(2) is HIGH
- RESET is ACTIVE HIGH then goes LOW
- $\overline{\text{PDOWN}}$ is HIGH

If both $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in ISA(AT) machines and a reserved condition in the PS/2 machines. AMD2 high ensures that WD90C24 is in ISA(AT) mode.

Reset controls a transparent latch as shown in Figure B-1.

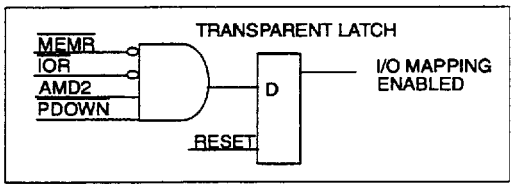


FIGURE B-1. ENABLING I/O MAPPING ON THE WD90C24

NOTE

Shaded areas in the table indicate new operations supported by the WD90C24A controller.

INPUT		OUTPUT	
PIN	**NAME**	**PIN**	**NAME**
1, 16	BMD0, BMD9	201	AMA0
3, 14	BMD1, BMD10	203	AMA1
8, 12	BMD3, BMD11	205	AMA2
6, 9	BMD2, BMD12	207	AMA3
7, 11	BMD13, BMD4	208	AMA4
4, 13	BMD14, BMD5	206	AMA5
2, 15	BMD15, BMD6	204	AMA6
17, 52	BMD7, PD16	202	AMA7
18, 51	BMD8, PD17	200	AMA8
42, 47	PD24, PD20	198	$\overline{\text{ARAS}}$
41, 46	PD25, PD21	196	$\overline{\text{AWE}}$
40, 45	PD26, PD22	24	$\overline{\text{BRAS}}$
39, 44	PD27, PD23	22	$\overline{\text{BWE}}$
20, 23	$\overline{\text{BCASL}}$, $\overline{\text{BCASH}}$	25	$\overline{\text{BOE}}$
38	PD28	172	VLBICS
37	PD29	165	PNLOFF
53, 115	SD15, SD5	123	STN13
54, 114	SD14, SD4	124	STN12
55, 112	SD13, SD3	126	STN11
56, 111	SD12, SD2	127	STN10

TABLE B-8. I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
58, 110	SD11, SD1	128	STN9
59, 109	SD10, SD0	129	STN8
71, 75, 78	$\overline{\text{IOCS16}}$, IRQ, $\overline{\text{ZWST}}$	119	XSCLK
61, 74	SD8, ALE	120	$\overline{\text{WPLT}}$
63, 85, 151	SLA17, SA5, SA29	137	VLD1
64, 86, 152	SLA18, SA6, SA30	136	VLD2
65, 87, 153	SLA19, SA7, SA31	135	VLD3
66, 89, 99	SLA20, SA8, $\overline{\text{IOW}}$	134	VUD0
67, 90, 98	SLA21, SA9, $\overline{\text{IOR}}$	133	VUD1
68, 91, 101	SLA22, SA10, $\overline{\text{MEMW}}$	132	VUD2
69, 92, 100	SLA23, SA11, $\overline{\text{MEMR}}$	131	VUD3
60, 70, 72	SD9, CLK486, $\overline{\text{MEMCS16}}$	77	IOCHRDY
73, 117	SBHE, SD7	121	$\overline{\text{RPLT}}$
76, 116	$\overline{\text{EIO}}$, SD6	122	STN14
80, 93, 146	SA0, SA12, SA24	144	FR

TABLE B-8. I/O MAPPING GROUPS

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
81, 94, 147	SA1, SA13, SA25	143	FP
82, 95, 148	SA2, SA14, SA26	142	LP
83, 95, 149	SA3, SA15, SA27	140	XSCLK
84, 97, 150	SA4, SA16, SA28	139	VLD0
161	EXCKEN	173	VSYNC
166	$\overline{\text{REFRESH}}$	168	FPUSR1, VCLK1
170	CKIN	167	FPUSR0
171	$\overline{\text{EBROM}}$, $\overline{\text{REFLCL}}$	164, 174	$\overline{\text{LCDENA}}$, HSYNC
175	PCLK	106	VCLK2
177, 190	AMD0, AMD9	28	BMA0
179, 188	AMD1, AMD10	30	BMA1
183, 186	AMD3, AMD11	32	BMA2
181, 184	AMD2, AMD12	34	BMA3
182, 185	AMD13, AMD4	35	BMA4
180, 187	AND14, AMD5	33	BMA5
178, 189	AMD15, AMD6	31	BMA6
50, 191	PD18, AMD7	29	BMA7
49, 192	PD19, AMD8	27	BMA8
194, 197	$\overline{\text{ACASL}}$, $\overline{\text{ACASH}}$	199	$\overline{\text{AOE}}$

TABLE B-8. I/O MAPPING GROUPS

B.7.0 PIN STATES FOR TYPICAL MODES

Table B-9 lists the connector pin states for typical operating modes.

KEY FOR TABLE B-9

H = pin in output high mode
I = pin in input mode
L = pin in output low
N = normal operation state
N÷8 = Normal frequency divided by 8
P = previous state held
Z = pin in high-impedance output mode
U = undetermined

NOTES FOR TABLE B-9

1. For internal PCLK mode, XMCLK and VCLK2 default to tristate, unless CNF(3)=1 which enables the VCLK2 output buffer. For external PCLK mode, these pins serve as the Memory and VCLK2 clock inputs.
2. $\overline{RAS}$ and $\overline{CAS}$ outputs are high except during refresh functions, where they operate as normal for the duration of the refresh cycle. If self-refresh is activated, $\overline{RAS}$ and $\overline{CAS}$ are sequenced low during powerdown modes.
3. When in external clock mode, this pin is input or output as determined by CNF(3) [AMD(3) high or low at reset].
4. Low if configured as an $\overline{FR}$ output, otherwise this is the normal $\overline{BLANK}$ signal to the external RAMDAC.
5. HSYNC and VSYNC are affected by programmable polarity options, and can be set static high with PR39 bit 2 = 0, or can be set static low by setting PR66 bit 3 = 1.
6. Output enable is usually low and write enable usually high to allow read cycles from display memory for screen updating.
7. This pin can be tristated by setting PR4, Bit 5 to 1.
8. This pin can be toggled using PR57, Bit 2.
9. This pin can be held static low by setting PR66, Bit 4 = 1.

NOTE

Shaded areas in the table indicate new operations supported by the WD90C24A controller.

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE REFRESH ACTIVE LOW	CRT MODE	LCD MODE	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES
EBROM	H	H	H	N	N	N	N	N	N
AMD(15:0)	I	N	N	Z	Z	Z	Z	Z	Z
AMA(8:0)	L	N	N	N	N	N	H	H	N
ARAS	H	N	N	L	L	L	N	N[2]	N[2]
ACASL/H	H	N	N	L	L	L	N	N[2]	N[2]
AOE	H	N[7]	N[7]	L	L	L	L	L	L
AWE	H	N[7]	N[7]	H	H	H	H	H	N
BMD(15:0)	I	N	N	Z	Z	Z	Z	Z	Z
BMA(8:0)	L	N	N	N	N	N	H	H	N
BRAS	H	N	N	L	L	L	N	N[2]	N[2]
BCASL/H	H	N	N	L	L	L	N	N[2]	N[2]
BOE	H	N[7]	N[7]	L	L	L	L	L	L
BWE	H	N[7]	N[7]	H	H	H	H	H	N
RED/ GREEN/ BLUE	U	U	N	N	N	L	L	L	L
HSYNC	L	L	L	N[6]	N[6]	L/H/N[6]	L	L	L
VSYNC	L	L	L	N[6]	N[6]	L/H/N[6]	L	L	L
PCLK	N[10]	N[10]	N[10]	N[10]	N[10]	N[10]	L	L	L
XMCLK[1]	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N
VCLK2[1,4]	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N	Z/N
FPUSR1/ VCLK1[4]	L/N	L/N	L/N	N	N	N	P/N	N	N
FPUSR0	L	L	L	N	N	N	P	N	N
LCDENA	H	H	H	N	H	L	H	H	H
PNLOFF	H	H	H	N[9]	H[9]	L[9]	H[9]	H[9]	H[9]
VUD(3:0), VLD(3:0)	L	L	L	N	N[10]	N	L/Z[8]	L/Z[8]	L/Z[8]
STN(14:8)	L	L	L	N	L	N	L/Z[8]	L/Z[8]	L/Z[8]
STN15/ RPLT	H	H	H	N	N	N	L/Z[8]	L/Z[8]	L/Z[8]
WPLT/ RGB4	H	H	H	N	N	N	L/Z[8]	L/Z[8]	L/Z[8]
XSCLKL/ RGB5	L	L	L	N	L	N	L/Z[8]	L/Z[8]	L/Z[8]
XSCLK	L	L	L	N	L	N	L/Z[8]	L/Z[8]	L/Z[8]
FR/ BLANK/ ENDATA	N	N	N	N	N[10]	N	L/Z[8]	L/Z[8]	L/Z[8]
LP	L	L	L	N	L	N	L/Z[8]	L/Z[8]	L/Z[8]
FP	L	L	L	N	L	N	L/Z[8]	L/Z[8]	L/Z[8]

NOTE: Refer to key and notes on the previous page.

TABLE B-9. RESET AND POWERDOWN STATES OF DISPLAY MEMORY AND VIDEO/PANEL INTERFACES

C.0 APPENDIX C - WD90C24A TO WD90C24A2 DIFFERENCE DATA

C.1 INTRODUCTION

This appendix describes the design and operational differences between the WD90C24A Controller and the WD90C24A2 Controller. Each of the controllers is thoroughly described in this data sheet. This appendix uses information contained in this data sheets to describe specific features and characteristics of the WD90C24A2 Controller that are not supported by the WD90C24A Controller.

C.1.1 PURPOSE

The information contained in the appendix is useful to electronic designers or developers who are already familiar with the WD90C24A Controller, and are now working with the WD90C24A2 Controller. The information in the appendix identifies the design differences to ease the transition to the newer controller.

C.1.2 ORDERING INFORMATION

Use the following number to order the WD90C24A2 controller:

90C24A2ZZ00

C.1.3 ADDITIONAL FEATURES OF THE WD90C24A2 CONTROLLER

The following paragraphs describe additional features and characteristics of the WD90C24A2 controller. Unless otherwise stated, the following features and characteristics apply only to the WD90C24A2 controller.

- Supports Monochrome TFT LCD Interface
- Provides fixed high-color modes (32K and 64K) so that these modes operate with the normal VCLK/MCLK ratio
- Drive strength for the VLBICS signal is increased from 8 mA to 16 mA
- Drive strength for the Local Bus data signals PD[30:16] is increased from 3 mA to 8 mA. The drive strength of PD31 and SD[15:0] remains as it was.

C.1.4 DRAM TIMING FOR WD90C24A2, REVISION B CONTROLLER

DRAM timing for the WD90C24A2 Controller (Revision D and subsequent) is given in Table 30-6. Table C-1 lists DRAM timing for the WD90C24A2, Revision B Controller only. For Table C-1, the nominal values are given at 39.8 MHz. The timing diagram is shown in Figure 30-5.

NOTE

To determine the specific DRAM address and control lines used for each display memory configuration, refer to Table 5-10.

NO.	SYMBOL /PARAMETER	MIN	MAX	NOMINAL AT 39.8 MHz	CONDITIONS
1	$\overline{ARAS}$, $\overline{BRAS}$ cycle time	6t - 2		151	Note 4
2	$\overline{ARAS}$, $\overline{BRAS}$ pulse width low	3t + 9		87	Note 4
3	$\overline{ARAS}$ high time (precharge)	2.5t + 5		64	Note 4
4	$\overline{ARAS}$ low to $\overline{ACASL}$, $\overline{ACASH}$ low, $\overline{BRAS}$ low to $\overline{BCASL}$, $\overline{BCASH}$ low	2.5t - 10		64	Note 4
5	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ cycle time	2t - 2		51	
6	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ pulse width low	1t + 2		31	Note 4
7	$\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high time (precharge)	1t - 10		19	Note 4
8	Row address setup to $\overline{ARAS}$, $\overline{BRAS}$ low	1t - 5		26	
9	Row address hold time from $\overline{ARAS}$, $\overline{BRAS}$ low	1t - 10		25	
10	Column address setup to $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 2		38	
11	Column address hold from $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 8		21	
12	Read Data valid before $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high	3		---	
13	Read data hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ high	10		---	
14	Write Data setup to $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	3t - 20		23	
15	Write Data hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	2t		76	
16	$\overline{AWE}$, $\overline{BWE}$ low setup before $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 5	1t + 3	25	
17	$\overline{AWE}$, $\overline{BWE}$ low hold after $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low	1t - 5	1t + 12	34	
18	$\overline{AOE}$, $\overline{BOE}$ high before $\overline{AWE}$, $\overline{BWE}$ low	2t - 8		49	
19	$\overline{AOE}$ low after $\overline{AWE}$ high, $\overline{BOE}$ low after $\overline{BWE}$ high	1t -10		13	
20	$\overline{ACAS}$, $\overline{BCAS}$ high for $\overline{CAS}$-before-$\overline{RAS}$ refresh	0.5t		42	
21	$\overline{ARAS}$, $\overline{BRAS}$ low from $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, $\overline{BCASH}$ low for $\overline{CAS}$-before-$\overline{RAS}$ refresh	1.5t		42	

TABLE C-1. DRAM TIMING FOR WD90C24A2, REVISION B CONTROLLERS

NOTES FOR TABLE C-1

[1]All values are given in nanoseconds (ns) unless otherwise specified.

[2]MCLK edge respective to $\overline{ARAS}$, $\overline{BRAS}$, $\overline{ACASL}$, $\overline{ACASH}$, $\overline{BCASL}$, and $\overline{BCASH}$, MA[8:0] edge delay may be up to 40 ns

[3]The timing is the result of setting PR33A (3C5, Index = 13) = XXX00000

[4]Timing is adjustable by PR33A.

[5]Memory write uses fast page early write, while keeping $\overline{AOE}$, $\overline{BOE}$ = 1

[6]Memory read uses fast page read, while keeping $\overline{AOE}$, $\overline{BOE}$ = 1

[7]$t = {}^{1}/_{MCLK}$

[8]The maximum MCLK frequency is dependent on DRAM speed as follows:
MCLK = 37.5 MHz for 80 ns DRAM
MCLK = 39.8 MHZ for some faster 80ns DRAM
MCLK = 44.3 MHZ for 70 ns DRAM
MCLK = 49.5 MHZ for 60 ns DRAM

C.1.5 SPECIFICATIONS FOR THE WD90C24A2 CONTROLLER

The following table lists the specifications for the WD90C24A2 controller.

Package Dimensions	Refer to Section 31.
Package temperature range (operating)	$0^{o}C$ to $80^{o}C$ (Refer to note.)
Storage Temperature	$-40^{o}C$ to $125^{o}C$
Power Supply Voltage	6.0 Volts
Voltage on all inputs and outputs with respect to V_{SS}	V_{SS} -0.3 to 7 Volts
Power Dissipation	1 Watt maximum
Electrostatic Discharge (ESD)	**REFER TO NOTE 3** All Pins except those listed below will withstand 1200V Human Body Model (HBM). The following pins will withstand 800V HBM: CKIN, REFRESH, AND RESET
Latch up Threshold	+/- 100 mA
Input Current	+/– 20 mA

NOTE:

1. The package temperature of $80^{o}C$ corresponds approximately to a $70^{o}C$ ambient temperature when the WD90C24A/A2 is mounted on FR4 or equivalent PC board material.
2. Unless otherwise specified, the values given in this table are absolute maximum ratings.
3. The ESD listed above is for the WD90C24A2 Controller. ESD for the WD90C24A Controller is listed in Section 27.

TABLE C-2. SPECIFICATIONS

CAUTION

Stresses above those listed in the table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

D.0 APPENDIX D - CHANGE RECORD for the WD90C24A/A2 DATA BOOK

D.1 SCOPE

This WD90C24A/A2 Data Book Change Record describes significant changes to the data book since it was last issued. This issue has been update and replaces the issue dated 6/30/94.

Whenever the data book is reissued, a new change record will be generated for that issue and all pages of the issue will carry the current issue date at the bottom of each page. This issue is dated 10/14/94.

D.2 DESCRIPTION OF CHANGES

This issue of the WD90C24A/A2 Data Book differs in significant ways from the previously published issue. The numbers of the pages that changed since the previous issue are listed in the change record. On each changed page, the changed text is marked by a change bar in the right margin of the text column. Changed figures are marked by a change bar on their title. These change bars are removed on subsequent issues and new change bars placed by the current changes.

Most editorial and typographical corrections are not marked. Also, data that was moved due to additions or deletions are not indicated by change bars.

D.3 CHANGE RECORD

The following table lists the page numbers for pages that were changed since the last issue date.

CURRENT ISSUE DATE	PREVIOUS ISSUE DATE	PAGES CHANGED SINCE THE PREVIOUS ISSUE
10/14/94	6/30/94	viii, 2, 11, 24, 107, 108, 115-117, 148, 149, 160, 161, 168, 169, 178, 188, 190, 191, 193, 197, 200, 207, 221, B-6, D-1

20.0 HARDWARE LINE DRAWING

This section describes hardware line drawing, which is used to generate Microsoft Windows compatible Strip line drawings.

20.1 CONDITIONS

The following conditions must be met for strip line drawing to function properly.

- The line drawing must always start from left to right, regardless of other parameters such as top to bottom, bottom to top, Y-major, or X-major.
- The software must set up the BLT registers as if it were performing a rectangular fill.
- Software must also provide information concerning XSTEP, RSTEP, DELTA X, DELTA Y, X-DIRECTION, Y-DIRECTION, X-MAJOR, AND Y-MAJOR.

20.2 ALTERED BLT REGISTER FUNCTIONS

Some BLT register functions are altered during line draw. The altered register functions are given in the following list:

BLT INDEX	BLT FUNCTION	LINE DRAW FUNCTION
1.11	Reserved	0 = other BLT function 1 = Line Draw
1.9	Reserved	0 = X-Major (slope is less than 1) 1 = Y-Major (slope is greater than 1)
1.8	Reserved	Y-Direction 0 = Top to bottom 1 = Bottom to top
2	Source Low	XSTEP [9:0]
3	Source High	RSTEP [9:0]
6	Dimension X	Delta-X
7	Dimension Y	Delta-Y

TABLE 20-1. BLT FUNCTIONS ALTERED BY LINE DRAW

20.3 LINE DRAW OPERATION

At the start of a Line Draw operation, the software must set up all necessary BITBLT registers for proper operation.

After completion of a Line Draw operation, BITBLT Register Index 1, bit 11 must be set to 0 before the next BITBLT operation.

(All data previously on this page has been deleted.. The page remains in place to preserve page numbering in the rest of the document.)

31.0 PACKAGE DIMENSIONS

Figure 31-1 illustrates the 208-pin MQFP package showing the dimensions in millimeters and inches.

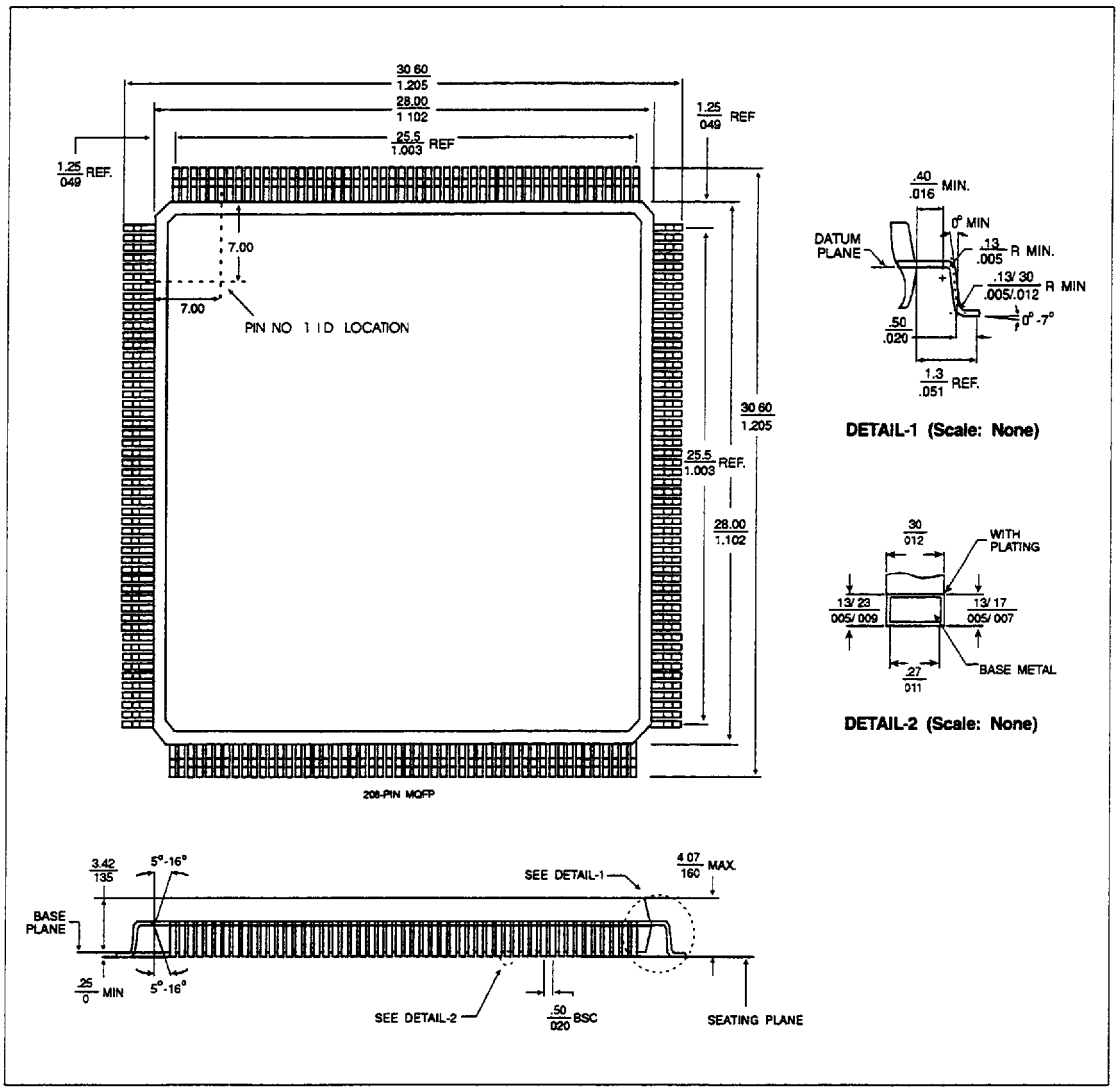


FIGURE 31-1. 208-PIN MQFP PACKAGE DIMENSIONS