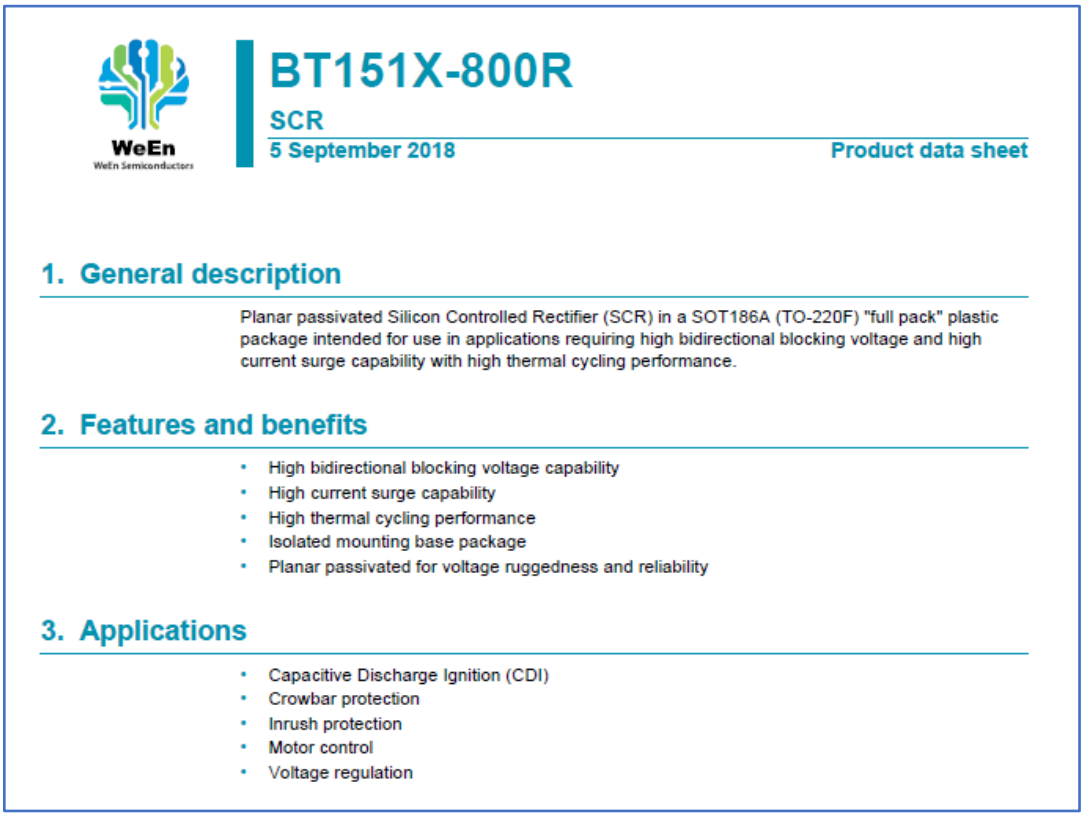
1. Introduction

Datasheets are not required to be created to a fixed international standard. This means datasheets must be read and interpreted carefully to ensure that parameter descriptions and values are correctly understood.

This datasheet note looks at the parameters defined and described in WeEn datasheets for SCRs.

2. Datasheet product profile

All WeEn's datasheets have the product name and type, revision number and publication date as the first page heading. This is followed by three sections, "General description", "Features and benefits" and "Applications". These sections describe the product to allow the reader to quickly understand its technology, main advantages and uses.



WeEn
WeEn Semiconductors

BT151X-800R

SCR

5 September 2018 **Product data sheet**

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high bidirectional blocking voltage and high current surge capability with high thermal cycling performance.

2. Features and benefits

- High bidirectional blocking voltage capability
- High current surge capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

Fig. 1 Example of a datasheet product profile (BT151X-800R)

The “Quick reference data” section highlights some important parameters for the product found in the main body of the datasheet.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 69$ °C		-	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	120	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	132	A
T_j	junction temperature			-	-	125	°C

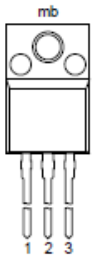
Fig. 2 Example of a datasheet product profile (BT151X-800R)

“Pinning information” contains a table and diagram to aid the correct identification of the product’s electrical terminals and package type.

“Ordering information” gives the product’s part number and package version. Sometimes there is a “Marking information” section. This gives data on the labelling printed on the device and data on the packing method.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-220F (SOT186A)	
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

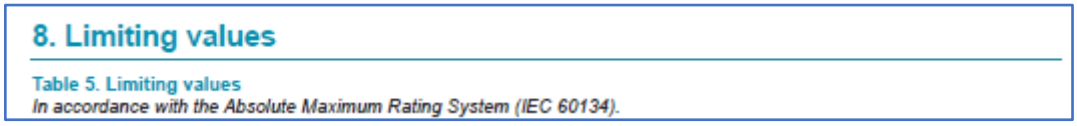
6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151X-800R	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

Fig. 3 Example of a datasheet product profile (BT151X-800R)

3. Datasheet "Limiting Values"



8. Limiting values

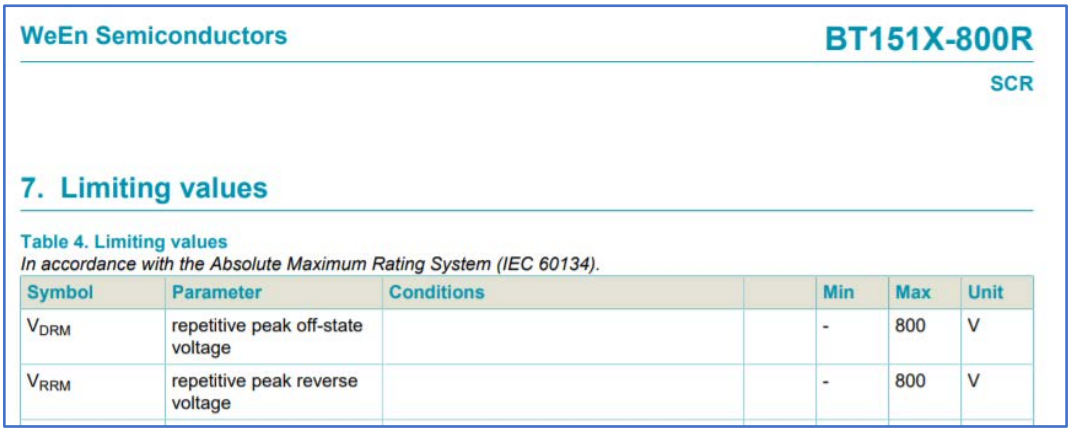
Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Fig. 4 Example of "Limiting Values" table heading

"Limiting Values" describe the limiting conditions that can be applied by a circuit without risk of damage to the SCR, and these limiting values reflect the SCR's capability. These are the absolute maximum ratings for *the operating and environmental conditions* and circuit designers should ensure these are not exceeded. These values may be maximum or minimum.

"Limiting" means that the value specified in the table must not be exceeded otherwise the product may malfunction, or "lose control" or even be damaged permanently. A limiting value is defined in accordance with the IEC-60134 international standard, known as the "Absolute Maximum Rating System".

3.1 V_{DRM} and V_{RRM}



WeEn Semiconductors BT151X-800R

SCR

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
V_{RRM}	repetitive peak reverse voltage			-	800	V

Fig. 5 Example of voltage ratings

V_{DRM} is the maximum allowable instantaneous repetitive peak off-state voltage (including transients) that the circuit can apply to the SCR when the gate is open circuit. "DRM" describes the voltage as "off-state" or "blocking", "Repetitive" and "Maximum". Similarly, in the reverse direction V_{RRM} is the maximum allowable repetitive reverse voltage including transients with "RRM" meaning "Reverse", "Repetitive" and "Maximum".

If V_{DRM} is exceeded the SCR *may* turn on without an applied gate current in the forward direction. If V_{RRM} is exceeded the SCR *may* conduct a large reverse avalanche current. Both situations could cause damage to an SCR depending on the circuit conditions.

The rated values of $V_{DRM(max)}$ and $V_{RRM(max)}$ may be applied continuously over the entire operating junction temperature range, provided that the thermal resistance between junction and ambient is low enough to avoid the possibility of thermal runaway.

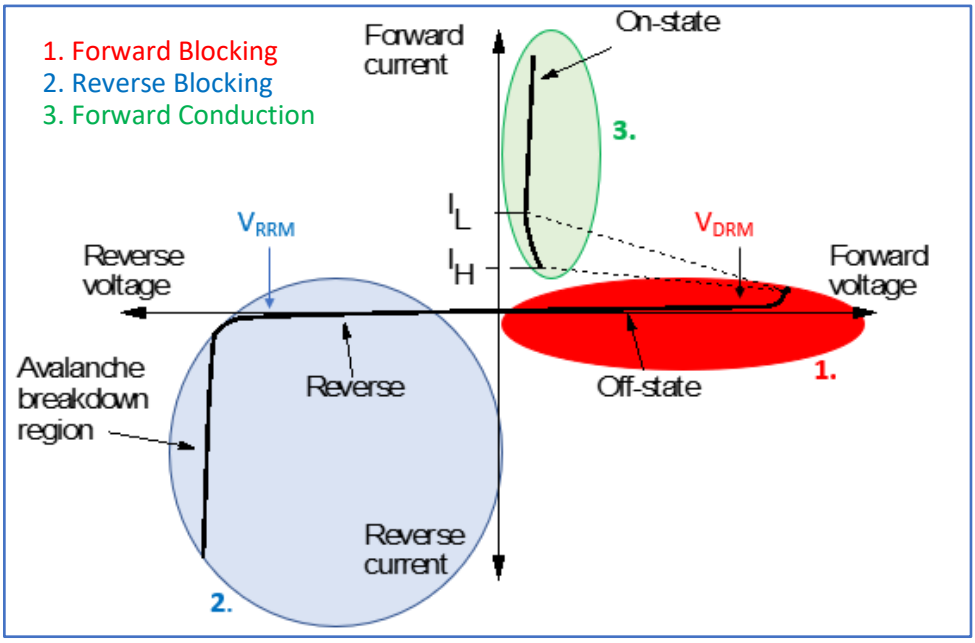


Fig. 6 Forward and reverse blocking voltage and on-state conduction operating regions

3.2 $I_{T(AV)}$ and $I_{T(RMS)}$

$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 69$ °C		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69$ °C; Fig. 1; Fig. 2; Fig. 3		-	12	A

Fig. 7 Example of current ratings

$I_{T(AV)}$ is the value of current for the SCR which under steady state conditions results in the rated temperature $T_{j(max)}$ being reached for a given package-related temperature condition. This temperature condition is specified as T_{mb} for “mounting-base” or “tab” type packages, T_h for plastic packages for “heatsink” mounting, T_{lead} for smaller plastic packages that cannot be heatsink mounted or T_{sp} for the solder point of surface mounted packages.

$I_{T(AV)}$ is related to the $I_{T(RMS)}$ current parameter by the equation, $I_{T(RMS)} / I_{T(AV)}$ = form factor.

Graphs relating these parameters to surge duration and temperature are usually found in WeEn datasheets.

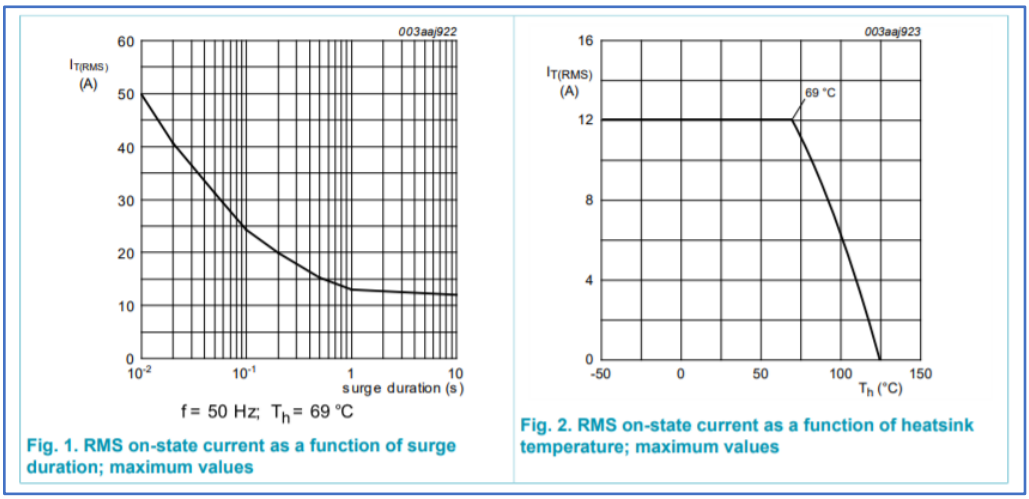


Fig. 1. RMS on-state current as a function of surge duration; maximum values

Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values

Fig. 8 Example of current graphics

The limiting value specified depends on the thermal resistance and size of any heatsink (for the package type in this example). The limiting value rises as the surge duration reduces below 2 seconds (see Fig. 8). A derating graph (Fig. 8) also indicates the reduction of the maximum current recommended for temperatures that may exceed T_h = 69 °C (for this BT151X-800R example).

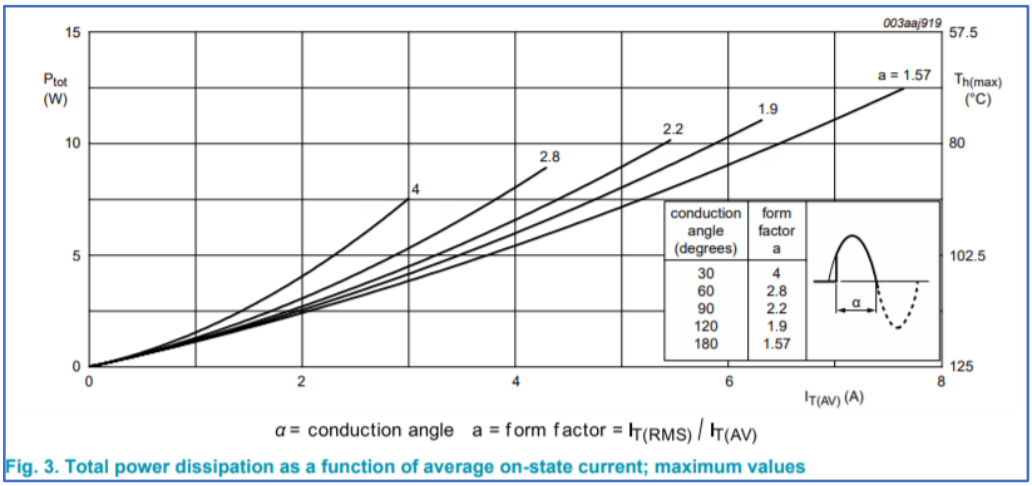


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

Fig. 9 Example of power dissipation graphic

The power dissipation of the SCR is directly proportional to the current and conduction angle. With the aid of the $T_{h(max)}$ values on the right-hand vertical axis, the maximum allowable power and $I_{T(AV)}$ for any given heatsink temperature is shown. For a given $I_{T(AV)}$, the power dissipated at small conduction angles is much higher than at large conduction angles. This is because of the higher $I_{T(RMS)}$ at small conduction angles. Operating the SCR at $I_{T(RMS)}$ values above the rated limiting value is likely to result in rapid thermal cycling which may affect the internal assembly of the SCR and lead to reliability issues.

3.3 I_{TSM}

I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	100	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	110	A

Fig. 10 Example of non-repetitive peak on state current rating

I_{TSM} is the maximum non-repetitive peak on-state surge current that may be applied to the SCR. It is specified for a one half-sine wave pulse at an initial junction temperature of 25 °C before surge with an AC mains frequency of 50 or 60Hz. The shorter the time period of the surge (higher frequency) the higher the I_{TSM} capability, but at very short durations the allowable I_{TSM} starts to decrease, as the rate of rise of current, dI_T/dt, becomes an additional limiting factor (see Fig. 11). Exceeding the I_{TSM} rating may damage the SCR. The I_{TSM} rating value decreases as the number of pulses increases and this is also shown in a graphic in the WeEn datasheet (see Fig. 12).

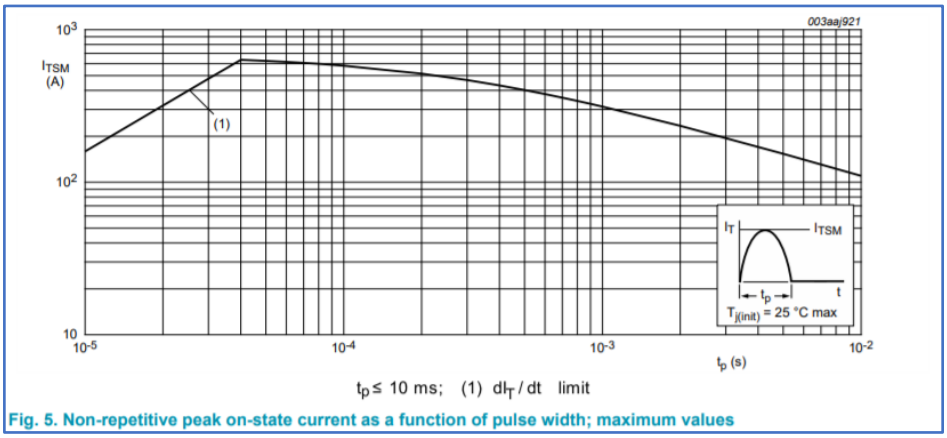


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

Fig. 11 Example of I_{TSM} versus pulse width

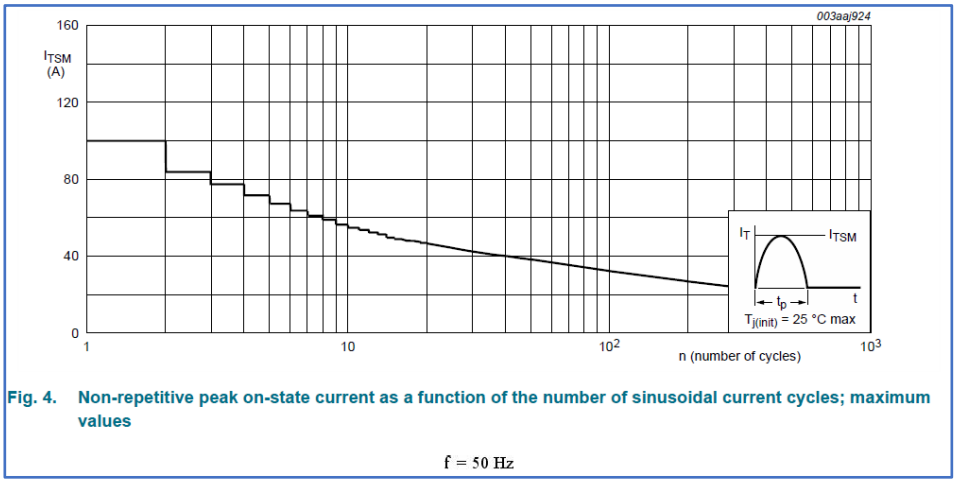


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

Fig. 12 Example of I_{TSM} versus number of pulses

3.4 I^2t

I^2t	I^2t for fusing	t_p = 10ms; sine wave	50	A^2s

Fig. 13 Example of I^2t rating

For correct circuit protection the I^2t of a protective fuse in series with the device must be less than the specified I^2t rating value of the device. This rating is numerically linked with the I_{TSM} rating by the equation:

$$I^2t = (I_{TSM}^2/2) \times t_p \equiv I_{TSM}^2/200$$

This is for t_p = 10ms (50Hz half-sine duration) fusing time.

The same value for I^2t is calculated when t_p = 8.33ms (60Hz half-sine duration) with the corresponding I_{TSM} rating at 60Hz.

3.5 dI_T/dt

dI_T/dt	rate of rise of on-state current	I_G = 30 mA		-	50	A/µs

Fig. 14 Example of rate of rise of on-state current rating

Maximum allowable rate of rise of on-state current after gate triggering is to limit local hot-spot heating close to the gate region of the SCR. After the gate is triggered and the SCR rapidly turns-on, such local heating takes place because of the SCR's internal structure and this can lead to degradation or complete failure. When an SCR is triggered by exceeding the breakdown voltage or by a high rate of rise of off-state voltage dV_D/dt, it is also important to consider limiting the dI_T/dt by good circuit design.

In the rating for the datasheet, a simple gate trigger condition is used. In fact, the magnitude of the gate current, rate of rise of the gate current, gate current pulse width and the peak load current limit are also important in determining the absolute rating for dI_T/dt.

3.6 P_{GM}, $P_{G(AV)}$, I_{GM}, V_{RGM}

I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W

Fig. 15 Example of gate ratings

The intention of these gate ratings is to reassure the circuit designer that the gate structure can handle the power that any real circuit may apply to it. The “average gate power” rating is intended to reflect designs where continuous gate current is applied, while the “peak gate power” rating is meant to apply to circuits where gate pulses are applied at the start of desired conduction.

For pulsed gate current, it is considered that the gate drive may be from a capacitor discharge with peak of current significantly higher than the pulse average. Hence, the peak gate power rating value is a factor of 10 above the average value. Provided the peak of those pulses does not exceed the peak gate current of 2A or peak gate power of 5W, then there is no risk of damage to the SCR gate structure.

It should be noted that these values of average and peak power are chosen to give a very good safety margin and reassurance to designers. They do not reflect the actual failure point of WeEn’s SCRs. In fact, the true capability of the gate structure of these SCRs is much higher than these values in the datasheet. However, it is WeEn’s judgement that these numbers are entirely adequate to cover all eventualities in design.

V_{RGM} is the rating that limits the maximum reverse voltage that can be applied across the gate and cathode pins without damaging the SCR.

The gate structure of an SCR is robust but when its capability to handle power is exceeded the SCR may degrade gradually or fail completely.

3.7 T_{stg}, T_j

T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

Fig. 16 Example of temperature ratings

T_{stg} gives the values for the range of temperature allowable for storage (dispatching, handling, warehousing) of the SCR. $T_{j(max)}$ is the maximum operating junction temperature for the SCR in the on-state or off-state. Although the junction temperature may transiently exceed $T_{j(max)}$ without damage, (e.g. during exceptional, brief, non-repetitive overload or fault conditions), for repetitive operation the peak junction temperature must remain below the absolute maximum rating.

3.8 V_{isol}, C_{isol}

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from anode to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

Fig. 17 Example of isolation ratings

The isolation voltage in this example is for the T0220F package. The capacitance value is a characteristic and is given as a typical value.

4. Datasheet "Characteristics"

"Characteristics" are the inherent measurable parameters for the SCR and are often stated with minimum or maximum values or both. Sometimes typical values are given. The limits define a range of values for the SCR's inherent parameter characteristics. These values are useful to the designer for optimizing the circuit and ensuring reliable operation.

4.1 Thermal characteristics

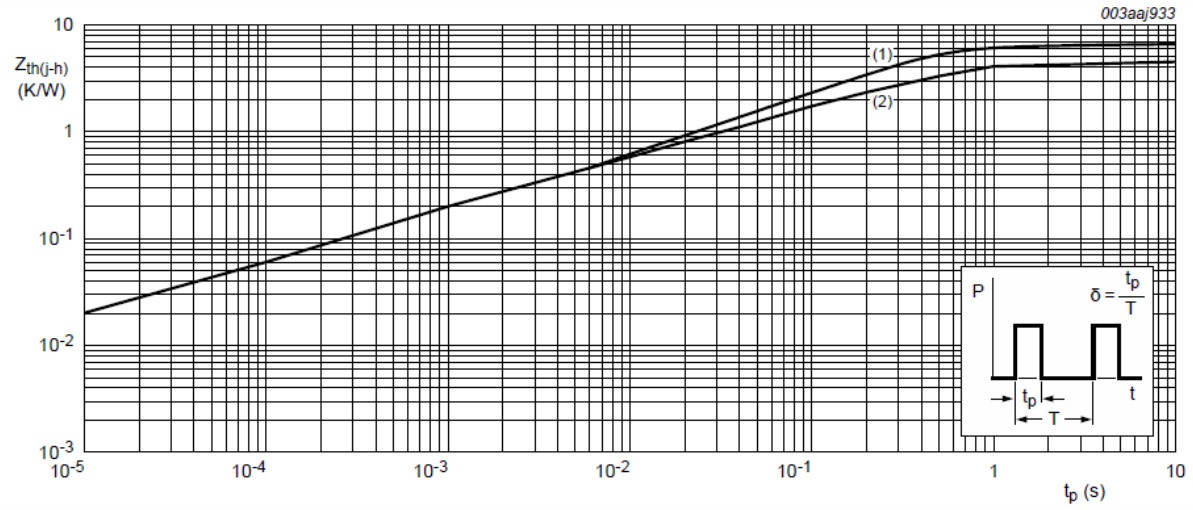
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6		-	-	4.5	K/W
		without heatsink compound; Fig. 6		-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W

Fig. 18 Example of thermal characteristics

Maximum steady-state thermal resistance values are given in the datasheet and are used to specify the SCR's current and power ratings. The average junction temperature rise for a given dissipation is the mathematical product of the average power dissipation and the thermal resistance.

A typical value of junction to ambient thermal resistance is given which assumes that through-hole leaded devices are mounted vertically on a PCB in free air. The value for surface mount packages is for a device soldered to a pad area on a given PCB material.



(1) Without heatsink compound
(2) With heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse width

Fig. 19 Example of transient thermal impedance graphic

Although average junction temperature rise may be calculated from the thermal resistance value, the peak junction temperature calculation requires knowledge of the current waveform and the transient thermal impedance curve. This curve in the datasheet is based on rectangular power pulses. Increasing the pulse duration results in higher transient thermal impedance (Z_{th}) until the steady-state, thermal resistance (R_{th}) is reached. If the application operates under transient (pulse) conditions, Z_{th} instead of R_{th} should be considered since R_{th} is applicable only to steady state, continuous operation. The temperature rise is calculated as the mathematical product of peak dissipation during the pulse by the thermal impedance for the given pulse width.

In practice, a power device frequently must handle composite waveforms rather than a simple rectangular pulse. This type of pulse can be simulated by superimposing several rectangular pulses which have a common time period but with both positive and negative amplitudes. Similarly, a burst of pulses can be treated as a composite waveform. Triangular, trapezoidal and sinusoidal waveforms can also be approximated by a series of rectangles. This analysis is covered elsewhere.

4.2 I_{GT}, I_L, I_H

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	7	20	mA

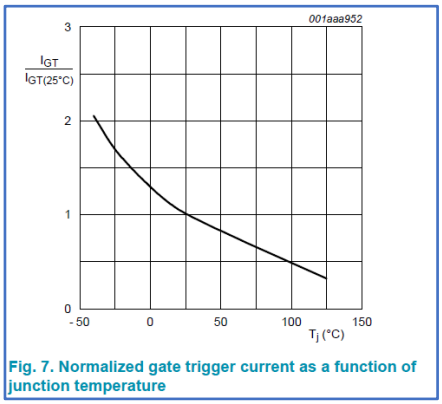


Fig. 7. Normalized gate trigger current as a function of junction temperature

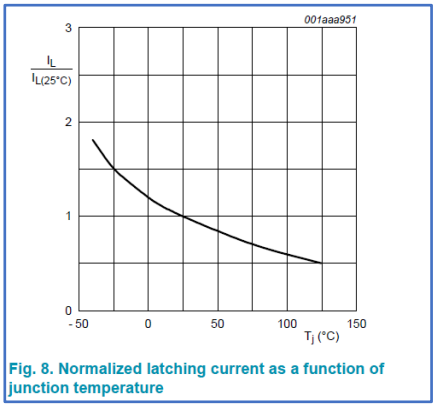


Fig. 8. Normalized latching current as a function of junction temperature

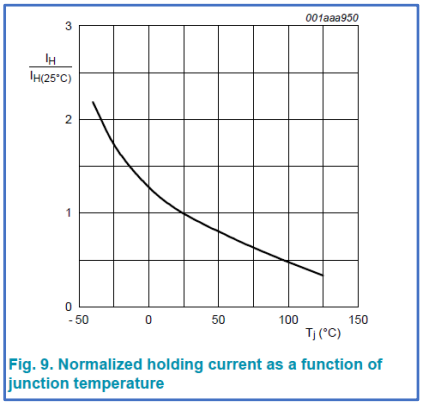


Fig. 9. Normalized holding current as a function of junction temperature

Fig. 20 Example of static characteristics, I_{GT}, I_L, I_H and temperature dependency graphics

The maximum gate trigger current, $I_{GT\,(max)}$, means that the triggering circuit must apply at least this value of gate current to guarantee triggering the SCR. If a minimum value is given in the datasheet, this indicates that below this value electrical noise on the gate will not trigger the SCR.

It is important to understand these values are stated for 25 °C. I_{GT} increases as junction temperature decreases and so in order to guarantee reliable triggering of the SCR the designer needs set the gate drive current for the lowest operating temperature for the application. The minimum recommended gate pulse width for reliable triggering is 10µs.

Latching current, I_L is the minimum current through the main terminals to keep the SCR "latched-on" after the gate current has been removed. I_L is also temperature dependent (see Fig. 20) and maximum and minimum operating temperatures must be considered when designing an optimal trigger circuit.

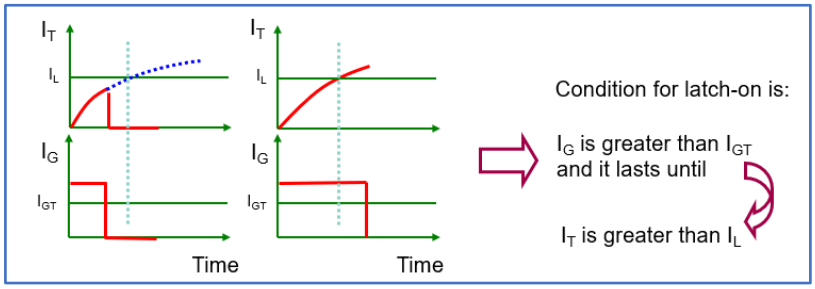


Fig. 21 Graphic showing interaction of I_{GT} and I_L

I_H is the value of holding current. The SCR will only turn off (commutate) when the current through the main terminals drops below this value. This current must remain below I_H for enough time to allow return to the off-state.

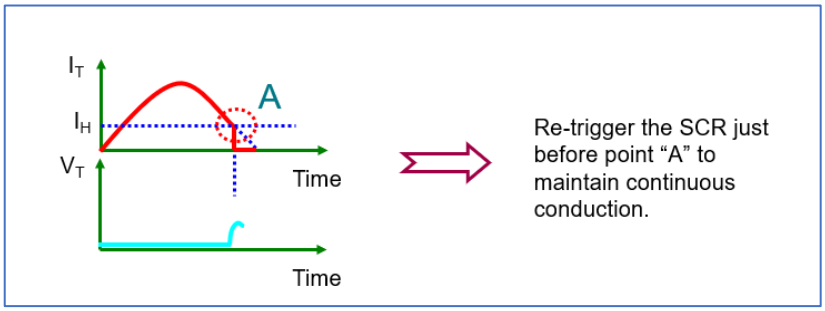


Fig. 22 Graphic showing interaction of I_T and I_H

I_H is also temperature dependent (see Fig. 20) and maximum and minimum operating temperatures must be considered to ensure conditions for safe commutation are met.

4.3 V_{GT}

V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.6	1	V
		V_D = 800 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V

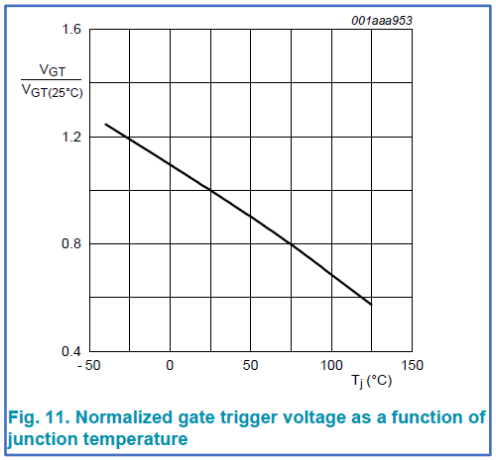


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

Fig. 23 Example of static characteristic V_{GT} and temperature dependency graphic

The datasheet shows values for the typical and maximum gate trigger voltage at a gate current equal to I_{GT} at 25 °C. The graph shows the dependency on temperature.

The maximum gate trigger voltage is the gate voltage required to trigger the SCR. The trigger circuit must be able to supply at least the maximum V_{GT} in order to drive current into the gate to cause triggering. To ensure that the SCR will not trigger, the gate voltage must be held below the minimum gate trigger voltage. The

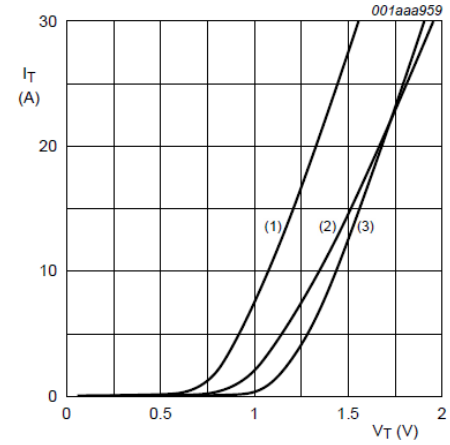
datasheet gives the minimum V_{GT} at the maximum junction temperature (125 °C in this example) and the maximum off-state voltage, V_{DRM}.

Because of the temperature dependency characteristics of I_{GT} and V_{GT}, the higher the junction temperature the easier it will be for the SCR to be wrongly triggered.

4.4 V_T

V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; Fig. 10		-	1.4	1.75	V

V_T is the on-state voltage for the SCR at 25 °C for a specified load current condition. This is the maximum instantaneous on-state voltage measured under pulse conditions to avoid excessive power dissipation.



V_o = 1.06 V; R_s = 0.0304 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

Fig. 24 Example of static characteristic V_T and graphic

The datasheet contains a graph with maximum and typical curves measured at the rated operating temperature (125 °C in this example) and at 25 °C. The maximum curve is used to calculate the power dissipation for a given average current. V_0 is the "knee voltage" and R_s is the slope resistance. If values for V_0 and R_s are not given in the data sheet, these can be generated manually as demonstrated in the graphic example (see Fig.25).

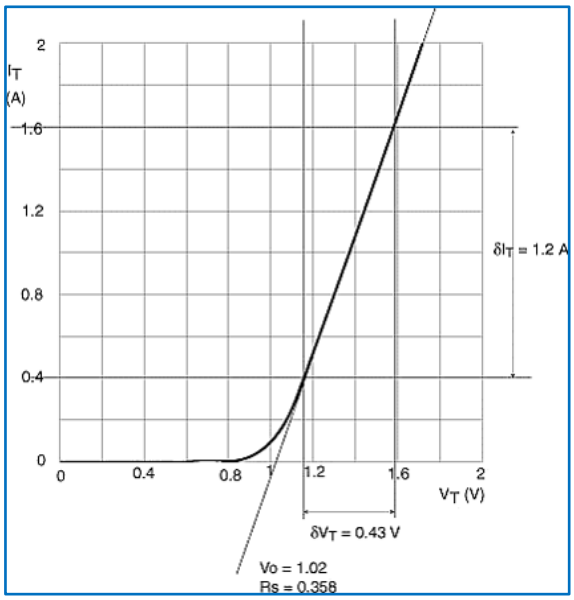


Fig. 25 Example graphic showing V_0 and R_s derivation

The on-state characteristic may be approximated by a linear model and the on-state voltage is then given by the equation: $V_T = V_0 + I_T.R_s$ and the instantaneous power dissipation is given by $P_T = V_0.\ I_T + I_T^2.R_s$ where I_T is the instantaneous on-state current.

It can be shown mathematically that the average on-state dissipation for any current waveform is given by the equation, $P_{T(AV)} = V_0.\ I_{T(AV)} + I_{T(RMS)}^2.R_s$, where $I_{T(AV)}$ is the on-state average current and $I_{T(RMS)}$ is the RMS value of the on-state current.

Therefore, in SCR datasheets, the graph for on-state dissipation can be calculated as a function of average current. Sinusoidal waveforms are assumed, and the graphs show the dissipation over a range of conduction angles. (See Fig. 9).

The derivation of V_0 and Rs and the power calculations are presented in WeEn Application Note WAN004.

4.5 I_D, I_R

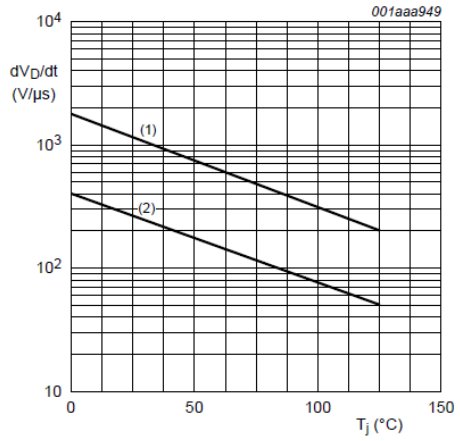
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 800 V; T_j = 125 °C		-	0.1	0.5	mA

Fig. 26 Example of static characteristics, I_D and I_R

The maximum and typical off-state leakages are at maximum operating junction temperature and maximum blocking and reverse voltage. Very high I_D leakage currents can lead to false triggering of the SCR, especially if it is a sensitive gate design with I_{GT} in the µA range.

4.6 Dynamic characteristics: dV_D/dt, t_{gt}, t_q

Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		200	1000	-	V/µs
		V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		50	130	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 100 mA; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 536 V; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; $R_{GK(ext)}$ = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs



(1) R_{GK} = 100 Ω;
(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

Fig. 27 Example of SCR dynamic characteristics with dV_D/dt graphic

Dynamic characteristics show how the SCR copes with fast-changing conditions in a circuit. These are not to be mistakenly understood as limiting values. “Dynamic” means continuous changes in voltage and current. Such characteristics are important when an SCR experiences a fast voltage transient while in the off-state. These characteristics are measured under specified conditions and often at maximum operating junction temperature.

The rate of change of blocking voltage (dV_D/dt) indicates an SCR’s ability to withstand a fast- changing voltage without causing spontaneous, unwanted turn-on of the SCR.

By convention this characteristic is tested with voltage set at 67% V_{DRM} and “dt” measured between 10% - 63% V_D with T_j = 125°C and gate open circuit.

There is internal junction capacitance between cathode and gate. The larger the junction area and the closer the geometries, the larger this capacitance. Consequently, very high dV_D/dt can generate or induce enough internal gate current to spontaneously trigger the SCR ($I_G = C.dV_D/dt$).

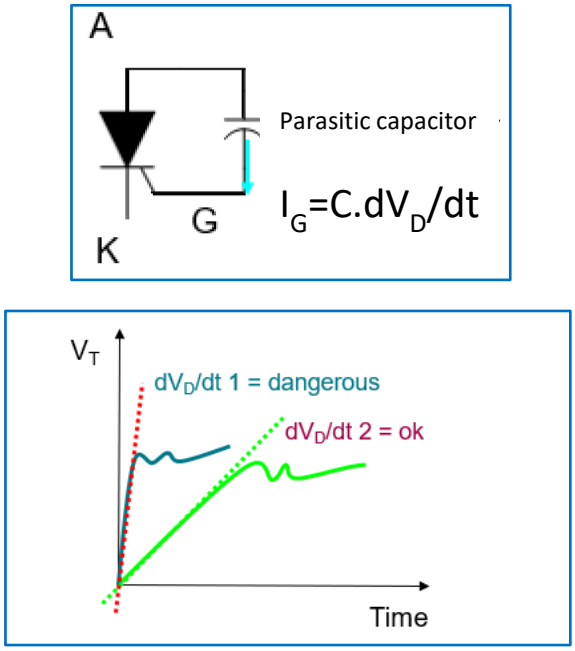


Fig. 28 dV_D/dt illustration

If in the circuit the maximum dV_D/dt is exceeded, the SCR may be triggered wrongly into conduction.

This event may not itself damage the SCR or adversely affect an application as this depends on the circuit, but such lack of control and susceptibility to electrical noise is not advisable. The higher the temperature and the lower the I_{GT}, the lower SCR's withstand capability and noise immunity.

Often for sensitive gate SCRs with I_{GT} in the μA range, a resistor of 1kΩ or lower is added in parallel with gate and cathode to reduce false triggering. This approach is less effective for standard gate SCRs with higher I_{GT}. Often, an RC snubber is added between anode and cathode to reduce the rate of rise of blocking voltage below the critical value. A resistance value of at least 47Ω and a capacitance value in the range 4.7nF to 100nF is suitable for the RC snubber.

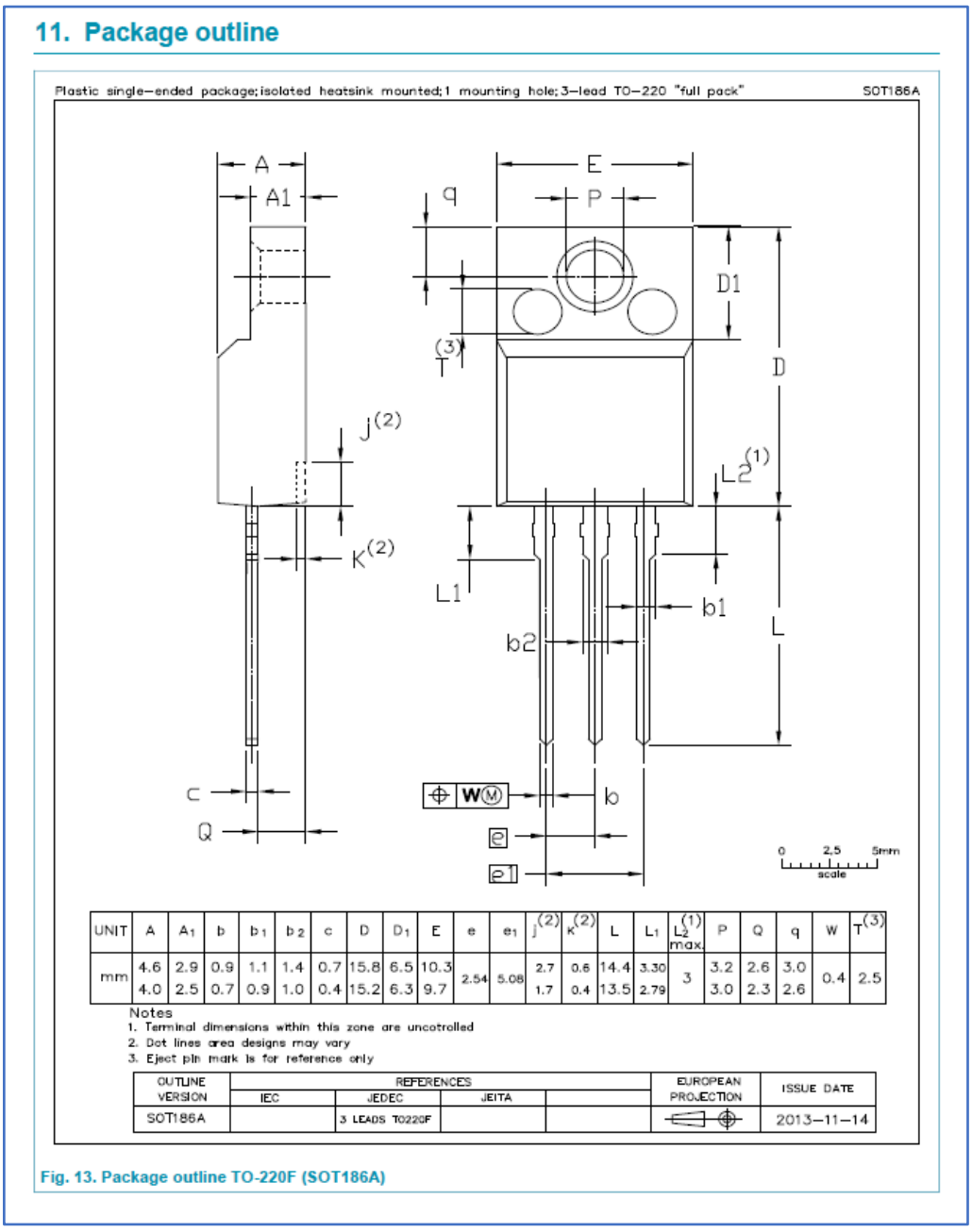
Larger capacitance and lower resistances cause greater stress to the SCR when triggering at non-zero volts and the designer needs to consider this. A fast discharge of the snubber capacitor can cause dI_T/dt damaging effects to the SCR if the resistance is too low.

A typical gate-controlled turn-on time, t_{gt} is specified for all SCRs.

A typical commutated turn-off time, t_q is specified for standard gate and sensitive gate SCRs.

5. Package outline drawing

The datasheet contains a package outline drawing of the device. If a surface mount package is described a soldering pad drawing may also be included.



11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	k(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncontrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

Fig. 13. Package outline TO-220F (SOT186A)

Fig. 29 Example package outline drawing (BT151X-800R)

Revision history

Rev	Date	Description
v.01	20190905	initial version
v.02	20190917	format updates, minor corrections and I^2t formula clarification
v.03	20190917	datasheet correction on I^2t value calculation

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