Asynchronous SRAM, 3.3V, 256Kx24

FEATURES

- 256Kx24 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 10, 12, and 15ns
  - Master Output Enable and Write Control
  - Three Chip Enables for Byte Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 119 Lead BGA (JEDEC MO-163), No. 391
  - Small Footprint, 14mmx22mm
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +3.3V (±5%) Supply Operation
- DSP Memory Solution
  - Motorola DSP5630x
  - Analog Devices SHARC™

DESCRIPTION

The WED8L24258VxxBC is a 3.3V, twelve megabit SRAM constructed with three 256Kx8 die mounted on a multi-layer laminate substrate. With 10 to 15ns access times, x24 width and a 3.3V operating voltage, the WED8L24258V is ideal for creating a single chip memory solution for the Motorola DSP5630x or a two chip solution for the Analog Devices SHARC™ DSP.

The single or dual chip memory solutions offer improved system performance by reducing the length of board traces and the number of board connections compared to using multiple monolithic devices.

The JEDEC Standard 119 lead BGA provides a 69% space savings over using six 256Kx4, 300 mil wide SOJs and the BGA package has a maximum height of 110 mils compared to 148 mils for the SOJ packages. The BGA package also allows the use of the same manufacturing and inspection techniques as the Motorola DSP, which is also in a BGA package.

FIG. 1 PIN CONFIGURATION

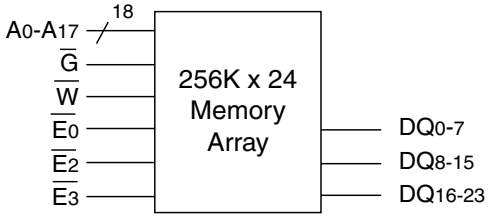
PIN SYMBOLS

	1	2	3	4	5	6	7
A	NC	AO	A1	A2	A3	A4	NC
B	NC	A5	A6	$\overline{E0}$	A7	A8	NC
C	I/012	NC	$\overline{E2}$	NC	$\overline{E3}$	NC	I/00
D	I/013	VCC	GND	GND	GND	VCC	I/01
E	I/014	GND	VCC	GND	VCC	GND	I/02
F	I/015	VCC	GND	GND	GND	VCC	I/03
G	I/016	GND	VCC	GND	VCC	GND	I/04
H	I/017	VCC	GND	GND	GND	VCC	I/05
J	NC	GND	VCC	GND	VCC	GND	NC
K	I/018	VCC	GND	GND	GND	VCC	I/06
L	I/019	GND	VCC	GND	VCC	GND	I/07
M	I/020	VCC	GND	GND	GND	VCC	I/08
N	I/021	GND	VCC	GND	VCC	GND	I/09
P	I/022	VCC	GND	GND	GND	VCC	I/010
R	I/023	NC	NC	NC	NC	A17	I/011
T	NC	A9	A10	$\overline{W}$	A11	A12	NC
U	NC	A13	A14	$\overline{G}$	A15	A16	NC

PIN NAMES

A_{0-17}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQ_{0-23}	Common Data Input/Output
VCC	Power (3.3V ±5%)
GND	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1.5 Watts
Output Current.	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

NOTE: For TEHQZ,TGHQZ and TWLQZ, Figure 3

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.135	3.3	3.465	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	–	VCC+0.3	V
Input Low Voltage	VIL	-0.3	–	0.8	V

FIG. 2

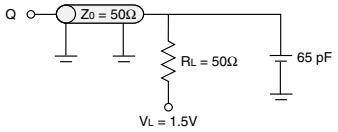
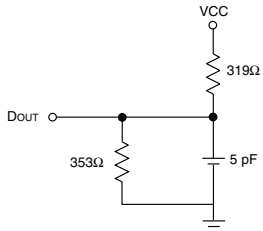


FIG. 3



DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				10ns	12-15ns	
Operating Power Supply Current	ICC1	$\overline{W}$= VIL, II/O = 0mA, Min Cycle		500	480	mA
Standby (TTL) Supply Current	ICC2	$\overline{E}$ > VIH, VIN < VIL or VIN > VIH, f=ØMHz		150	150	mA
Full Standby CMOS Supply Current	ICC3	E > VCC-0.2V VIN > VCC-0.2V or VIN < 0.2V		90	90	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±10	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±10	±10	µA
Output High Volltage	VOH	IOH = -4.0mA	2.4			V
Output Low Voltage	VOL	IOL = 4.0mA		0.4	0.4	V

TRUTH TABLE

G	$\overline{E0}$	$\overline{E2}$	$\overline{E3}$	W	Mode	Output	Power
X	H	H	H	X	Standby	High Z	ICC2,ICC3
H	L	L	L	H	Output Deselect	High Z	ICC1
L	L	L	L	H	Read (24 bit)	DOUT	ICC1
L	L	H	H	H	Read	DQ0-7	ICC1
L	H	L	H	H	Read	DQ8-15	ICC1
L	H	H	L	H	Read	DQ16-23	ICC1
X	L	L	L	L	Write (24 bit)	DIN	ICC1
X	L	H	H	L	Write	DQ0-7	ICC1
X	H	L	H	L	Write	DQ8-15	ICC1
X	H	H	L	L	Write	DQ16-23	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	8	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	$\overline{W}$, $\overline{G}$	8	pF
Chip Enable Lines	$\overline{EØ}$, $\overline{E2}$, $\overline{E3}$	8	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Read Cycle Time	TAVAV	TRC	10		12		15		ns
Address Access Time	TAVQV	TAA		10		12		15	ns
Chip Enable Access Time	TELQV	TACS		10		12		15	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6		7	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		6		7	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		5		6		7	ns

NOTE 1: Parameter is guaranteed, but not tested.

FIG. 4 READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

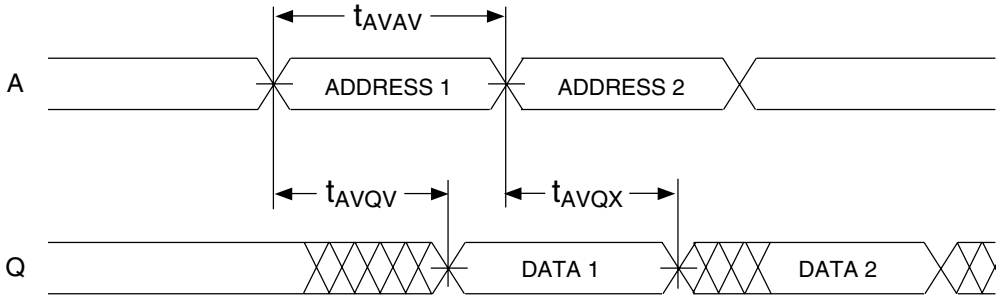
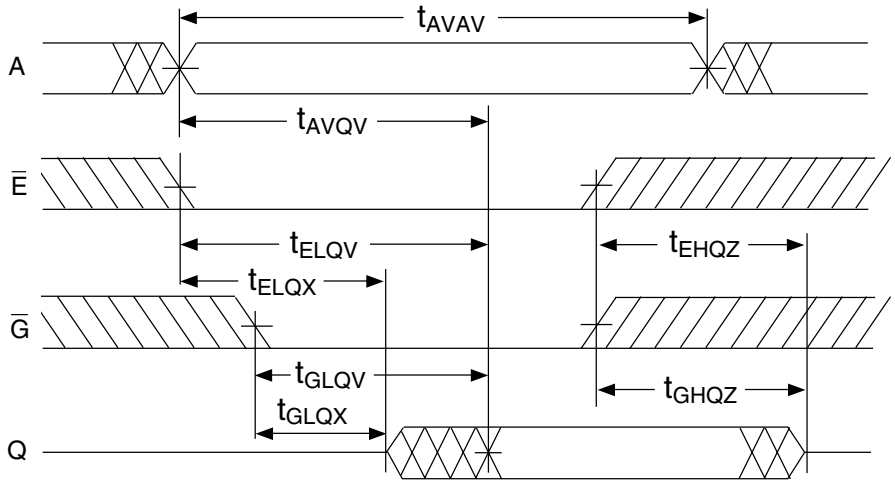


FIG. 5 READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Alt.	10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Write Cycle Time	TAVAV	TWC	10		12		15		ns
Chip Enable to End of Write	TELWH	TCW	8		9		9		ns
	TELEH	TCW	8		9		9		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	8		9		10		ns
	TAVEH	TAW	8		9		10		ns
Write Pulse Width	TWLWH	TWP	8		10		11		ns
	TWLEH	TWP	8		10		11		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	ns
Data to Write Time	TDVWH	TDW	6		6		7		ns
	TDVEH	TDW	6		6		7		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

NOTE 1: Parameter is guaranteed, but not tested.

FIG. 6 WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

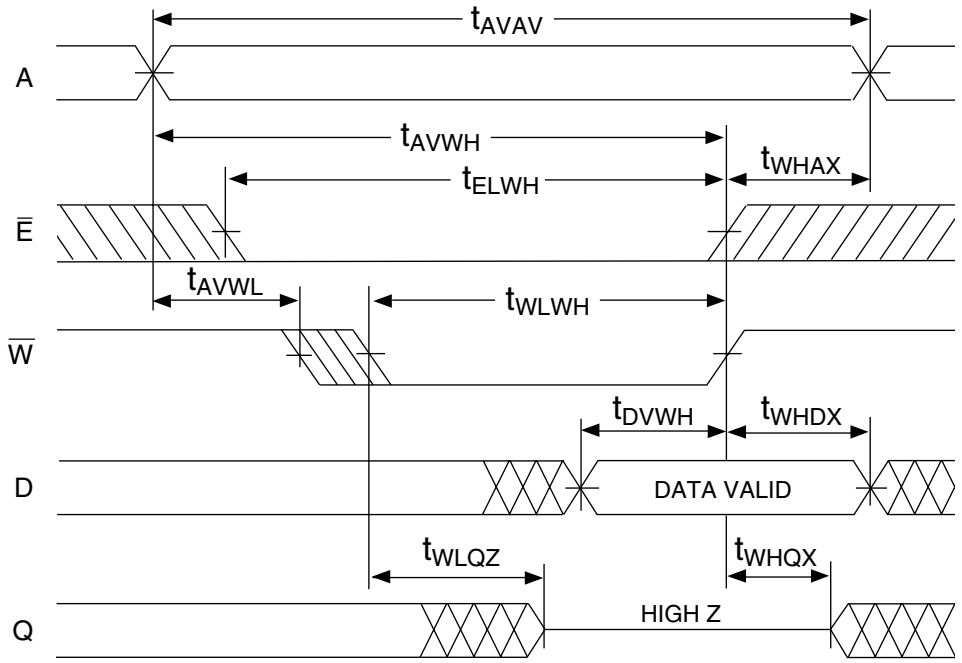
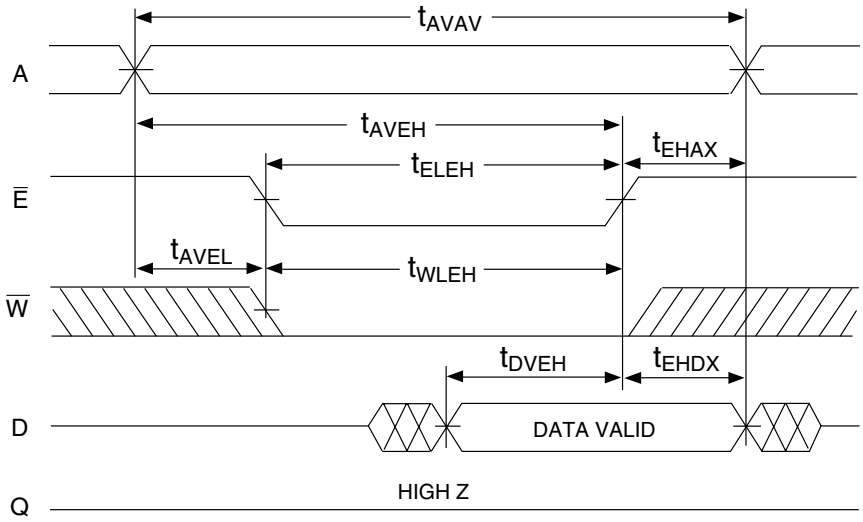


FIG. 7 WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



ORDERING INFORMATION

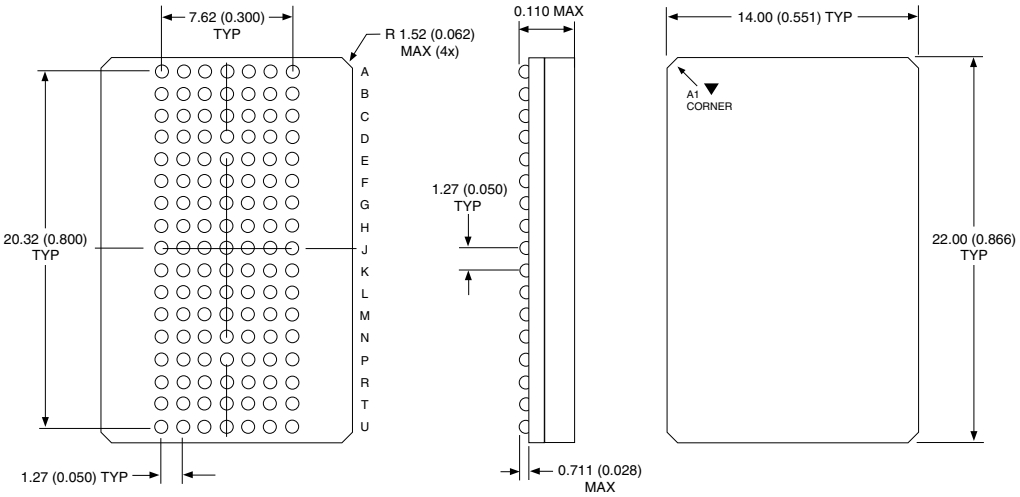
Commercial (0°C to +70°C)

Part Number	Speed (ns)	Package No.
WED8L24258V10BC	10	391
WED8L24258V12BC	12	391
WED8L24258V15BC	15	391

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
WED8L24258V12BI	12	391
WED8L24258V15BI	15	391

PACKAGE NO. 391
119 LEAD BGA
JEDEC MO-163



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES