2Mx16 NOR Flash MODULE
SMD 5962-97610*

WF2M16-XXX5

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
  - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
  - 44 pin Ceramic SOJ (Package 102)**
- Sector Architecture
  - 32 equal size sectors of 64KBytes each
  - Any combination of sectors can be erased. Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx16; User Configurable as 2 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation.
- RESET# pin resets internal state machine to the read mode.
- Ready/Busy (RY#/BY#) output for detection of program or erase cycle completion.
- Multiple Ground Pins for Low Noise Operation

This product is subject to change without notice.

* For reference only. See table page 7.

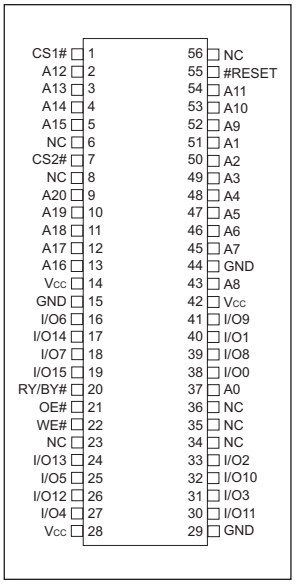
** Package to be developed.

Note: For programming information and waveforms refer to Flash Programming 16M5 Application Notes AN0038.

FIGURE 1 – PIN CONFIGURATIONS

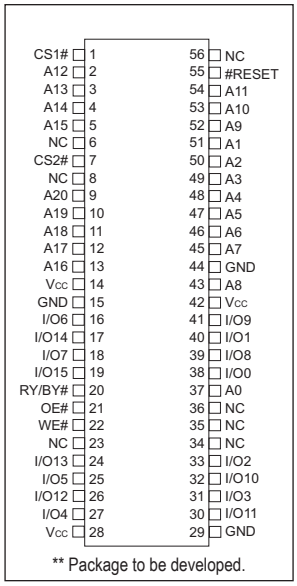
WF2M16-XDAX5
56 CSOP

TOP VIEW



WF2M16-XXX5
44 CSOJ (DL)**

TOP VIEW



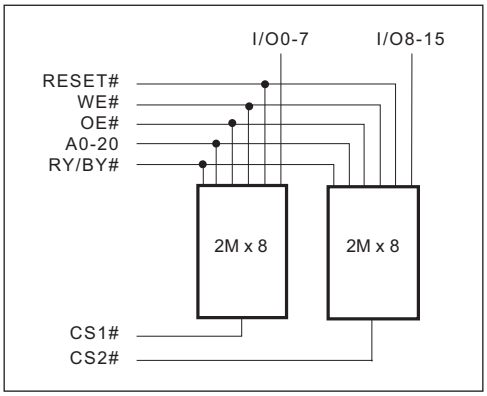
** Package to be developed.

NOTE:
1. RY/BY# is an open drain output and should be pulled up to Vcc with an external resistor.
2. Address compatible with Intel 2M8 56 SSOP.

PIN DESCRIPTION

I/O0-15	Data Inputs/Outputs
A0-20	Address Inputs
WE#	Write Enable
CS1-2#	Chip Select
OE#	Output Enable
Vcc	Power Supply
Vss	Ground
RY/BY#	Ready/Busy
RESET#	Reset

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-2.0 to +7.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Data Retention (Mil Temp)		20	years
Endurance — write/erase cycles (Mil, Q)		100,000 min.	cycles

NOTES:
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See . Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See .
2. Minimum DC input voltage on A9, OE#, RESET# pins is –0.5V. During voltage transitions, A9, OE#, RESET# pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Maximum DC input voltage on A9, OE#, and RESET# is 12.5 V which may overshoot to 13.5 V for periods up to 20 ns.

Stresses greater than those listed in this section may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	25	pF
WE# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz	25	pF
CS# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	15	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	15	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	–	+0.8	V
Operating Temperature (Mil, Q)	T_A	-55	–	+125°C	°C
Operating Temperature (Ind)	T_A	-40	–	+85	°C
Operating Temperature (Com)	T_A	0	–	+70	°C

DC CHARACTERISTICS – CMOS COMPATIBLE

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = $V_{CC\ MAX}$, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	V_{CC} = $V_{CC\ MAX}$, V_{OUT} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		80	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		120	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = $V_{CC\ MAX}$, CS# = V_{CC} ± 0.5V, f = 5MHz, RESET# = V_{CC} ± 0.5V		4.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = $V_{CC\ MIN}$		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -2.5 mA, V_{CC} = $V_{CC\ MIN}$	0.85xV_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The Icc current is typically less than 4mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns
RESET# Pulse Width		t_{RP}	500		500		500		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Read Cycle Time	T_{AVAV}	T_{RC}	90		120		150		ns
Address Access Time	T_{AVQV}	T_{ACC}		90		120		150	ns
Chip Select Access Time	T_{ELQV}	T_{CE}		90		120		150	ns
Output Enable to Output Valid	T_{GLQV}	T_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	T_{EHQZ}	T_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	T_{GHQZ}	T_{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	T_{AXQX}	T_{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		T_{READY}		20		20		20	µs

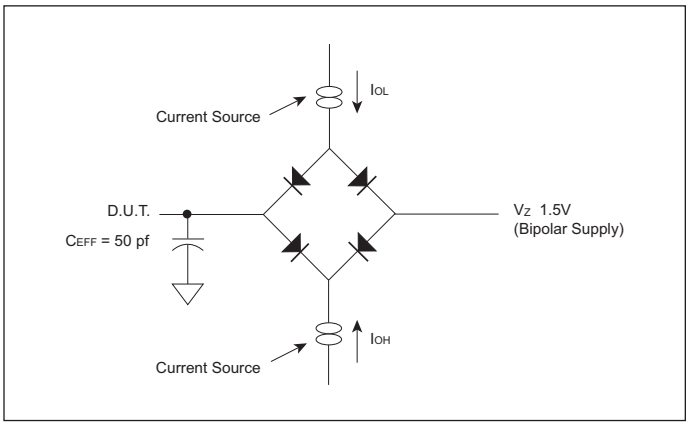
1. Guaranteed by design, not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

Parameter	Symbol		-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT

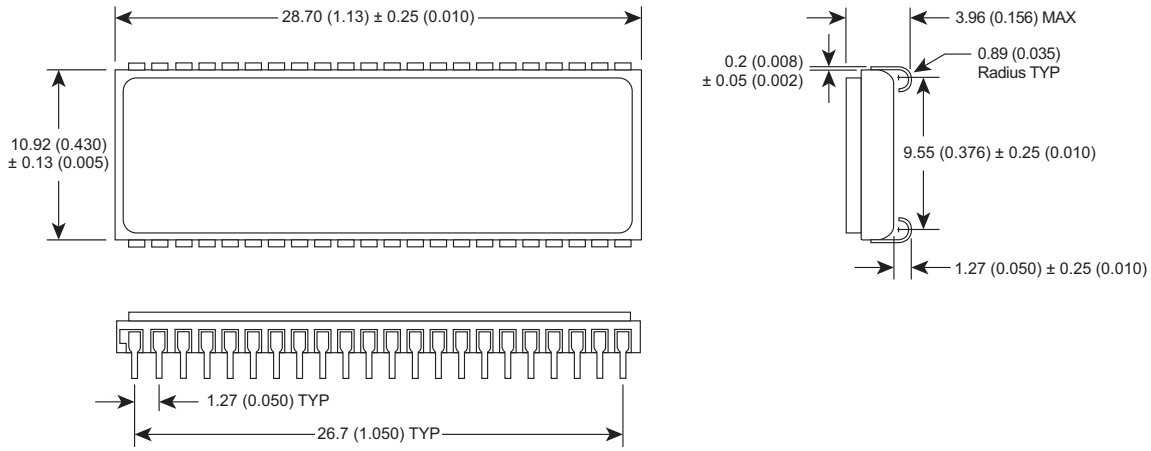


AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 ý.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.ATE tester includes jig capacitance.

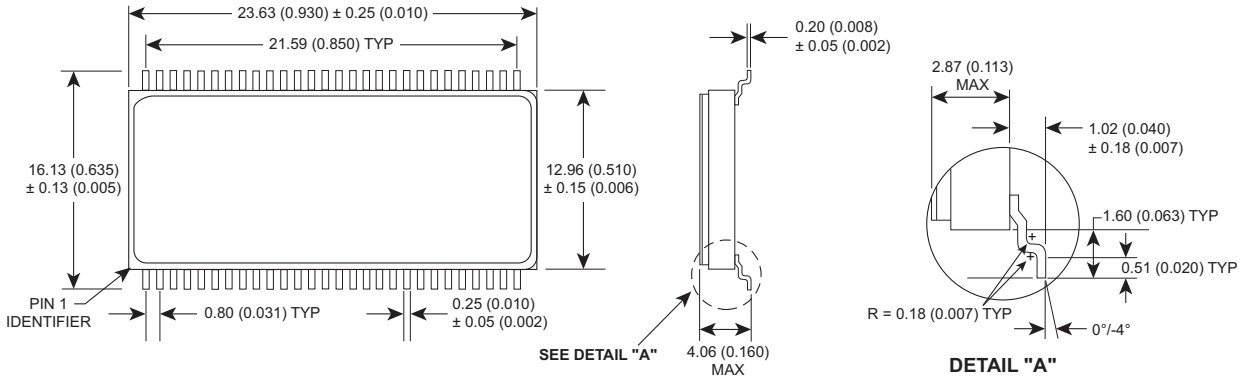
PACKAGE 102 – 44 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

PACKAGE 207 – 56 LEAD, CERAMIC SOP*

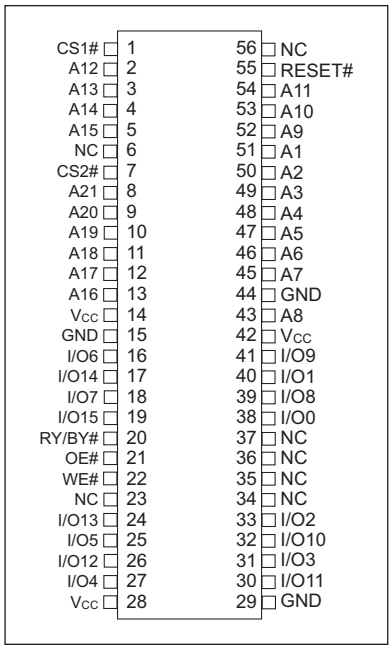


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

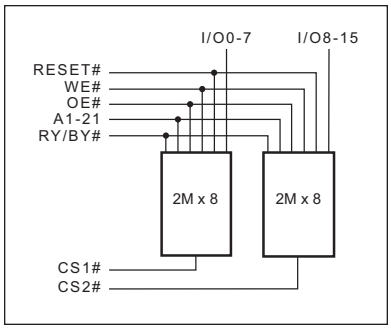
* Package Dimensions subject to change

FIGURE 8 – ALTERNATE PIN CONFIGURATION FOR WF2M16W-XDAX5

56 CSOP
TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-15	Data Inputs/Outputs
A0-21	Address Inputs
WE#	Write Enable
CS1-2#	Chip Select
OE#	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
RY/BY#	Ready/Busy
RESET#	Reset

NOTE:

1. RY/BY# is an open drain output and should be pulled up toV_{CC} with an external resistor.
2. Address compatible with Intel 1M16 56 SSOP.

ORDERING INFORMATION

W F 2M16 X - XXX X X 5 X

MERCURY SYSTEMS

NOR FLASH

ORGANIZATION of 2M x 16

User configurable as 2 x 2M x 8

IMPROVEMENT MARK:

- ***Address Pinout for 56 CSOP Package***

W = Word Wide Applications

ACCESS TIME (ns)

PACKAGE TYPE:

DA = 56 Lead CSOP (Package 207)
fits standard 56 SSOP footprint

DL = 44 Lead Ceramic SOJ (Package 102)*

DEVICE GRADE:

Q = Military Grade**.....-55°C to +125°C

M = Military Screened .....-55°C to +125°C

I = Industrial .....-40°C to +85°C

C = Commercial .....0°C to +70°C

V_{PP} PROGRAMMING VOLTAGE

5 = 5V

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

* Package to be developed.
** This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Mercury Systems data sheet.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 16 Flash MCP		150ns		5962-97610 04HXX
2M x 16 Flash MCP		120ns		5962-97610 05HXX
2M x 16 Flash MCP		90ns		5962-97610 06HXX

NOTE: This table is for reference only. For 5962-97610 ordering information and specifications refer to latest SMD document.

Document Title

2Mx16 NOR Flash MODULE, SMD 5962-97610

Revision History

Rev #	History	Release Date	Status
Rev 6	Changes (Pg. 1-13) 6.1 Change document layout from White Electronic Designs to Microsemi 6.2 Add document Revision History page	June 2011	Preliminary
Rev 7	Changes (Pg. 1, 13) 7.1 Add "NOR" to headline	August 2011	Final
Rev 8	Changes (Pg. 1, 13) 8.1 Update Features 8.2 Delete 44 Flatpack (FL)** from Figure 1 8.3 Update *Absolute Maximum Ratings*, *Recommended DC Operating Conditions* and *DC Characteristics* charts. 8.4 Delete subhead from *AC Characteristics* charts 8.5 Delete Figure 3 and all *AC Waveforms* diagrams 8.6 Update Packages 102, 208 and 207. 8.7 Update Ordering Information 8.8 Add note to SMD chart	June 2012	Final
Rev 9	Change (Pg. 7) 9.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 10	Change (Pg. 7) 10.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant" to "Military Grade."	August 2014	Final
Rev 11	Change (Pg. 5) (ECN 9789) 11.1 Changed lead dimensions on Package 207	January 2016	Final
Rev 12	Changes (Pg. All) (ECN 10156) 12.1 Change document layout from Microsemi to Mercury Systems	August 2016	Final