

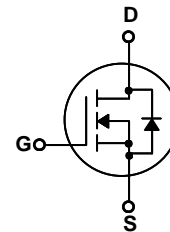
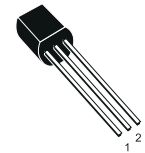


WFN1N60

600V N-Channel MOSFET

Features

- Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Extended Safe Operating Area
- Unrivalled Gate Charge :Qg= 10nC (Typ.)
- BVDS=600V,ID=1A
- R_{DS(on)} : 8 Ω (Max) @VG=10V
- 100% Avalanche Tested



TO-92

G-Gate,D-Drain,S-Source

Absolute Maximum Ratings *T_c=25°C unless other wise noted*

Symbol	Parameter	WFN1N60	Units
V _{DSS}	Drain-Source Voltage	600	V
I _D	Drain Current -continuous (T _c =25°C)	1*	A
	-continuous (T _c =100°C)	0.63*	A
V _{GS}	Gate-Source Voltage	± 30	V
E _{AS}	Single Pulsed Avanche Energy (Note1)	25	mJ
I _{AR}	Avalanche Current (Note2)	1	A
P _D	Power Dissipation (T _c =25°C)	23	W
T _J ,T _{STG}	Operating and Storage Temperature Range	-55 ~ +150	°C
TL	Maximum lead temperature for soldering purpose,1/8" from case for 5 seconds	300	°C

Thermal Characteristics

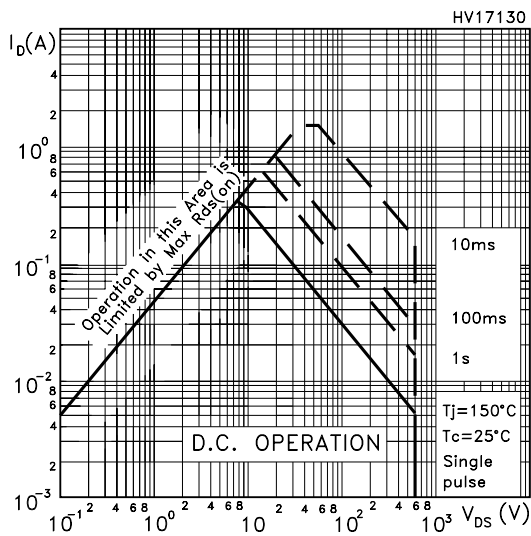
Symbol	Parameter	Typ.	Max	Units
R _{θJC} Thermal	Resistance,Junction to Case --			°C/W
R _{θJA}	Thermal Resistance,Junction to Ambient --	40		°C/W

* Drain current limited by maximum junction temperature.

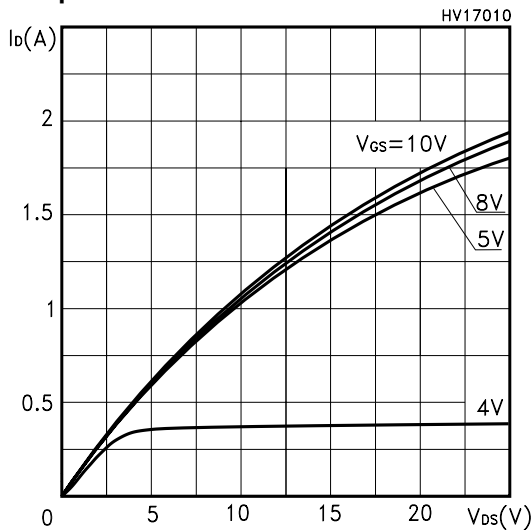
Electrical Characteristics $T_c=25^\circ\text{C}$ unless other wise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\ \mu\text{A}$, $V_{GS}=0$	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\ \mu\text{A}$, Reference to 25°C	--	3	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{ds}=600\text{V}$, $V_{gs}=0\text{V}$	--	--	1	μA
		$V_{ds}=480\text{V}$, $T_c=125^\circ\text{C}$			10	μA
I_{GSSF}	Gate-body leakage Current, Forward	$V_{gs}=+30\text{V}$, $V_{ds}=0\text{V}$	--	--	100	nA
I_{GSSR}	Gate-body leakage Current, Reverse	$V_{gs}=-30\text{V}$, $V_{ds}=0\text{V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$I_D=250\ \mu\text{A}$, $V_{ds}=V_{gs}$	2	--	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$I_D=0.5\text{A}$, $V_{gs}=10\text{V}$	--	--	8	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$	--	156		pF
C_{oss}	Output Capacitance		--	23.6		pF
C_{rss}	Reverse Transfer Capacitance		--	3.8		pF
Switching Characteristics						
$T_d(on)$	Turn-On Delay Time	$V_{DD}=300\text{V}$, $I_D=1\text{A}$ $R_G=25\ \Omega$ (Note 3,4)	--	6.5	--	nS
T_r	Rise Time		--	5	--	nS
$T_d(off)$	Turn-Off Delay Time		--	19	--	nS
T_f	Turn-Off Fall Time		--	25	--	nS
Q_g	Total Gate Charge	$V_{DS}=480$, $V_{GS}=10\text{V}$, $I_D=1\text{A}$ (Note 3,4)	--	7	10	nC
Q_{gs}	Gate-Source Charge		--	1.1	--	nC
Q_{gd}	Gate-Drain Charge			3.4	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	4	A
V_{SD}	Drain-Source Diode Forward Voltage	$I_D=1\text{A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=1\text{A}$, $V_{GS}=0\text{V}$	--	229	--	nS
Q_{rr}	Reverse Recovery Charge	$di_f/dt=100\text{A}/\mu\text{s}$ (Note3)	--	337	--	μC
*Notes	1, $L=55\text{mH}$, $I_{AS}=1.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J=25^\circ\text{C}$ 2, Repetitive Rating : Pulse width limited by maximum junction temperature 3, Pulse Test : Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$ 4, Essentially Independent of Operating Temperature					

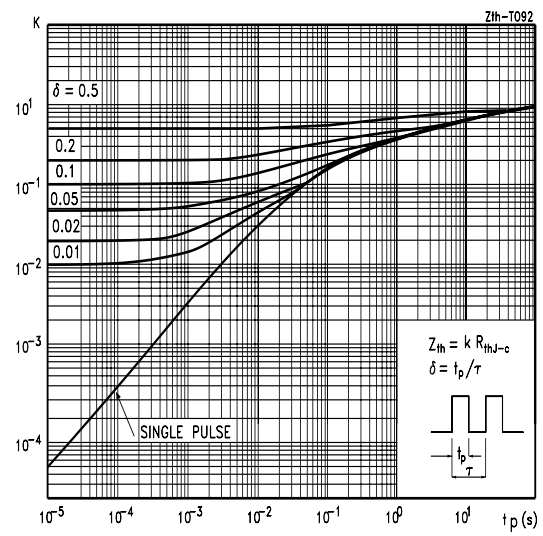
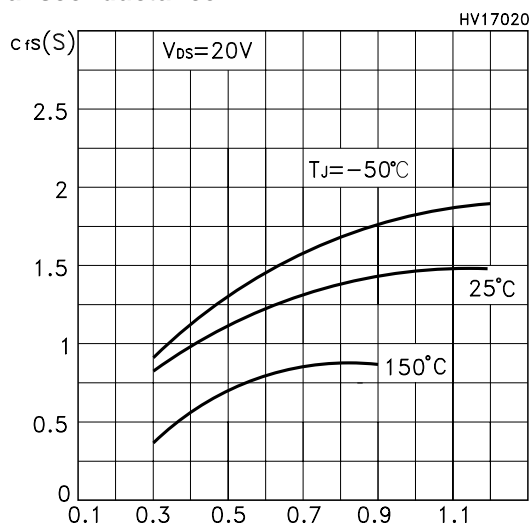
Typical Characteristics



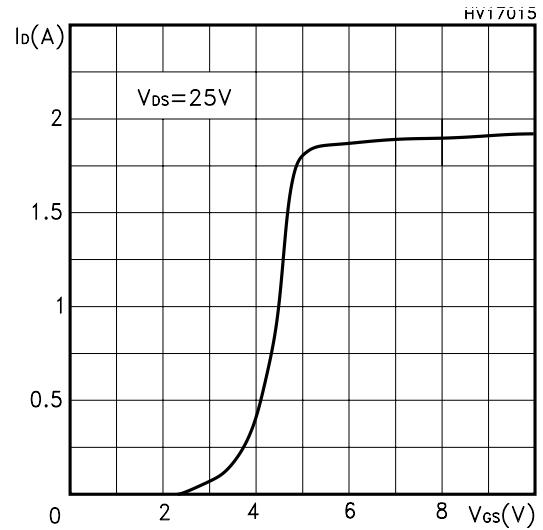
Output Characteristics



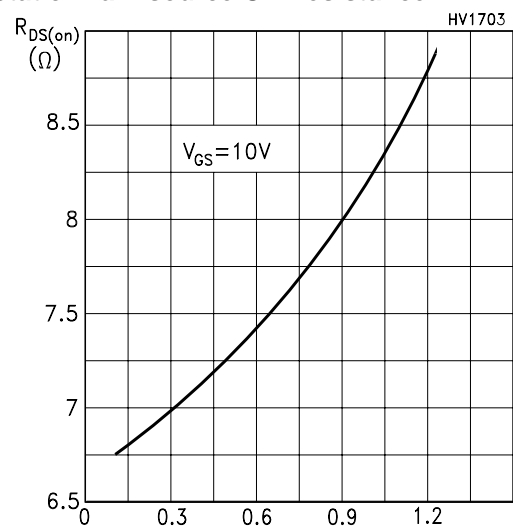
Transconductance



Transfer Characteristics

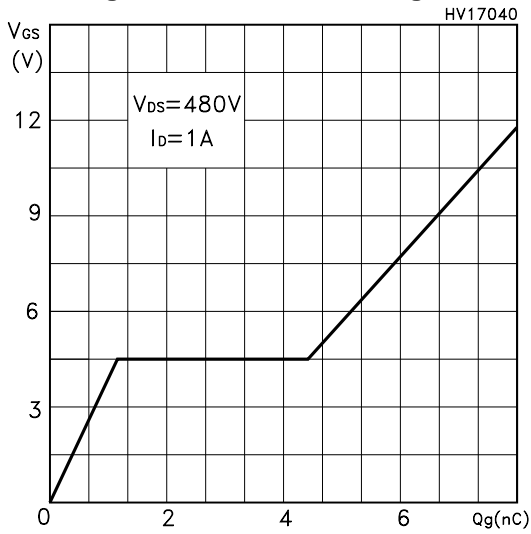


Static Drain-source On Resistance

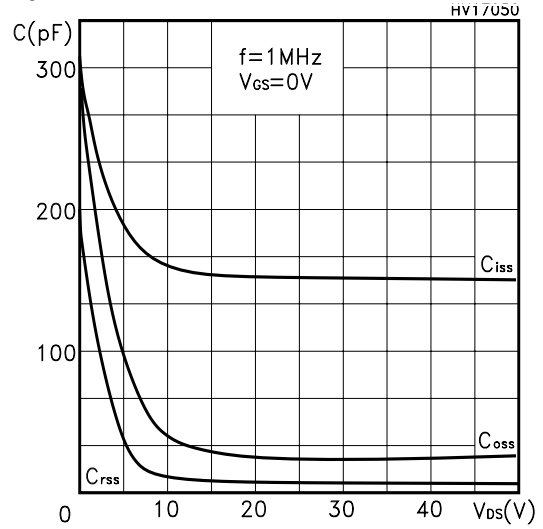


Typical Characteristics (Continued)

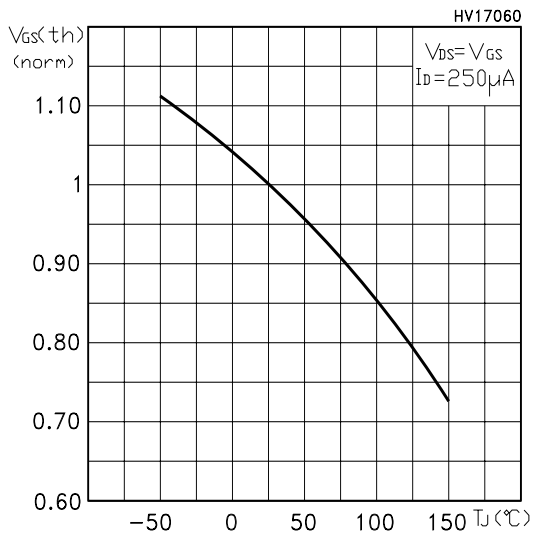
Gate Charge vs Gate-source Voltage



Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature

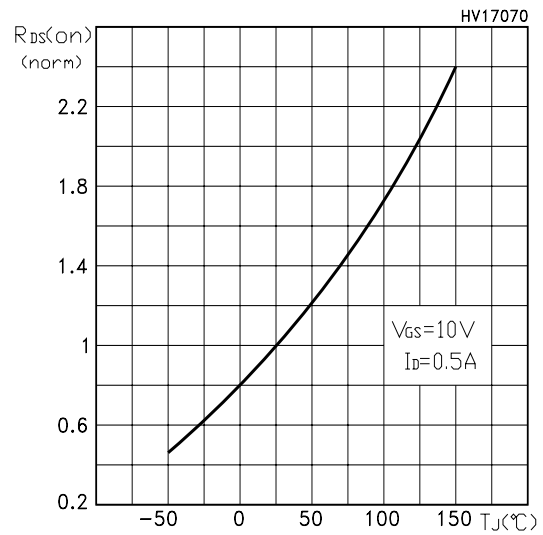


Fig. 1: Unclamped Inductive Load Test Circuit

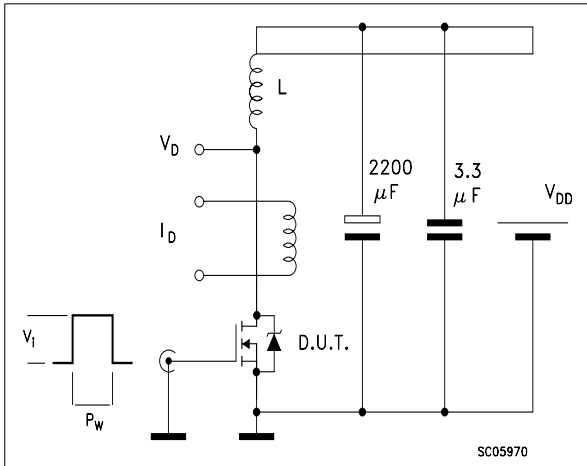


Fig. 2: Unclamped Inductive Waveform

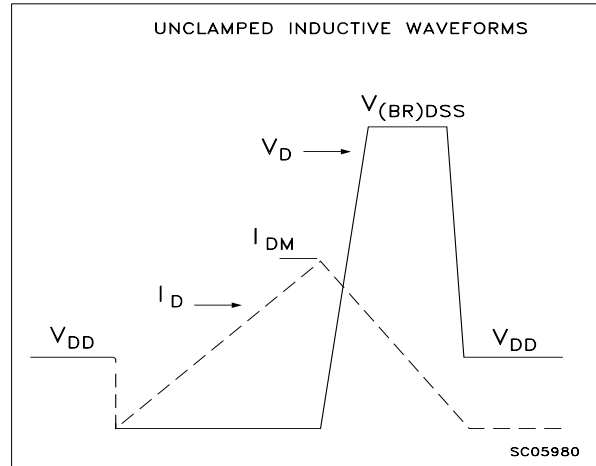


Fig. 3: Switching Times Test Circuit For Resistive Load

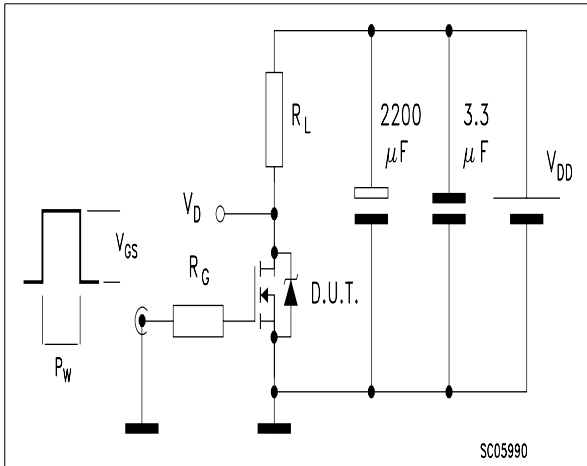


Fig. 4: Gate Charge test Circuit

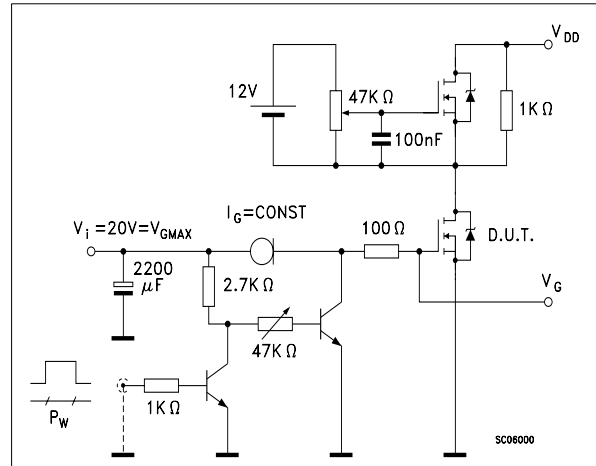


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

