

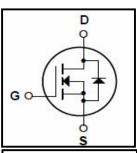
Silicon N-Channel MOSFET

Features

- 20A,60V, RDS(on)(Max39mΩ)@VGS=10V
- Ultra-low Gate Charge(Typical 6.1nC)
- High Current Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150°C)



This Power MO S FET is produced using Win se m i 's advanced planar stripe, This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch mode power supply. electronic Lamp ballasts based on half bridge and UPS.





Absolute Maximum Ratings

Symbol	Parameter	Value	Units
Voss	Drain Source Voltage	60	V
ΙD	Continuous Drain Current(@Tc=25°C)	20	А
	Continuous Drain Current(@Tc=100℃)	13	А
Ірм	Drain Current Pulsed tp=10us	76	А
Vgs	Gate to Source Voltage-Continuous	±20	V
Vgs	Gate to Source Voltage-Non-Repetitive(tp<10us)	±30	V
Eas	Single Pulsed Avalanche Energy (Note 2)	18	mJ
Is	Source Current (Body Diode)	20	А
PD	Total Power Dissipation(@Tc=25℃)	36	W
TJ, Tstg	Junction and Storage Temperature	-55~150	℃
TL	Channel Temperature(1/8" from case for 10s)	260	°C

Thermal Characteristics

Symbol	Doromotor		Lloito		
	Parameter	Min	Тур	Max	Units
Rajc	Thermal Resistance, Junction-to-Case	-	3.5	-	°C/W
RQJA	Thermal Resistance, Junction-to-Ambient	-	45	-	°C/W





Electrical Characteristics (Tc = 25°C)

Charac	teristics	Symbol	Test Condition	Min	Туре	Max	Unit
Gate leakage current		I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±100	nA
Gate-source breakdown voltage		V _{(BR)GSS}	Ig = 250µA, Vps = 0 V	60	-	-	V
Drain cut-off current		V _{DS} =100V, V _{GS} =0V, Tc = 25°C		-	-	1.0	μA
		lbss V _{DS} =100V, V _{GS} =0V,Tc= 125℃	-	-	100	μА	
Drain-source breakdown voltage		V(BR)DSS	ID = 250 μA, VGS = 0 V	60	-	-	V
Break Voltage Temperature		ΔBV _{DSS} /		-	60	-	mV/°C
Coefficient		ΔTJ	I _D =250µA,Referenced to 25°C				
Gate threshold voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 μA	1.0	1.8	3.0	V
Drain-source ON resistance		RDS(ON)	Vgs = 10 V, ID = 10A	-	26	39	mΩ
Forward Transconductance		gfs	V _{DS} = 15 V, I _D = 10A	-	8.0	-	S
Input capacitance	Input capacitance		V _{DS} = 25 V,	-	675		
Reverse transfer	Reverse transfer capacitance		V _G S = 0 V,	-	47		pF
Output capacitance		Coss	f = 1 MHz	-	68		
	Rise time	tr	V _{DD} =48	-	12.6		
Switching time	Turn-on time	ton	V _{DS} = 10V	-	6.5		ns
	Fall time	tf	 I _D =20A	-	2.4		
	Turn-off time	toff	R _G =2.5Ω	-	18.2		
Total gate charge (gate-source		Qg	V _{Ds} =48V		7.6		
plus gate-drain)			Vgs =10V	-	7.6		nC
Gate-source charge		Qgs	ID =20A	-	2.2	-	
Gate-drain ("miller") Charge		Qgd		-	4.3	-	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Туре	Max	Unit
Continuous drain reverse current	I _{DR}	-	-		20	Α
Pulse drain reverse current	IDRP	-	-		76	Α
Forward voltage (diode)	VDSF	IDR = 10A, VGS = 0 V	-	0.87	1.2	V
Reverse recovery time	trr	IDR = 1A, VGS = 0 V,	-	17	-	ns
Reverse recovery charge	Qrr	dl _{DR} / dt = 100 A / μs	-	12	-	μC

Note 1. Surface-mounted on FR4 board using 1 in sq pad size(Cu area = 1.127 in sq [2 oz] including traces.

This transistor is an electrostatic sensitive device, Please handle with caution

^{2.} Pulse Test: Pulse Width ≤ 300 s, Duty Cycle ≤ 2%.

^{3.} Switching characteristics are independent of operating junction temperatures.



TYPICAL PERFORMANCE CURVES

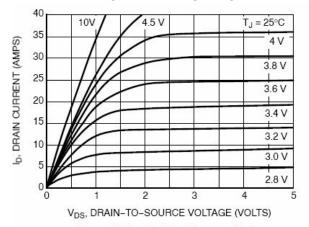


Figure 1. On-Region Characteristics

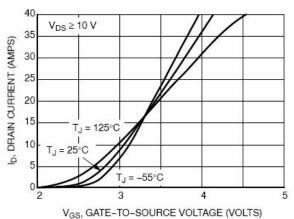


Figure 2. Transfer Characteristics

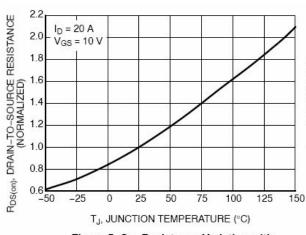


Figure 5. On-Resistance Variation with Temperature

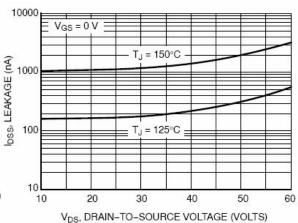


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

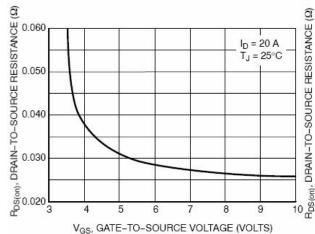


Figure 3. On-Resistance vs. Gate-to-Source Voltage

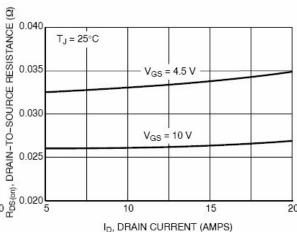


Figure 4. On-Resistance vs. Drain Current and Gate Voltage



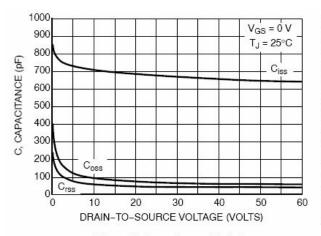


Figure 7. Capacitance Variation

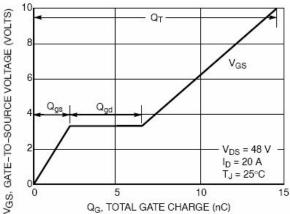


Figure 8. Gate-To-Source Voltage vs.
Total Charge

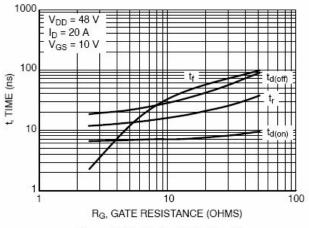


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

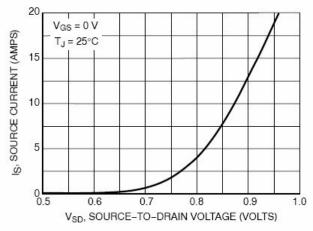


Figure 10. Diode Forward Voltage vs. Current

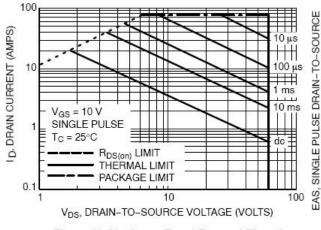


Figure 11. Maximum Rated Forward Biased Safe Operating Area

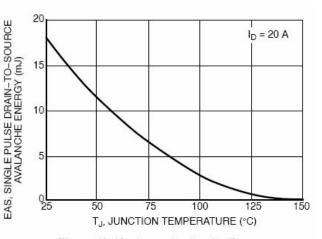


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature



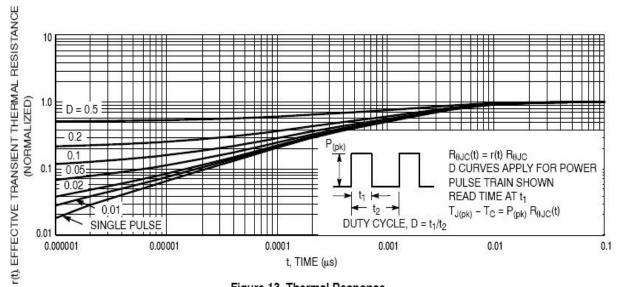


Figure 13. Thermal Response



TO251 Package Dimension

