Current Mode PWM Controller

FEATURES

- Burst Mode function
- Low startup current (4uA)
- Low operating current (1.4mA)
- Built-edge blanking
- Built-in synchronized slope compensation
- Current mode
- External Programmable PWM Switching Frequency
- By-cycle current limit protection (OCP)
- VDD over-voltage clamping protection
- Low voltage shut down function (UVLO)
- Gate Drive Output Voltage Clamp (18V)
- Frequency jitter feature
- Constant output power limit
- Overload protection (OLP)
- Work does not produce audio noise

APPLICATIONS

Offline AC/DC flyback converter for

- Power Adaptor
- Open-frame SMPS
- Battery Charger
- Set-Top Box Power Supplies

GERNERAL DESCRIPTION

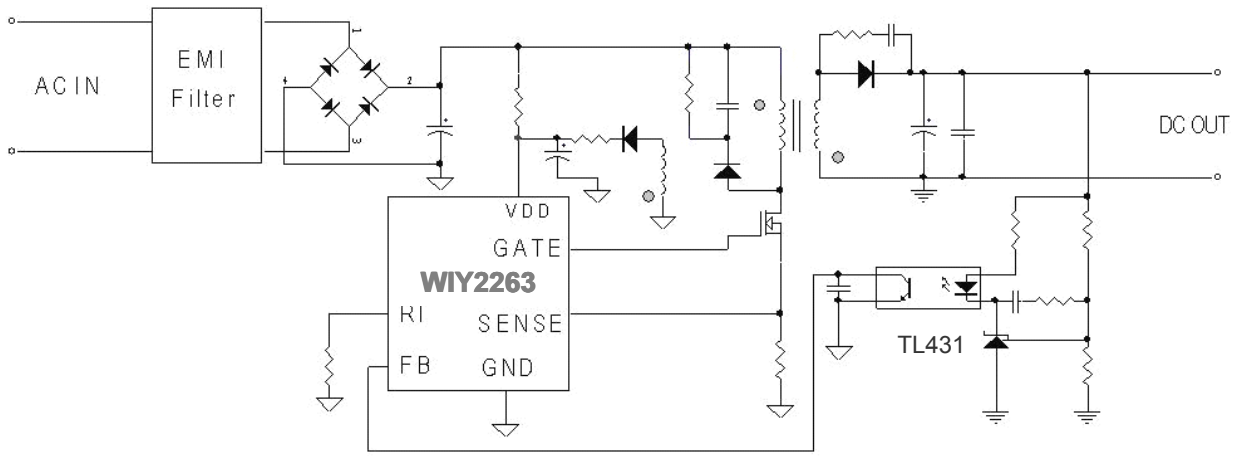
WIY2263 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 30W range.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with WIY2263. A large value resistor could thus be used in the startup circuit to minimize the standby power. The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design.

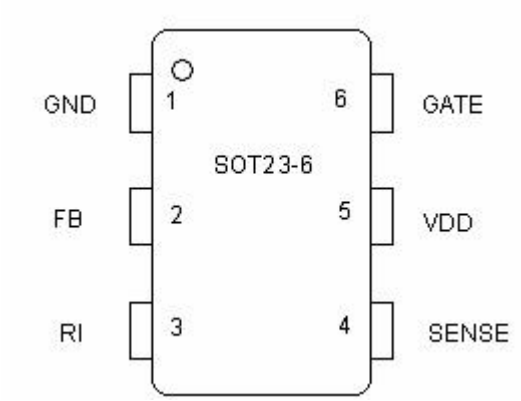
WIY2263 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET. Excellent EMI performance is achieved with Winsemi proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

TYPICAL APPLICATION

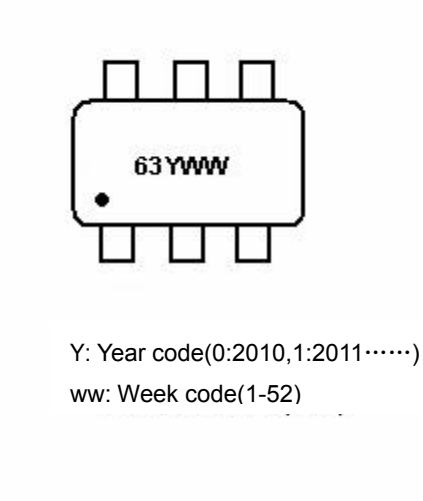


GENERAL INFORMATION

Pin Configuration



Marking Information



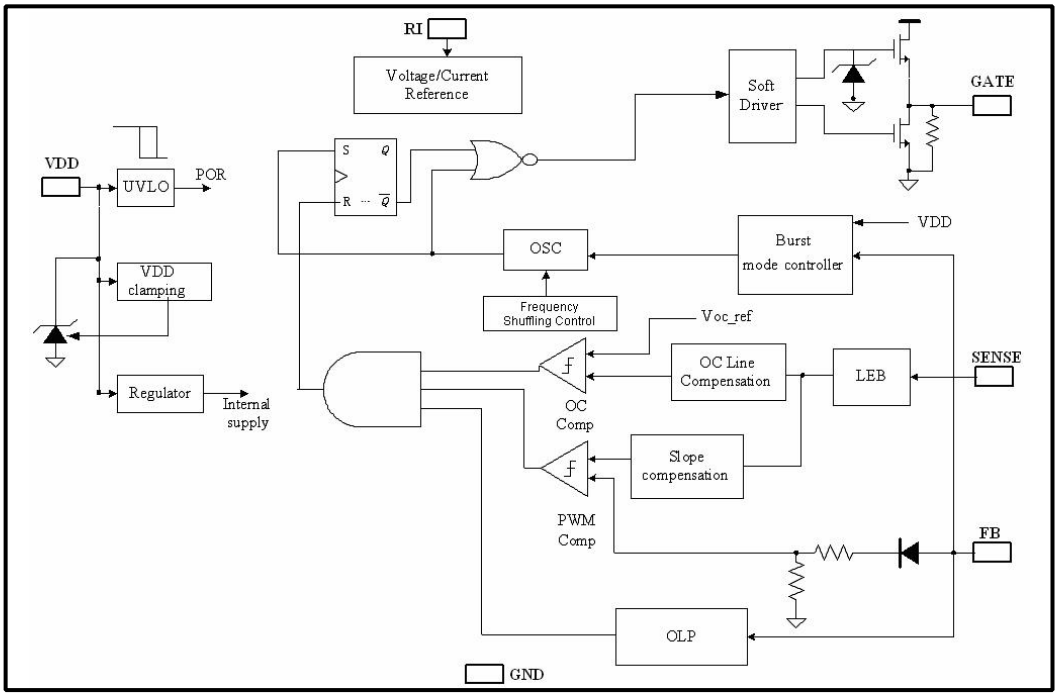
Y: Year code(0:2010,1:2011……)

ww: Week code(1-52)

TERMINAL ASSIGNMENTS

Pin Name	Pin No.	I/O	Description
GND	1	P	Ground
FB	2	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input
RI	3	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
SENSE	4	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	5	P	Chip DC power supply pin
GATE	6	O	Totem-pole gate drive output for the power MOSFET.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	10	30	V
RI	RI Resistor Value	100		KΩ
T	Operating Ambient Temperature	-20	85	℃

ABSOLUTE MAXIMUM RATINGS

Pin Name	Parameter	Ratings	Units
V_{DD}	V_{DD} Pin input voltage	30	V
V_{FB}	V_{FB} Pin input voltage	-0.3~7	V
V_{SENSE}	V_{SENSE} Pin input voltage	-0.3~7	V
V_{RI}	V_{RI} Pin input voltage	-0.3~7	V
T_J	Operating Junction Temperature	-20~150	℃
T_S	Storage Temperature	-55~160	℃
Vcv	V_{DD} DC Clamping Voltage	34	V
I_{CC}	V_{DD} DC Clamping Current	10	mA

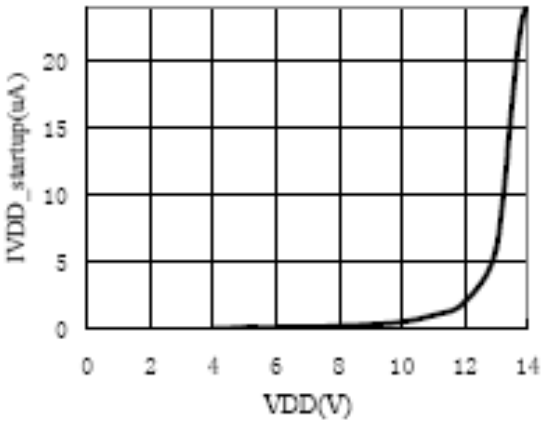
Note: more than the limit specified in the table parameters will result in permanent damage to the device. The device is not recommended in these extreme conditions of work, working conditions in the limit above which may affect device reliability.

Electrical Characteristics (Tc = 25°C)

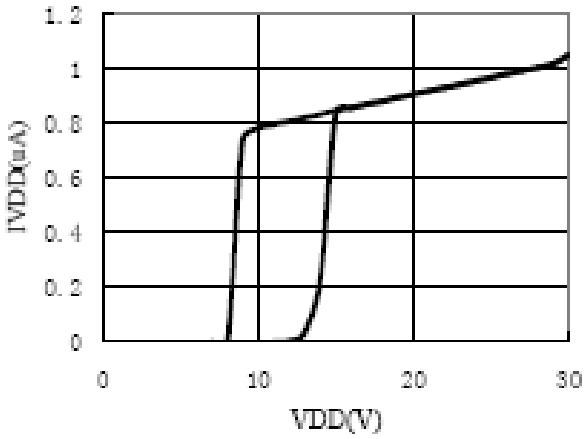
Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (V_{DD})						
Operation voltage	VDD_OP				30	V
Turn on threshold Voltage	UVLO_ON		7.8	8.8	9.8	V
Turn-off threshold Voltage	UVLO_OFF		13	14	15	V
Start up current	I_VDD_ST	V_{DD}=13V,RI=100K		4	20	μA
Operation Current	I_VDD_OP	V_{DD}=16V,RI=100K,V_{FB}=3V, GATE with 1nF to GND		1.4	2.4	mA
V_{DD} Zener Clamp Voltage	VDD_Clamp	I_{VDD}=10mA		33		V
Feedback Input Section(FB Pin)						
PWM Input Gain	A_{VCS}	ΔV_{FB} /ΔV_{cs}		2.0		V/V
VFB Open Loop Voltage	V_{FB}_Open			4.8		V
FB pin short circuit current	I_{FB}_Short	FB Shorted to GND		1.2		mA
Zero Duty Cycle FB Threshold Voltage	V_{TH}_0D	VDD = 16V,RI=100Kohm			0.75	V
Power Limiting FB Threshold Voltage	V_{TH}_PL			3.7		V
Power limiting Debounce Time	T_D_PL		-	35	-	ms
Input Impedance	Z_{FB}_IN		-	6	-	KΩ
Maximum Duty Cycle	DC_MAX		-	75	-	%
Current Sense Input(Sense Pin)						
Leading edge Blanking Time	T_{LEB}		-	330	-	8ns

Input impedance	Zsense		-	40	-	kΩ
Over Current Detection and Control Delay	T_{D_OC}	GATE with 1nF to GND		80		ns
Over Current Threshold Voltage at zero Duty Cycle	V_{TH_OC}	FB＝3V	0.70	0.75	0.80	V
Oscillator Section						
Frequency	Fosc	Oscillation @RI=100K,CS=0,FB=3V	60	65	70	KHz
Burst mode frequency	Fosc_BM	Oscillation @RI=100K,CS=0,FB=1.1V	-	22	-	KHz
Frequency variation versus temp. Deviation	Δf_temp	TEMP = -20 to 85℃	-	5	-	%
Frequency variation versus VDD	Δf_VDD	VDD = 12 to 25V	-	5	-	%
Operating RI Range	RI_range		50	100	150	KΩ
open Load Voltage	V_RI_Open		-	2	-	V
Gate Output Section						
Output voltage Low level	VOL	VDD = 16V, Io = -20mA	-	-	0.8	V
Output voltage high level	VOH	VDD = 16V, Io = 20mA	10	-	-	V
Output clamp voltage	VClamp		-	18	-	V
Rising time	tr	VDD = 16V, GATE with 1nF to GND	-	200	-	s
Falling time	tf	VDD = 16V, GATE with 1nF to GND	-	70	-	s
Frequency Shuffling						
Frequency Modulation range /Base frequency	Δf_OSC	RI=100K	-3	-	3	%
Shuffling Frequency	f_shuffling	RI=100K		64		Hz

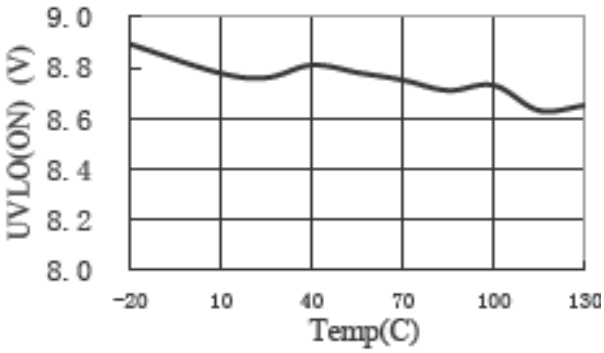
IVDD_startup vs VDD



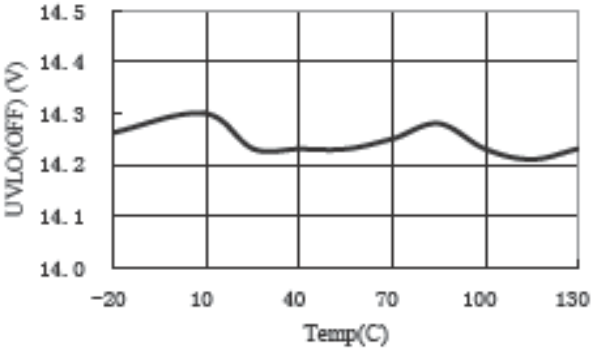
IVDD vs VDD



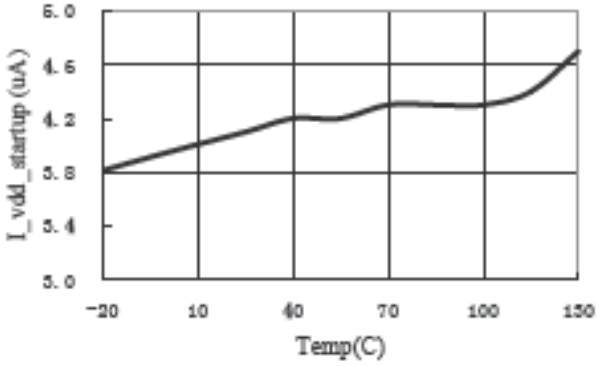
UVLO(ON) vs Temp



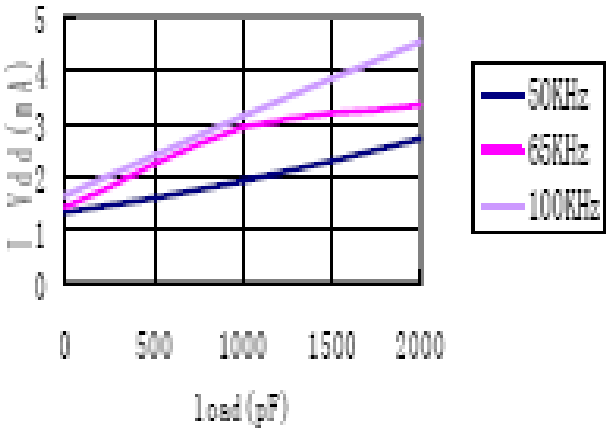
UVLO(OFF) vs Temp

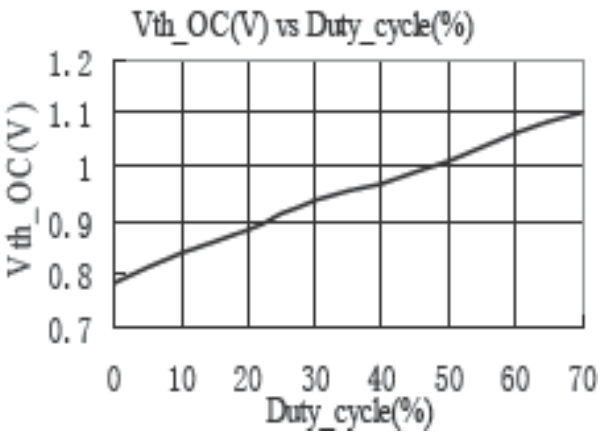


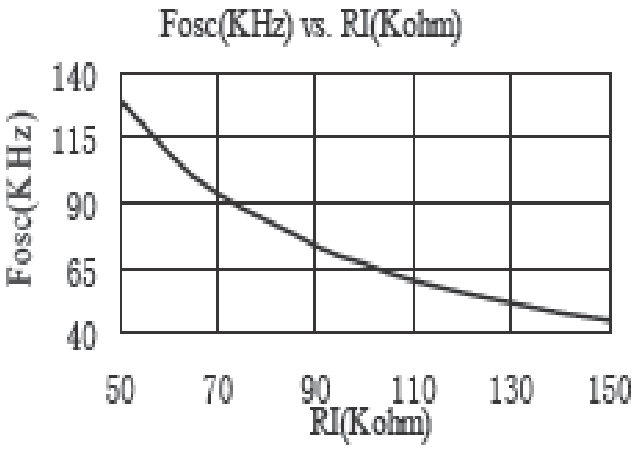
I_VDD_startup vs. Temp

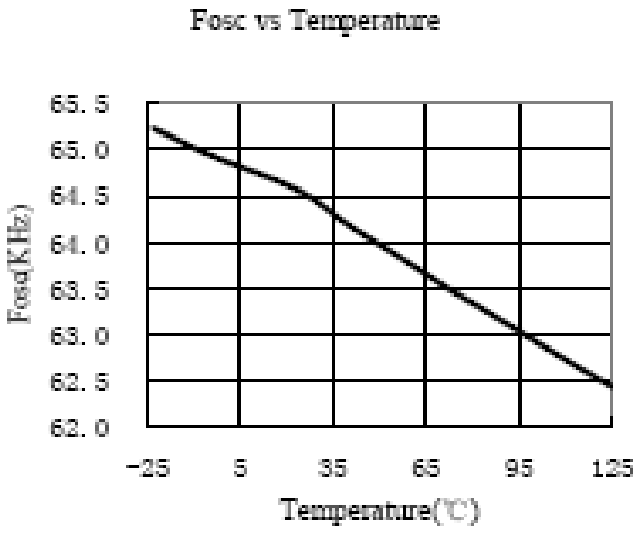


I_Vdd vs Gate load




Vth_OC(V) vs Duty_cycle(%)
Vth_OC(V)
1.2
1.1
1
0.9
0.8
0.7
0
10
20
30
40
50
60
70
Duty_cycle(%)


Fosc(KHz) vs. RI(Kohm)
Fosc(KHz)
140
115
90
65
40
50
70
90
110
130
150
RI(Kohm)


Fosc vs Temperature
Fosc(KHz)
65.5
65.0
64.5
64.0
63.5
63.0
62.5
62.0
-25
5
35
65
95
125
Temperature(℃)

OPERATION DESCRIPTION

The WIY2263 is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 30W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of WIY2263 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The Operating current of WIY2263 is low at 1.4mA. Good efficiency is achieved with WIY2263 low operating current together with extended burst mode control features.

Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in WIY2263. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Extended Burst Mode Operation

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. WIY2263 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = \frac{6500}{RI(K\Omega)}(KHz)$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in WIY2263 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

WIY2263 Gate is connected to an external MOSFET gate

for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

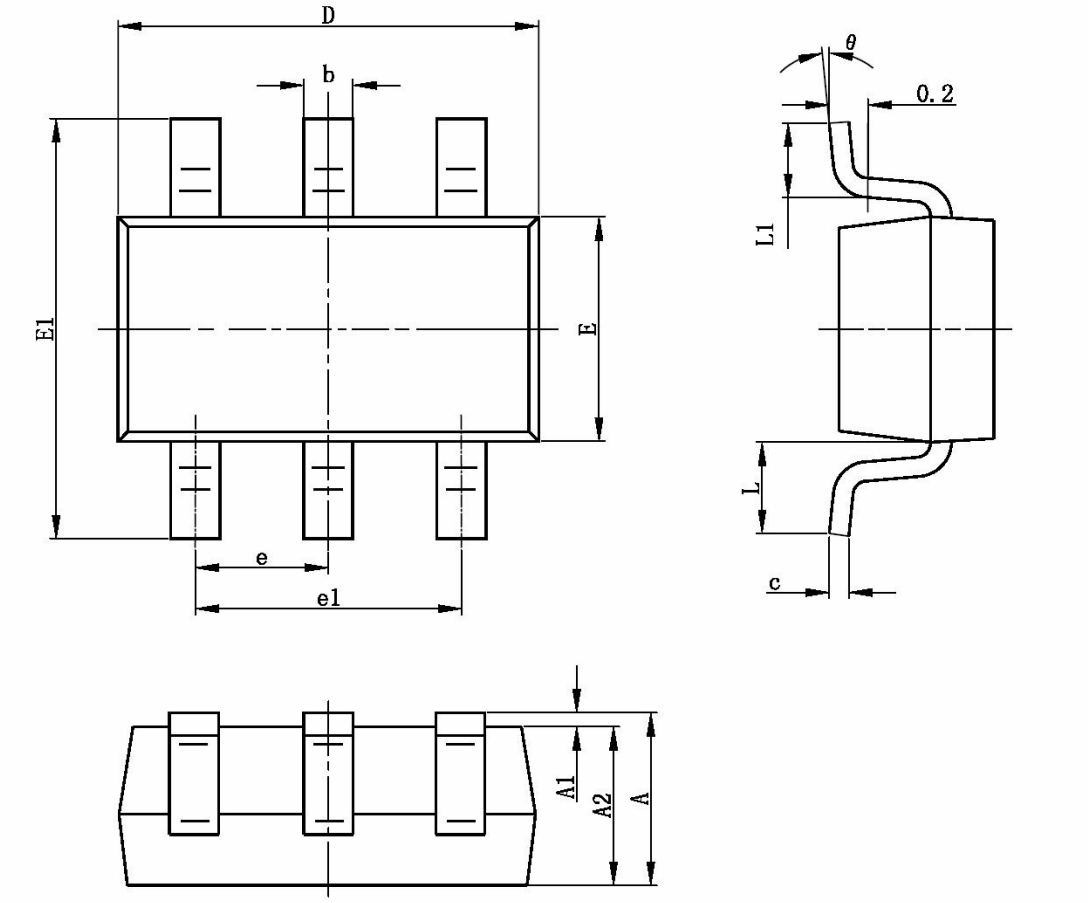
Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, UnderVoltage Lockout on VDD (UVLO)

With Winsemi Proprietary technology, the OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

SOT23-6 Package Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°