intel®

Intel® LXT972A Single-Port 10/100 Mbps PHY Transceiver

Datasheet

The Intel® LXT972A Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT972A Transceiver) directly supports both 100BASE-TX and 10BASE-T applications. The LXT972A Transceiver is IEEE compliant and provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT972A Transceiver supports full-duplex operation at 10 Mbps and 100 Mbps. Operating conditions for the LXT972A Transceiver can be set using auto-negotiation, parallel detection, or manual control. The LXT972A Transceiver is fabricated with an advanced CMOS process and requires only a single 2.53.3 V power supply with 2.5 V MII interface support.

Applications

- Combination 10BASE-T/100BASE-TX Network Interface Cards (NICs)
- Network printers
- 10/100 Personal Computer Memory Card International Association (PCMCIA) cards
- Cable Modems and Set-Top Boxes

Product Features

- 3.3 V Operation
- Low power consumption (300 mW typical)
- 10BASE-T and 100BASE-TX using a single RJ-45 connection
- IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters
- Auto-negotiation and parallel detection
- MII interface with extended register capability
- Robust baseline wander correction
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) or full-duplex operation
- JTAG boundary scan
- MDIO serial port or hardware pin configurable
- Integrated, programmable LED drivers
- 64-Pin Low-profile Quad Flat Package (LQFP)
  - LXT972ALC - Commercial (0° to 70 °C ambient)

Datasheet

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Revision History

| Intel® LXT972A Transceiver Revision 004 Revision Date: 25-Oct-2005 ||
Page	Description
1	Front page text changed.
11	Added Table 1 "Related Documents from Intel"
95	Added Section 10.1, "Top Label Markings".
96	Modified Table 57 "Product Ordering Information" and Table 39 "Order Matrix for Intel® LXT972A Transceiver" under Section 11.0, "Product Ordering Information".

| Intel® LXT972A Transceiver Revision 003 Revision Date: August 6, 2002 ||
Page	Description
1	Added "JTAG Boundary Scan" to Product Features on front page.
10	Modified Figure 1 "LXT972A 64-Pin LQFP Assignments" (replaced TEST1 and TEST0 with GND).
11	Modified Table 1 "LQFP Numeric Pin List" (replaced TEST1 and TEST0 with GND).
13	Added note under Section 2.0, "Signal Descriptions": "Intel recommends that all inputs and multi-function pins be tied to the inactive states and all outputs be left floating, if unused."
14	Modified Table 4 "LXT972A Miscellaneous Signal Descriptions".
15	Modified Table 5 "LXT972A Power Supply Signal Descriptions".
16	Added Table 8 "LXT972A Pin Types and Modes".
19	Added Section 3.2.2.1, "Increased MII Drive Strength".
24	Modified Figure 7 "Hardware Configuration Settings".
41	Modified Table 13 "Supported JTAG Instructions".
41	Modified Table 14 "Device ID Register".
45	Modified Table 17 "Absolute Maximum Ratings".
45	Modified Table 18 "Operating Conditions": Added Typ values to Vcc current.
46	Modified Table 20 "Digital I/O Characteristics - MII Pins".
47	Modified Table 22 "I/O Characteristics - LED/CFG Pins".
48	Added Table 26 "LXT972A Thermal Characteristics".
51	Modified Table 29 "10BASE-T Receive Timing Parameters".
58	Modified Table 38 "Register Bit Map" (added Address 26 information).
71	Added Table 53 "Digital Config Register (Address 26)".
72	Modified Table 54 "Transmit Control Register #2 (Address 30)".
74	Added Section 8.0, "Product Ordering Information".

| Intel® LXT972A Transceiver Revision 002
Revision Date: January 2001 ||
Page	Description
N/A	Clock Requirements: Modified language under Clock Requirements heading.
N/A	I/O Characteristics REFCLK (table): Changed values for Input Clock Duty Cycle under Min from 40 to 35 and under Max from 60 to 65.

Datasheet

1.0   Introduction to This Document

This document includes information on the Intel® LXT972A Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT972A Transceiver).

1.1   Document Overview

This document includes the following subjects:

- Chapter 2.0, "Block Diagram for Intel® LXT972A Transceiver"
- Chapter 3.0, "Pin Assignments for Intel® LXT972A Transceiver"
- Chapter 4.0, "Signal Descriptions for Intel® LXT972A Transceiver"
- Chapter 5.0, "Functional Description"
- Chapter 6.0, "Application Information"
- Chapter 7.0, "Electrical Specifications"
- Chapter 8.0, "Register Definitions - IEEE Base Registers"
- Chapter 9.0, "Register Definitions - Product-Specific Registers"
- Chapter 10.0, "Intel® LXT972A Transceiver Package Specifications"
- Chapter 11.0, "Product Ordering Information"

1.2   Related Documents

Table 1.   Related Documents from Intel

Document Title	Document Number
Intel® LXT971A , LXT972A , LXT972M Single-Port 10/100 Mbps PHY Transceivers Specification Update	249354
Intel® LXT971A, LXT972A, and LXT972M 3.3V PHY Transceivers Design and Layout Guide - Application Note	249016
Magnetic Manufacturers for Networking Product Applications - Application Note	248991

2.0   Block Diagram for Intel® LXT972A Transceiver

Figure 1 is a block diagram of the LXT972A Transceiver.

The LXT972A Transceiver has on-board blocks from Optimal Signal Processing™ (OSP™).

Figure 1. Intel® LXT972A Transceiver Block Diagram
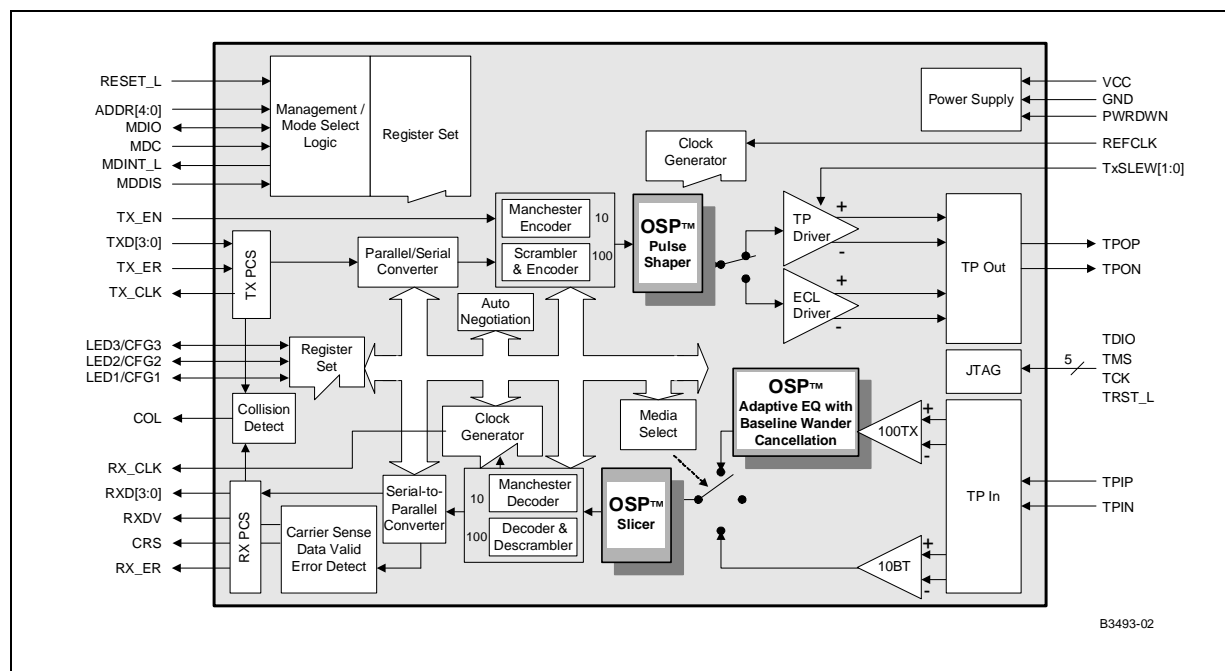
3.0   Pin Assignments for Intel® LXT972A Transceiver

Figure 2 shows the pin assignments for the LXT972A Transceiver LQFP package.

Figure 2. Pins for Intel® LXT972A Transceiver 64-Pin LQFP Package

B3388-03
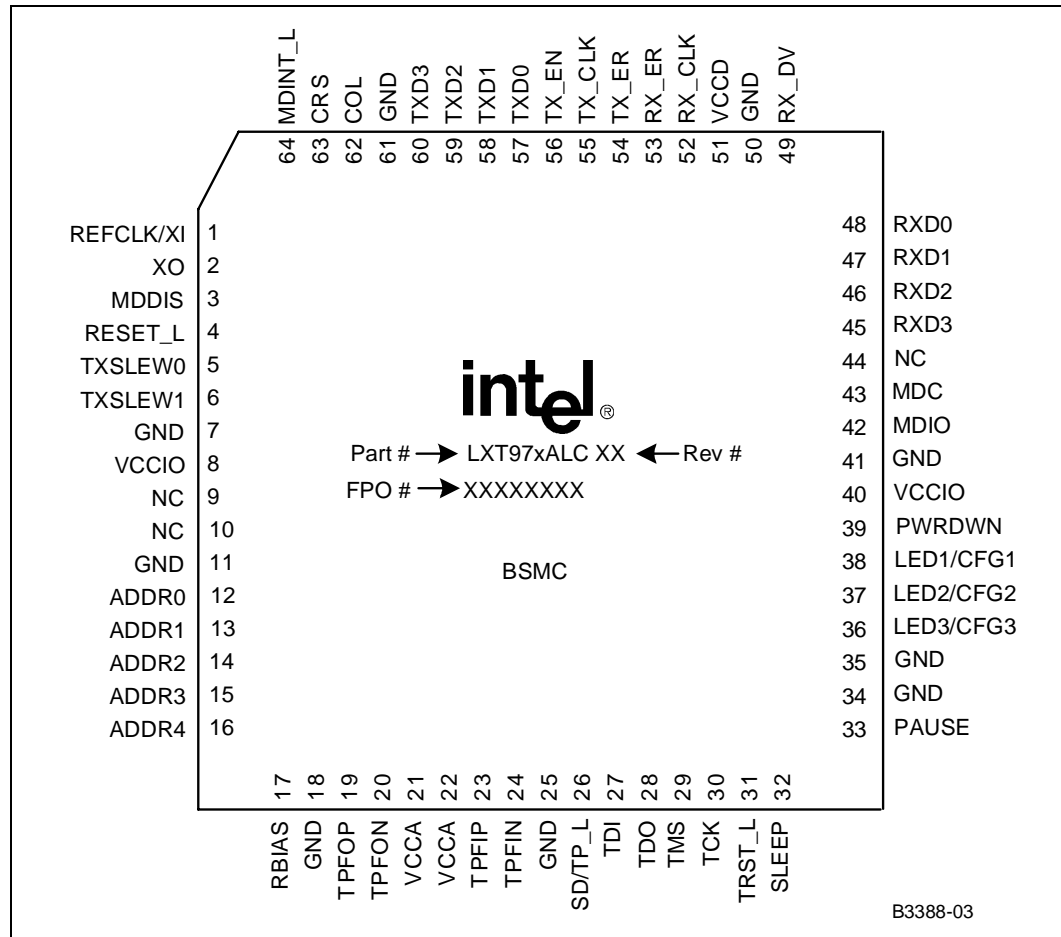
Table 2 lists LXT972A Transceiver LQFP pin numbers, symbols, and pin types.

Table 2. Intel® LXT972A Transceiver LQFP Numeric Pin List (Sheet 1 of 2)

Pin	Symbol	Type
1	REFCLK/XI	I
2	XO	O
3	MDDIS	I
4	RESET_L	I
5	TxSLEW0	I
6	TxSLEW1	I
7	GND	–
8	VCCIO	–
9	NC	–
10	NC	–
11	GND	–
12	ADDR0	I
13	GND	–
14	GND	–
15	GND	–
16	GND	–
17	RBIAS	AI
18	GND	–
19	TPOP	O
20	TPON	O
21	VCCA	–
22	VCCA	–
23	TPIP	I
24	TPIN	I
25	GND	–
26	GND	–
27	TDI	I
28	TDO	Output
29	TMS	I
30	TCK	I
31	TRST_L	I
32	GND	–
33	PAUSE	I
34	GND	–
34.	TEST0	I
35	GND	–

Table 2.   Intel® LXT972A Transceiver LQFP Numeric Pin List (Sheet 2 of 2)

Pin	Symbol	Type
35.	TEST1	Input
36	LED/CFG3	I/O
37	LED/CFG2	I/O
38	LED/CFG1	I/O
39	PWRDWN	I
40	VCCIO	–
41	GND	–
42	MDIO	I/O
43	MDC	I
44	NC	–
45	RXD3	O
46	RXD2	O
47	RXD1	O
48	RXD0	O
49	RX_DV	O
50	GND	–
51	VCCD	–
52	RX_CLK	O
53	RX_ER	O
54	TX_ER	I
55	TX_CLK	O
56	TX_EN	I
57	TXD0	I
58	TXD1	I
59	TXD2	I
60	TXD3	I
61	GND	–
62	COL	O
63	CRS	O
64	MDINT_L	OD

4.0 Signal Descriptions for Intel® LXT972A Transceiver

Intel recommends the following configurations for unused pins:

- **Unused inputs.** Configure all unused inputs and unused multi-function pins for inactive states.
- **Unused outputs.** Leave all unused outputs floating.
- **No connects.** Do not use pins designated as NC (no connect), and do not terminate them.

Note: For the tables in this section, the abbreviations listed in Table 3 are used for the "Type" column.

Table 3. Intel® LXT972A Transceiver Signal Types

Abbreviation	Meaning
A	Analog
AI	Analog Input
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Tables in this section include the following

- Table 4, "Intel® LXT972A Transceiver MII Data Interface Signal Descriptions"
- Table 5, "Intel® LXT972A Transceiver MII Controller Interface Signal Descriptions"
- Table 6, "Intel® LXT972A Transceiver Network Interface Signal Descriptions"
- Table 7, "Intel® LXT972A Transceiver Standard Bus and Interface Signal Descriptions"
- Table 8, "Intel® LXT972A Transceiver Configuration and LED Driver Signal Descriptions"
- Table 9, "Intel® LXT972A Transceiver Power, Ground, No-Connect Signal Descriptions"
- Table 10, "Intel® LXT972A Transceiver JTAG Test Signal Descriptions"
- Table 11, "Intel® LXT972A Transceiver Pin Types and Modes"

Table 4 lists signal descriptions of the LXT972A Transceiver MII data interface pins.

Table 4. Intel® LXT972A Transceiver MII Data Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
60 59 58 57	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data.** TXD is a group of parallel data signals that are driven by the MAC. TXD[3:0] transition synchronously with respect to TX_CLK. TXD[0] is the least-significant bit.
56	TX_EN	I	**Transmit Enable.** The MAC asserts this signal when it drives valid data on TXD. This signal must be synchronized to TX_CLK.
55	TX_CLK	O	**Transmit Clock.** TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
45 46 47 48	RXD3 RXD2 RXD1 RXD0	O	**Receive Data.** RXD is a group of parallel signals that transition synchronously with respect to RX_CLK. RXD[0] is the least-significant bit.
49	RX_DV	O	**Receive Data Valid.** The LXT972A Transceiver asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
53	RX_ER	O	**Receive Error.** Signals a receive error condition has occurred. This output is synchronous to RX_CLK.
54	TX_ER	I	**Transmit Error.** Signals a transmit error condition. This signal must be synchronized to TX_CLK.
52	RX_CLK	O	**Receive Clock.** 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation. For details, see "Clock Requirements" on page 30 in Chapter 5.0, "Functional Description".
62	COL	O	**Collision Detected**. The LXT972A Transceiver asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full- duplex operation.
63	CRS	O	**Carrier Sense**. During half-duplex operation (Register bit 0.8 = 0), the LXT972A Transceiver asserts this output when either transmitting or receiving data packets. During full-duplex operation (Register bit 0.8 = 1), CRS is asserted only during receive. CRS assertion is asynchronous with respect to RX_CLK. CRS is de-asserted on loss of carrier, synchronous to RX_CLK.

Table 5 lists signal descriptions of the LXT972A Transceiver MII controller interface pins.

Table 5.   Intel® LXT972A Transceiver MII Controller Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
3	MDDIS	I	**Management Data Disable**. When MDDIS is High, the MDIO is disabled from read and write operations. When MDDIS is Low at power-up or reset, the Hardware Control Interface pins control only the initial or "default" values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
43	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
42	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
64	MDINT_L	OD	**Management Data Interrupt**. When Register bit 18.1 = 1, a Low output on this active-low pin indicates a status change. Interrupt is cleared by reading Register 19.

Table 6 lists signal descriptions of the LXT972A Transceiver network interface pins.

Table 6. Intel® LXT972A Transceiver Network Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
19 20	TPOP TPON	O	**Twisted-Pair Outputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPOP/N pins drive IEEE 802.3 compliant pulses onto the line.
23 24	TPIP TPIN	I	**Twisted-Pair Inputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPIP/N pins receive differential 100BASE-TX or 10BASE-T signals from the line.

Table 7 lists signal descriptions of the LXT972A Transceiver standard bus and interface signals.

Table 7. Intel® LXT972A Transceiver Standard Bus and Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
12	ADDR0	I	**Address 0.** Sets device address.

Table 8 lists signal descriptions of the LXT972A Transceiver configuration and LED driver pins.

Note: Pull-up/pull-down resistors of 10k Ohms can be implemented if LEDs are not used in the design.

Table 8. Intel® LXT972A Transceiver Configuration and LED Driver Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
5 6	TxSLEW0 TxSLEW1	I	**Tx Output Slew Controls 0 and 1**. These pins select the TX output slew rate (rise and fall time) as follows: TxSLEW1 / TxSLEW0 / Slew Rate (Rise and Fall Time) 0 / 0 / 3.0 ns 0 / 1 / 3.4 ns 1 / 0 / 3.9 ns 1 / 1 / 4.4 ns
4	RESET_L	I	**Reset**. This active Low input is ORed with the control register Reset bit (Register bit 0.15). The transceiver reset cycle is extended to 258 µs (nominal) after reset is de-asserted.
17	RBIAS	AI	**Reference Current Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor.
33	PAUSE	I	**Pause**. When set High, the transceiver advertises Pause capabilities during auto-negotiation.
39	PWRDWN	I	**Power Down**. When set High, this pin puts the transceiver in a power-down mode.
1 2	REFCLK/XI XO	I and O	**Reference Clock Input / Crystal Input and Crystal Output**. A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI. Refer to Section 5.3.2, "Clock Requirements" on page 30 in the Functional Description section.
38 37 36	LED/CFG1 LED/CFG2 LED/CFG3	I/O	**LED Drivers 1-3.** These pins drive LED indicators. Each LED can display one of several available status conditions as selected by the LED Configuration Register. (For details, see Table 55, "LED Configuration Register - Address 20, Hex 14" on page 91.) **Configuration Inputs 1-3.** These pins also provide initial configuration settings. (For details, see Table 12, "Hardware Configuration Settings for Intel® LXT972A Transceiver" on page 35.)

Table 9 lists signal descriptions of the LXT972A Transceiver power, ground, and no-connect pins.

Table 9. Intel® LXT972A Transceiver Power, Ground, No-Connect Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
51	VCCD	–	**Digital Power.** Requires a 3.3 V power supply.
7, 11, 13, 14, 15, 16, 18, 25, 26, 32, 34, 35, 41, 50, 61	GND	–	**Ground.**
8, 40	VCCIO	–	**MII Power.** Requires either a 3.3 V or a 2.5 V supply. Must be supplied from the same source used to power the MAC on the other side of the MII. For the LXT972A Transceiver, VCCIO is 3.3 V.
21, 22	VCCA	–	**Analog Power.** Requires a 3.3 V power supply.
9, 10, 44	NC	-	**No Connection**. These pins are not used and should not be terminated.

Table 10 lists signal descriptions of the LXT972A Transceiver Joint Test Action Group (JTAG) pins.

Note: If a JTAG port is not used, these pins do not need to be terminated.

Table 10. Intel® LXT972A Transceiver JTAG Test Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
27	TDI	I	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
28	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
29	TMS	I	**Test Mode Select**.
30	TCK	I	**Test Clock**. Clock input for boundary scan.
31	TRST_L	I	**Test Reset**. This active-low test reset input is sourced by ATE.

Table 11 lists pin types and modes of the LXT972A Transceiver.

Note:

- DH = Driven High (Logic 1)
- DL = Driven Low (Logic 0)
- HZ = High Impedance
- ID = Internal Pull-Down (Weak)

Table 11. Intel® LXT972A Transceiver Pin Types and Modes

Modes	RXD3:0	RX_DV	Tx/Rx CLKS Output	RX_ER Output	COL Output	CRS Output	TXD3:0 Input	TX_EN Input	TX_ER Input
HWReset	DL	DL	DH	DL	DL	DL	ID	ID	ID
SFTPWRDN	DL	DL	Active	DL	DL	DL	ID	ID	ID
HWPWRDN	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z	High Z
ISOLATE	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	ID	ID	ID

5.0   Functional Description

This chapter has the following sections:

- Section 5.1, "Device Overview"
- Section 5.2, "Network Media / Protocol Support"
- Section 5.3, "Operating Requirements"
- Section 5.4, "Initialization"
- Section 5.5, "Establishing Link"
- Section 5.6, "MII Operation"
- Section 5.7, "100 Mbps Operation"
- Section 5.8, "10 Mbps Operation"
- Section 5.9, "Monitoring Operations"
- Section 5.10, "Boundary Scan (JTAG 1149.1) Functions"

5.1   Device Overview

The LXT972A Transceiver is a single-port Fast Ethernet 10/100 transceiver that supports 10 Mbps and 100 Mbps networks. It complies with applicable requirements of IEEE 802.3. It directly drives either a 100BASE-TX line or a 10BASE-T line.

5.1.1   Comprehensive Functionality

The LXT972A Transceiver provides a standard Media Independent Interface (MII) for 10/100 MACs. The LXT972A Transceiver performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X standard. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

The LXT972A Transceiver reads its configuration pins on power-up to check for forced operation settings.

If the LXT972A Transceiver is not set for forced operation, it uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT972A Transceiver auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT972A Transceiver automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and sets its operating conditions accordingly.

The LXT972A Transceiver provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

5.1.2   Optimal Signal Processing Architecture

The LXT972A Transceiver incorporates high-efficiency Optimal Signal Processing (OSP) design techniques, which combine optimal properties of digital and analog signal processing.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT972A Transceiver provides improved data recovery, EMI performance, and low power consumption.

5.2 Network Media / Protocol Support

This section includes the following:

- Section 5.2.1, "10/100 Network Interface"
- Section 5.2.2, "MII Data Interface"
- Section 5.2.3, "Configuration Management Interface"

The LXT972A Transceiver supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair.

5.2.1 10/100 Network Interface

The network interface port consists of two differential signal pairs. For specific pin assignments, see Chapter 4.0, "Signal Descriptions for Intel® LXT972A Transceiver".

The LXT972A Transceiver output drivers can generate one of the following outputs:

- 100BASE-TX
- 10BASE-T

When not transmitting data, the LXT972A Transceiver generates IEEE 802.3-compliant link pulses or idle code. Depending on the mode selected, input signals are decoded as one of the following:

- 100BASE-TX
- 10BASE-T

Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

5.2.1.1   Twisted-Pair Interface

The LXT972A Transceiver supports either 100BASE-TX or 10BASE-T connections over 100 Ω, Category 5, Unshielded Twisted Pair (UTP) cable. When operating at 100 Mbps, the LXT972A Transceiver continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT972A Transceiver generates "IDLE" symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.

Only a transformer, RJ-45 connector, load resistor, and bypass capacitors are required to complete this interface. On the transmit side, the LXT972A Transceiver has an active internal termination and does not require external termination resistors. Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings allow the designer to match the output waveform to the magnetic characteristics. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit. (For the slew rate settings, see Table 56, "Transmit Control Register - Address 30, Hex 1E" on page 93.)

5.2.1.2   Remote Fault Detection and Reporting

The LXT972A Transceiver supports the remote fault detection and reporting mechanisms. "Remote Fault" refers to a MAC-to-MAC communication function that is transparent to PHY layer devices. It is used only during auto-negotiation, and is applicable only to twisted-pair links.

Remote Fault Detection. Register bit 4.13 in the Auto-Negotiation Advertisement Register is reserved for Remote Fault indications. It is typically used when re-starting the auto-negotiation sequence to indicate to the link partner that the link is down because the advertising device detected a local fault.

When the LXT972A Transceiver receives a Remote Fault indication from its partner during auto-negotiation, the following occurs:

- Register bit 5.13 in the Link Partner Base Page Ability Register is set.
- Remote Fault Register bit 1.4 in the MII Status Register is set to pass this information to the local controller.

5.2.2 MII Data Interface

The LXT972A Transceiver supports a standard Media Independent Interface (MII). The MII consists of a data interface and a management interface. The MII Data Interface passes data between the LXT972A Transceiver and a Media Access Controller (MAC). Separate parallel buses are provided for transmit and receive. This interface operates at either 10 Mbps or 100 Mbps. The speed is set automatically, once the operating conditions of the network link have been determined. For details, see Section 5.6, "MII Operation" on page 38.

Increased MII Drive Strength. A higher Media Independent Interface (MII) drive strength may be desired in some designs to drive signals over longer PCB trace lengths, or over high-capacitive loads, through multiple vias, or through a connector. The MII drive strength in the LXT972A Transceiver can be increased by setting Register bit 26.11 through software control. Setting Register bit 26.11 = 1 through the MDC/MDIO interface sets the MII pins (RXD[3:0], RX_DV, RX_CLK, RX_ER, COL, CRS, and TX_CLK) to a higher drive strength.

5.2.3 Configuration Management Interface

The LXT972A Transceiver provides both an MDIO interface and a reduced hardware control interface for device configuration and management.

5.2.3.1 MDIO Management Interface

MDIO management interface topics include the following:

- Section 5.2.3.1.1, "MDIO Addressing for Intel® LXT972A Transceiver"
- Section 5.2.3.1.2, "MDIO Frame Structure"

The LXT972A Transceiver supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT972A Transceiver. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers.

Some registers are required and their functions are defined by the IEEE 802.3 standard. The LXT972A Transceiver also supports additional registers for expanded functionality. The LXT972A Transceiver supports multiple internal registers, each of which is 16 bits wide. Specific register bits are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used.

5.2.3.1.1 MDIO Addressing for Intel® LXT972A Transceiver

The MDIO addressing protocol allows a controller to communicate with multiple LXT972A Transceivers. Pin ADDR0 determines the PHY device address that is selected as follows.

- Connect pin ADDR0 low to get PHY address 0.
- Connect pin ADDR0 high to get PHY address 1.

5.2.3.1.2   MDIO Frame Structure

The physical interface consists of a data line (MDIO) and clock line (MDC). The frame structure is shown in Figure 3 and Figure 4 (Read and Write).

MDIO Interface timing is given in Chapter 7.0, "Electrical Specifications".

Figure 3. Management Interface Read Frame Structure
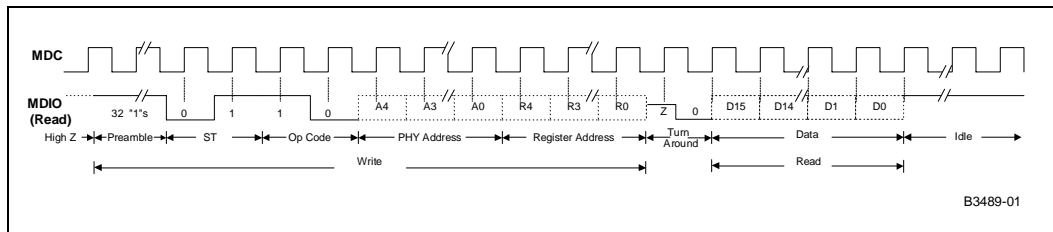
Figure 4. Management Interface Write Frame Structure
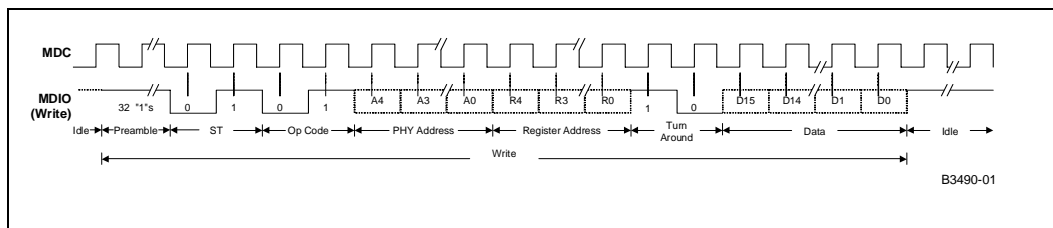
5.2.3.1.3   MII Interrupts

Figure 5 shows the MII interrupt logic. The LXT972A Transceiver provides a hardware interrupt pin (MDINT_L) and two dedicated interrupt registers, Register 18 and Register 19.

- Register 18 provides interrupt enable and mask functions. Setting Register bit 18.1 = 1 enables the device to request interrupt via the MDINT_L pin. An active Low on this pin indicates a status change on the LXT972A Transceiver. Interrupts may be caused by any of the following four conditions:

  — Auto-negotiation complete

  — Speed status change

  — Duplex status change

  — Link status change

- Register 19 provides the interrupt status.

Figure 5. Intel® LXT972A Transceiver MII Interrupt Logic
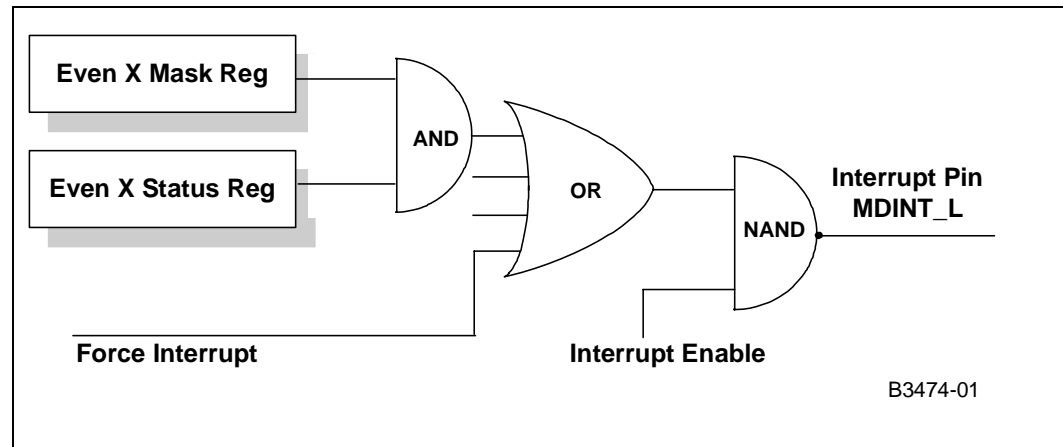
5.2.3.2   Hardware Control Interface

The LXT972A Transceiver provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the hardware configuration pins to set device configuration. For details, see Section 5.4.4, "Hardware Configuration Settings" on page 35.

5.3   Operating Requirements

5.3.1   Power Requirements

The LXT972A Transceiver requires three power supply inputs:

- VCCA
- VCCD
- VCCIO

The digital and analog circuits require 3.3 V supplies (VCCA and VCCD). These inputs may be supplied from a single source. Each supply input must be de-coupled to ground.

An additional supply may be used for the MII (VCCIO).   The supply may be either +2.5 V or +3.3 V. Also, the inputs on the MII interface are tolerant to 5 V signals from the controller on the other side of the MII interface. For MII I/O characteristics, see Table 23, "Digital I/O Characteristics1 - MII Pins" on page 64.

Note: Bring up power supplies as close to the same time as possible.

Note: As a matter of good practice, keep power supplies as clean as possible.

5.3.2   Clock Requirements

5.3.2.1   External Crystal/Oscillator

The LXT972A Transceiver requires a reference clock input that is used to generate transmit signals and recover receive signals. It may be provided by either of two methods: by connecting a crystal across the oscillator pins (XI and XO) with load capacitors, or by connecting an external clock source to pin XI.

The connection of a clock source to the XI pin requires the XO pin to be left open. To minimize transmit jitter, Intel recommends a crystal-based clock instead of a derived clock (that is, a PLL-based clock).

A crystal is typically used in NIC applications. An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. For clock timing requirements, see Table 24, "I/O Characteristics - REFCLK/XI and XO Pins" on page 65.

5.3.2.2   MDIO Clock

The MII management channel (MDIO) also requires an external clock. The managed data clock (MDC) speed is a maximum of 8 MHz. For details, see Table 37, "Intel® LXT972A Transceiver MDIO Timing" on page 75.

5.4　Initialization

This section includes the following topics:

- Section 5.4.1, "MDIO Control Mode and Hardware Control Mode"

- Section 5.4.2, "Reduced-Power Modes"

- Section 5.4.3, "Reset for Intel® LXT972A Transceiver"

- Section 5.4.4, "Hardware Configuration Settings"

When the LXT972A Transceiver is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link.

Figure 6 shows the initialization sequence for the LXT972A Transceiver. The configuration bits may be set by the Hardware Control or MDIO interface.

Figure 6. Initialization Sequence for Intel® LXT972A Transceiver
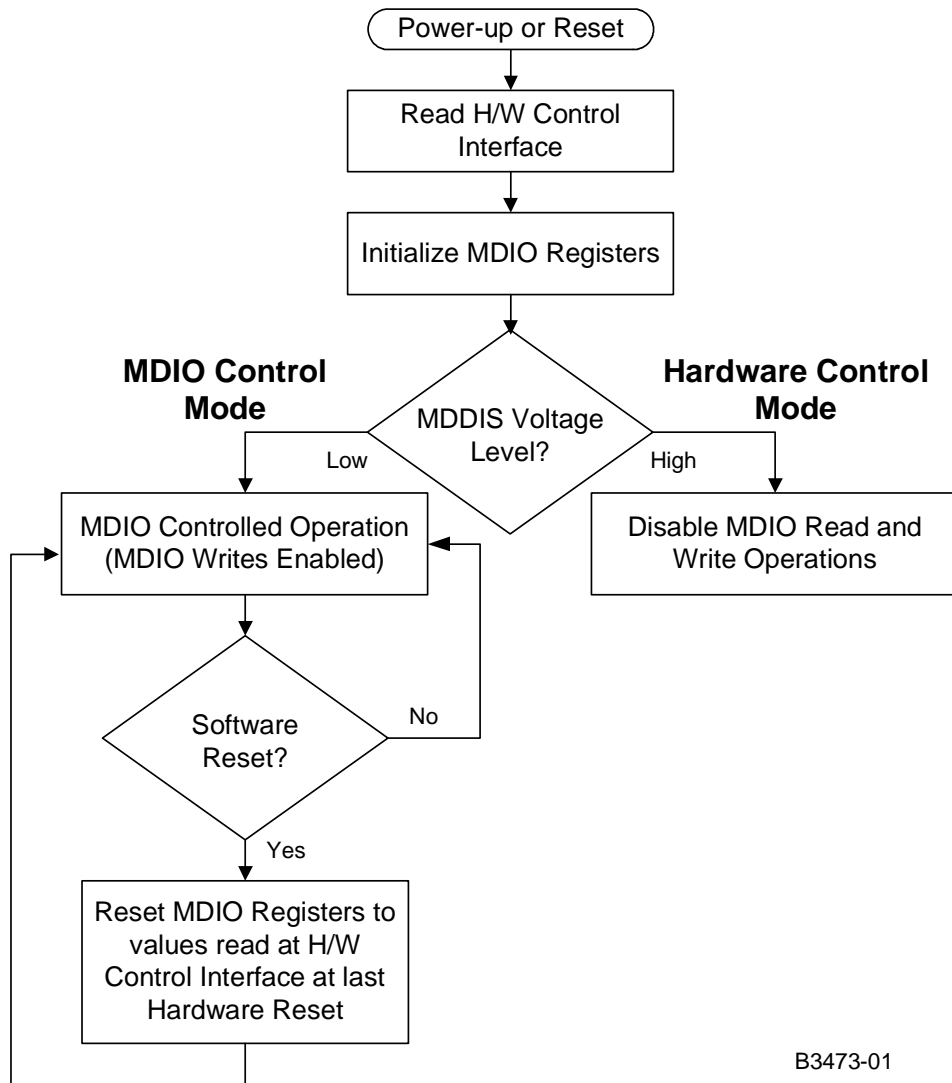
B3473-01

5.4.1 MDIO Control Mode and Hardware Control Mode

In the MDIO Control mode, the LXT972A Transceiver reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

The following modes are available using either Hardware Control or MDIO control:

- Force network link operation to:
  — 100BASE-TX, Full-Duplex
  — 100BASE-TX, Half-Duplex
  — 10BASE-T, Full-Duplex
  — 10BASE-T, Half-Duplex
- Allow auto-negotiation/parallel-detection

In the Hardware Control Mode, the LXT972A Transceiver disables direct-write operations to the MDIO registers through the MDIO Interface. On power-up or hardware reset, the LXT972A Transceiver reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

When the network link is forced to a specific configuration, the LXT972A Transceiver immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT972A Transceiver begins the auto-negotiation/parallel-detection operation.

5.4.2 Reduced-Power Modes

This section discusses the LXT972A Transceiver reduced-power modes.

5.4.2.1 Hardware Power Down

The hardware power-down mode is controlled by the PWRDWN pin. When PWRDWN is High, the following conditions are true:

- The LXT972A Transceiver network port and clock are shut down.
- All outputs are tristated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.

5.4.2.2 Software Power Down

Software power-down control is provided by Register bit 0.11 in the Control Register. (See Table 41 on page 79.) During soft power-down, the following conditions are true:

- The network port is shut down.
- The MDIO registers remain accessible.

5.4.3   Reset for Intel® LXT972A Transceiver

The LXT972A Transceiver provides both hardware and software resets, each of which manage differently the configuration control of auto-negotiation, speed, and duplex-mode selection.

For a software reset, Register bit 0.15 = 1. For register bit definitions used for software reset, see Table 41, "Control Register - Address 0, Hex 0" on page 79.

- During a software reset, bit settings in Table 45, "Auto-Negotiation Advertisement Register - Address 4, Hex 4" on page 82 are not re-read from the LXT972A Transceiver configuration pins. Instead, the bit settings revert to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset are not detected during a software reset.

- During a software reset, registers are available for reading. To see when the LXT972A Transceiver has completed reset, the reset bit can be polled (that is, Register bit 0.15 = 0).

For pin settings used during a hardware reset, see Section 5.4.4, "Hardware Configuration Settings". During a hardware reset, configuration settings for auto-negotiation and speed are read in from pins, and register information is unavailable for 1 ms after de-assertion of the reset.

5.4.4 Hardware Configuration Settings

The LXT972A Transceiver provides a hardware option to set the initial device configuration. As listed in Table 12, the hardware option uses the hardware configuration pins, the settings for which provide control bits.

Table 12. Hardware Configuration Settings for Intel® LXT972A Transceiver

Desired Mode			LED/CFG Pin Settings[1]			Resulting Register Bit Values						
						Control Register			Auto-Negotiation Advertisement Register			
Auto-Neg.	Speed (Mbps)	Duplex	1	2	3	Auto-Neg. 0.12	Speed 0.13	Full-Duplex 0.8	100 BASE-TX Full-Duplex 4.8	100 BASE-TX 4.7	10 BASE-T Full-Duplex 4.6	10 BASE-T 4.5
Disabled	10	Half	L	L	L	0	0	0	N/A Auto-Negotiation Advertisement			
		Full	L	L	H		0	1				
	100	Half	L	H	L		1	0				
		Full	L	H	H		1	1				
Enabled	100 Only	Half	H	L	L	1	1	0	0	1	0	0
		Full/Half	H	L	H		1	1	1	1	0	0
	10/100	Half Only	H	H	L		1	0	0	1	0	1
		Full or Half	H	H	H		1	1	1	1	1	1

1. L = Low, and H = High. For LED/CFG pin assignments, see Chapter 3.0, "Pin Assignments for Intel® LXT972A Transceiver".

5.5 Establishing Link

Figure 7 shows an overview of link establishment for the LXT972A Transceiver.

Note: When a link is established by parallel detection, the LXT972A Transceiver sets the duplex mode to half-duplex, as defined by the IEEE 802.3 standard.

Figure 7. Intel® LXT972A Transceiver Link Establishment Overview
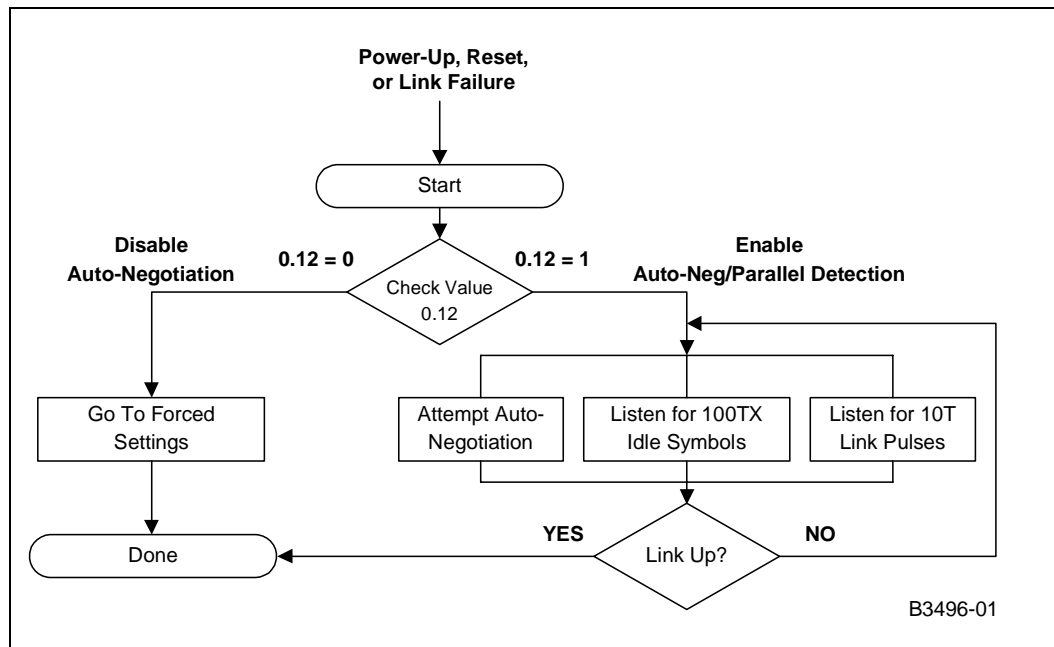
5.5.1 Auto-Negotiation

If not configured for forced operation, the LXT972A Transceiver attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of up to 33 link pulses spaced 62.5 μs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be absent or present to indicate a '0' or a '1'. Each FLP burst exchanges 16 bits of data, which are referred to as a "link code word". All devices that support auto-negotiation must implement the "Base Page" defined by the IEEE 802.3 standard (Registers 4 and 5).

The LXT972A Transceiver also supports the optional "Next Page" function as listed in Table 48, "Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7" on page 85 and Table 49, "Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8" on page 85.

5.5.1.1 Base Page Exchange

By exchanging Base Pages, the LXT972A Transceiver and its link partner communicate their capabilities to each other. Both sides must receive at least three consecutive identical base pages for negotiation to continue. Each side identifies the highest common capabilities that both sides support, and each side configures itself accordingly.

5.5.1.2   Manual Next Page Exchange

"Next Page Exchange" information is additional information that exceeds the information required by Base Page exchange and that is sent by "Next Pages". The LXT972A Transceiver fully supports the IEEE 802.3 standard method of negotiation through the Next Page exchange.

The Next Page exchange uses Register 7 to send information and Register 8 to receive it. Next Page exchange occurs only if both ends of the link partners advertise their ability to exchange Next Pages. Register bit 6.1 is used to make manual next page exchange easier for software. This register bit is cleared when a new negotiation occurs, preventing the user from reading an old value in Register 6 and assuming there is valid information in Registers 5 and 8.

5.5.1.3   Controlling Auto-Negotiation

When auto-negotiation is controlled by software, Intel recommends the following steps:

1. After power-up, power-down, or reset, the power-down recovery time (specified in Table 39, "Intel® LXT972A Transceiver RESET_L Pulse Width and Recovery Timing" on page 77) must be exhausted before proceeding.

2. Set the Auto-Negotiation Advertisement Register bits.

3. Enable auto-negotiation. (Set MDIO Register bit 0.12 = 1.)

4. To ensure proper operation, enable or restart auto-negotiation as soon as possible after writing to Register 4.

5.5.2   Parallel Detection

In parallel with auto-negotiation, the LXT972A Transceiver also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either symbol is detected, the device automatically reverts to the corresponding speed in half-duplex mode. Parallel detection allows the LXT972A Transceiver to communicate with devices that do not support auto-negotiation.

When parallel detection resolves a link, the link must be established in half-duplex mode. According to IEEE standards, the forced link partner cannot be configured to full-duplex. If the auto-negotiation link partner does not advertise half-duplex capability at the speed of the forced link partner, link is not established. The IEEE Standard prevents full-duplex-to-half-duplex link connections.

5.6 MII Operation

This section includes the following topics:

- Section 5.6.1, "MII Clocks"
- Section 5.6.2, "Transmit Enable"
- Section 5.6.3, "Receive Data Valid"
- Section 5.6.4, "Carrier Sense"
- Section 5.6.5, "Error Signals"
- Section 5.6.6, "Collision"
- Section 5.6.7, "Loopback"

The LXT972A Transceiver implements the Media Independent Interface (MII) as defined by the IEEE 802.3 standard. Separate channels are provided for transmitting data from the MAC to the LXT972A Transceiver (TXD), and for passing data received from the line (RXD) to the MAC. Each channel has its own clock, data bus, and control signals.

The following signals are used to pass received data to the MAC:

- COL
- CRS
- RX_CLK
- RX_DV
- RX_ER
- RXD[3:0]

The following signals are used to transmit data from the MAC:

- TX_CLK
- TX_EN
- TXD[3:0]

The LXT972A Transceiver supplies both clock signals as well as separate outputs for carrier sense and collision. Data transmission across the MII is normally implemented in 4-bit-wide nibbles.

5.6.1   MII Clocks

The LXT972A Transceiver is the master clock source for data transmission, and it supplies both MII clocks (RX_CLK and TX_CLK). It automatically sets the clock speeds to match link conditions.

- When the link is operating at 100 Mbps, the clocks are set to 25 MHz.

- When the link is operating at 10 Mbps, the clocks are set to 2.5 MHz.

Figure 8 through Figure 10 show the clock cycles for each mode.

Note: The transmit data and control signals must always be synchronized to TX_CLK by the MAC. The LXT972A Transceiver samples these signals on the rising edge of TX_CLK.

Figure 8. Clocking for 10BASE-T
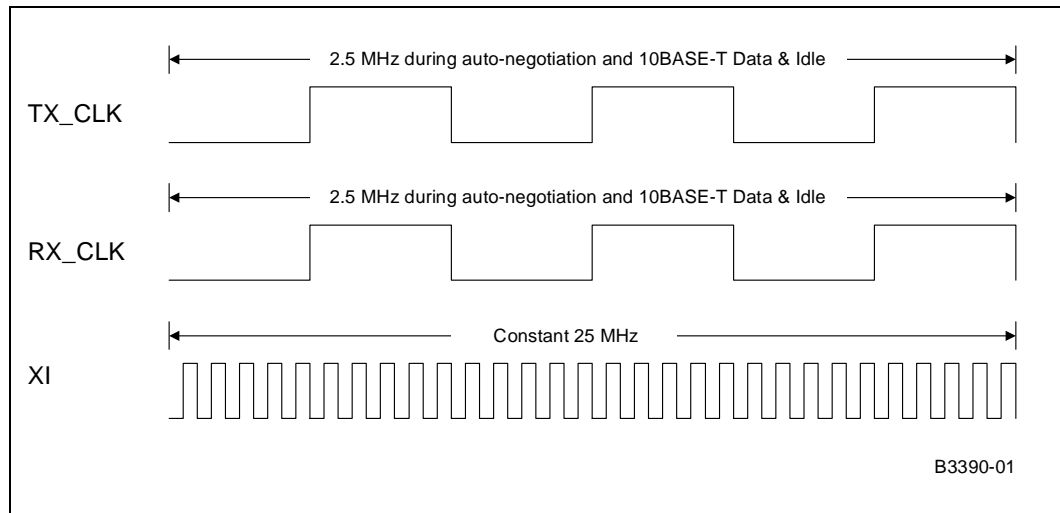
Figure 9. Clocking for 100BASE-X
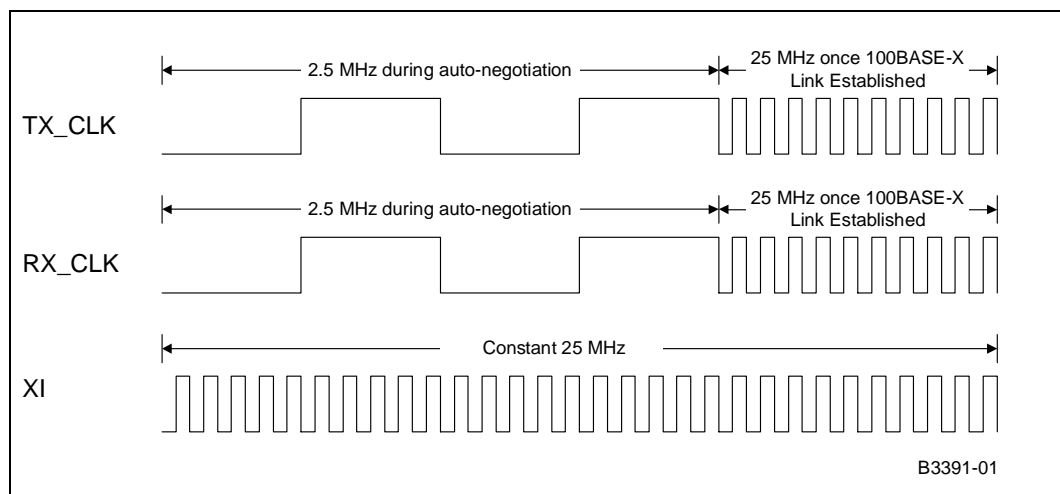
Figure 10. Clocking for Link Down Clock Transition

Link-Down Condition/Auto-Negotiate Enabled

RX_CLK
TX_CLK

Any
Clock

2.5 MHz
Clock

Clock transition time does not exceed
2X the nominal clock period:
10 Mbps = 2.5 MHz
100 Mbps = 25 MHz

B3503-01
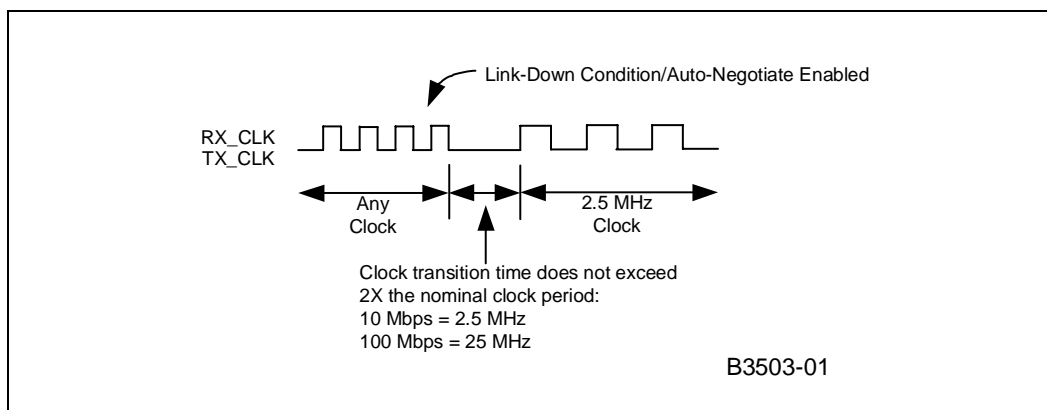
5.6.2   Transmit Enable

The MAC must assert TX_EN the same time as the first nibble of preamble and de-assert TX_EN after the last nibble of the packet.

5.6.3   Receive Data Valid

The LXT972A Transceiver asserts RX_DV when it receives a valid packet. Timing changes depend on line operating speed:

*   For 100BASE-TX links, RX_DV is asserted from the first nibble of preamble to the last nibble of the data packet.

*   For 10BASE-T links, the entire preamble is truncated. RX_DV is asserted with the first nibble of the Start of Frame Delimiter (SFD) "5D" and remains asserted until the end of the packet.

5.6.4 Carrier Sense

Carrier Sense (CRS) is an asynchronous output.

- CRS is always generated when the LXT972A Transceiver receives a packet from the line.

- CRS is also generated when the LXT972A Transceiver is in half-duplex mode when a packet is transmitted.

Table 13 summarizes the conditions for assertion of carrier sense, data loopback, and collision signals. Carrier sense is not generated when a packet is transmitted and in full-duplex mode.

Table 13. Carrier Sense, Loopback, and Collision Conditions

Speed	Duplex Condition	Carrier Sense	Test Loop-back[1, 2]	Operational Loop-back[1, 2]	Collision
100 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex	Transmit or Receive	No	No	Transmit and Receive
10 Mbps	Full-Duplex	Receive Only	Yes	No	None
	Half-Duplex, Register bit 16.8 = 0	Transmit or Receive	Yes	Yes	Transmit and Receive
	Half-Duplex, Register bit 16.8 = 1	Transmit or Receive	No	No	Transmit and Receive

1. Test Loopback is enabled when Register bit 0.14 = 1.
2. For descriptions of Test Loopback and Operational Loopback, see Section 5.6.7, "Loopback" on page 42.

5.6.5 Error Signals

When the LXT972A Transceiver is in 100 Mbps mode and receives an invalid symbol from the network, it asserts RX_ER and drives "0101" on the RXD pins.

When the MAC asserts TX_ER, the LXT972A Transceiver drives "H" symbols out on the TPOP/N pins.

5.6.6 Collision

The LXT972A Transceiver asserts its collision signal asynchronously to any clock whenever the line state is half-duplex and the transmitter and receiver are active at the same time. Table 13 summarizes the conditions for assertion of carrier sense, data loopback, and collision signals.

5.6.7   Loopback

The LXT972A Transceiver provides the following loopback functions:

- Section 5.6.7.1, "Operational Loopback"
- Section 5.6.7.2, "Internal Digital Loopback (Test Loopback)"

Figure 11 shows LXT972A Transceiver operational and test loopback paths. (An internal digital loopback path is not shown.) For more information on loopback functions, see Table 13, "Carrier Sense, Loopback, and Collision Conditions" on page 41.

Figure 11. Intel® LXT972A Transceiver Loopback Paths
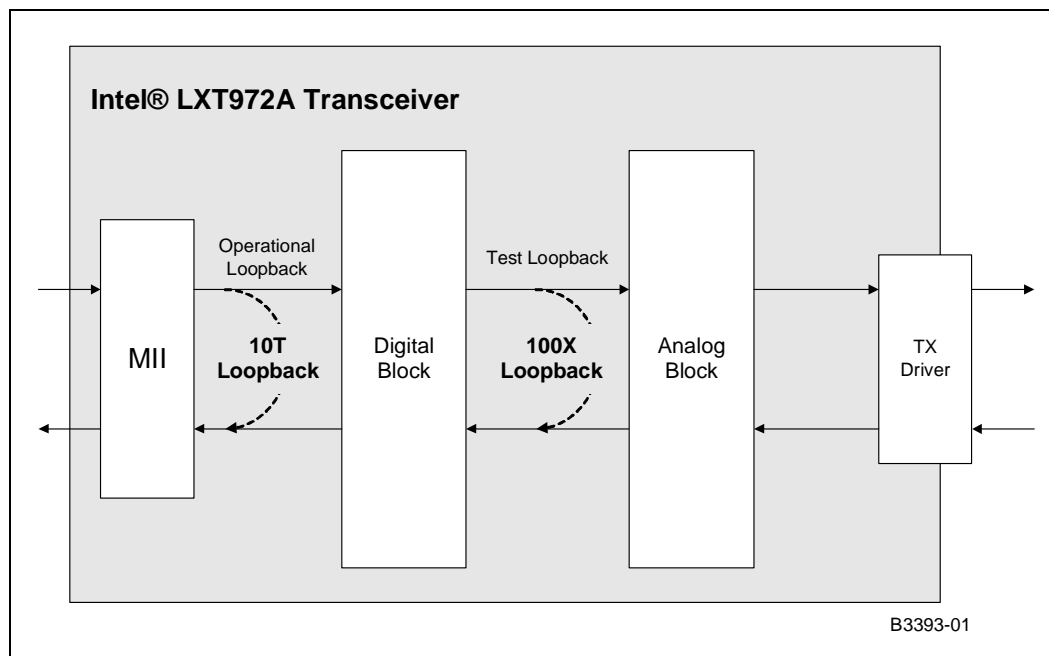
5.6.7.1   Operational Loopback

- Operational loopback is provided for 10 Mbps half-duplex links when Register bit 16.8 = 0. Data that the MAC (TXData) transmits loops back on the receive side of the MII (RXData).
- Operational loopback is not provided for 100 Mbps links, full-duplex links, or when Register 16.8 = 1.

5.6.7.2 Internal Digital Loopback (Test Loopback)

A test loopback function is provided for diagnostic testing of the LXT972A Transceiver. During test loopback, twisted-pair and fiber interfaces are disabled. Data transmitted by the MAC is internally looped back by the LXT972A Transceiver and returned to the MAC.

Test loopback is available for both 100BASE-TX and 10BASE-T operation, and is enabled by setting the following register bits:

- Register bit 0.14 = 1 (Setting to enable loopback mode)
- Register bit 0.8 = 1 (Setting for full-duplex mode)
- Register bit 0.12 = 0. (Disable auto-negotiation.)

5.7 100 Mbps Operation

5.7.1 100BASE-X Network Operations

During 100BASE-X operation, the LXT972A Transceiver transmits and receives 5-bit symbols across the network link.

Figure 12 shows the structure of a standard frame packet in 100BASE-X mode. When the MAC is not actively transmitting data, the LXT972A Transceiver sends out Idle symbols on the line.

As Figure 12 shows, the MAC starts each transmission with a preamble pattern. As soon as the LXT972A Transceiver detects the start of preamble, it transmits a Start-of-Stream Delimiter (SSD, symbols J and K) to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD, packet data, and CRC.

Once the packet ends, the LXT972A Transceiver transmits the End-of-Stream Delimiter (ESD, symbols T and R) and then returns to transmitting Idle symbols.

For details on the symbols used, see 4B/5B coding listed in Table 14, "4B/5B Coding" on page 48.

Figure 12. 100BASE-X Frame Format
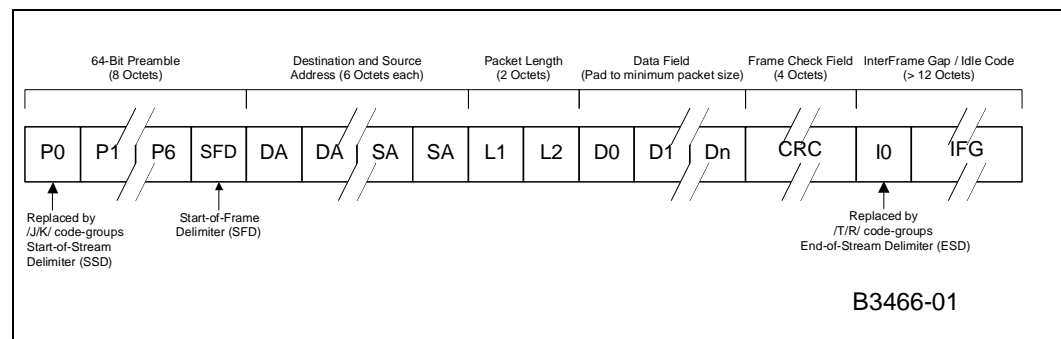
As shown in Figure 13, in 100BASE-TX mode, the LXT972A Transceiver scrambles and transmits the data to the network using MLT-3 line code. MLT-3 signals received from the network are descrambled, decoded, and sent across the MII to the MAC.

Figure 13. 100BASE-TX Data Path
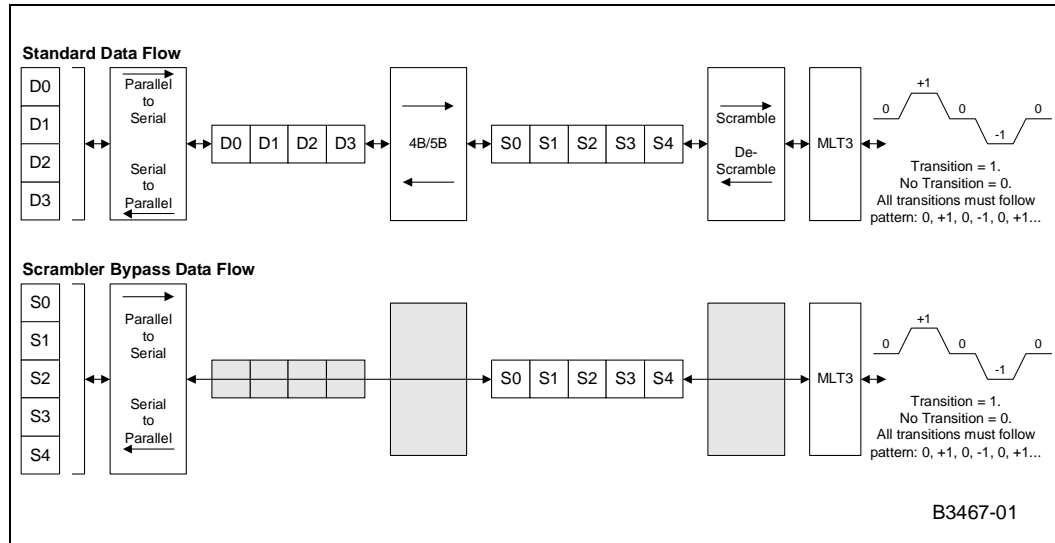
Figure 14 shows normal reception with no errors.

Figure 14. 100BASE-TX Reception with No Errors
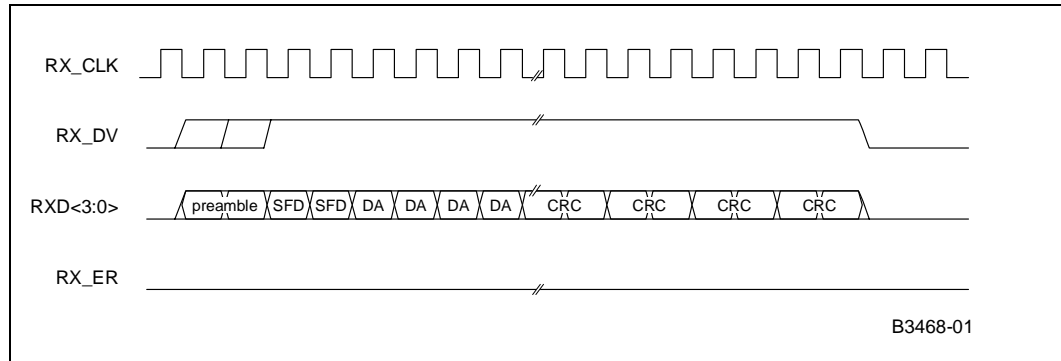
As shown in Figure 15, when the LXT972A Transceiver receives invalid symbols from the line, it asserts RX_ER.

Figure 15. 100BASE-TX Reception with Invalid Symbol
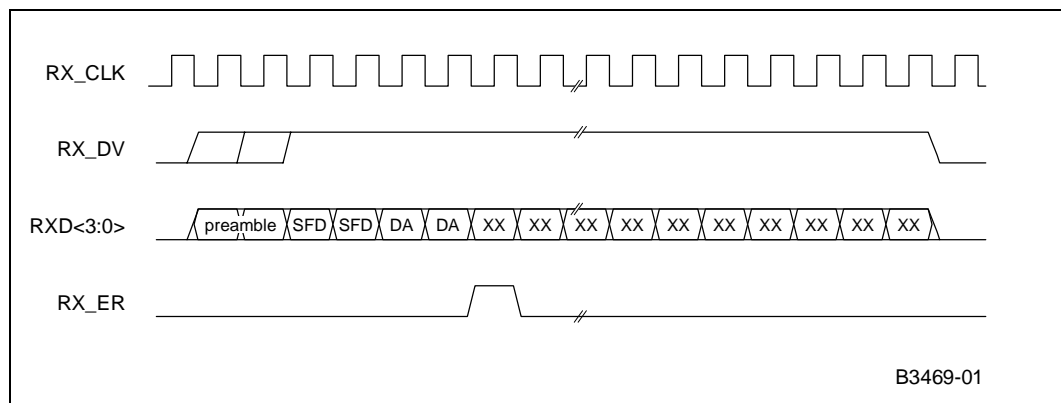
5.7.2 Collision Indication

Figure 16 shows normal transmission.

Figure 16. 100BASE-TX Transmission with No Errors
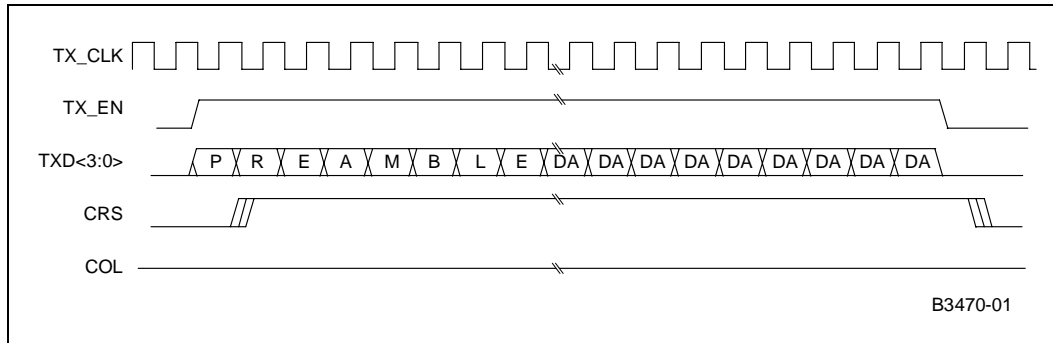
Upon detection of a collision, the COL output is asserted and remains asserted for the duration of the collision as shown in Figure 17.

Figure 17. 100BASE-TX Transmission with Collision
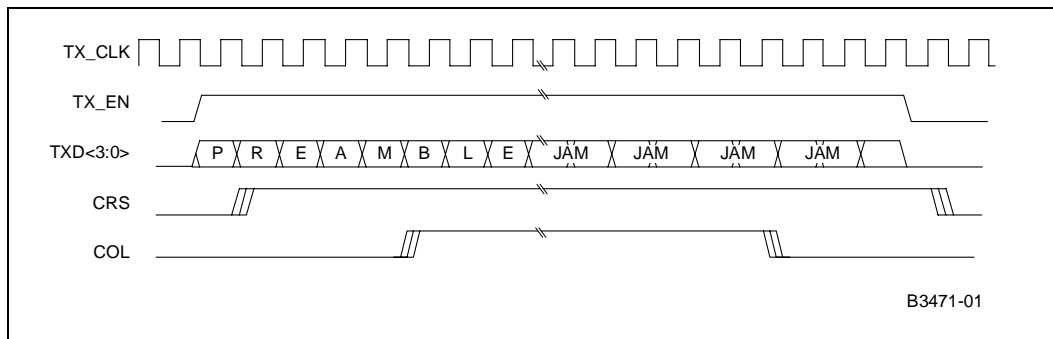
5.7.3   100BASE-X Protocol Sublayer Operations

With respect to the 7-layer communications model, the LXT972A Transceiver is a Physical Layer 1 (PHY) device.

The LXT972A Transceiver implements the following sublayers of the reference model defined by the IEEE 802.3 standard, and discussed from the reference model point of view:

- Section 5.7.3.1, "Physical Coding Sublayer"
- Section 5.7.3.2, "Physical Medium Attachment Sublayer"
- Section 5.7.3.3, "Twisted-Pair Physical Medium Dependent Sublayer"

Figure 18 shows the LXT972A Transceiver protocol sublayers.

Figure 18. Intel® LXT972A Protocol Sublayers
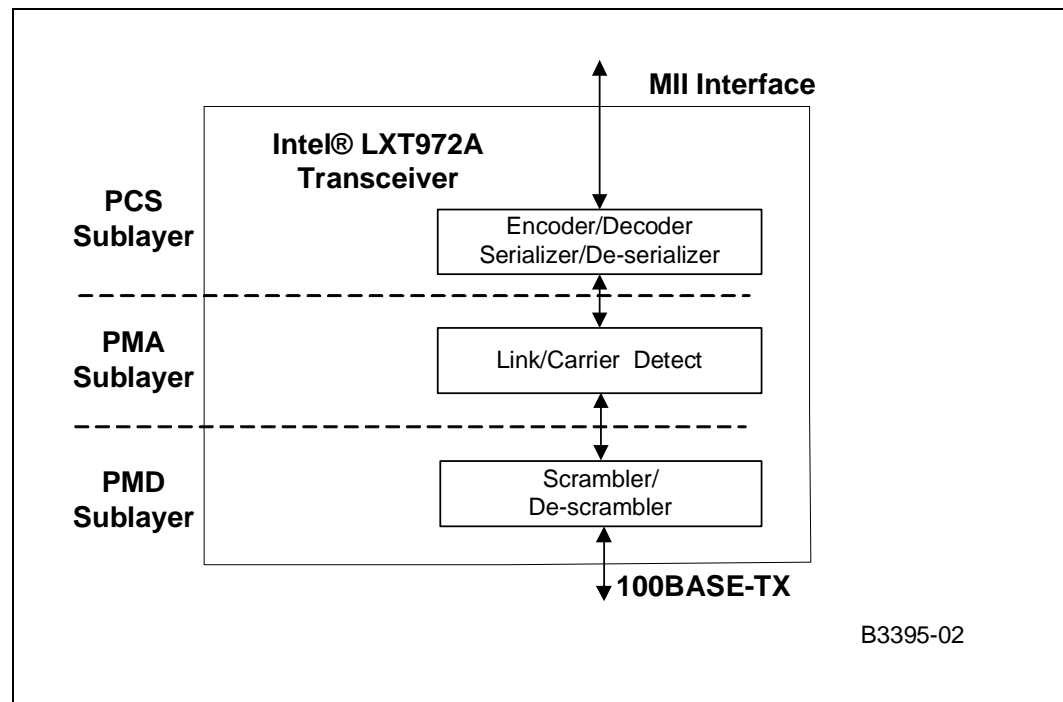
5.7.3.1   Physical Coding Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/decoding function.

For 100BASE-TX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TX_EN is de-asserted.

5.7.3.1.1   Preamble Handling

When the MAC asserts TX_EN, the PCS substitutes a /J/K symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data, following the 4B/5B coding in Table 14, until TX_EN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD. In 100 Mbps operation, preamble is always passed through the PCS layer to the MII interface.

Table 14. 4B/5B Coding (Sheet 1 of 2)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Used as inter-stream fill code

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs, and /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs, and /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 14. 4B/5B Coding (Sheet 2 of 2)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
CONTROL	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	Undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	Undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
INVALID	Undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	Undefined	Invalid	0 0 0 0 0	Invalid
	Undefined	Invalid	0 0 0 0 1	Invalid
	Undefined	Invalid	0 0 0 1 0	Invalid
	Undefined	Invalid	0 0 0 1 1	Invalid
	Undefined	Invalid	0 0 1 0 1	Invalid
	Undefined	Invalid	0 0 1 1 0	Invalid
	Undefined	Invalid	0 1 0 0 0	Invalid
	Undefined	Invalid	0 1 1 0 0	Invalid
	Undefined	Invalid	1 0 0 0 0	Invalid
	Undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs, and /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs, and /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

5.7.3.2   Physical Medium Attachment Sublayer

5.7.3.2.1   Link

In 100 Mbps mode, link is established when the descrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 16 consecutive idle symbols in any 2 ms period. This operation filters out small noise hits that may disrupt the link.

In 100 Mbps mode, link is established when the descrambler becomes locked and remains locked for approximately 50 ms. Link remains up unless the descrambler receives less than 16 consecutive idle symbols in any 2 ms period. This operation filters out small noise hits that may disrupt the link.

For short periods, MLT-3 idle waveforms meet all criteria for 10BASE-T start delimiters. A working 10BASE-T receive may temporarily indicate link to 100BASE-TX waveforms. However, the PHY does not bring up a permanent 10 Mbps link.

The LXT972A Transceiver reports link failure through the MII status bits (Register bits 1.2 and 17.10) and interrupt functions. Link failure causes the LXT972A Transceiver to re-negotiate if auto-negotiation is enabled.

5.7.3.2.2   Link Failure Override

The LXT972A Transceiver normally transmits data packets only if it detects the link is up. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT972A Transceiver to transmit data packets even when the link is down. This feature is provided as a transmit diagnostic tool.

Note: Auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT972A Transceiver automatically transmits FLP bursts if the link is down.

Caution: During normal operation, Intel does not recommend setting Register bit 16.14 for 100 Mbps receive functions because receive errors may be generated.

5.7.3.2.3   Carrier Sense

For 100BASE-TX links, a start-of-stream delimiter (SSD) or /J/K symbol pair causes assertion of carrier sense (CRS). An end-of-stream delimiter (ESD) or /T/R symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R. However, in this case RX_ER is asserted for one clock cycle when CRS is de-asserted.

Intel does not recommend using CRS for Interframe Gap (IFG) timing for the following reasons:

- CRS de-assertion time is slightly longer than CRS assertion time. As a result, an IFG interval appears somewhat shorter to the MAC than it actually is on the wire.
- CRS de-assertion is not aligned with TX_EN de-assertion on transmit loopbacks in half-duplex mode.

5.7.3.2.4   Receive Data Valid

The LXT972A Transceiver asserts RX_DV to indicate that the received data maps to valid symbols. In 100 Mbps operation, RX_DV is active with the first nibble of preamble.

5.7.3.3   Twisted-Pair Physical Medium Dependent Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides signal scrambling and de-scrambling functions, line coding and decoding functions (MLT-3 for 100BASE-TX, Manchester for 10BASE-T), as well as receiving, polarity correction, and baseline wander correction functions.

5.7.3.3.1   Scrambler/Descrambler

The purpose of the scrambler/descrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, data-independent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

Scrambler Seeding. Once the transmit data (or Idle symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Five seed bits are determined by the PHY address, and the remaining bits are hard coded in the design.

Scrambler Bypass. The scrambler/de-scrambler can be bypassed by setting Register bit 16.12 = 1. Scrambler bypass is provided for diagnostic and test support.

5.7.3.3.2   Polarity Correction

The 100 Mbps twisted pair signaling is not polarity sensitive. As a result, the polarity status is not a valid status indicator.

5.7.3.3.3   Baseline Wander Correction

The LXT972A Transceiver provides a baseline wander correction function for when the LXT972A Transceiver is under network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition "unbalanced". As a result, the average value of the signal voltage can "wander" significantly over short time intervals (tenths of seconds). This wander can cause receiver errors at long-line lengths (100 meters) in less robust designs. Exact characteristics of the wander are completely data dependent.

The LXT972A Transceiver baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case packets over all cable lengths.

5.7.3.3.4   Programmable Slew Rate Control

The LXT972A Transceiver device supports a programmable slew-rate mechanism whereby one of four pre-selected slew rates can be used. (For details, see Table 56, "Transmit Control Register - Address 30, Hex 1E" on page 93.) The slew-rate mechanism allows the designer to optimize the output waveform to match the characteristics of the magnetics.

5.8   10 Mbps Operation

The LXT972A Transceiver operates as a standard 10BASE-T transceiver and LXT972A supports standard 10 Mbps functions. During 10BASE-T operation, the LXT972A Transceiver transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT972A Transceiver drives link pulses onto the line.

In 10BASE-T mode, the polynomial scrambler/de-scrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT972A Transceiver and sent across the MII to the MAC.

Note: The LXT972A Transceiver does not support fiber connections.

5.8.1   10BASE-T Preamble Handling

The LXT972A Transceiver offers two options for preamble handling, selected by Register bit 16.5.

- In 10BASE-T mode when Register bit 16.5 = 0, the LXT972A Transceiver strips the entire preamble off of received packets. CRS is asserted coincident with the start of the preamble. RX_DV is held Low for the duration of the preamble. When RX_DV is asserted, the very first two nibbles driven by the LXT972A Transceiver are the SFD "5D" hex followed by the body of the packet.

- In 10BASE-T mode when Register bit 16.5 = 1, the LXT972A Transceiver passes the preamble through the MII and asserts RX_DV and CRS simultaneously. (In 10BASE-T loopback, the LXT972A Transceiver loops back whatever the MAC transmits to it, including the preamble.)

5.8.2   10BASE-T Carrier Sense

For 10BASE-T links, CRS assertion is based on reception of valid preamble, and CRS de-assertion is based on reception of an end-of-frame (EOF) marker. Register bit 16.7 allows CRS de-assertion to be synchronized with RX_DV de-assertion. For details, see Table 51, "Configuration Register - Address 16, Hex 10" on page 87.

5.8.3   10BASE-T Dribble Bits

The LXT972A Transceiver handles dribble bits in all modes. If one to four dribble bits are received, the nibble is passed across the MII, padded with ones if necessary.   If five to seven dribble bits are received, the second nibble is not sent to the MII bus.

5.8.4   10BASE-T Link Integrity Test

In 10BASE-T mode, the LXT972A Transceiver always transmits link pulses.

- If the Link Integrity Test function is enabled (the normal configuration), the LXT972A Transceiver monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission is disabled.

- If the Link Integrity Test function is disabled (which can be done by setting Configuration Register bit 16.14 to '1'), the LXT972A Transceiver transmits to the connection regardless of detected link pulses.

5.8.5   Link Failure

Link failure occurs if the Link Integrity Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT972A Transceiver returns to the auto-negotiation phase if auto-negotiation is enabled. If the Link Integrity Test function is disabled by setting Configuration Register bit 16.14 to '1', the LXT972A Transceiver transmits packets, regardless of link status.

5.8.6   10BASE-T SQE (Heartbeat)

By default, the Signal Quality Error (SQE) or heartbeat function is disabled on the LXT972A Transceiver. To enable this function, set Register bit 16.9 = 1. When this function is enabled, the LXT972A Transceiver asserts its COL output for 5 to 15 bit times (BT) after each packet.

5.8.7   10BASE-T Jabber

If a transmission exceeds the jabber timer, the LXT972A Transceiver disables the transmit and loopback functions. For jabber timing parameters, see Figure 27, "Intel® LXT972A Transceiver 10BASE-T Jabber and Unjabber Timing" on page 72.

The LXT972A Transceiver automatically exits jabber mode after the unjabber time has expired. This function can be disabled by setting Register bit 16.10 = 1.

5.8.8   10BASE-T Polarity Correction

The LXT972A Transceiver automatically detects and corrects for the condition in which the receive signal (TPIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses - or four inverted end-of-frame (EOF) markers - are received consecutively. If link pulses or data are not received by the maximum receive time-out period (96 to 128 ms), the polarity state is reset to a non-inverted state. When polarity reversal is detected in 10BASE-T operation, register 17.5 is set to 1. (For details, see bit 17.5 in Table 52, "Status Register #2 - Address 17, Hex 11" on page 88.)

5.9 Monitoring Operations

5.9.1 Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Register bit 17.7 is set to '1' once the auto-negotiation process is completed.
- Register bits 1.2 and 17.10 are set to '1' once the link is established.
- Register bits 17.14 and 17.9 can be used to determine the link operating conditions (speed and duplex).

Note: When the LXT972A Transceiver detects incorrect polarity for a 10BASE-T operation, Register bit 17.5 is set to '1'.

5.9.2 Monitoring Next Page Exchange

The LXT972A Transceiver offers an Alternate Next Page mode to simplify the next page exchange process. Normally, Register bit 6.1 (Page Received) remains set until read. When Alternate Next Page mode is enabled, Register bit 6.1 is automatically cleared whenever a new negotiation process takes place. This action prevents the user from reading an old value in bit 6.1 and assuming that Registers 5 and 8 (Partner Ability) contain valid information. Additionally, the LXT972A Transceiver uses Register bit 6.5 to indicate when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to a new negotiation process starting. Register bits 6.1 and 6.5 are cleared when read.

5.9.3   LED Functions

The LXT972A Transceiver has these direct LED driver pins: LED1/CFG1, LED2/CFG2, and LED3/CFG3.

On power-up, all the drivers are asserted for approximately 1 second after reset de-asserts. Each LED driver can be programmed using the LED Configuration Register (Table 55, "LED Configuration Register - Address 20, Hex 14" on page 91) to indicate one of the following conditions:

- Collision Condition
- Duplex Mode
- Link Status
- Operating Speed
- Receive Activity
- Transmit Activity

The LED drivers can also be programmed to display various combined status conditions. For example, setting Register bits 20.15:12 to '1101' produces the following combination of Link and Activity indications:

- If Link is down, LED is off. If activity is detected from the MAC, the LED still blinks even if the link is down.
- If Link is up, LED is on.
- If Link is up and activity is detected, the LED blinks at the stretch interval selected by Register bits 20.3:2 and continues to blink as long as activity is present.

For the LXT972A Transceiver, the LED driver pins also provide initial configuration settings. The LED pins are sensitive to polarity and automatically pull up or pull down to configure for either open drain or open collector circuits (10 mA Max current rating) as required by the hardware configuration. For details, see the discussion of "Hardware Configuration Settings" on page 35.

5.9.4   LED Pulse Stretching

The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. The pulse stretch time is extended further if the event occurs again during this pulse stretch period.

When an event such as receiving a packet occurs, the event is edge detected and it starts the stretch timer. The LED driver remains asserted until the stretch timer expires. If another event occurs before the stretch timer expires, then the stretch timer is reset and the stretch time is extended.

When a long event (such as duplex status) occurs, the event is edge detected and it starts the stretch timer. When the stretch timer expires, the edge detector is reset so that a long event causes another pulse to be generated from the edge detector, which resets the stretch timer and causes the LED driver to remain asserted.

Figure 19 shows how the stretch operation functions.

Figure 19. LED Pulse Stretching

Note: The direct drive LED outputs in this diagram are shown as active Low.

B3475-01
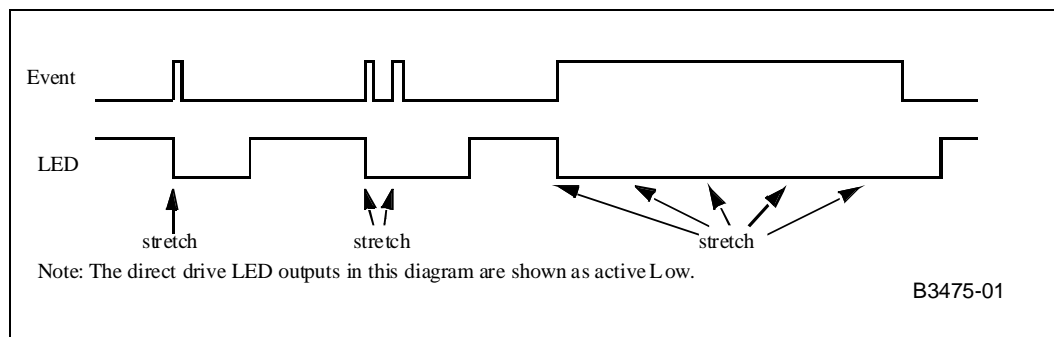
5.10 Boundary Scan (JTAG 1149.1) Functions

The LXT972A Transceiver includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

Note: For the related BSDL file, contact your local sales office or access the Intel website (www.intel.com).

5.10.1 Boundary Scan Interface

The boundary scan interface consists of five pins (TMS, TDI, TDO, TRST_L, and TCK). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are pulled up internally. TCK is pulled down internally. TDO does not have an internal pull-up or pull-down.

5.10.2 State Machine

The TAP controller is a state machine, with 16 states driven by the TCK and TMS pins. Upon reset, the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are high for five TCK periods.

5.10.3 Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures the correct data flow to the Data registers according to the current instruction.

Table 15 lists valid JTAG instructions for the LXT972A Transceiver.

Table 15. Valid JTAG Instructions

Name	Code	Description	Mode	Data Register
EXTEST	1111 1111 1110 1000	External Test	Test	BSR
IDCODE	1111 1111 1111 1110	ID Code Inspection	Normal	ID REG
SAMPLE	1111 1111 1111 1000	Sample Boundary	Normal	BSR
HIGHZ	1111 1111 1100 1111	Force Float	Normal	Bypass
CLAMP	1111 1111 1110 1111	Control Boundary to 1/0	Test	Bypass
BYPASS	1111 1111 1111 1111	Bypass Scan	Normal	Bypass

5.10.4 Boundary Scan Register

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. Table 16 lists the four BSR modes of operation.

Table 16. BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

5.10.5 Device ID Register

Table 17 lists the bits for the Device ID register. For the current version of the JEDEC continuation characters, see the specification update for the LXT972A Transceiver.

Table 17. Device ID Register for Intel® LXT972A Transceiver

Bits 31:28	Bits 27:12	Bits 11:8	Bits 7:1	Bit 0
Version	Part ID (Hex)	JEDEC Continuation Characters	JEDEC ID[1]	Reserved
XXXX	03CB	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. The MSB is for parity and is ignored. The Intel JEDEC ID is FE (1111 1110), which becomes 111 1110.

6.0   Application Information

6.1   Magnetics Information

The LXT972A Transceiver requires a 1:1 ratio for both the receive and transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. For transformer/magnetics requirements, see Table 18.

Note: Before committing to a specific component, contact the manufacturer for current product specifications and validate the magnetics for the specific application.

Table 18.   Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	–
Tx turns ratio	–	1 : 1	–	–	–
Insertion loss	0.0	0.6	1.1	dB	–
Primary inductance	350	–	–	μH	–
Transformer isolation	–	1.5	–	kV	–
Differential to common mode rejection	40	–	–	dB	0.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

6.2   Typical Twisted-Pair Interface

Table 19 provides a comparison of the RJ-45 connections for NIC and Switch applications in a typical twisted-pair interface setting.

Table 19.   I/O Pin Comparison of NIC and Switch RJ-45 Setups

Symbol	RJ-45	
	Switch	NIC
TPIP	1	3
TPIN	2	6
TPOP	3	1
TPON	6	2

Figure 20 shows the LXT972A Transceiver in a typical twisted-pair interface, with the RJ-45 connections crossed over for a Switch configuration.

Figure 20. Intel® LXT972A Transceiver Typical Twisted-Pair Interface - Switch

1. Center tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the LXT972A Transceiver.
3. Magnetics without a receive pair center-tap do not require a 2 kV termination.
4. RJ-45 connections shown are for a standard switch application.

Figure 21 shows the LXT972A Transceiver in a typical twisted-pair interface, with the RJ-45 connections configured for a NIC application.

Figure 21. Intel® LXT972A Transceiver Typical Twisted-Pair Interface - NIC
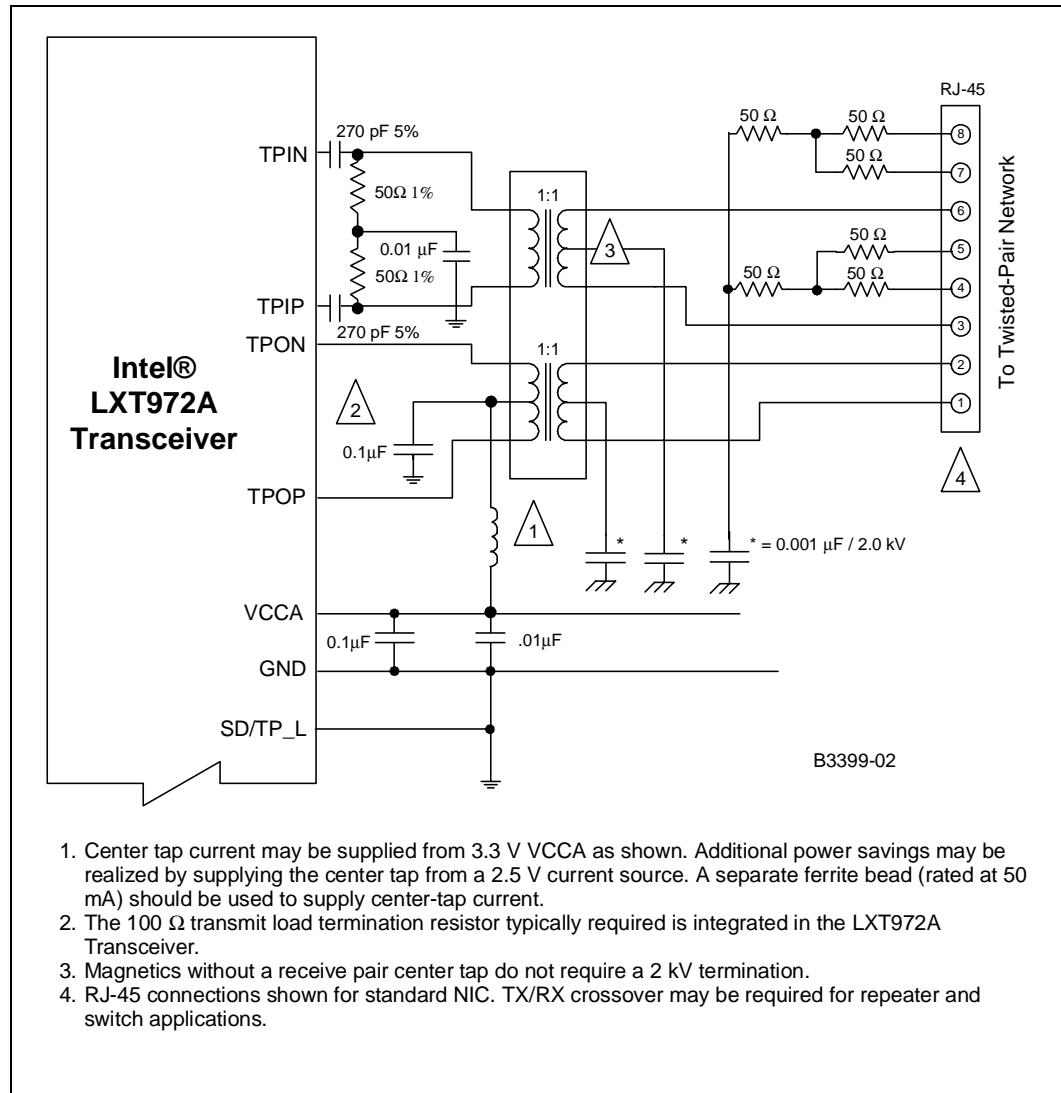
1. Center tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center-tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the LXT972A Transceiver.
3. Magnetics without a receive pair center tap do not require a 2 kV termination.
4. RJ-45 connections shown for standard NIC. TX/RX crossover may be required for repeater and switch applications.

Figure 22 shows a typical media independent interface (MII) for the LXT972A Transceiver.

Figure 22. Intel® LXT972A Transceiver Typical Media Independent Interface
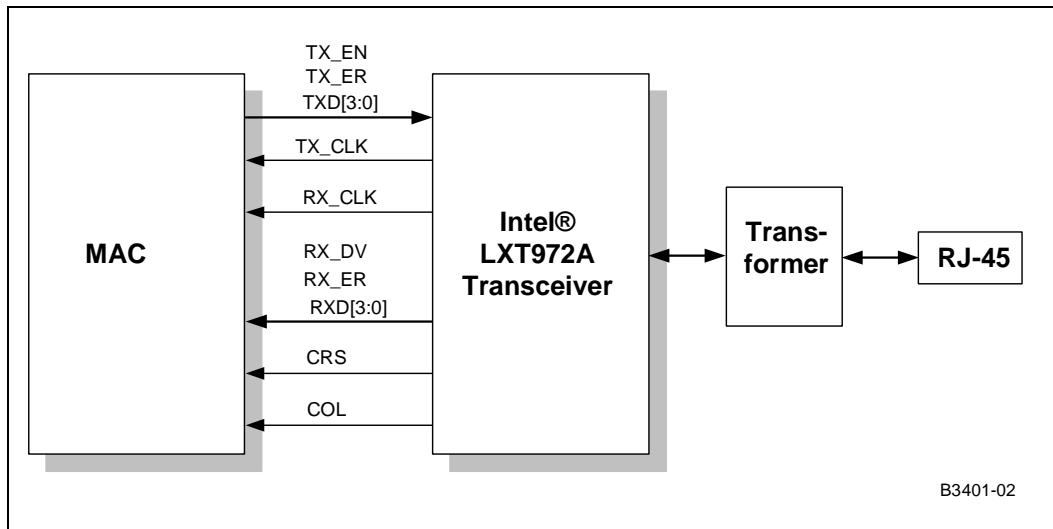
7.0 Electrical Specifications

This chapter includes test specifications for the LXT972A Transceiver. These specifications are guaranteed by test except where noted "by design".

- Table 20 lists the absolute maximum ratings.
- Table 21 lists the recommended operating conditions.
- Table 22 through Table 39 list the minimum and maximum values that apply over the recommended operating conditions specified.

7.1 Electrical Parameters

Table 20 lists absolute maximum ratings for the LXT972A Transceiver.

Caution:

- Exceeding the absolute maximum rating values may cause permanent damage.
- Functional operation under these conditions is not implied.
- Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Absolute Maximum Ratings for Intel® LXT972A Transceiver

Parameter	Sym	Min	Max	Units
Supply Voltage	Vcc	-0.3	4.0	V
Storage Temperature	Tst	-65	+150	ºC

Table 21 lists the recommended operating conditions for the LXT972A Transceiver.

Table 21. Recommended Operating Conditions for Intel® LXT972A Transceiver

Parameter	Sym	Min	Typ[1]	Max	Units
Recommended operating temperature	Topa	0	–	70	ºC
VCC current - 100 BASE-TX	Icc	–	92	110	mA
VCC current - 10 BASE-T	Icc	–	66	82	mA
Hard Power Down	Icc	–	–	1	mA
Soft Power Down	Icc	–	51	–	mA
Auto-Negotiation	Icc	–	90	110	mA

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Voltages are with respect to ground unless otherwise specified.

Table 22 lists digital I/O characteristics for all pins except the MII, XI/XO, and LED/CFG pins.

Table 22. Digital I/O Characteristics (Except for MII, XI/XO, and LED/CFG Pins)

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	$I_{OL} = 4$ mA
Output High voltage	V_{OH}	2.4	–	–	V	$I_{OH} = -4$ mA

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Table 23 lists digital I/O characteristics for the MII pins.

Table 23. Digital I/O Characteristics[1] - MII Pins

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-10	–	10	µA	$0.0 < V_I < VCCIO$
Output Low voltage	V_{OL}	–	–	0.4	V	$I_{OL} = 4$ mA
Output High voltage	V_{OH}	2.2	–	–	V	$I_{OH} = -4$ mA, VCCIO = 3.3 V
	V_{OH}	2.0	–	–	V	$I_{OH} = -4$ mA, VCCIO = 2.5 V
Driver output resistance (Line driver output enabled)	Ro^3	–	100	–	Ω	VCCIO = 2.5 V
	Ro^3	–	100	–	Ω	VCCIO = 3.3 V

1. MII digital I/O pins are tolerant to 5 V inputs.
2. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
3. Parameter is guaranteed by design and not subject to production testing.

Table 24 lists the I/O characteristics for the REFCLK/XI and XO pins.

Table 24. I/O Characteristics - REFCLK/XI and XO Pins

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Clock Frequency Tolerance[2]	Δf	–	–	±100	ppm	–
Input Clock Duty Cycle[2]	Tdc	35	–	65	%	–
Input Capacitance	C_{IN}	–	3.0	–	pF	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Parameter is guaranteed by design and not subject to production testing.

Table 25 lists the I/O characteristics for the LXT972A Transceiver LED/CFG pins.

Table 25. I/O Characteristics - LED/CFG Pins

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Current	I_I	-10	–	10	µA	0 < V_I < VCCIO
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}	2.0	–	–	V	I_{OH} = -10 mA

Table 26 lists the 100BASE-TX characteristics.

Table 26. 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	T_{RF}	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	T_{RFS}	–	–	0.5	ns	Note 2
Duty cycle distortion	D_{CD}	35	50	65	%	Offset from 16 ns pulse width at 50% of pulse peak
Overshoot/Undershoot	V_{OS}	–	–	5	%	–
Jitter (measured differentially)	–	–	–	1.4	ns	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100 Ω(+/-1%) resistor.

Table 27 lists the 10BASE-T characteristics.

Table 27. 10BASE-T Transceiver Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	V_{OP}	2.2	2.5	2.8	V	With transformer, line replaced by 100 Ω resistor
Transition timing jitter added by the MAU and PLS sections	–	0	2	11	ns	After line model specified by IEEE 802.3 for 10BASE-T MAU
Receiver						
Receive Input Impedance	Z_{IN}	–	–	22	kΩ	–
Differential Squelch Threshold	V_{DS}	300	420	585	mV	–

Table 28 lists the 10BASE-T link integrity timing characteristics.

Table 28. 10BASE-T Link Integrity Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Time Link Loss Receive	T_{LL}	50	–	150	ms	–
Link Pulse	T_{LP}	2	–	7	Link Pulses	–
Link Min Receive Timer	T_{LR} Min	2	–	7	ms	–
Link Max Receive Timer	T_{LR} Max	50	–	150	ms	–
Link Transmit Period	Tlt	8	–	24	ms	–
Link Pulse Width	Tlpw	60	–	150	ns	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Table 29 lists the thermal characteristics.

Table 29. Intel® LXT972A Transceiver Thermal Characteristics

Parameter	LXT972A Transceiver
Package	1 0x 10 x1.4 64 LD LQFP
Theta-JA	58 C/W
Theta-JC	27 C/W
Psi - JT	3.4 C/W

7.2   Timing Diagrams

Figure 23. Intel® LXT972ATransceiver 100BASE-TX Receive Timing

Note: Timing diagram depicts 4B mode.   B3492-03
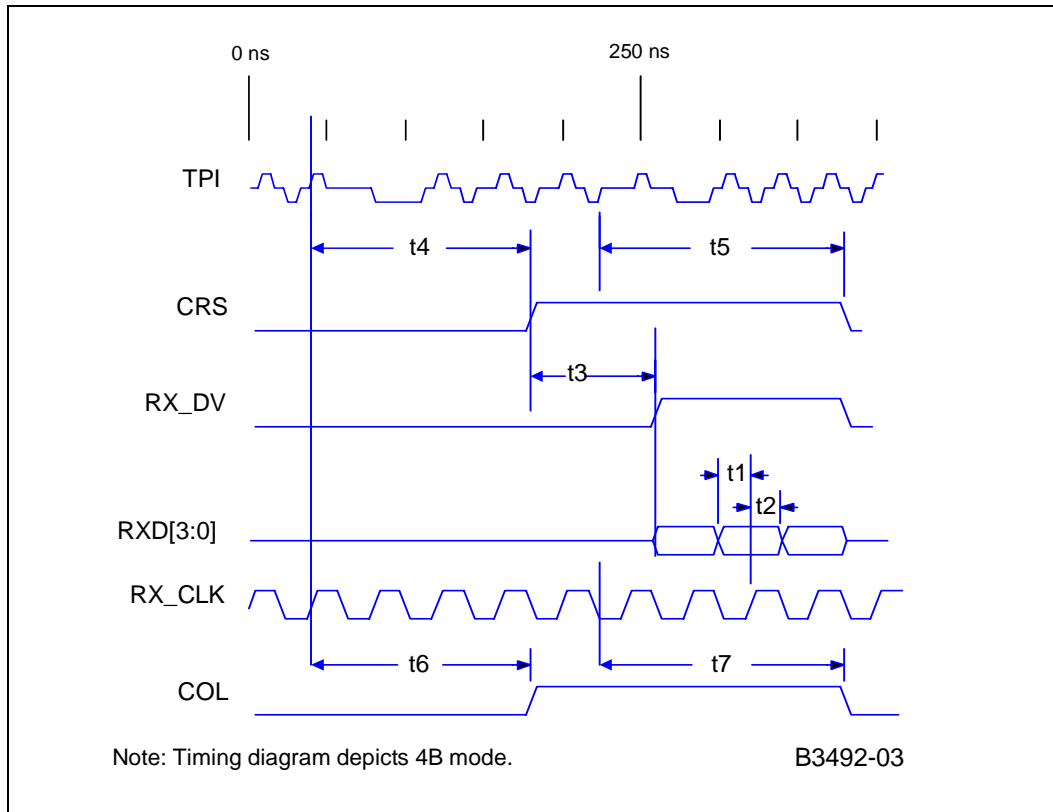
Table 30. Intel® LXT972A Transceiver 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD[3:0], RX_DV, RX_ER[3] setup to RX_CLK High	t1	10	–	–	ns	–
RXD[3:0], RX_DV, RX_ER hold from RX_CLK High	t2	10	–	–	ns	–
CRS asserted to RXD[3:0], RX_DV	t3	3	–	5	BT	–
Receive start of "J" to CRS asserted	t4	12	–	16	BT	–
Receive start of "T" to CRS de-asserted	t5	10	–	17	BT	–
Receive start of "J" to COL asserted	t6	16	–	22	BT	–
Receive start of "T" to COL de-asserted	t7	17	–	20	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.
3. RX_ER is not shown in the figure.

Figure 24. Intel® LXT972A Transceiver 100BASE-TX Transmit Timing
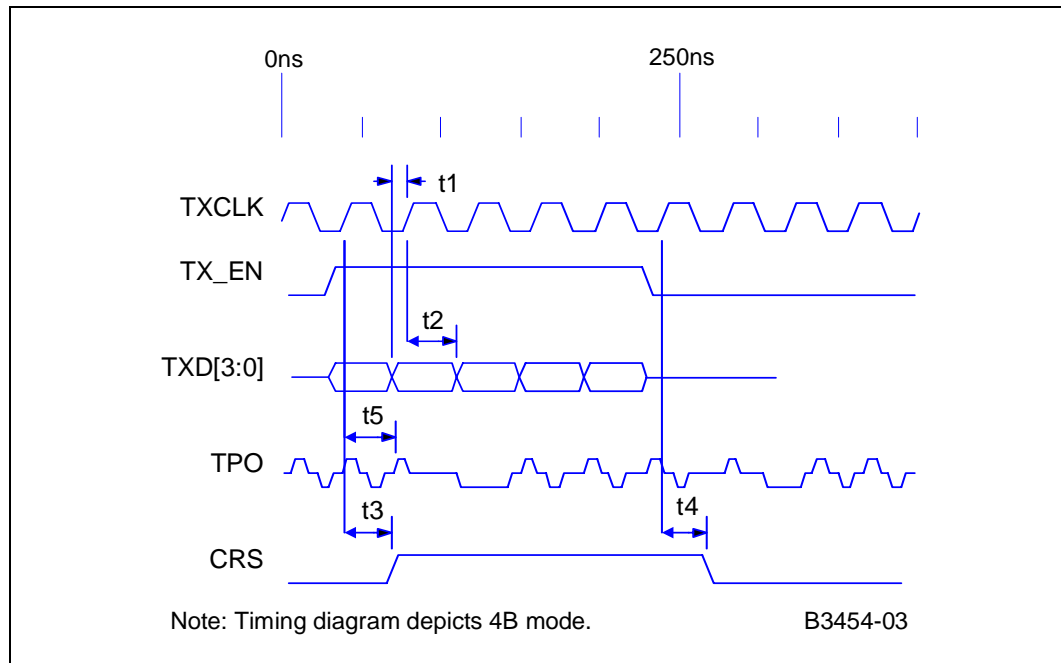
Figure 24 does not show the TX_ER signal.

Table 31. Intel® LXT972A Transceiver 100BASE-TX Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD[3:0], TX_EN, TX_ER setup to TX_CLK High	t1	12	–	–	ns	–
TXD[3:0], TX_EN hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	20	–	24	BT	–
TX_EN sampled to CRS de-asserted	t4	24	–	28	BT	–
TX_EN sampled to TPO out (Tx latency)	t5	5.3	–	5.7	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = 10^{-8} s or 10 ns.

Figure 25. Intel® LXT972A Transceiver 10BASE-T Receive Timing

B3457-01
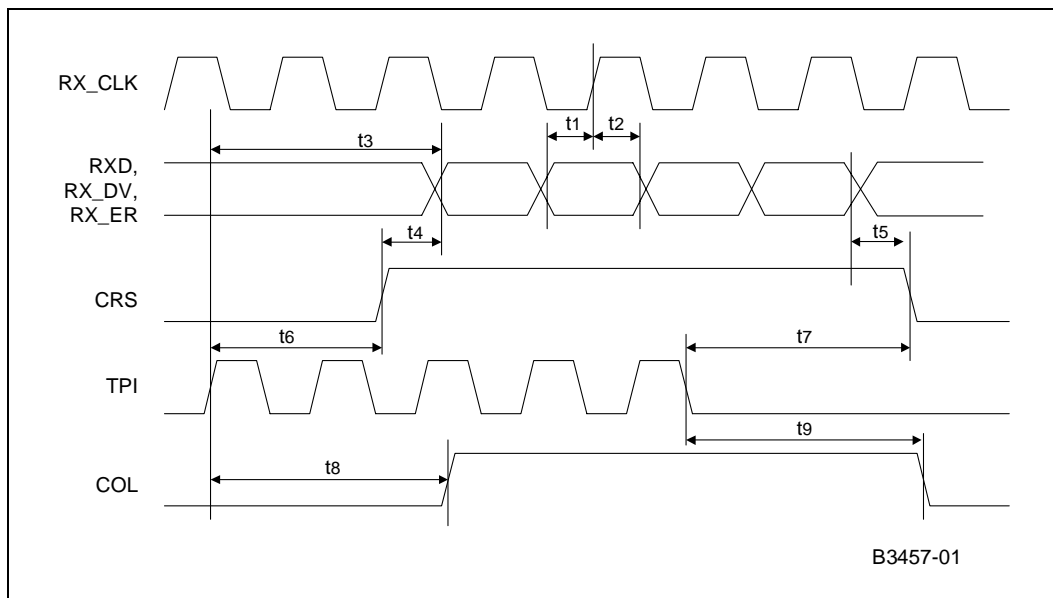
Table 32. Intel® LXT972A Transceiver 10BASE-T Receive Timing

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, TX_ER (not shown in figure). Setup to RX_CLK High	t1	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	10	–	–	ns	–
TPIP/N in to RXD out (Rx latency)	t3	4.2	–	6.6	BT	–
CRS asserted to RXD, RX_DV, RX_ER asserted	t4	5	–	32	BT	–
RXD, RX_DV, RX_ER de-asserted to CRS de-asserted	t5	0.3	–	0.5	BT	–
TPI in to CRS asserted	t6	2	–	28	BT	–
TPI quiet to CRS de-asserted	t7	6	–	10	BT	–
TPI in to COL asserted	t8	1	–	31	BT	–
TPI quiet to COL de-asserted	t9	5	–	10	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = 10^{-7} s or 100 ns.

Figure 26. Intel® LXT972A Transceiver 10BASE-T Transmit Timing

B3460-01
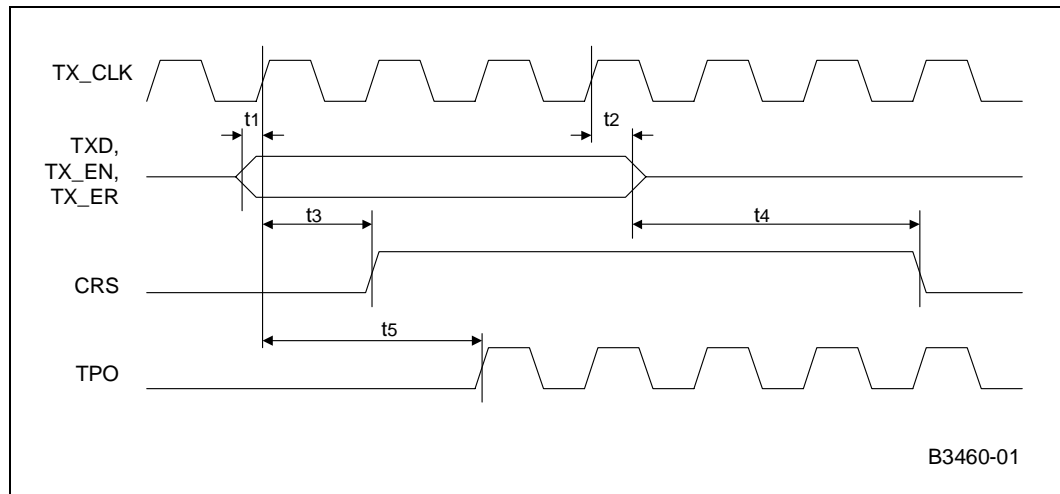
Table 33. Intel® LXT972A Transceiver 10BASE-T Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER setup to TX_CLK High	t1	10	–	–	ns	–
TXD, TX_EN, TX_ER hold from TX_CLK High	t2	0	–	–	ns	–
TX_EN sampled to CRS asserted	t3	–	2	–	BT	–
TX_EN sampled to CRS de-asserted	t4	–	1	–	BT	–
TX_EN sampled to TPO out (Tx latency)	t5	–	72.5	–	BT	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.
2. BT (Bit Time) is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = 10^{-7} s or 100 ns.

Figure 27. Intel® LXT972A Transceiver 10BASE-T Jabber and Unjabber Timing

B3455-01
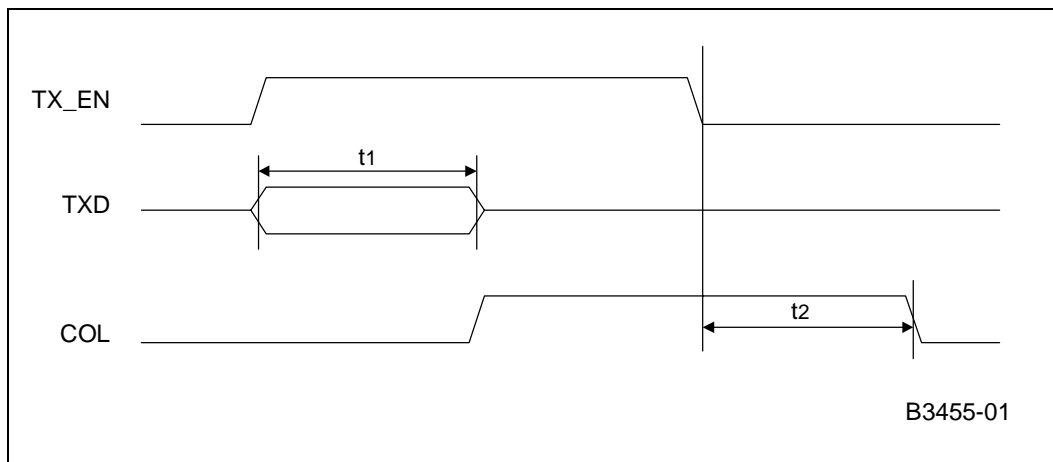
Table 34. Intel® LXT972A Transceiver 10BASE-T Jabber and Unjabber Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Maximum transmit time	t1	20	–	150	ms	–
Unjabber time	t2	250	–	750	ms	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 28. Intel® LXT972A Transceiver 10BASE-T SQE (Heartbeat) Timing

B3458-01
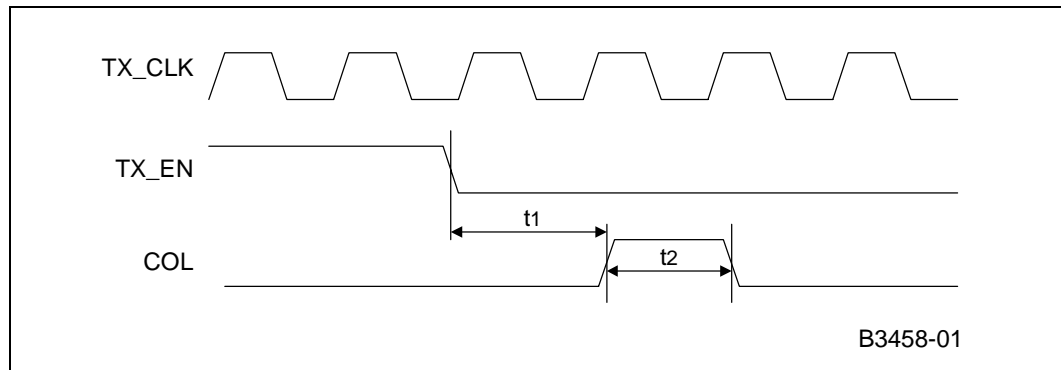
Table 35. Intel® LXT972A Transceiver 10BASE-T SQE (Heartbeat) Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) Delay after TX_EN off	t1	0.65	–	1.6	us	–
COL (SQE) Pulse duration	t2	0.5	–	1.5	us	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 29. Intel® LXT972A Transceiver Auto-Negotiation and Fast Link Pulse Timing

B3464-01
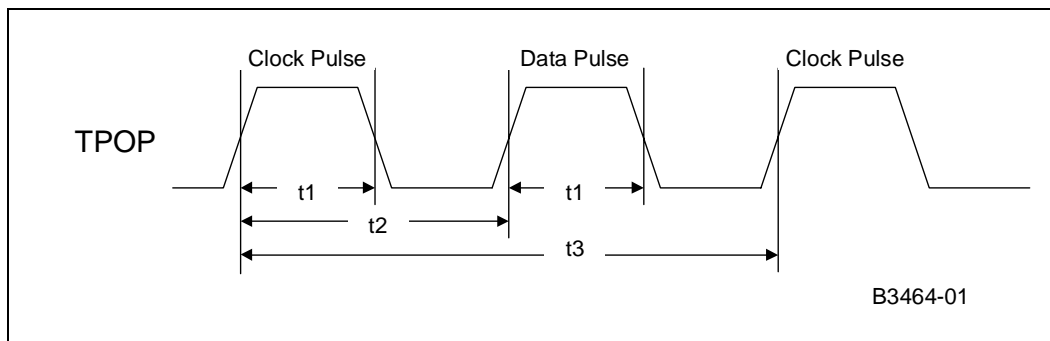
Figure 30. Intel® LXT972A Transceiver Fast Link Pulse Timing

B3465-01
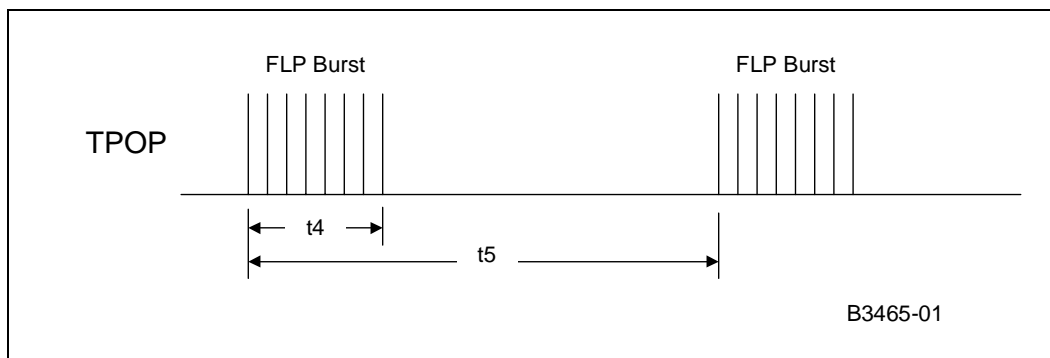
Table 36. Intel® LXT972A Transceiver Auto-Negotiation / Fast Link Pulse Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	63.8	µs	–
Clock pulse to Clock pulse	t3	123	–	127	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	12	24	ms	–
Clock/Data pulses per burst	–	17	–	33	Each clock pulse or data pulse	–

1. Typical values are at 25 °C and are for design aid only, not guaranteed, and not subject to production testing.

Figure 31. Intel® LXT972A Transceiver MDIO Input Timing
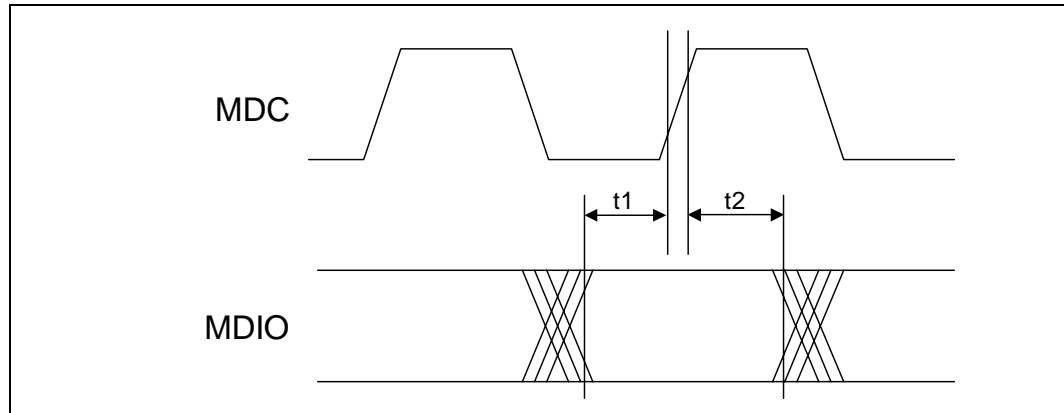
Figure 32. Intel® LXT972A Transceiver MDIO Output Timing
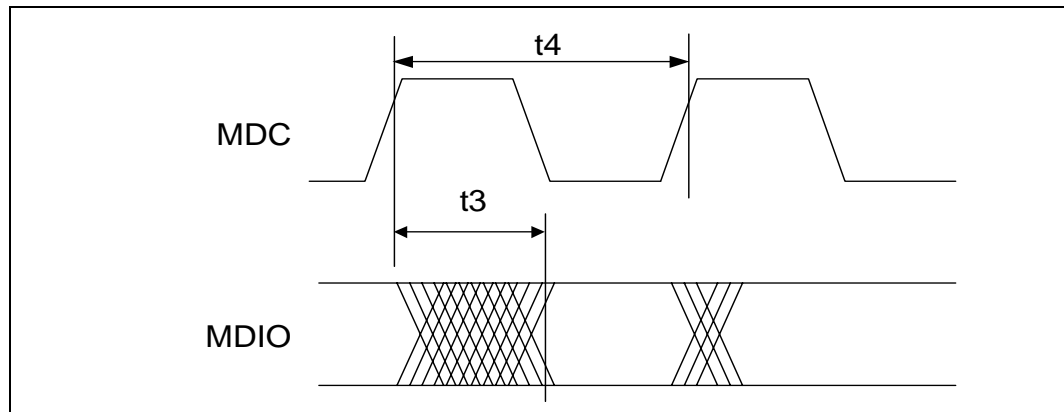
Table 37. Intel® LXT972A Transceiver MDIO Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	–
MDIO hold after MDC, sourced by STA	t2	5	–	–	ns	–
MDC to MDIO output delay, sourced by PHY	t3	–	–	150	ns	–
MDC period	t4	125	–	–	ns	MDC = 8 MHz
1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.						

Figure 33. Intel® LXT972A Transceiver Power-Up Timing

B3494-01
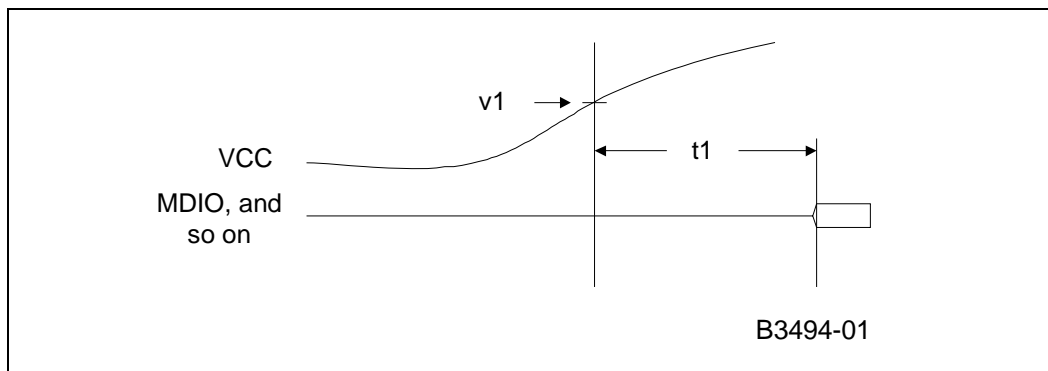
Table 38. Intel® LXT972A Transceiver Power-Up Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	–	2.9	–	V	–
Power Up delay[2]	t1	–	–	300	µs	–

1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.
2. Power-up delay is specified as a maximum value because it refers to the PHY guaranteed performance. The PHY comes out of reset after a delay of no more than 300 µs. System designers should consider this value as a minimum value. After threshold v1 is reached, the MAC should delay no less than 300 µs before accessing the MDIO port.

Figure 34. Intel® LXT972A Transceiver RESET_L Pulse Width and Recovery Timing

B3495-01
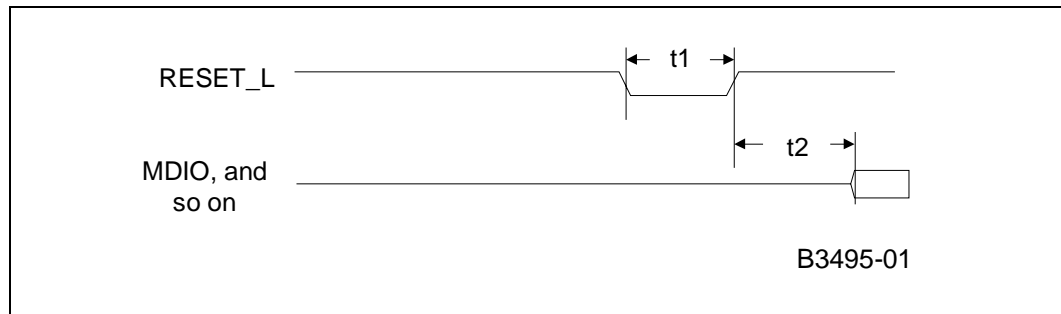
Table 39. Intel® LXT972A Transceiver RESET_L Pulse Width and Recovery Timing

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
RESET_L pulse width	t1	10	–	–	ns	–
RESET_L recovery delay[2]	t2	–		300	µs	–

1. Typical values are at 25° C and are for design aid only, not guaranteed, and not subject to production testing.
2. Reset Recovery Delay is specified as a maximum value because it refers to the PHY guaranteed performance. The PHY comes out of reset after a delay of no more than 300 µs. System designers should consider this value as a minimum value. After de-asserting RESET_L, the MAC should delay no less than 300 µs before accessing the MDIO port.

8.0 Register Definitions - IEEE Base Registers

This chapter includes definitions for the IEEE base registers used by the LXT972A Transceiver. Chapter 9.0, "Register Definitions - Product-Specific Registers" includes definitions of additional product-specific LXT972A Transceiver registers, which are defined in accordance with the IEEE 802.3 standard for adding unique device functions.

The LXT972A Transceiver register set has multiple 16-bit registers.

- Table 40 is a register set listing of the IEEE base registers.
- Table 41 through Table 49 provide bit descriptions of the base registers (address 0 through 8), which are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 standard.

Table 40. Register Set for IEEE Base Registers

Address	Register Name	Bit Assignments
0	Control Register	See Table 41
1	Status Register #1	See Table 42.
2	PHY Identification Register 1	See Table 43.
3	PHY Identification Register 2	See Table 44.
4	Auto-Negotiation Advertisement Register	See Table 45
5	Auto-Negotiation Link Partner Base Page Ability Register	See Table 46.
6	Auto-Negotiation Expansion Register	See Table 47.
7	Auto-Negotiation Next Page Transmit Register	See Table 48.
8	Auto-Negotiation Link Partner Next Page Receive Register	See Table 49.
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
11 to 14	Reserved	Not Implemented
15	Extended Status Register	Not Implemented

Table 41 lists control register bits.

Table 41. Control Register - Address 0, Hex 0

Bit	Name	Description			Type [1]	Default
0.15	Reset	0 = Normal operation 1 = PHY reset			R/W SC	0
0.14	Loopback	0 = Disable loopback mode 1 = Enable loopback mode			R/W	0
0.13	Speed Selection	0.6	0.13	Speed Selected	R/W	Note 2
		0	0	10 Mbps		
		0	1	100 Mbps		
		1	0	1000 Mbps (not supported)		
		1	1	Reserved		
0.12	Auto-Negotiation Enable	0 = Disable auto-negotiation process 1 = Enable auto-negotiation process			R/W	Note 2
0.11	Power-Down	0 = Normal operation 1 = Power-down			R/W	0
0.10	Isolate	0 = Normal operation 1 = Electrically isolate PHY from MII			R/W	0
0.9	Restart Auto-Negotiation	0 = Normal operation 1 = Restart auto-negotiation process			R/W SC	0
0.8	Duplex Mode	0 = Half-duplex 1 = Full-duplex			R/W	Note 2
0.7	Collision Test	0 = Disable COL signal test 1 = Enable COL signal test			R/W	0
0.6	Speed Selection	0.6	0.13	Speed Selected	R/W	0
		0	0	10 Mbps		
		0	1	100 Mbps		
		1	0	1000 Mbps (not supported)		
		1	1	Reserved		
0.5:0	Reserved	Write as '0'. Ignore on Read.			R/W	00000

1. R/W = Read/Write
   SC = Self Clearing
2. Some bits have their default values determined at reset by hardware configuration pins. For default details for these bits, see Section 5.4.4, "Hardware Configuration Settings".

Table 42 lists MII status register bits.

Table 42. MII Status Register #1 - Address 1, Hex 1

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4 Not Supported	0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full-Duplex	0 = PHY not able to perform full-duplex 100BASE-X 1 = PHY able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half-Duplex	0 = PHY not able to perform half-duplex 100BASE-X 1 = PHY able to perform half-duplex 100BASE-X	RO	1
1.12	10 Mbps Full-Duplex	0 = PHY not able to operate at 10 Mbps full-duplex mode 1 = PHY able to operate at 10 Mbps in full-duplex mode	RO	1
1.11	10 Mbps Half-Duplex	0 = PHY not able to operate at 10 Mbps in half-duplex 1 = PHY able to operate at 10 Mbps in half-duplex mode	RO	1
1.10	100BASE-T2 Full-Duplex Not Supported	0 = PHY not able to perform full-duplex 100BASE-T2 1 = PHY able to perform full-duplex 100BASE-T2	RO	0
1.9	100BASE-T2 Half-Duplex Not Supported	0 = PHY not able to perform half-duplex 100BASE-T2 1 = PHY able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	0 = No extended status information in register 15 1 = Extended status information in register 15	RO	0
1.7	Reserved	Ignore when read.	RO	0
1.6	MF Preamble Suppression	0 = PHY cannot accept management frames with preamble suppressed 1 = PHY accepts management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	0 = Auto-negotiation not complete 1 = Auto-negotiation complete	RO	0
1.4	Remote Fault	0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0
1.3	Auto-Negotiation Ability	0 = PHY is not able to perform auto-negotiation 1 = PHY is able to perform auto-negotiation	RO	1
1.2	Link Status	0 = Link is down 1 = Link is up	RO/LL	0
1.1	Jabber Detect	0 = Jabber condition not detected 1 = Jabber condition detected	RO/LH	0
1.0	Extended Capability	0 = Basic register capabilities 1 = Extended register capabilities	RO	1
1. RO = Read Only LL = Latching Low LH = Latching High				

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For Table 43 and Table 44, see Figure 35.

Table 43. PHY Identification Register 1 - Address 2, Hex 2

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier is composed of bits 3 through 18 of the Organizationally Unique Identifier (OUI).	RO	0013 hex
1. RO = Read Only				

Table 44. PHY Identification Register 2 - Address 3, Hex 3

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier is composed of bits 19 through 24 of the OUI.	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	001110
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	For current revision ID information, see the Specification Update.
1. RO = Read Only				

Figure 35. PHY Identifier Bit Mapping
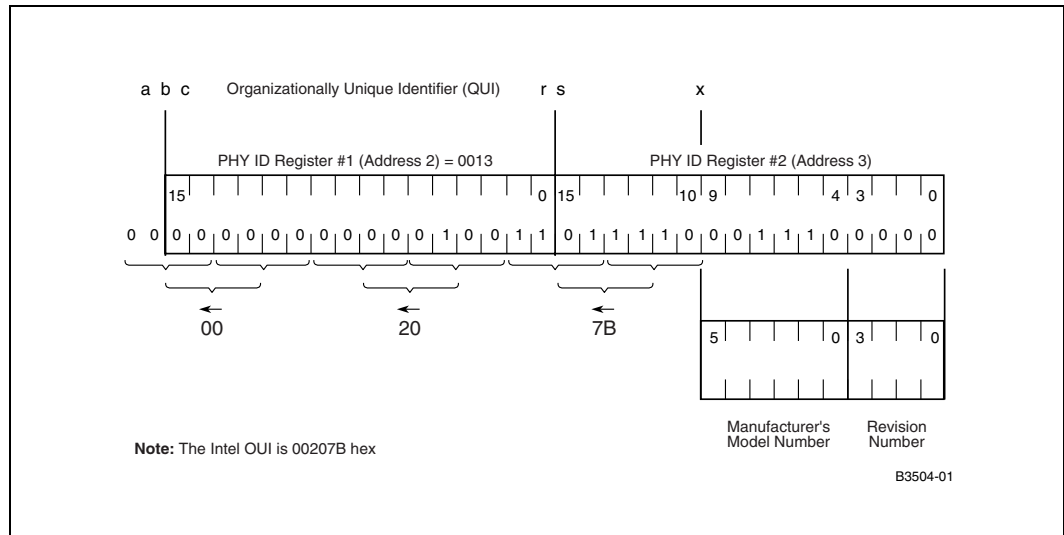
Table 45 lists auto-negotiation advertisement bits.

Table 45. Auto-Negotiation Advertisement Register - Address 4, Hex 4

Bit	Name	Description	Type [1]	Default
4.15	Next Page	0 = Port has no ability to send multiple pages. 1 = Port has ability to send multiple pages.	R/W	0
4.14	Reserved	Ignore when read.	RO	0
4.13	Remote Fault	0 = No remote fault. 1 = Remote fault.	R/W	0
4.12	Reserved	Write as '0'. Ignore on Read.	R/W	0
4.11	Asymmetric Pause	Pause operation defined in IEEE 802.3 Standard, Clause 40 and 27	R/W	0
4.10	Pause	0 = Pause operation disabled. 1 = Pause operation enabled for full-duplex link.	R/W	Note 2
4.9	100BASE-T4	0 = 100BASE-T4 capability is not available. 1 = 100BASE-T4 capability is available. **NOTE:** The LXT972A Transceiver does not support 100BASE-T4 but allows this bit to be set to advertise in the auto-negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 Transceiver can be switched in if this capability is desired.	R/W	0
4.8	100BASE-TX full-duplex (For LXT972A Transceiver)	0 = Port is not 100BASE-TX full-duplex capable. 1 = Port is 100BASE-TX full-duplex capable.	R/W	Note 3
4.7	100BASE-TX (For LXT972A Transceiver)	0 = Port is not 100BASE-TX capable. 1 = Port is 100BASE-TX capable.	R/W	Note 3
4.6	10BASE-T full-duplex (For LXT972A Transceiver)	0 = Port is not 10BASE-T full-duplex capable. 1 = Port is 10BASE-T full-duplex capable.	R/W	Note 3
4.5	10BASE-T	0 = Port is not 10BASE-T capable. 1 = Port is 10BASE-T capable.	R/W	Note 3
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future auto-negotiation development. <11111> = Reserved for future auto-negotiation development. **NOTE:** Unspecified or reserved combinations must not be transmitted.	R/W	00001

1. R/W = Read/Write
RO = Read Only
2. Default setting is determined by pin 33 at reset.
3. Some bits have their default values determined at reset by hardware configuration pins. For default details for these bits, see Section 5.4.4, "Hardware Configuration Settings".

Table 46 lists auto-negotiation link partner base page ability bits.

Table 46. Auto-Negotiation Link Partner Base Page Ability Register - Address 5, Hex 5

Bit	Name	Description	Type [1]	Default
5.15	Next Page	0 = Link Partner has no ability to send multiple pages. 1 = Link Partner has ability to send multiple pages.	RO	0
5.14	Acknowledge	0 = Link Partner has not received Link Code Word from the LXT972A Transceiver. 1 = Link Partner has received Link Code Word from the LXT972A Transceiver.	RO	0
5.13	Remote Fault	0 = No remote fault. 1 = Remote fault.	RO	0
5.12	Reserved	Ignore when read.	RO	0
5.11	Asymmetric Pause	Pause operation defined in IEEE 802.3 Standard, Clause 40 and 27. 0 = Link Partner is not Pause capable. 1 = Link Partner is Pause capable.	RO	0
5.10	Pause	0 = Link Partner is not Pause capable. 1 = Link Partner is Pause capable.	RO	0
5.9	100BASE-T4	0 = Link Partner is not 100BASE-T4 capable. 1 = Link Partner is 100BASE-T4 capable.	RO	0
5.8	100BASE-TX Full-Duplex	0 = Link Partner is not 100BASE-TX full-duplex capable. 1 = Link Partner is 100BASE-TX full-duplex capable.	RO	0
5.7	100BASE-TX	0 = Link Partner is not 100BASE-TX capable. 1 = Link Partner is 100BASE-TX capable.	RO	0
5.6	10BASE-T Full-Duplex	0 = Link Partner is not 10BASE-T full-duplex capable. 1 = Link Partner is 10BASE-T full-duplex capable.	RO	0
5.5	10BASE-T	0 = Link Partner is not 10BASE-T capable. 1 = Link Partner is 10BASE-T capable.	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future auto-negotiation development. <11111> = Reserved for future auto-negotiation development. Unspecified or reserved combinations must not be transmitted.	RO	0
1. RO = Read Only				

Table 47 lists auto-negotiation expansion bits.

Table 47. Auto-Negotiation Expansion - Address 6, Hex 6

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore when read.	RO	0
6.5	Base Page	This bit indicates the status of the auto-negotiation variable base page. It flags synchronization with the auto-negotiation state diagram, allowing detection of interrupted links. This bit is used only if Register bit 16.1 (that is, Alternate NP feature) is set. 0 = Base page = False (base page not received) 1 = Base page = True (base page received)	RO/LH	0
6.4	Parallel Detection Fault	0 = Parallel detection fault has not occurred. 1 = Parallel detection fault has occurred.	RO/LH	0
6.3	Link Partner Next Page Able	0 = Link partner is not next page able. 1 = Link partner is next page able.	RO	0
6.2	Next Page Able	0 = Local device is not next page able. 1 = Local device is next page able.	RO	1
6.1	Page Received	This bit is cleared on Read. If Register bit 16.1 is set, the Page Received bit is also cleared when either mr_page_rx = false or transmit_disable = true. 1 = Indicates a new page is received and the received code word is loaded into Register 5 (Base Pages) or Register 8 (Next Pages) as specified in Clause 28 of IEEE 802.3.	RO/LH	0
6.0	Link Partner A/N Able	0 = Link partner is not auto-negotiation able. 1 = Link partner is auto-negotiation able.	RO	0
1. RO = Read Only LH = Latching High				

Table 48 lists auto-negotiation next page transmit bits.

Table 48. Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	0 = Last page 1 = Additional next pages follow	R/W	0
7.14	Reserved	Ignore when read.	RO	0
7.13	Message Page (MP)	0 = Register bits 7.10:0 are user defined. 1 = Register bits 7.10.0 follow IEEE message page format.	R/W	1
7.12	Acknowledge 2 (ACK2)	0 = Cannot comply with message 1 = Complies with message	R/W	0
7.11	Toggle (T)	0 = Previous value of the transmitted Link Code Word equalled logic one 1 = Previous value of the transmitted Link Code Word equalled logic zero	R/W	0
7.10:0	Message/ Unformatted Code Field	If Register bits 7.13 = 0, Register bits 7.10:0 are user-defined. If Register bits 7.13 = 1, Register bits 7.10:0 follow IEEE message page format.	R/W	00000000 001
1. RO = Read Only. R/W = Read/Write				

Table 49 lists auto-negotiation link partner next page receive bits.

Table 49. Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	0 = Link Partner has no additional next pages to send 1 = Link Partner has additional next pages to send	RO	0
8.14	Acknowledge (ACK)	0 = Link Partner has not received Link Code Word from LXT972A Transceiver. 1 = Link Partner has received Link Code Word from LXT972A Transceiver.	RO	0
8.13	Message Page (MP)	0 = Register bits 8.10:0 are user defined. 1 = Register bits 8.10:0 follow IEEE message page format.	RO	0
8.12	Acknowledge 2 (ACK2)	0 = Link Partner cannot comply with the message 1 = Link Partner complies with the message	RO	0
8.11	Toggle (T)	0 = Previous value of transmitted Link Code Word equal to logic one 1 = Previous value of transmitted Link Code Word equal to logic zero	RO	0
8.10:0	Message/Unformatted Code Field	If Register bit 8.13 = 0, Register bits 18.10:0 are user defined. If Register bit 8.13 = 1, Register bits 18.10:0 follow IEEE message page format.	RO	000000 0000
1. RO = Read Only.				

9.0 Register Definitions - Product-Specific Registers

This chapter includes definitions of product-specific LXT972A Transceiver registers that are defined in accordance with the IEEE 802.3 standard for adding unique device functions. (For definitions of the IEEE base registers used by the LXT972A Transceiver, see Chapter 8.0, "Register Definitions - IEEE Base Registers".)

- Table 50 lists the register set of the product-specific registers.
- Table 51 through Table 56 provide bit descriptions of the product-specific registers (address 17 through 30).

Table 50. Register Set for Product-Specific Registers

Address	Register Name	Bit Assignments
16	Port Configuration Register	See Table 51
17	Status Register #2	See Table 52
18	Interrupt Enable Register	See Table 53
19	Status Change Register	See Table 54
20	LED Configuration Register	See Table 55
21	Reserved	
22-25	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Transmit Control Register	See Table 56
31	Reserved	

Table 51 lists configuration bits.

Table 51. Configuration Register - Address 16, Hex 10

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.14	Force Link Pass	0 = Normal operation 1 = Force Link pass	R/W	0
16.13	Transmit Disable	0 = Normal operation 1 = Disable Twisted Pair transmitter	R/W	0
16.12	Bypass Scrambler (100BASE-TX)	0 = Normal operation 1 = Bypass Scrambler and Descrambler	R/W	0
16.11	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.10	Jabber (10BASE-T)	0 = Normal operation 1 = Disable Jabber Correction	R/W	0
16.9	SQE (10BASE-T)	0 = Disable Heart Beat 1 = Enable Heart Beat	R/W	0
16.8	TP Loopback (10BASE-T)	0 = Normal operation 1 = Disable TP loopback during half-duplex operation	R/W	0
16.7	CRS Select (10BASE-T)	0 = Normal Operation 1 = CRS deassert extends to RX_DV deassert	R/W	1
16.6	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.5	PRE_EN	Preamble Enable. 0 = Set RX_DV high coincident with SFD. 1 = Set RX_DV high and RXD = preamble when CRS is asserted. **NOTE:** Preamble is always enabled in 100 Mbps operation.	R/W	0
16.4:3	Reserved	Write as '0'. Ignore on Read.	R/W	00
16.2	Reserved	Write as '0'. Ignore on Read.	R/W	0
16.1	Alternate NP feature	0 = Disable alternate auto negotiate next page feature. 1 = Enable alternate auto negotiate next page feature. This bit enables or disables the register bit 6.5 capability.	R/W	0
16.0	Reserved	Write as '0'. Ignore on Read.	R/W	0
1. R/W = Read /Write				

Table 52 lists register #2 status bits.

Table 52. Status Register #2 - Address 17, Hex 11

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0.	RO	0
17.14	10/100 Mode	0 = LXT972A Transceiver is not operating 100BASE-TX mode. 1 = LXT972A Transceiver is operating in 100BASE-TX mode.	RO	0
17.13	Transmit Status	0 = LXT972A Transceiver is not transmitting a packet. 1 = LXT972A Transceiver is transmitting a packet.	RO	0
17.12	Receive Status	0 = LXT972A Transceiver is not receiving a packet. 1 = LXT972A Transceiver is receiving a packet.	RO	0
17.11	Collision Status	0 = No collision. 1 = Collision is occurring.	RO	0
17.10	Link	0 = Link is down. 1 = Link is up.	RO	0
17.9	Duplex Mode	0 = Half-duplex. 1 = Full-duplex.	RO	0
17.8	Auto-Negotiation	0 = LXT972A Transceiver is in manual mode. 1 = LXT972A Transceiver is in auto-negotiation mode.	RO	0
17.7	Auto-Negotiation Complete	0 = Auto-negotiation process not completed. 1 = Auto-negotiation process completed. This bit is valid only when auto negotiate is enabled. The value is equivalent to the value of Register bit 1.5.	RO	0
17.6	Reserved	Always 0.	RO	0
17.5	Polarity	0 = Polarity is not reversed. 1 = Polarity is reversed. **NOTE:** Polarity is not a valid status in 100 Mbps mode.	RO	0
17.4	Pause	0 = The LXT972A Transceiver is not Pause capable. 1 = The LXT972A Transceiver is Pause capable.	R	0
17:3	Error	0 = No error occurred 1 = Error occurred (Remote Fault, jabber, parallel detect fault) **NOTE:** The register bit is cleared when the registers that generate the error condition are read.	RO	0
17:2	Reserved	Always 0.	RO	0
17:1	Reserved	Always 0.	RO	0
17:0	Reserved	Always 0.	RO	0
1. RO = Read Only. R/W = Read/Write				

Table 53 lists interrupt enable bits.

Table 53. Interrupt Enable Register - Address 18, Hex 12

Bit	Name	Description	Type [1]	Default
18.15:9	Reserved	Write as '0'. Ignore on Read.	R/W	N/A
18.8	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.7	ANMSK	Mask for Auto Negotiate Complete 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 0 = Do not allow event to cause interrupt. 1 = Enable event to cause interrupt.	R/W	0
18.3	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.2	Reserved	Write as '0'. Ignore on Read.	R/W	0
18.1	INTEN	Interrupt Enable. 0 = Disable interrupts. 1 = Enable interrupts.	R/W	0
18.0	TINT	Test Force Interrupt 0 = Normal operation. 1 = Force interrupt on MDINT_L	R/W	0
1. R/W = Read /Write				

Table 54 lists status change bits.

Table 54. Status Change Register - Address 19, Hex 13

Bit	Name	Description	Type [1]	Default
19.15:9	Reserved	Ignore on Read.	RO	N/A
19.8	Reserved	Ignore on Read.	RO	0
19.7	ANDONE	Auto-negotiation Status 0 = Auto-negotiation has not completed. 1 = Auto-negotiation has completed.	RO/SC	N/A
19.6	SPEEDCHG	Speed Change Status 0 = A Speed Change has not occurred since last reading this register. 1 = A Speed Change has occurred since last reading this register.	RO/SC	0
19.5	DUPLEXCHG	Duplex Change Status 0 = A Duplex Change has not occurred since last reading this register. 1 = A Duplex Change has occurred since last reading this register.	RO/SC	0
19.4	LINKCHG	Link Status Change Status 0 = A Link Change has not occurred since last reading this register. 1 = A Link Change has occurred since last reading this register.	RO/SC	0
19.3	Reserved	Ignore on Read.	RO	0
19.2	MDINT_L	Management data interrupt (MII interrupt) Status. 0 = No MII interrupt pending. 1 = MII interrupt pending.	RO	0
19.1	Reserved	Ignore on Read.	RO	0
19.0	Reserved	Ignore on Read.	RO	0
1. R/W = Read/Write, RO = Read Only, SC = Self Clearing.				

Table 55 lists LED configuration bits.

Table 55. LED Configuration Register - Address 20, Hex 14 (Sheet 1 of 2)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default) 0001 = Display Transmit Status (Stretched) 0010 = Display Receive Status (Stretched) 0011 = Display Collision Status (Stretched) 0100 = Display Link Status (Continuous) 0101 = Display Duplex Status (Continuous) 0110 = Unused 0111 = Display Receive or Transmit Activity (Stretched) 1000 = Test mode - turn LED on (Continuous) 1001 = Test mode - turn LED off (Continuous) 1010 = Test mode - blink LED fast (Continuous) 1011 = Test mode - blink LED slow (Continuous) 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status 0011 = Display Collision Status 0100 = Display Link Status (Default) 0101 = Display Duplex Status 0110 = Unused 0111 = Display Receive or Transmit Activity 1000 = Test mode - turn LED on 1001 = Test mode - turn LED off 1010 = Test mode - blink LED fast 1011 = Test mode - blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0100

1. R/W = Read /Write. RO = Read Only. LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
   Activity causes the LED to blink, regardless of the link status.
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings
   are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are approximations. Not guaranteed or production tested.

Table 55. LED Configuration Register - Address 20, Hex 14 (Sheet 2 of 2)

Bit	Name	Description	Type [1]	Default
20.7:4	LED3 Programming bits	0000 = Display Speed Status 0001 = Display Transmit Status 0010 = Display Receive Status (Default) 0011 = Display Collision Status 0100 = Display Link Status 0101 = Display Duplex Status 0110 = Unused 0111 = Display Receive or Transmit Activity 1000 = Test mode- turn LED on 1001 = Test mode- turn LED off 1010 = Test mode- blink LED fast 1011 = Test mode- blink LED slow 1100 = Display Link and Receive Status combined [2] (Stretched)[3] 1101 = Display Link and Activity Status combined [2] (Stretched)[3] 1110 = Display Duplex and Collision Status combined [4] (Stretched)[3] 1111 = Unused	R/W	0010
20.3:2	LEDFREQ[5]	00 = Stretch LED events to 30 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00
20.1	PULSE-STRETCH	0 = Disable pulse stretching of all LEDs. 1 = Enable pulse stretching of all LEDs.	R/W	1
20.0	Reserved	Write as '0'. Ignore on Read.	R/W	0

1. R/W = Read /Write. RO = Read Only. LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
   Activity causes the LED to blink, regardless of the link status.
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are approximations. Not guaranteed or production tested.

Table 56 lists transmit control bits.

Table 56. Transmit Control Register - Address 30, Hex 1E

Bit	Name	Description	Type[2]	Default
30.15:13	Reserved	Write as '0'. Ignore on Read.	R/W	000
30.12	Transmit Low Power	Transmit Low Power 0 = Normal transmission. 1 = Forces the transmitter into low power mode. Also forces a zero-differential transmission.	R/W	0
30.11:10	Port Rise Time Control[1]	Port Rise Time Control 00 = 3.0 ns (Default = Setting on TXSLEW[1:0] pins) 01 = 3.4 ns 10 = 3.9 ns 11 = 4.4 ns	R/W	Note 3
30.9:0	Reserved	Ignore on Read.	R/W	0000000000

1. Values are approximations and may vary outside indicated values based upon implementation loading conditions. Not guaranteed.
2. R/W = Read/Write
3. Latch State during Reset is based on the state of hardware configuration pins at RESET_L.

10.0   Intel® LXT972A Transceiver Package Specifications

Figure 36. Intel® LXT972A Transceiver LQFP Package Specifications

64-Pin Low-Profile Quad Flat Pack

NOTE: The package figure is generic and used only to demonstrate package dimensions. (The figure does not show the same number of pins as for the Intel® LXT972A Transceiver LQFP.)

Dim	Millimeters	
	Min	**Max**
A	–	1.60
A_1	0.05	0.15
A_2	1.35	1.45
B	0.17	0.27
D	11.85	12.15
D_1	9.9	10.1
E	11.85	12.15
E_1	9.9	10.1
e	0.50 BSC[1]	
L	0.45	0.75
L_1	1.00 REF	
θ_3	11°	13°
θ	0°	7°

1. Basic Spacing between Centers

Datasheet
Document Number: 249186-004
Revision Date: 25-Oct-2005

10.1   Top Label Markings

Figure 37 shows a sample LQFP package for the LXT972A Transceiver.

Note: In contrast to the Pb-Free (RoHS-compliant) LQFP package, the non-RoHS-compliant package does not have the "e3" symbol in the last line of the package label.

Figure 37. Sample LQFP Package - Intel® LXT972A Transceiver
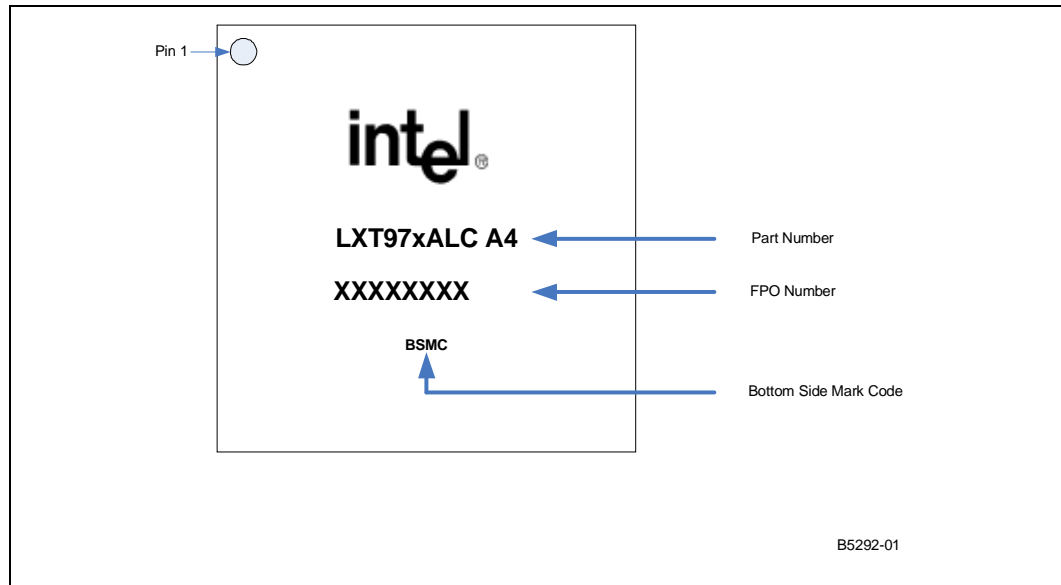
Figure 38 shows a sample Pb-Free (RoHS-compliant) LQFP package for the LXT972A Transceiver.

Figure 38.   Sample Pb-Free (RoHS-Compliant) LQFP Package - Intel® LX972A Transceiver
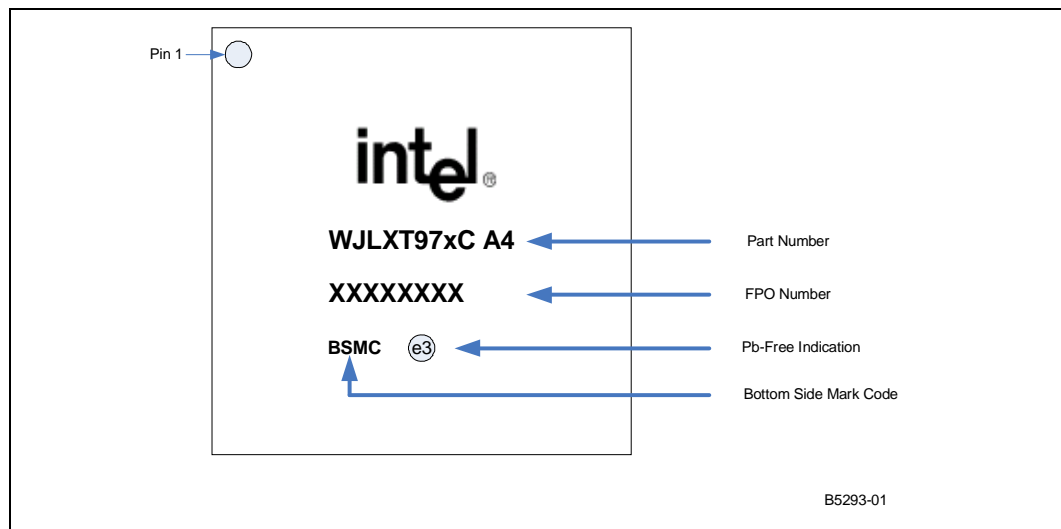
11.0   Product Ordering Information

Table 57 lists product ordering information for the LXT972A Transceiver.

Table 57.   Product Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT972ALC.A4	A4	LQFP	64	No
WJLXT972ALC.A4	A4	LQFP	64	Yes

Figure 39 shows an order matrix with sample information for ordering an LXT972A Transceiver.

Figure 39. Order Matrix for Intel® LXT972A Transceiver

DJ LXT 972A L C A4

Product Revision
xn = 2 Alphanumeric characters

Temperature Range
A = Ambient (0 – 55^0 C)
C = Commercial (0 – 70^0 C)
E = Extended (-40 – 85^0 C)
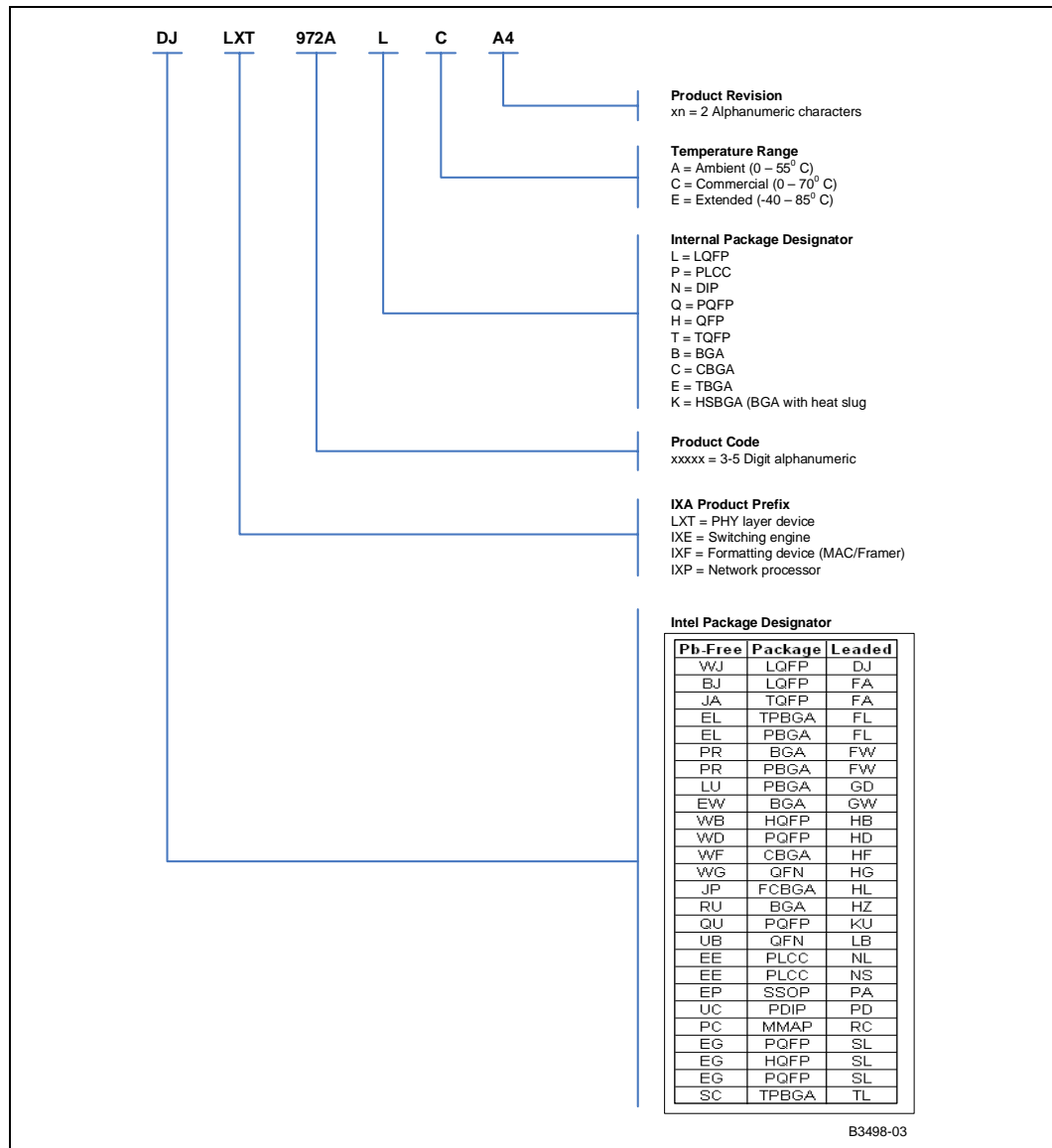
Internal Package Designator
L = LQFP
P = PLCC
N = DIP
Q = PQFP
H = QFP
T = TQFP
B = BGA
C = CBGA
E = TBGA
K = HSBGA (BGA with heat slug

Product Code
xxxxx = 3-5 Digit alphanumeric

IXA Product Prefix
LXT = PHY layer device
IXE = Switching engine
IXF = Formatting device (MAC/Framer)
IXP = Network processor

Intel Package Designator

Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL

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