SPECIFICATIONS FOR MODULE

CUSTOMER	STD
MODEL	WM-FL042V-RFLWa VER. 01
CUSTOMER APPROVED	

APPROVED BY	CHECKED BY	ORGANIZED BY
LCM 產品部 2011/4/15 黃建民	LCM 產品部 2011/04/15 夏勝華	LCM 產品部 2011/4/15 黃紅艷

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☐ APPROVAL FOR SPECIFICATIONS AND SAMPLE

No.10, Jianguo Rd., Tanzi Dist., Taichung City 42760, Taiwan (R.O.C.)

TEL:886- 4-25318899, FAX: 886- 4-25310868

History of Version

Version	Contents	Date	Note
a1	NEW VERSION	2011.4.15	SPEC.

Contents Page

Absolute Maximum Ratings

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Operating Temperature	TOP	-20	-	+70	℃
Storage Temperature	TST	-30	-	+85	℃
Supply Voltage for Analog	VCI-VSS	-0.3	-	+4.0	V
Supply Voltage for Digital	VDD-VSS	-0.3	-	+3.6	V
Static Electricity	Be sure that you are grounded when handing LCM.				

(1) LCM

1.1 Electrical Characteristics

(Ta=25℃)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage for Analog	VCI	-	2.7	2.8	2.9	V
Supply Voltage for Digital	VDD	-	1.65	1.85	1.95	V
Input Signal High Voltage	VIH	-	0.7VDD	-	VDD	V
Input Signal Low Voltage	VIL	-	0	-	0.3VDD	V
Output Signal High Voltage	VOH	IOH=-1.0mA	0.8VDD	-	VDD	V
Output Signal Low Voltage	VOL	IOL=1.0mA	0	-	0.2VDD	V
Supply Current for Analog	*ICI	-	-	-	TBD.	mA
Supply Current for Digital	*IDD	-	-	-	TBD.	mA

*ICI Measurement condition is for all pixels on
*IDD Measurement condition is for all pixels on

1.2 Interface Pin Function

CN1:

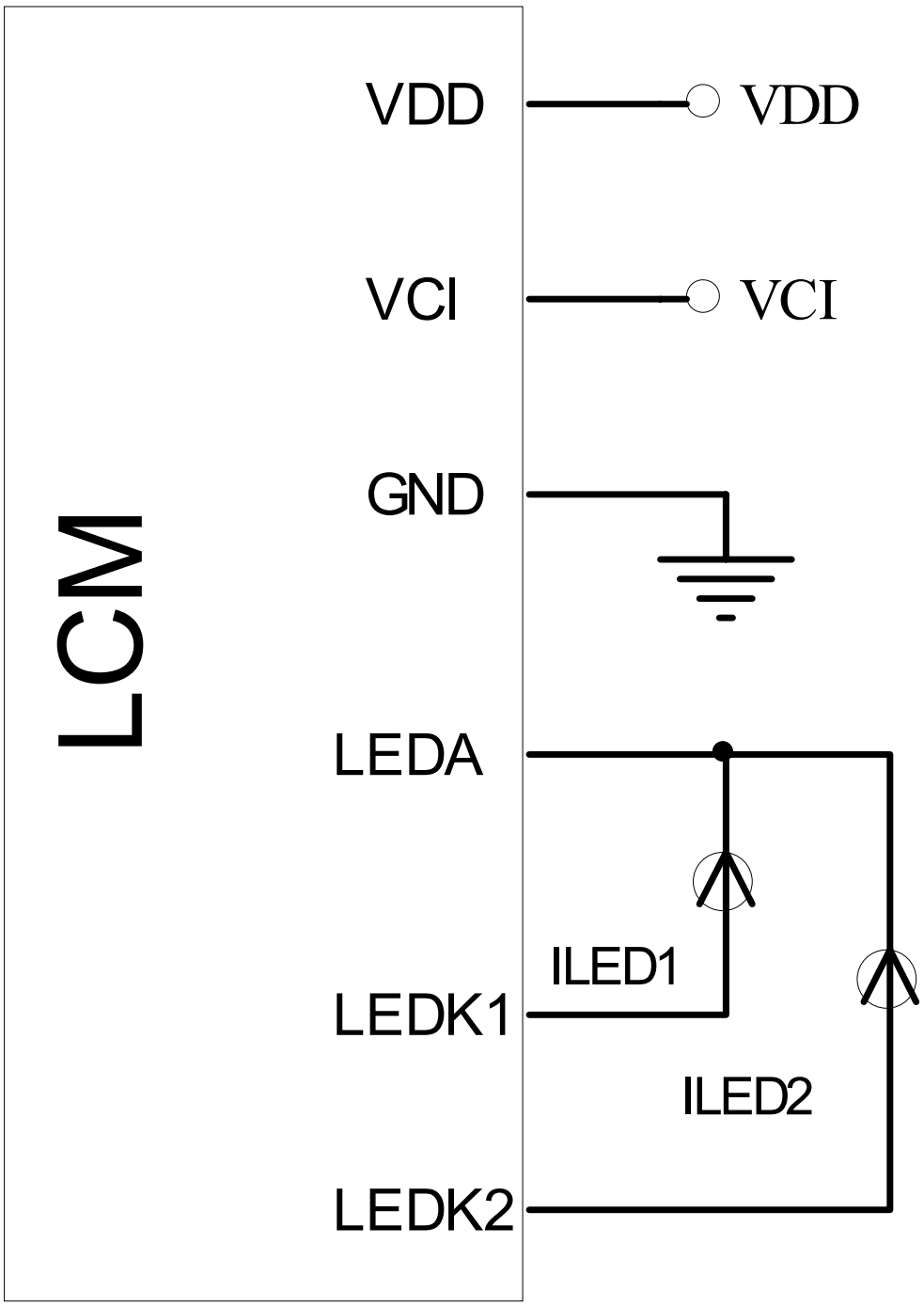
NO	SYMBOL	I / O	FUNCTION
1	GND	P	GND
2	GND	P	GND
3	NC	-	No connection
4	LEDA	P	Anode of LED back light
5	LEDK2	P	Cathode of LED back light
6	LEDK1	P	Cathode of LED back light
7	GND	P	GND
8	VCI	P	Power supply for analog 2.8V
9	NC	-	No connection
10	VDDI	P	Power supply for I/O 1.85V
11	TE	O	Tearing Effect pin
12	SDO	O	Serial data output.
13	SDI	I	Serial data input pin in serial interface operation.
14	WR/SCL	I	Data / Command Selection pin.
15	CSX	I	Chip select signal.
16	RESX	I	Reset pin.
17	DB23	I/O	Date bus
18	DB22	I/O	Date bus
19	DB21	I/O	Date bus
20	DB20	I/O	Date bus
21	DB19	I/O	Date bus
22	DB18	I/O	Date bus
23	DB17	I/O	Date bus
24	DB16	I/O	Date bus
25	DB15	I/O	Date bus
26	DB14	I/O	Date bus
27	DB13	I/O	Date bus
28	DB12	I/O	Date bus

29	DB11	I/O	Date bus
30	DB10	I/O	Date bus
31	DB9	I/O	Date bus
32	DB8	I/O	Date bus
33	DB7	I/O	Date bus
34	DB6	I/O	Date bus
35	DB5	I/O	Date bus
36	DB4	I/O	Date bus
37	DB3	I/O	Date bus
38	DB2	I/O	Date bus
39	DB1	I/O	Date bus
40	DB0	I/O	Date bus
41	DE	I	A data enable signal in RGB I/F mode.
42	PCLK	I	Dot clock signal.
43	HS	I	Line synchronizing signal.
44	VS	I	Serves VS signal pin on RGB interface.
45	LEDPWM	O	Backlight on/fff control pin.
46	NC	-	No connection
47	DCX	I	Command Selection pin
48	RDX	I	Read / Write enable.
49	IM0	I	Select the MPU interface.
50	IM1	I	Select the MPU interface.
51	GND	P	GND

Note:

IM1	IM0	MPU interface mode	DB pins
0	0	DBI TYPE-B 8 bit	DB23-DB8: Unused DB7-DB0: Data
0	1	DBI TYPE-B 9 bit	DB23-DB9: Unused DB8-DB0: Data
1	0	DBI TYPE-B 16 bit	DB23-DB16: Unused DB15-DB0: Data
1	1	DBI TYPE-B 18 bit	DB23-DB18: Unused DB17-DB0: Data

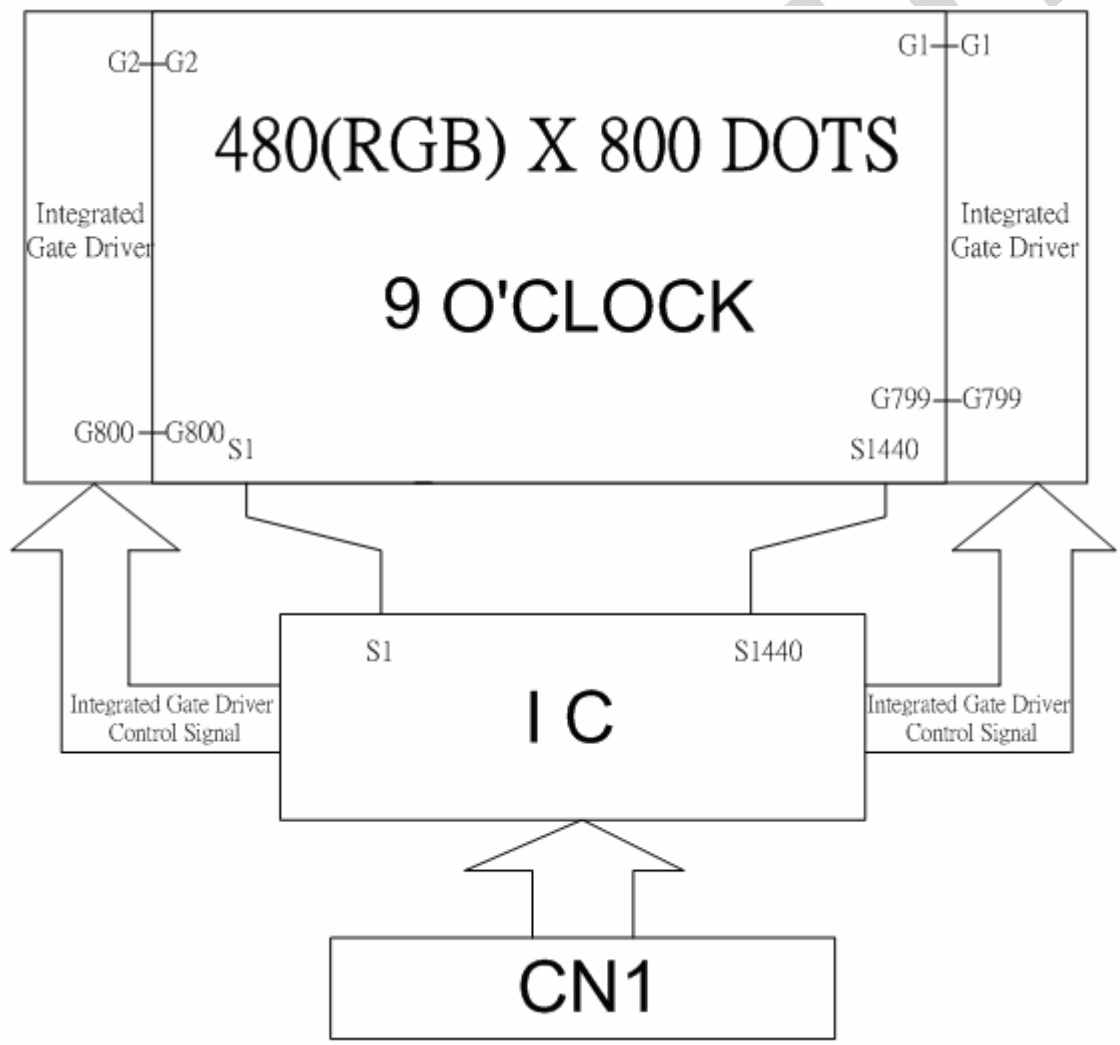
1.3 Power Supply for LCD Module



Note: VDD=1.85V, VCI=2.8V
The LED must be current driving. ILED=20mA

1.4 Block Diagram with Display RAM Address

1.4-1. Block Diagram



1.4-2. Initialization Table:

NO	Document Number	Attachment file
1	MF4880Y-IN2-101	

Double-Click the “Attachment Icon” above for opening attachment file.

1.5 Timing Characteristic

8.4.2 DBI Type B interface characteristics

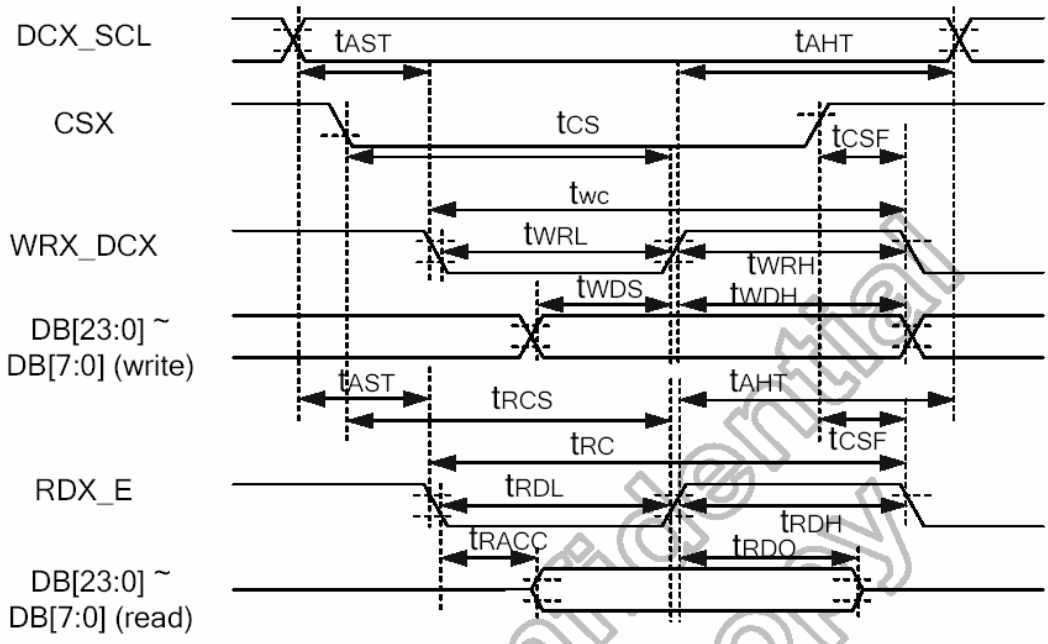


Figure 8.2: DBI Type B interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25°C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSX	t_{CS} t_{RCS} t_{RCSFM} t_{CSF}	Chip select setup time (Write) Chip select setup time (Read ID) Chip Select setup time (Read FM) Chip select wait time (Write/Read)	20 45 355 20	- - - -	ns	-
WRX_DCX	t_{WC} t_{WC} t_{WC} t_{WRH} t_{WRL}	Write cycle (write register) Write cycle (write GRAM@SLPOUT) Write cycle (write GRAM@SLPIN) Control pulse "H" duration Control pulse "L" duration	100 33 100 15 15	790 790 790 630 160	ns	-
RDX_E	t_{RC} t_{RC} t_{RDH} t_{RDL}	Read cycle (read register) Read cycle (GRAM) Control pulse "H" duration Control pulse "L" duration	100 350 30 20	790 790 630 160	ns	-
DB23-DB0	t_{WDS} t_{WDH} t_{RACC} t_{RDO}	Data setup time Data hold time Read access time Output disable time	15 25 10 10	- - - -	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.5: DBI Type B interface characteristics

8.4.5 Reset input timing

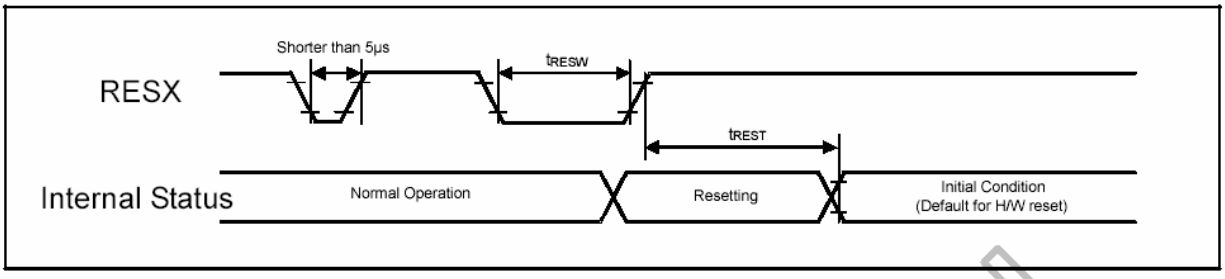


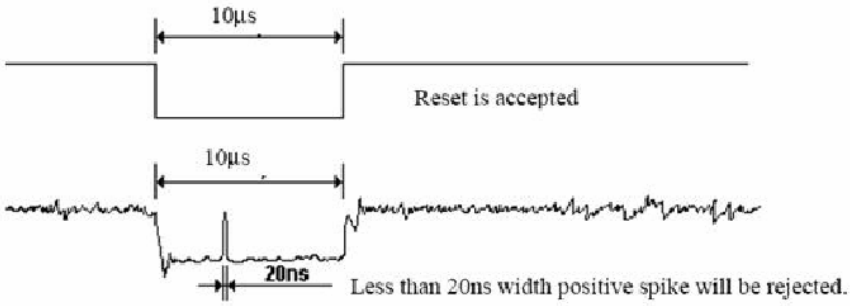
Figure 8.7: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	-	-	5	When reset is applied during Sleep In mode	ms
		-	-	-	120	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.10: Reset timing

1.6 Power ON/OFF SEQUENCE

Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

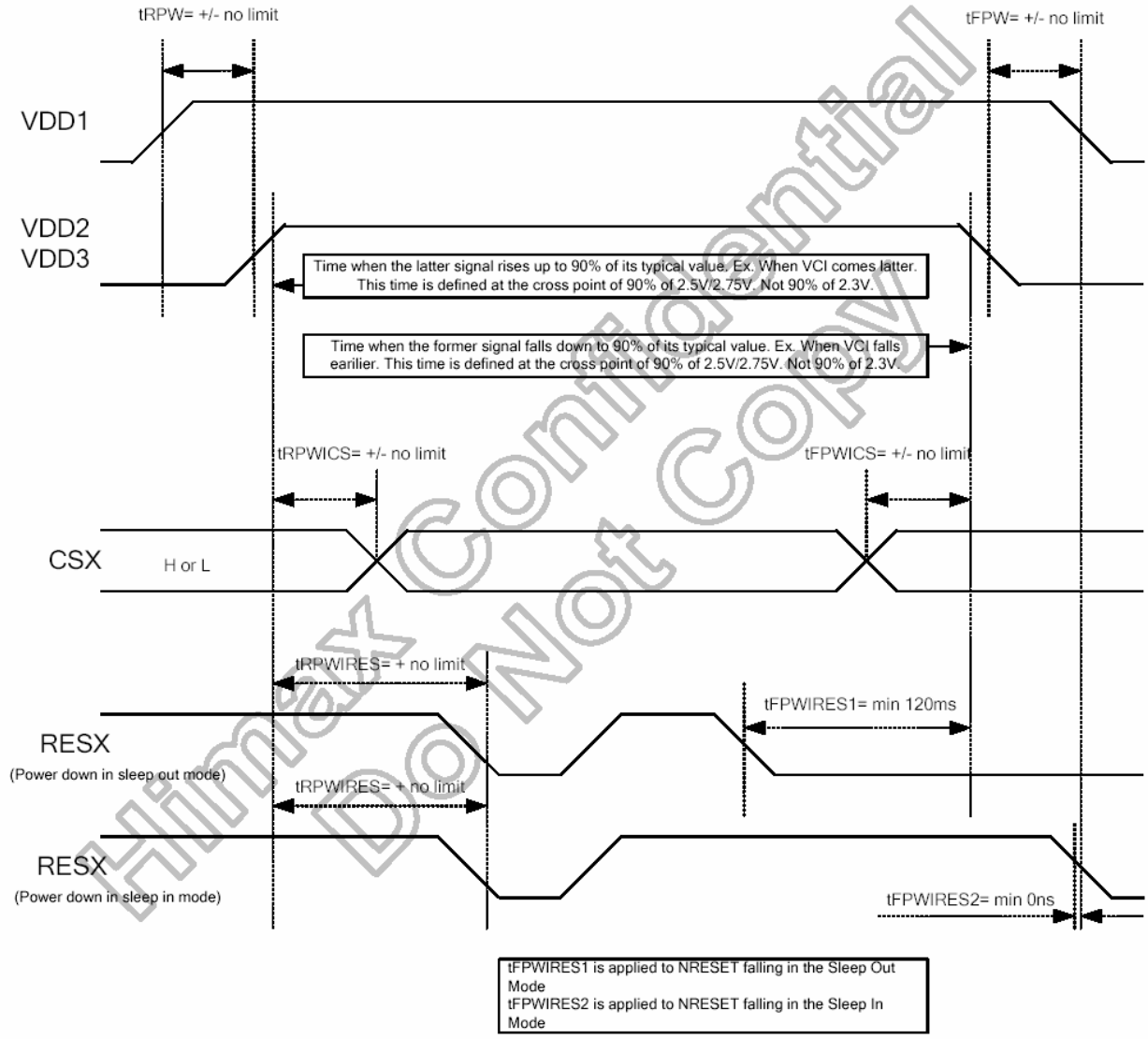


Figure 5.35: Case 1: RESX line is held high or unstable by host at power on

Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.

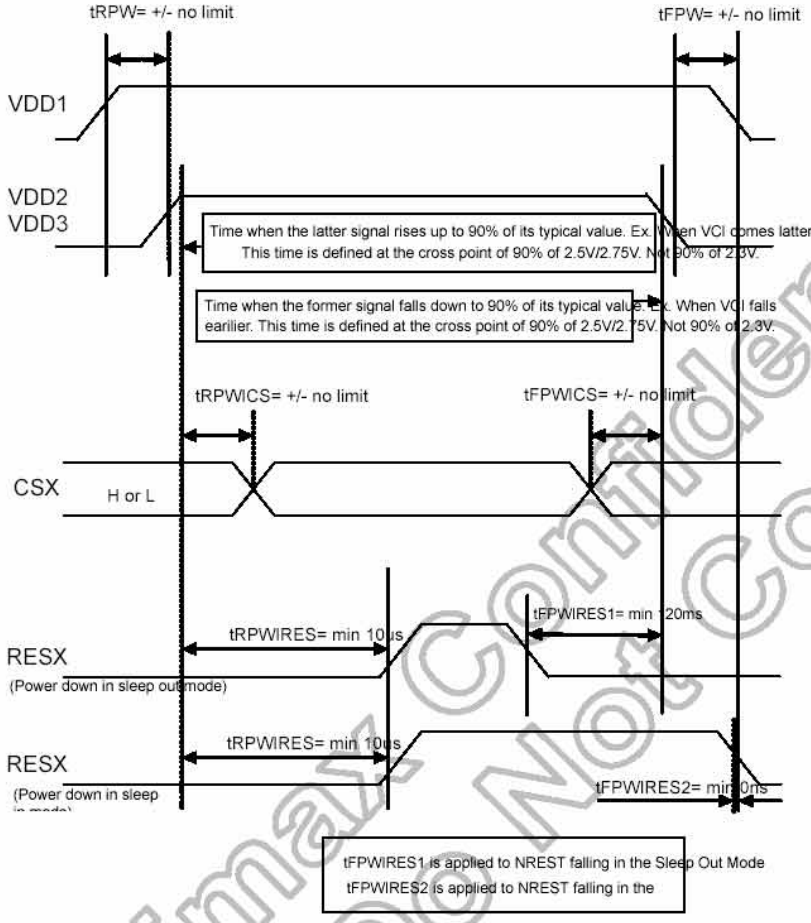
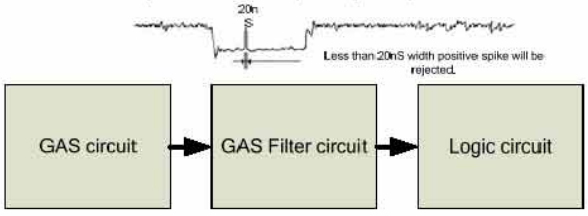


Figure 5.36: Case 2: RESX line is held low by host at power on

Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

Note: HX8369-A01 is support the noise reject filter (20ns) to reject spike or noise.



(2) ATT(Advanced Touch Technology)

2.1 ATT Electrical Characteristics

(Ta=25℃)

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Power Voltage		V_{DD_TP}	-	3.2	3.3	3.4	V
Input Signal Voltage	H Level	V_{IH}	-	0.7 V_{DD_TP}	-	V_{DD_TP}	V
	L Level	V_{IL}	-	GND	-	0.3 V_{DD_TP}	V
Report Rate		-	-	-	TBD	-	Hz
Interface		-	-	I2C			
Touch Panel Resolution		-	-	480*800			
Supply Current		*IDD	-	-	-	TBD.	mA
Input		2 points					

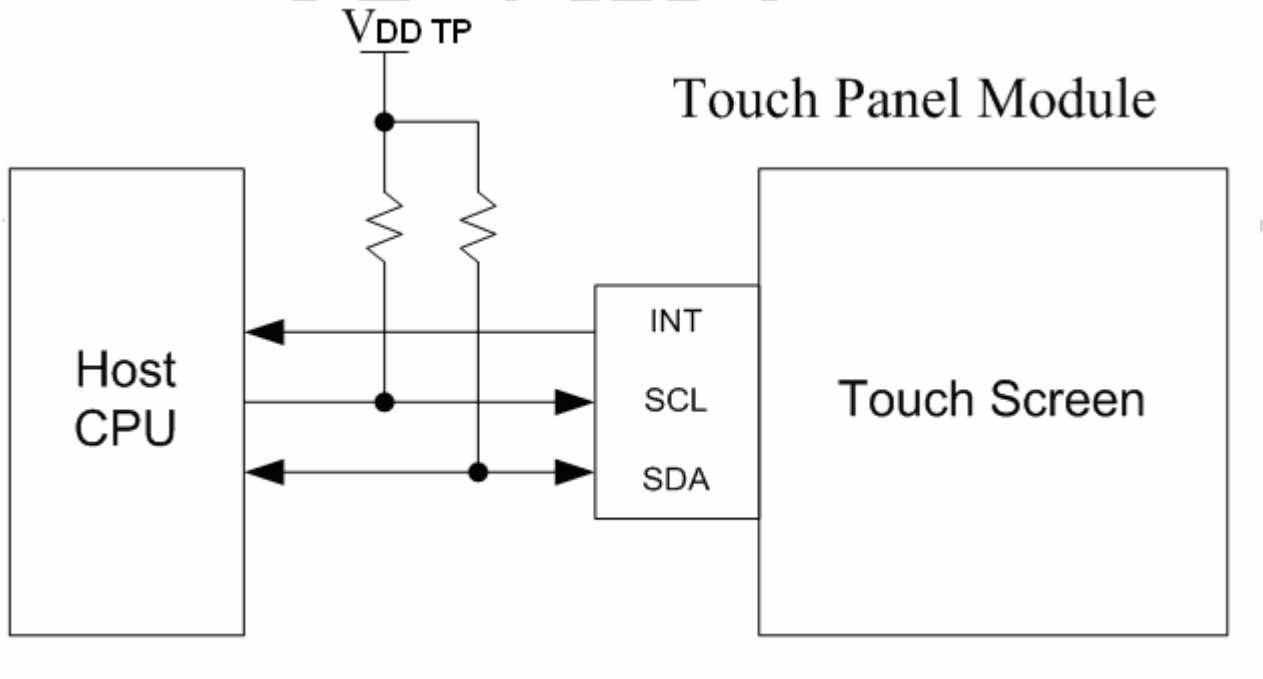
2.2 ATT Interface Pin Function

NO.	SYMBOL	I/O	FUNCTION
1	VDD	P	Touch panel power supply
2	GND	P	Ground
3	SAT	I	I2C request pad
4	SCL	I	I2C pin
5	SDA	I/O	I2C pin
6	XRES	I	Global reset input. (Low Active)

2.3 ATT Interface Diagram

The system block diagram is as shown in below. There are three communication pins connected between CPU and Sensor Module, which are including external interrupt INT, I2C pins SCL and SDA. The INT is active low while the touch state is calculated by Sensor Module and the touch information can be translated via I2C communication interface. The I2C data format, protocol and report packet are described as following.

System block diagram



2.4 ATT Timing Characteristic

I2C interface

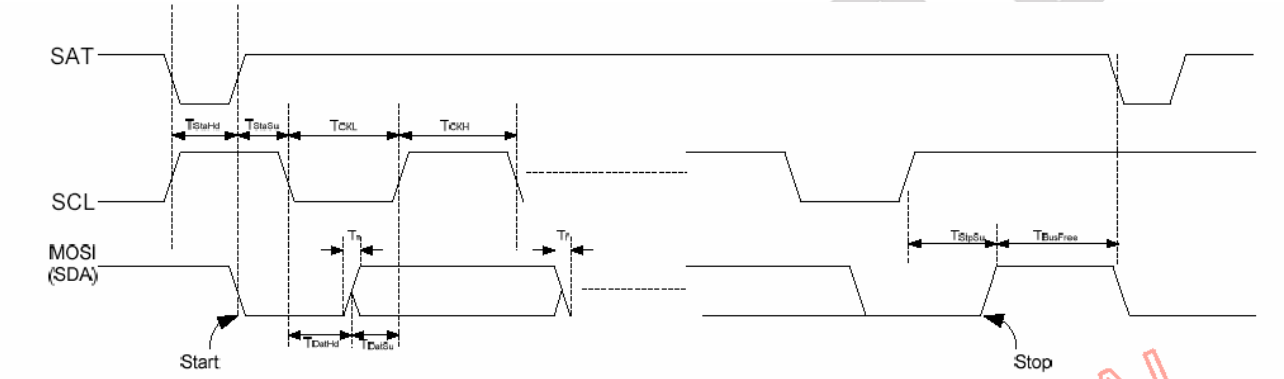


Table 3. I^2C Timing Table

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Working Frequency	Fclk	0		400	KHz	VDD =3.3V, T_A=25℃.
I^2C Clock Low	T_{CKL}	1250			ns	VDD =3.3V, T_A=25℃.
I^2C Clock High	T_{CKH}	1250			ns	VDD =3.3V, T_A=25℃.
I^2C Data Rising Time	T_r			300	ns	VDD =3.3V, T_A=25℃.
I^2C Data Falling Time	T_f			300	ns	VDD =3.3V, T_A=25℃.
I^2C Data Hold Time	T_{DatHd}	0			ns	VDD = 3.3V, T_A=25℃.
I^2C Data Setup Time	T_{DatSu}	100			ns	VDD = 3.3V, T_A=25℃.
I^2C Start Condition Hold Time	T_{StaHd}	600			ns	VDD = 3.3V, T_A=25℃.
I^2C Start Condition Setup Time	T_{StaSu}	600			ns	VDD = 3.3V, T_A=25℃.
I^2C Stop Condition Setup Time	T_{StpSu}	600			ns	VDD = 3.3V, T_A=25℃.
I^2C Bus Free Time	$T_{BusFree}$	1300			ns	VDD = 3.3V, T_A=25℃.

2.5 ATT Protocol

TBD.

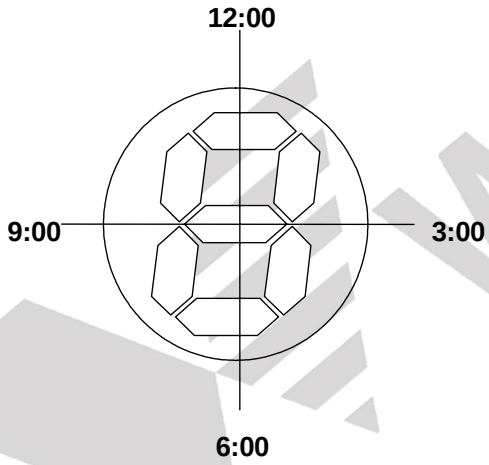
(3) Electro-optical Unitss

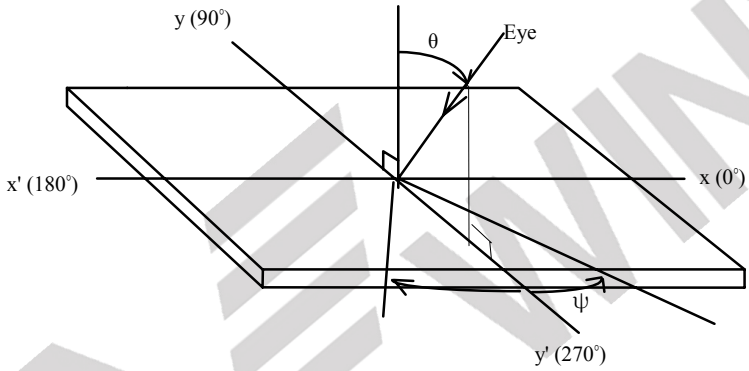
3.1 Electro-optical Characteristics

ITEM	SYMBOL		CONDITION	MIN.	TYP.	MAX.	UNIT
View Angle (Transmissive)	ψ= 90 ° (12H)		CR>=10	80	85	-	deg.
	ψ= 270 ° (6H)			80	85	-	deg.
	ψ= 180 ° (9H)			80	85	-	deg.
	ψ= 0 ° (3H)			80	85	-	deg.
Contrast Ratio (Transmissive)	CR		Ta=25℃	400	500	-	-
Response Time	Tr		Ta=25℃	-	15	30	ms
	Td			-	10	20	ms
Color Coordinate	Red	Rx	Ta=25℃	0.53	0.58	0.63	-
		Ry		0.30	0.35	0.40	
	Green	Gx		0.29	0.34	0.39	
		Gy		0.53	0.58	0.63	
	Blue	Bx		0.10	0.15	0.20	
		By		0.09	0.14	0.19	
	White	Wx		0.26	0.31	0.36	
		Wy		0.26	0.31	0.36	
	NTSC			-	45	-	%
LCD Type	TFT , (NEGATIVE / Transmissive)						

Notes： All the optical data should be measured when the display's driven under the TYP. condition.

3.2 Optical Definitions





View Angle

(4) LCM Mechanical Units

4.1 LCM Mechanical Diagram

NO	Document Number	Attachment file
1	MFL042V-AS1-101	

Double-Click the "Attachment Icon" above for opening attachment file.

4.2 Back-light Specification

LED Backlight Styles:

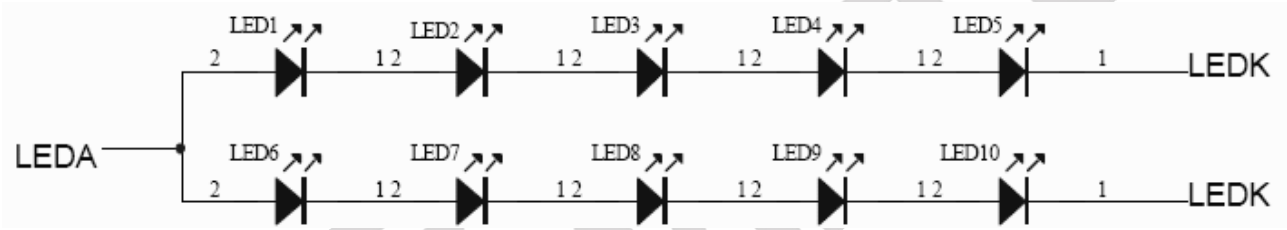
The LED chips are distributed over the whole light area of the illumination unit, which gives the most uniform light.

4.2-1. Data About LED Backlight

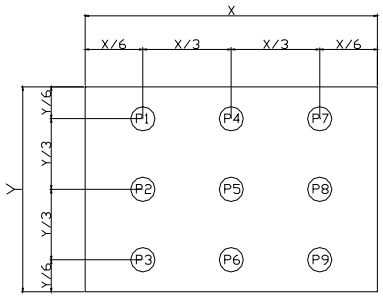
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	NOTE
Backlight Type	LED / WHITE						-
Supply Current	ILED	-	20	-	mA	VLED<=17.5V	-
Reverse Voltage (Single chip)	VR	-	-	5	V	-	-
Luminous Intensity	IV	400	-	-	cd/m2	-	-
Luminous Intensity Ratio	-	70	-	-	%	-	-

NOTE：1. Average Luminous Intensity of P1 – P9 2. Luminous Intensity Ratio = (MIN. / MAX.)*100%

4.2-2. Internal Circuit Diagram



4.2-3. MEASURED METHOD (X*Y: Light Area)



(Effective spatial Distribution)

Hole Diameter φ3mm;1 to 9 per Position Measured Luminous Intensity Ratio

4.3 Packing Method

NO	Document Number	Attachment file
1	MFL042V-M1-01	

Double-Click the "Attachment Icon" above for opening attachment file.

(5) Quality Units

5.1 Specification of Quality Assurance

5.1-1.Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by WINTEK CORPORATION (Supplier).

5.1-2.Standard for Quality Test

a. Inspection :

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ANSI/ASQC Z1.4-2003.General Inspection Level Ⅱ take a single time.**

(ii) The defects classify of AQL as following:

Major defect: AQL=0.65

Minor defect: AQL=2.5

Total defects: AQL=2.5

5.1-3.Nonconforming Analysis & Deal With Manners

a. Nonconforming analysis:

(i) Purchaser should supply the detail data of non-conforming sample and the non-suitable state.

(ii) After accepting the detail data from purchaser, the analysis of nonconforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before two weeks.

b. Disposition of nonconforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of nonconforming when the reason of nonconforming is not sure.

5.1-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides think that it must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

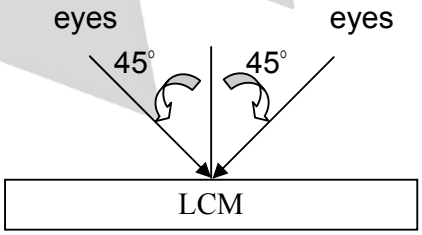
5.1-5. Standard of The Product Appearance Test

a. Manner of appearance test:

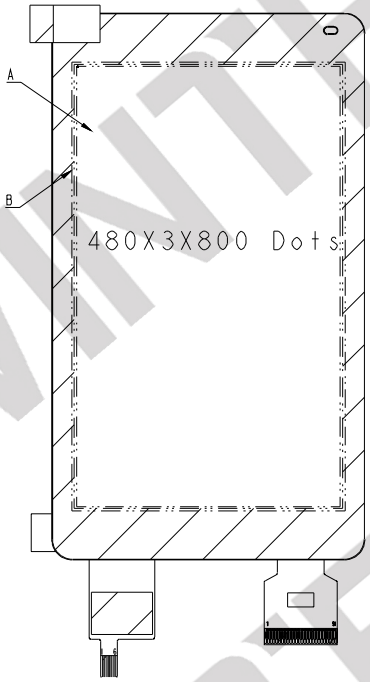
(i) The test must be under 20W Ｘ 2 or 40W fluorescent light, and the distance of view must be at 30 cm.

(ii) When display on use front-light test, while display off use back-light test.

(iii)The test direction is base on about around 45° of vertical line.



(iv) Definition of area:



A Area : Viewing area.

B Area : Out of viewing area (Outside viewing area)

Any defect at area B could be ignored. If customer has particular requirement, this requirement should be clearly defined in inspection specification. If inspection specification has defined other criteria, the final judgement should follow the inspection specification .

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

(iii) Must add new item on time when it is necessary.

5.1-6. Inspection specification

NO	Document Number	Attachment file
1	M1L070012	

Double-Click the "Attachment Icon" above for opening attachment file.

5.2 Standard Specification for Reliability

NO	Document Number	Attachment file
1	M3ET090001	

Double-Click the "Attachment Icon" above for opening attachment file.

5.3 Precautions in Use of LCM

5.3-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.

5.3-2 Storage

- Store in an ambient temperature of 25℃ ± 5℃, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

5.3-3 Soldering

- Use the Sn-Ag-Cu (96.5, 3.0, 0.5) solder
- Iron : Temperature 300℃ and less than 5-6 sec during soldering.
- Rewiring : no more than 3 times.

5.3-4 Assembly

The front polarizer is covered with a protective foil which should be removed before use.

(6) Substance Management Units

6.1 Product Substances Management Documentation

NO	Document Number	Attachment file
1	Environment management standard(EMS-P-017-01)	

Double-Click the "Attachment Icon" above for opening attachment file.