WM1811

Multi-Channel Audio Hub CODEC for Smartphones

DESCRIPTION

The WM1811 is a highly integrated ultra-low power hi-fi CODEC designed for smartphones and other portable devices rich in multimedia features.

An integrated stereo class D speaker driver and class W headphone driver minimize power consumption during audio playback.

The device requires only two voltage supplies, with all other internal supply rails generated from integrated LDOs.

Stereo full duplex asynchronous sample rate conversion and multi-channel digital mixing combined with powerful analogue mixing allow the device to support a huge range of different architectures and use cases.

A programmable parametric EQ provides speaker compensation in the digital playback paths. The dynamic range controller can be used in record or playback paths for maintaining a constant signal level, maximizing loudness and protecting speakers against overloading and clipping.

A smart digital microphone interface provides power regulation, a low jitter clock output and decimation filters for up to two digital microphones. Microphone activity detection with interrupt is available. Impedance sensing and measurement is provided for external accessory / push-button detection.

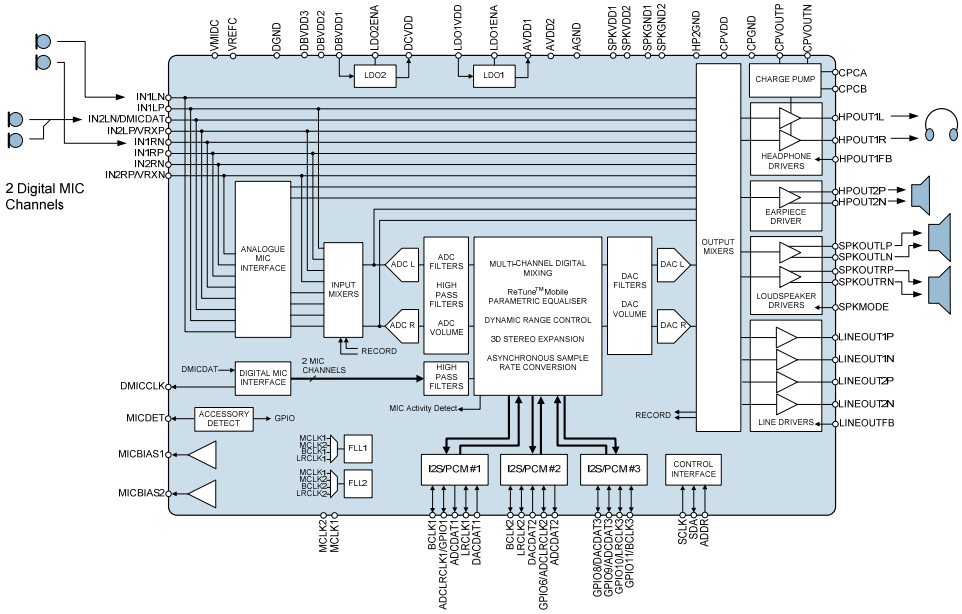
Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity. Active ground loop noise rejection and DC offset correction help prevent pop noise and suppress ground noise on the headphone outputs.

FEATURES

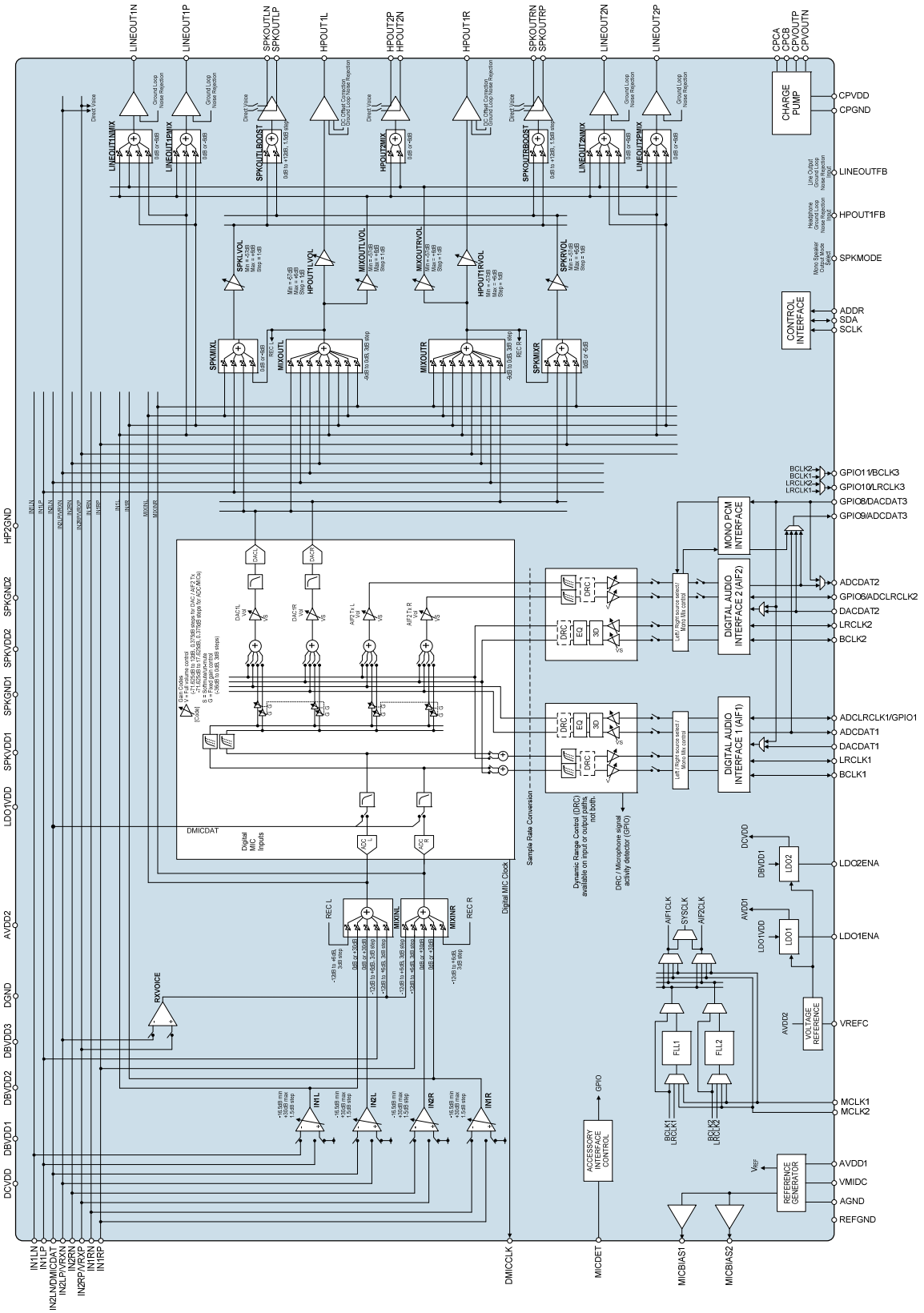
- 24-bit 2-channel Hi-Fi DAC and 2-channel Hi-Fi ADC
- 100dB SNR during DAC playback ('A' weighted)
- Smart MIC interface
  - Power, clocking and data input for up to two digital MICs
  - High performance analogue MIC interface
  - MIC activity detect & interrupt allows processor to sleep
  - Impedance sensing for accessory / push-button detection
- 2W stereo (2 x 2W) class D speaker driver
- Capless Class W headphone drivers
  - Integrated charge pump
  - 5.3mW total power for DAC playback to headphones
- 4 Line outputs (single-ended or differential)
- BTL Earpiece driver
- Digital audio interfaces for multi-processor architecture
  - Asynchronous stereo duplex sample rate conversion
  - Powerful mixing and digital loopback functions
- ReTune™ Mobile 5-band, 4-channel parametric EQ
- Dynamic range controller
- Dual FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Active noise reduction circuits
  - DC offset correction removes pops and clicks
  - Ground loop noise cancellation
- Integrated LDO regulators
- 80-ball W-CSP package (4.148 x 3.866 x 0.596mm)

APPLICATIONS

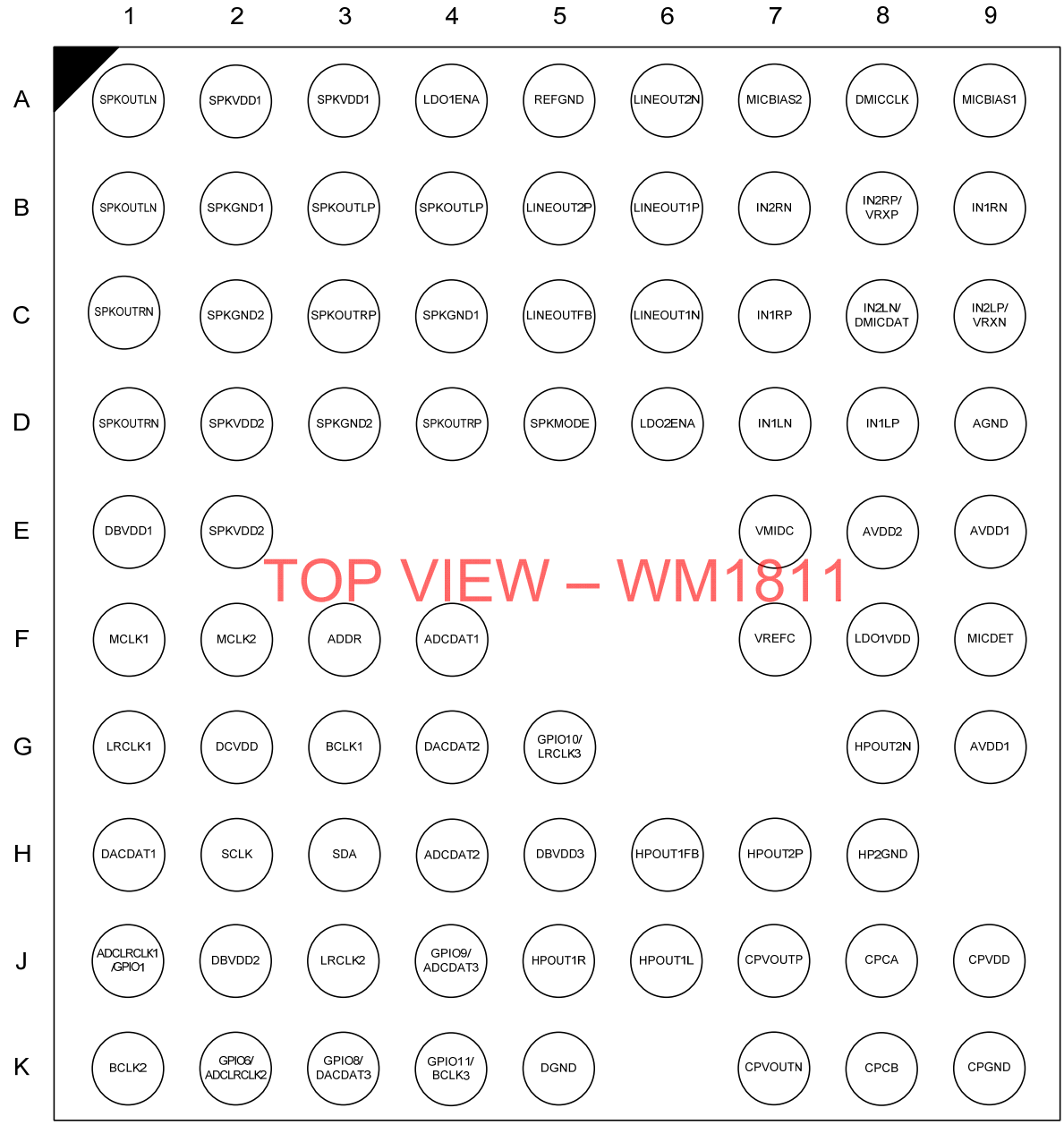
- Smartphones and music phones
- Portable navigation
- Tablets
- eBooks
- Portable Media Players



BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM1811ECS/R	-40°C to +85°C	80-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 5000

PIN DESCRIPTION

A description of each pin on the WM1811 is provided below.
Note that a table detailing the associated power domain for every input and output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

PIN NO	NAME	TYPE	DESCRIPTION
F4	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
H4	ADCDAT2	Digital Input / Output	Audio interface 2 ADC digital audio data
J1	ADCLRCLK1/ GPIO1	Digital Input / Output	Audio interface 1 ADC left / right clock / General Purpose pin GPIO 1
F3	ADDR	Digital Input	2-wire (I2C) address select
D9	AGND	Supply	Analogue ground (Return path for AVDD1)
E9, G9	AVDD1	Supply / Analogue Output	Analogue core supply / LDO1 Output
E8	AVDD2	Supply	Bandgap reference, analogue class D and FLL supply
G3	BCLK1	Digital Input / Output	Audio interface 1 bit clock
K1	BCLK2	Digital Input / Output	Audio interface 2 bit clock
J8	CPCA	Analogue Output	Charge pump fly-back capacitor pin
K8	CPCB	Analogue Output	Charge pump fly-back capacitor pin
K9	CPGND	Supply	Charge pump ground (Return path for CPVDD)
J9	CPVDD	Supply	Charge pump supply
K7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1L, HPOUT1R)
J7	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1L, HPOUT1R)
H1	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
G4	DACDAT2	Digital Input / Output	Audio interface 2 DAC digital audio data
E1	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
J2	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
H5	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
G2	DCVDD	Supply / Analogue Output	Digital core supply / LDO2 output
K5	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2, DBVDD3)
A8	DMICCLK	Digital Output	Digital MIC clock output
G5	GPIO10/ LRCLK3	Digital Input / Output	General Purpose pin GPIO 10 / Audio interface 3 left / right clock
K4	GPIO11/ BCLK3	Digital Input / Output	General Purpose pin GPIO 11 / Audio interface 3 bit clock
K2	GPIO6/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 6 / Audio interface 2 ADC left / right clock
K3	GPIO8/ DACDAT3	Digital Input / Output	General Purpose pin GPIO 8 / Audio interface 3 DAC digital audio data
J4	GPIO9/ ADCDAT3	Digital Input / Output	General Purpose pin GPIO 9 / Audio interface 3 ADC digital audio data
H8	HP2GND	Supply	Analogue ground
H6	HPOUT1FB	Analogue Input	HPOUT1L and HPOUT1R ground loop noise rejection feedback
J6	HPOUT1L	Analogue Output	Left headphone output
J5	HPOUT1R	Analogue Output	Right headphone output
G8	HPOUT2N	Analogue Output	Earpiece speaker inverted output
H7	HPOUT2P	Analogue Output	Earpiece speaker non-inverted output
D7	IN1LN	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
D8	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
B9	IN1RN	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input

PIN NO	NAME	TYPE	DESCRIPTION
C7	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
C8	IN2LN/ DMICDAT	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Digital MIC data input
C9	IN2LP/VRXN	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential negative input (RXVOICE -)
B7	IN2RN	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input
B8	IN2RP/VRXP	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential positive input (RXVOICE +)
A4	LDO1ENA	Digital Input	Enable pin for LDO1
F8	LDO1VDD	Supply	Supply for LDO1
D6	LDO2ENA	Digital Input	Enable pin for LDO2
C6	LINEOUT1N	Analogue Output	Negative mono line output / Positive left or right line output
B6	LINEOUT1P	Analogue Output	Positive mono line output / Positive left line output
A6	LINEOUT2N	Analogue Output	Negative mono line output / Positive left or right line output
B5	LINEOUT2P	Analogue Output	Positive mono line output / Positive left line output
C5	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
G1	LRCLK1	Digital Input / Output	Audio interface 1 left / right clock
J3	LRCLK2	Digital Input / Output	Audio interface 2 left / right clock
F1	MCLK1	Digital Input	Master clock 1
F2	MCLK2	Digital Input	Master clock 2
A9	MICBIAS1	Analogue Output	Microphone bias 1
A7	MICBIAS2	Analogue Output	Microphone bias 2
F9	MICDET	Analogue Input	Microphone & accessory sense input
A5	REFGND	Supply	Analogue ground
H2	SCLK	Digital Input	Control interface clock input
H3	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
B2, C4	SPKGND1	Supply	Ground for speaker driver (Return path for SPKVDD1)
C2, D3	SPKGND2	Supply	Ground for speaker driver (Return path for SPKVDD2)
D5	SPKMODE	Digital Input	Mono / Stereo speaker mode select
A1, B1	SPKOUTLN	Analogue Output	Left speaker negative output
B3, B4	SPKOUTLP	Analogue Output	Left speaker positive output
C1, D1	SPKOUTRN	Analogue Output	Right speaker negative output
C3, D4	SPKOUTRP	Analogue Output	Right speaker positive output
A2, A3	SPKVDD1	Supply	Supply for speaker driver 1 (Left channel)
D2, E2	SPKVDD2	Supply	Supply for speaker driver 2 (Right channel)
E7	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
F7	VREFC	Analogue Output	Bandgap reference decoupling capacitor

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, DBVDD2, DBVDD3)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, DBVDD1)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDD1, SPKVDD2, LDO1VDD)	-0.3V	+7.0V
Voltage range digital inputs (DBVDD1 domain)	DGND -0.3V	DBVDD1 +0.3V
Voltage range digital inputs (DBVDD2 domain)	DGND -0.3V	DBVDD2 +0.3V
Voltage range digital inputs (DBVDD3 domain)	DGND -0.3V	DBVDD3 +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD1 +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.00	1.05	2.0	V
Digital supply range (I/O)	DBVDD1	1.62	1.8	2.0	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.62	1.8	3.6	V
Analogue supply 1 range	AVDD1	2.4	3.0	3.3	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
LDO1 supply range	LDO1VDD	2.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND		0		V
Power supply rise time (notes 6, 7 and 8)	All supplies	1			µs

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. There is no power sequencing requirement; the supplies may be enabled in any order.
3. AVDD1 must be less than or equal to SPKVDD1 and SPKVDD2.
4. When AVDD1 is supplied externally (not from LDO1), the LDO1VDD voltage must be greater than or equal to AVDD1.
5. When DCVDD is supplied externally (not from LDO2), the DBVDD1 voltage must be greater than or equal to DCVDD.
6. DCVDD and AVDD1 minimum rise times do not apply when these domains are powered using the internal LDOs.
7. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed (see “Applications Information” section).
8. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

DEVICE DESCRIPTION

The WM1811 is a low power, high quality audio codec designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones. Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity.

Three sets of audio interface pins are available in order to provide independent and fully asynchronous connections to multiple processors, typically an application processor, baseband processor and wireless transceiver. Any two of these interfaces can operate totally independently and asynchronously while the third interface can be synchronised to either of the other two and can also provide ultra low power loopback modes to support, for example, wireless headset voice calls.

The WM1811 provides a two-channel digital microphone interface, suitable for noise cancellation and other applications. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs (single-ended or differential), plus multiple stereo or mono line inputs. Connections to an external voice CODEC, FM radio, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes. A 'Direct Voice' path from a voice CODEC directly to the Speaker or Earpiece output drivers is included.

Impedance sensing and measurement for external accessories is provided, for detection of the insertion or removal of microphones and other accessories. Push-button detection of up to 7 inputs can be supported using this feature.

Nine analogue output drivers are integrated, including a stereo pair of high power, high quality Class D speaker drivers; these can support 2W each in stereo mode. It is also possible to configure the speaker drivers as a mono output, giving enhanced performance. A mono earpiece driver is provided, providing output from the output mixers or from the low-power differential 'Direct Voice' path.

One pair of ground-referenced headphone outputs is provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, thereby suppressing pops and reducing power consumption. Four line outputs are provided, with multiple configuration options including 4 x single-ended output or 2 x differential outputs. The line outputs are suitable for output to a voice CODEC, an external speaker driver or line output connector. Ground loop feedback is available on the headphone outputs and the line outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

Internal differential signal routing and amplifier configurations have been optimised to provide the highest performance and lowest possible power consumption for a wide range of usage scenarios, including voice calls and music playback. The speaker drivers offer low leakage and high PSRR; this enables direct connection to a Lithium battery. The speaker drivers provide eight levels of AC and DC gain to allow output signal levels to be maximised for many commonly-used SPKVDD/AVDD1 combinations.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst integrated ultra-low power dual FLLs provide additional flexibility. A high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controllers (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. 'Anti-clip' and 'quick release' algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

The WM1811 has highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

A powerful digital mixing core allows data from each audio interface channel and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the DAC output paths. The digital mixing core can operate synchronously with either Audio Interface 1 or Audio Interface 2, with asynchronous stereo full duplex sample rate conversion performed on the other audio interface as required.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from one of the MCLK1 or MCLK2 pins or via one of two integrated FLLs, providing flexibility to support a wide range of clocking schemes, including self-clocking FLL modes. Typical portable system MCLK frequencies, and sample rates from 8kHz to 96kHz are all supported. A low frequency (eg. 32.768kHz) clock can be used as the input reference to the FLLs, providing further flexibility. Automatic configuration of the clocking circuits is available, derived from the sample rate and from the MCLK / SYSCLK ratio.

The WM1811 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

APPLICATIONS INFORMATION

The recommended external components for WM1811 are illustrated below.

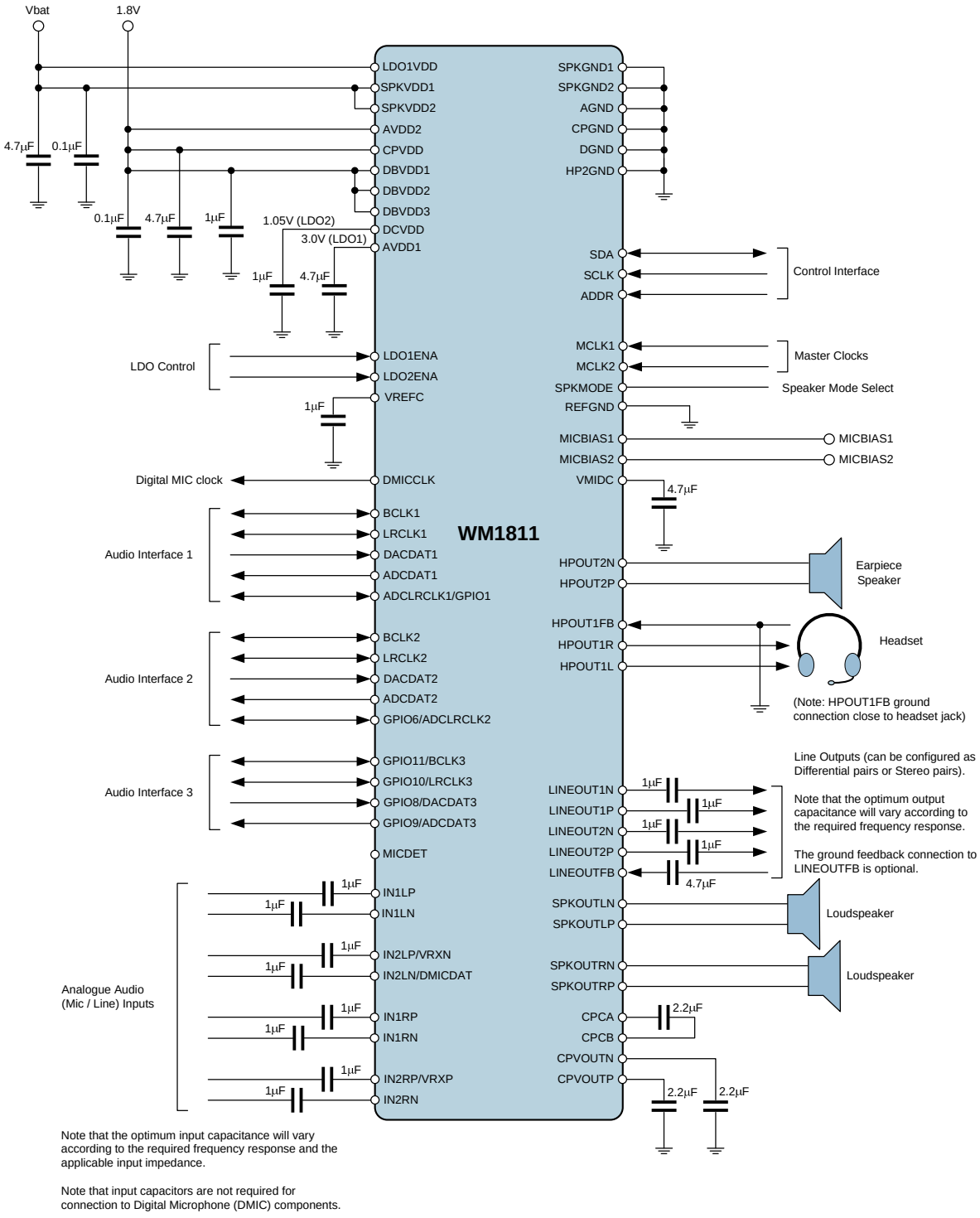
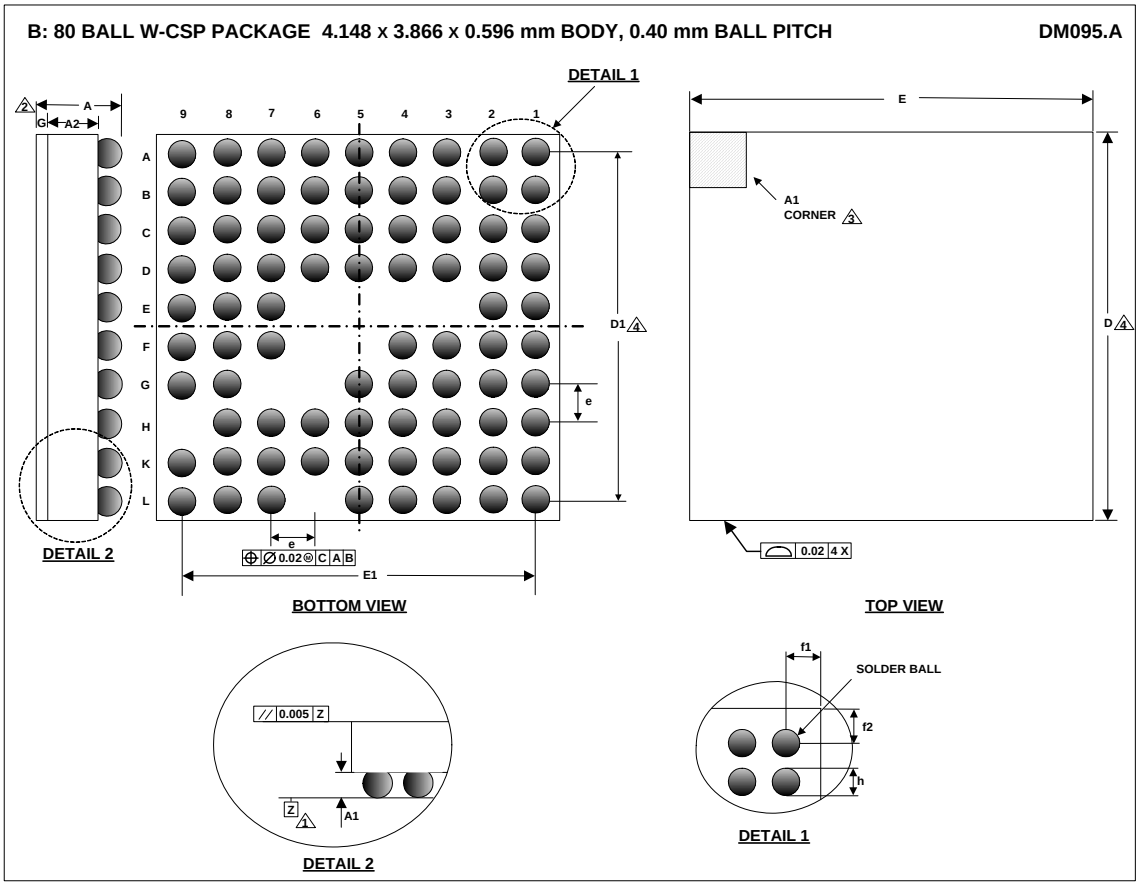


Figure 1 Recommended External Components Diagram

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.579	0.596	0.613	
A1	0.186	0.191	0.196	
A2	0.368	0.380	0.392	
D	4.128	4.148	4.168	4
D1		3.600 BSC		
E	3.846	3.866	3.886	4
E1		3.200 BSC		
e		0.400 BSC		5
f1		0.333 BSC		8
f2		0.274 BSC		9
g		0.025		
h		0.270		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1', SILICON THICKNESS AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.
8. f1 = NOMINAL DISTANCE OF BALL CENTRE TO DIE EDGE X AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.
9. f2 = NOMINAL DISTANCE OF DIE CENTRE TO DIE EDGE IN Y AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.

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ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
08/02/11	2.0	Initial version		PH