DESCRIPTION

The WM2148 is a 14-bit, 8 MSPS analogue to digital converter with an on-chip voltage reference, high bandwidth sample and hold amplifier and programmable gain. The analogue input is differential, giving excellent common-mode noise immunity and low distortion.

The WM2148 is designed for use in highly integrated, low-power 3.3V systems. A high speed, microprocessor compatible parallel interface allows control of the ADC input gain, digital DC offset, internal / external reference and output data format. Both binary and two's complement formats are supported. The device also features an out of range indicator pin to show when the input signal exceeds the converter's full-scale range.

In Power Down mode, all analogue circuitry is internally disconnected from the power supply, reducing total supply current to 20μA.

The WM2148 is available in a 1mm thin 48-pin TQFP package in standard commercial and industrial temperature ranges.

FEATURES

- 14-bit resolution ADC
- 8 MSPS conversion rate
- Differential input
- 3.3V single supply
- Very low current power down mode - 20μA typical
- Microprocessor compatible parallel interface
- Internal or external voltage reference
- High bandwidth sample and hold amplifier
  - 140MHz full-power bandwidth
- Programmable Gain Amplifier (PGA)
- Programmable DC offset
- Binary or two's complement output format
- Out of range indicator
- 48-pin TQFP package, body thickness 1mm

APPLICATIONS

- Communications
- xDSL Front ends
- Industrial control
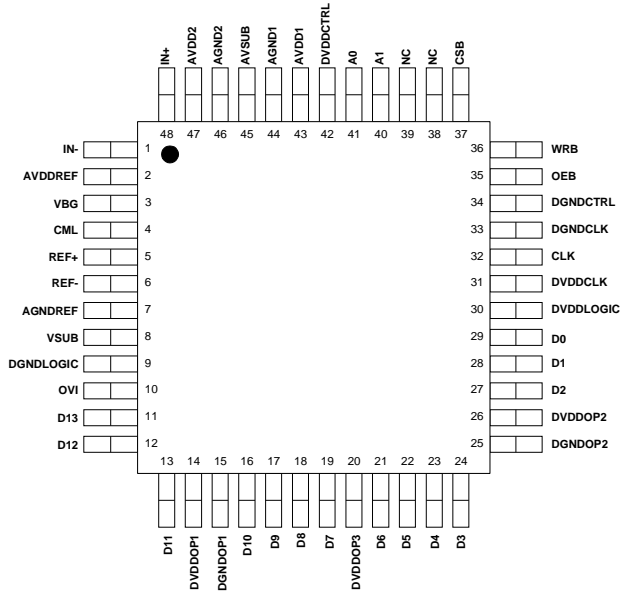- Instrumentation

BLOCK DIAGRAM
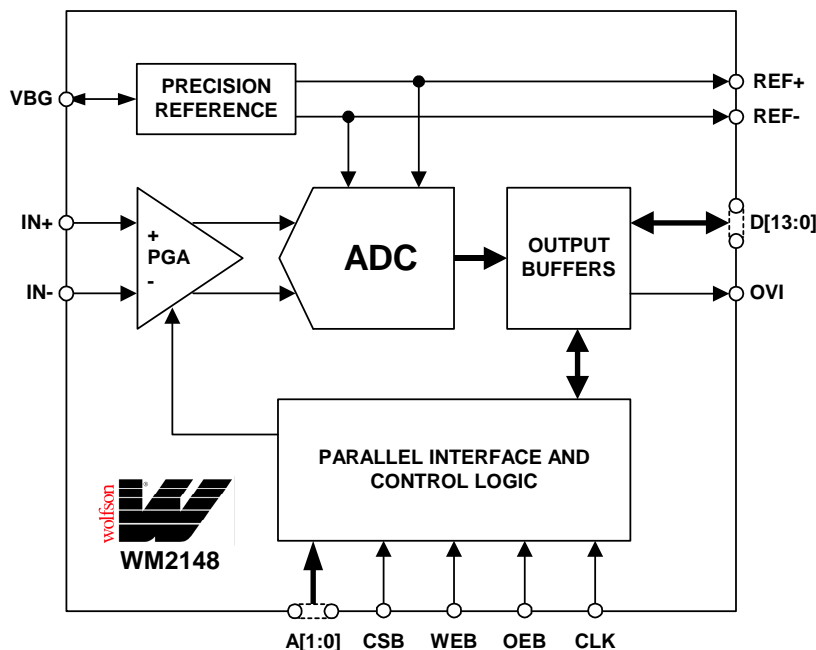
PIN CONFIGURATION

ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2148CFT/V	0 to +70°C	48-pin TQFP 1 mm thick body
WM2148IFT/V	-40 to +85°C	

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	IN-	Analogue Input	Negative Differential Analogue Input
2	AVDDREF	Supply	Positive Supply Voltage for Reference
3	VBG	Analogue I/O	Bandgap Voltage / External Reference
4	CML	Analogue Output	Reference Decoupling Point
5	REF+	Analogue Output	Positive Reference Voltage
6	REF-	Analogue Output	Negative Reference Voltage
7	AGNDREF	Supply	Reference Block Ground
8	VSUB	Supply	Device Substrate
9	DGNDLOGIC	Supply	Digital Ground for Logic Block
10	OVI	Digital Output	Out of Range Indicator
11	D13	Digital I/O	Data Bit 13
12	D12	Digital I/O	Data Bit 12
13	D11	Digital I/O	Data Bit 11
14	DVDDOP1	Supply	Positive Supply for Output Drivers
15	DGNDOP1	Supply	Ground for Output Drivers
16	D10	Digital I/O	Data Bit 10
17	D9	Digital I/O	Data Bit 9
18	D8	Digital I/O	Data Bit 8
19	D7	Digital I/O	Data Bit 7
20	DVDDOP3	Supply	Positive Supply for Output Drivers
21	D6	Digital I/O	Data Bit 6
22	D5	Digital I/O	Data Bit 5
23	D4	Digital I/O	Data Bit 4
24	D3	Digital I/O	Data Bit 3
25	DGNDOP2	Supply	Ground for Output Drivers
26	DVDDOP2	Supply	Positive Supply for Output Drivers

PIN	NAME	TYPE	DESCRIPTION
27	D2	Digital I/O	Data Bit 2
28	D1	Digital I/O	Data Bit 1
29	D0	Digital I/O	Data Bit 0
30	DVDDLOGIC	Supply	Positive Supply Voltage for Logic Block
31	DVDDCLK	Supply	Positive Supply Voltage for Clock
32	CLK	Digital Input	Sample Clock
33	DGNDCLK	Supply	Ground for Clock
34	DGNDCTRL	Supply	Ground for Control Pins
35	OEB	Digital Input	Output Enable (active low)
36	WRB	Digital Input	Write Signal (active low)
37	CSB	Digital Input	Chip Select (active low)
38	NC	Test Output	This pin must be left unconnected
39	NC	Test Output	This pin must be left unconnected
40	A1	Digital Input	Address Bit 1
41	A0	Digital Input	Address Bit 0
42	DVDDCTRL	Supply	Positive Supply for Control Pins
43	AVDD1	Supply	Positive Supply for ADC
44	AGND1	Supply	Ground for ADC
45	AVSUB	Substrate	ADC substrate
46	AGND2	Supply	Positive Supply for ADC Op-amps
47	AVDD2	Supply	Ground for ADC Op-amps
48	IN+	Analogue Input	Positive Differential Analogue Input

Note:

1.   It is recommended that each pair of supply pins, especially the analogue supplies, have a separate decoupling capacitor. The most critical are pins 46 and 47. The ADC substrate (pin 45) should be as noise free as possible.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112 and A113, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION		MIN	MAX
Analogue Supply Voltage (AV_{DD} to AGND)		-0.3	4 V
Digital Supply Voltage (DV_{DD} to DGND)		-0.3	4 V
Reference Input Voltage Range (VBG)		AGND -0.3V	AV_{DD} +0.3V
Analogue Inputs Voltage Range		AGND -0.3V	AV_{DD} +0.3V
Digital Inputs Voltage Range		DGND -0.3V	DV_{DD} +0.3V
Operating temperature range (T_A)	C suffix	0°C	+70°C
	I suffix	-40°C	+85°C
Storage temperature		-65°C	+150°C
Lead temperature (soldering 10 seconds, 1.6 mm from package body)			+260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltages (digital and analogue)	AV_{DD}, DV_{DD}		3.0	3.3	3.6	V
Reference Input Voltage	V_{BG}	External reference	1.425	1.5	1.575	V
Digital Input HIGH Level	V_{IH}		2	3.3		V
Digital Input LOW Level	V_{IL}			0	0.8	V
Load Capacitance	C_L			5	15	pF
Clock Frequency	f_{CLK}		0.1	8	8	MHz
Clock Duty Cycle			40	50	60	%
Operating Free-air Temperature	T_A	C Suffix	0	25	70	°C
		I Suffix	-40	25	85	

ELECTRICAL CHARACTERISTICS

Electrical characteristics over recommended temperature range, $AV_{DD} = DV_{DD} = 3.3V$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
Analogue Supply Current	AI_{DD}	$AV_{DD} = 3.6V$		81	90	mA
Digital Supply Current	DI_{DD}	$DV_{DD} = 3.6V$		5	10	mA
Power Consumption	P	$AV_{DD} = DV_{DD} = 3.6V$		270	360	mW
Power Down Supply Current (sum of all supply currents)	$I_{PD} = AI_{DD}+DI_{DD}$	Power down mode CLK signal stopped		20		µA
DC Characteristics						
Resolution			14			bits
Differential Nonlinearity	DNL			± 0.6	± 1	bits
Integral Nonlinearity	INL	Best Fit		± 3	± 5	bits
Offset Error		IN+ = IN-, 0dB gain			0.3	% of FSR
Gain Error		0 dB gain			1	% of FSR
AC Characteristics						
Analogue Input Bandwidth				140		MHz
Total Harmonic Distortion	THD	F_{IN} = 100kHz		-81		dB
		F_{IN} = 1MHz		-78		
		F_{IN} = 4MHz		-77		
Signal to Noise Ratio	SNR	F_{IN} = 1MHz	70	72		dB
		F_{IN} = 4MHz		71		
Signal to Noise plus Distortion	SINAD	F_{IN} = 1MHz	69	70		dB
		F_{IN} = 4MHz		70		
Spurious Free Dynamic Range	SFDR	F_{IN} = 1MHz	73	80		dB
		F_{IN} = 4MHz		80		
Effective Number of Bits	ENOB		11.2	11.5		bits
Reference Voltage						
Bandgap Voltage	V_{BG}	Internal reference	1.425	1.5	1.575	V
Temperature Coefficient				40		ppm / °C
Supply Voltage Coefficient				200		ppm / V
V_{BG} Input Impedance		External reference		40		kΩ
Positive Reference Voltage	V_{REF+}	$V_{REF+} = V_{BG} (1 + ^2/_3)$		2.5		V
Negative Reference Voltage	V_{REF-}	$V_{REF+} = V_{BG} (1 - ^2/_3)$		0.5		V
Reference Voltage Difference	ΔV_{REF}	$\Delta V_{REF} = V_{REF+} - V_{REF-}$		2.0		V
Analog Inputs						
Positive Analogue Input Voltage	V_{IN+}		0		AV_{DD}	V
Negative Analogue Input Voltage	V_{IN-}		0		AV_{DD}	V
Input Voltage Difference	ΔV_{IN}	$\Delta V_{IN} = V_{IN+} - V_{IN-}$	$-\Delta V_{REF}$		ΔV_{REF}	V
Input impedance	Z_{IN}			25		kΩ
PGA Range			0		7	dB
PGA Step Size				1		dB
PGA Gain Error					± 0.25	dB
Digital Inputs						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2			V
Input current	I_{IN}				± 1	µA
Input capacitance	C_{IN}			5		pF

Digital Outputs						
Output LOW level	V_{OL}	I_{OUT} = -50µA			0.4	V
Output HIGH level	V_{OH}	I_{OUT} = +50µA	2.6			V
High Impedance Output Current	I_{OZ}				±10	µA

TERMINOLOGY

1. DNL is the variation in the analogue step size associated with one digital output code across the input range, normalised to full scale.

2. INL is the maximum deviation of the analogue input voltage associated with a digital code from its ideal value, normalised to full scale. Using the 'best fit' method, ideal values are taken from a straight line fitted to the ADC curve. The INL figure thus obtained therefore characterises linearity only and is not affected by gain and offset errors.

3. SNR is the ratio in dB of signal to noise amplitude when a full-scale sine wave is applied to the input.

4. THD is the ratio in dB of the sum of all harmonics to signal amplitude when a full scale sine wave is applied to the input.

5. SFDR is the amplitude ratio the output signal to the largest spur (artifact) produced by the device.
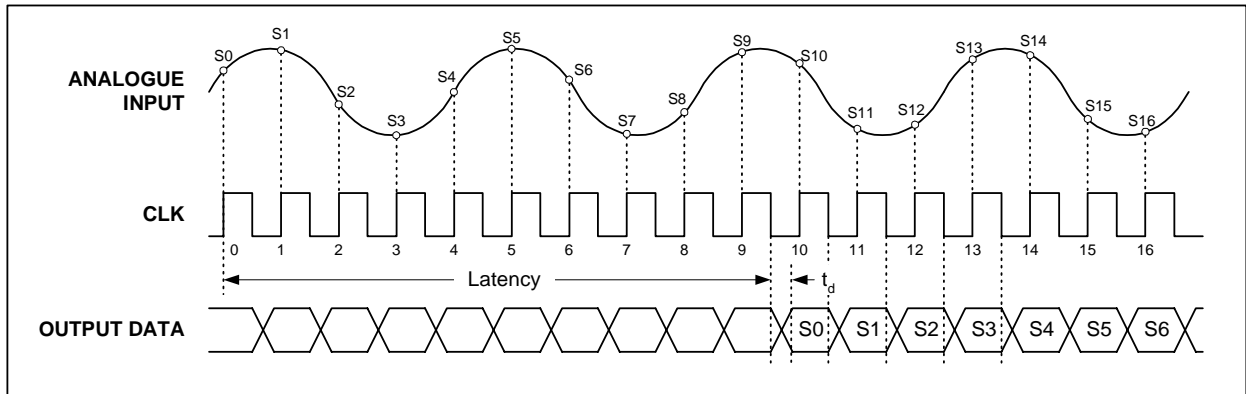

Figure 1 Latency

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Timing						
Clock Frequency	f_{CLK}	CS = Low	0.1	8	8	MHz
Output Delay Time	t_d	CS = Low			25	ns
Latency		CS = Low		9.5		cycles
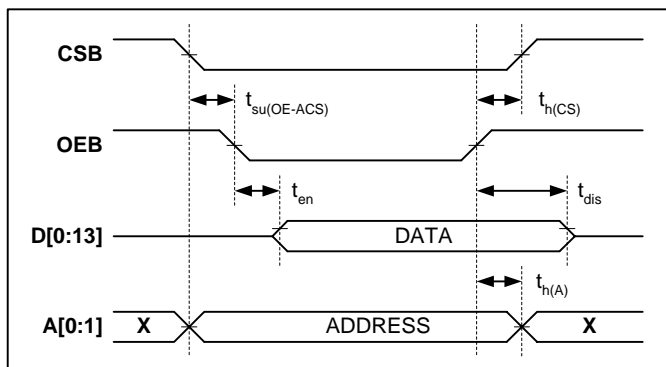
Figure 2 Read Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Read Timing						
Address and Chip select Setup Time	$t_{su(OE\text{-}ACS)}$	$C_{Load} = 15pF$	4			ns
Output Enable	t_{en}	$C_{Load} = 15pF$			15	ns
Output Disable	t_{dis}	$C_{Load} = 15pF$		10		ns
Address Hold Time	$t_{h(A)}$	$C_{Load} = 15pF$	1			ns
Chip select Hold Time	$t_{h(CS)}$	$C_{Load} = 15pF$	0			ns

Note:

1.   All timing parameters refer to a 50% level.
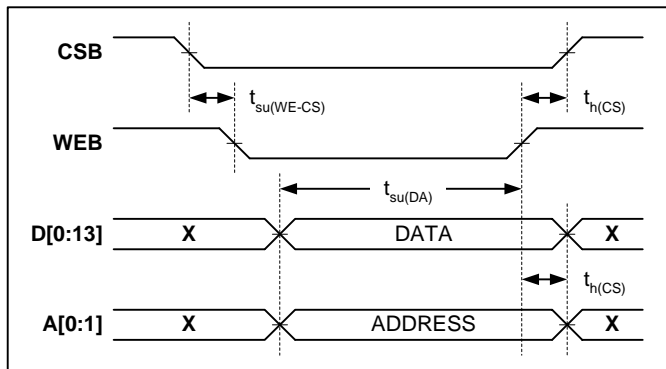
Figure 3 Write Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Write Timing						
Chip Select Setup Time	$t_{su(WE\text{-}CS)}$	$C_{Load} = 15pF$	4			ns
Data and Address Setup Time	$t_{su(DA)}$	$C_{Load} = 15pF$	29			ns
Data and Address Hold Time	$t_{h(DA)}$	$C_{Load} = 15pF$	0			ns
Chip Select Hold Time	$t_{h(CS)}$	$C_{Load} = 15pF$	0			ns
Write Pulse Duration HIGH	$t_{wH(WE)}$	$C_{Load} = 15pF$	15			ns

Note

1.   Data is written to the addressed register at the rising edge of WEB. All timing parameters refer to a 50% level.

DEVICE DESCRIPTION

INTRODUCTION

The WM2184 is a fast, low-power 14-bit ADC designed for leading edge telecommunications applications such as xDSL front-ends. It consists of a high bandwidth programmable gain input stage, a high resolution ADC, a parallel control interface, and internal voltage reference circuitry. Its fully differential design gives it excellent noise immunity.

The analogue signal first enters the programmable gain amplifier (PGA), whose gain can be controlled in 1dB steps between 0dB and 7dB, using the PGA gain register. The signal is then digitised with respect to the two reference voltages, V_{REF+} and V_{REF-}, in the ADC core. To compensate for DC offsets in the system, a programmable value of between -128 and +127 LSBs can be added to the digitised data. This is achieved by writing the offset value to the offset register and setting the DCO bit (bit 7) in the control register.

Two different output formats are supported to suit the user's needs. In unsigned binary format, an all-zero output represents the minimum analogue input level, while in two's complement format it refers to the middle level between minimum and maximum (see Table 1, below).

ANALOGUE INPUT		DIGITAL OUTPUT (Unsigned Binary)	DIGITAL OUTPUT (Two's Complement)
Minimum	$\Delta V_{IN} = -\Delta V_{REF}$	0	-8192
Midrange	$\Delta V_{IN} = 0$	8192	0
Maximum	$\Delta V_{IN} = \Delta V_{REF}$	16383	8191

Table 1 Unsigned Binary vs Two's Complement Output Format

The out-of-range indicator (OVI) output indicates that the analogue input signal is out of range. It is asserted whenever the differential input voltage ΔV_{IN} exceeds the differential reference voltage ΔV_{REF} or $-\Delta V_{REF}$. This signal is updated simultaneously with the digital data outputs and is subject to the same pipeline delay. It can be used to adjust the gain of the internal PGA to prevent the ADC from clipping.

The WM2148 incorporates a differential voltage reference circuit based on a 1.5V bandgap reference. The two reference voltages derived from the bandgap, V_{REF+} and V_{REF-}, are two-thirds above and below the bandgap voltage V_{BG}, at 2.5V and 0.5V respectively. The analogue input range is between the two references. To use an external reference, the on-chip bandgap circuit is disabled by setting the REF bit (bit 12) in the control register. The external reference voltage can then be applied at the VBG pin. V_{REF+} and V_{REF-} are still buffered in the same by the internal reference amplifiers, such that:

$$V_{REF+} = V_{BG} \times \left(1 + \frac{2}{3}\right) \qquad \text{and} \qquad V_{REF-} = V_{BG} \times \left(1 - \frac{2}{3}\right)$$

For best performance, V_{BG}, V_{REF+}, V_{REF-} and CML (reference midpoint, pin 4) should all be separately decoupled (see Recommended External Components).

The WM2184 requires a single 3.3V supply voltage. In Power Down mode, the supply to all analogue circuitry in the device is switched off, reducing standby current to 20µA provided that the clock is stopped (a running clock will increase the power consumption of the digital sections).

CONTROL INTERFACE

All functions of the WM2184 are accessed through its parallel interface. There are four internal registers to retrieve the ADC conversion data, set the device gain and DC offset, and control other features such as Power Down, reference voltage and output format.

The parallel interface of the WM2148 features three-state buffers for direct connection to a shared data bus. Driving the OEB pin low enables the output buffers.

ADDRESS	A1	A0	REGISTER
0	0	0	ADC Conversion Result
1	0	1	PGA gain
2	1	0	DC Offset
3	1	1	Control

Table 2 WM2148 Internal Registers

The ADC data register contains the result of the last analogue to digital conversion. It can also be used to reset the device to its default state by writing a '1' to the LSB (D0). This will set all the bits in the gain, offset and control registers to '0'. All other bits should always be set to zero when writing to the ADC data register.

The PGA gain is controlled using the last three bits of Address 1. The eight possible binary values of 000 to 111 (decimal 7) correspond to a gain of 0 to 7dB, respectively.

The lower byte of Address 2 holds the offset value (in LSBs). This value is added to the ADC data if the DCO bit in the Control register is set. The offset is in Two's complement format, providing a range of -128 to +127 LSB.

REG. / BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADC Data	MSB	…	…	…	…	…	…	…	…	…	…	…	…	LSB/SR
PGA Gain	X	X	X	X	X	X	X	X	X	X	X	G2	G1	G0
DC Offset	X	X	X	X	X	X	MSB	…	…	…	…	…	…	LSB
Control	PWD	REF	FOR	TM2	TM1	TM0	DCO	X	X	X	X	X	X	X

Table 3 WM2148 Register Map

The Control register (address 3) has four bits to program the device's operation and three test mode bits. Setting the Power Down bit (PWD) takes the device into Power Down mode. DCO enables the addition of the offset value held at Address 2 to the ADC output data. REF selects between internal and external reference voltages, and FOR between unsigned binary and Two's complement output format.

BIT	DESCRIPTION	0	1
PWD	Power Down	Normal Operation	Power Down
REF	Reference Select	Internal Reference	External Reference
FOR	Output Format	Unsigned Binary	Two's Complement
DCO	DC Offset	Enable	Disable
SR	Software Reset	Normal Operation	Reset
X	Reserved	Always set to 0 when writing to any register.	

Table 4 Control Bits and Software Reset

The ADC core can be tested by selecting one of six different test modes, which apply various voltages to the analogue inputs. This may be useful for calibration purposes. The test modes are controlled by the three test mode bits in the control register, TM0 to TM2 (see Table 5 below).

TM2	TM1	TM0	FUNCTION
0	0	0	Normal Operation
0	0	1	Both inputs = REF-
0	1	0	IN+ at V_{ref}/2, IN- at REF-
0	1	1	IN+ at REF+, IN- at REF-
1	0	0	Normal Operation
1	0	1	Both inputs = REF+
1	1	0	IN+ at REF-, IN- at V_{ref}/2
1	1	1	IN+ at REF-, IN- at REF+

Table 5 Test Modes

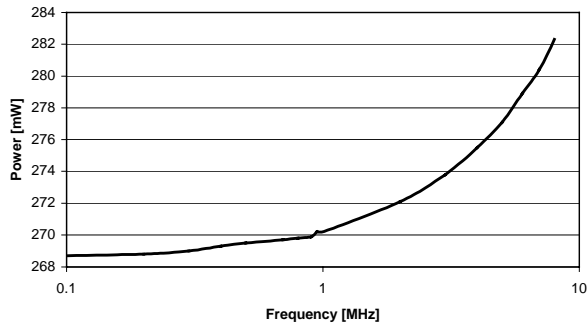## PERFORMANCE DATA (TYPICAL)

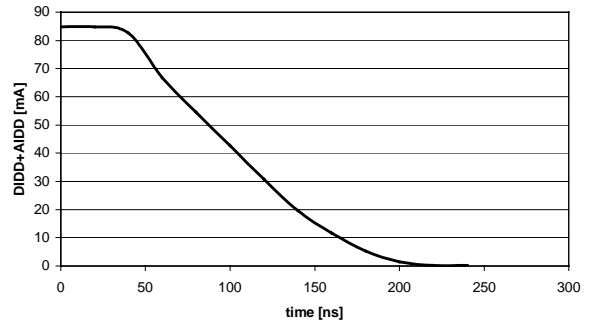**Figure 4 Power Consumption vs Sample Clock**

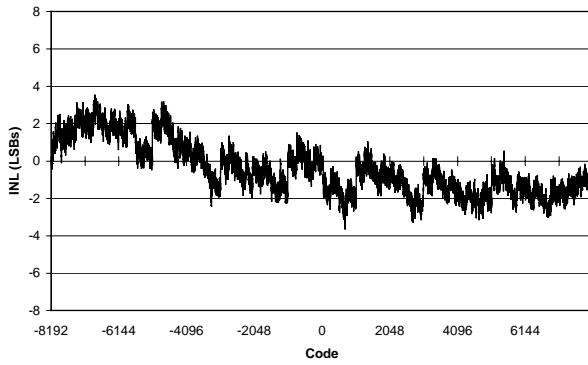**Figure 5 Supply Current vs Time (Power Down)**
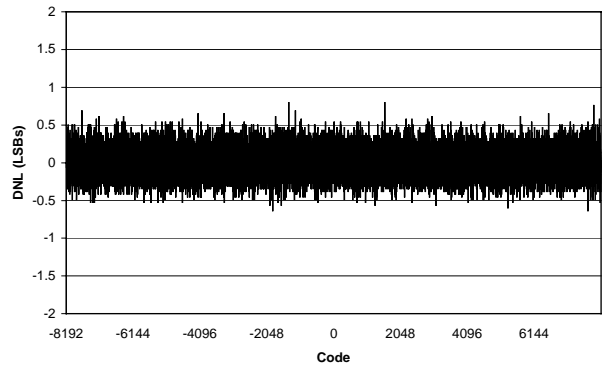
Figure 6 Integral Nonlinearity at 8MSPS

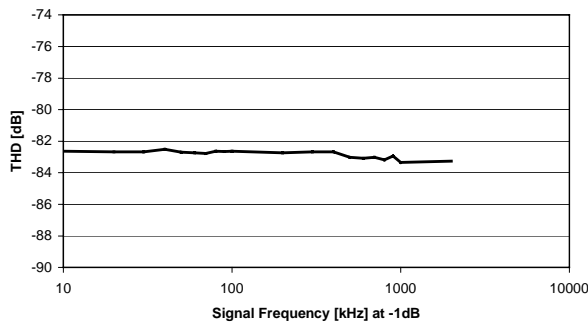**Figure 7 Differential Nonlinearity at 8MSPS**

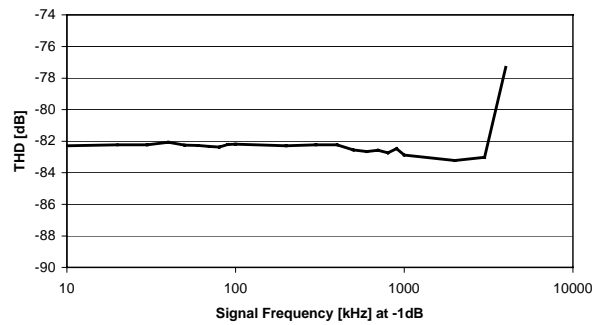**Figure 8 Total Harmonic Distortion at 3MSPS**
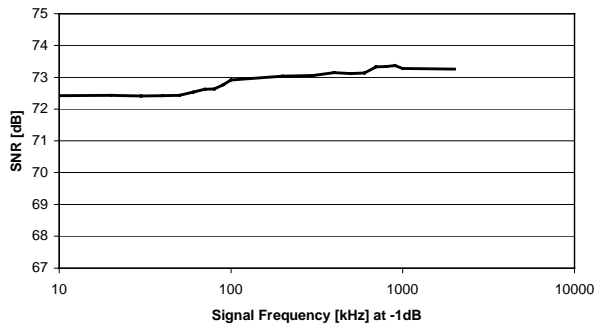
Figure 9 Total Harmonic Distortion at 8MSPS

Figure 10 Signal to Noise Ratio at 3MSPS
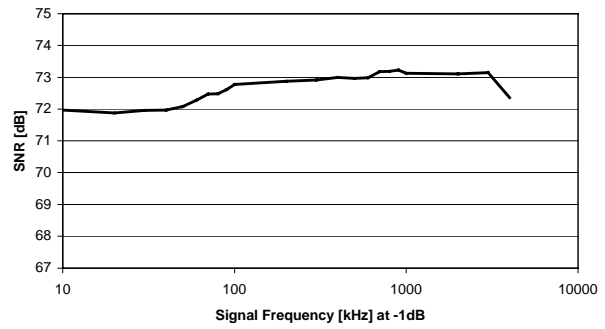

Figure 11 Signal to Noise Ratio at 8MSPS

APPLICATION INFORMATION

DRIVING THE ANALOGUE INPUT

The WM2148 has a fully differential input. This is advantageous for signal to noise ratio, spurious free dynamic range, and harmonic distortion. It is recommended that the analogue input pins IN+ and IN- are connected as shown in Figure 12 below.
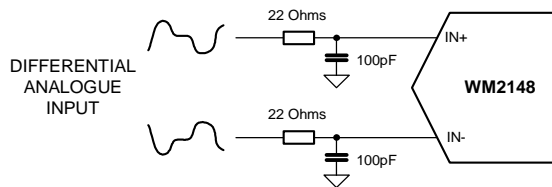

Figure 12 Recommended Input Configuration

In this configuration, the ADC converts the difference ΔV_{IN} of the two input signals V_{IN+} and V_{IN-}. The resistors and capacitors on the inputs decouple the driving source output from the ADC and also serve as first order low pass filters to reduce out of band noise.

The input range on both inputs is 0V to AV_{DD}. The full-scale value is determined by the voltage reference. The positive full-scale output is reached when ΔV_{IN} equals ΔV_{REF}, and the negative full-scale output is reached when ΔV_{IN} equals $-\Delta V_{REF}$.

ΔV_{IN}	OUTPUT
$-\Delta V_{REF}$	- full scale
0	0
ΔV_{REF}	+ full scale

DIGITAL I/O

The digital outputs of the WM2148 are 3V CMOS compatible. In order to avoid current feedback errors, the capacitive load on these outputs should be as low as possible (maximum 15pF). Adding 100Ω series resistors on the digital outputs cam improve system performance by limiting the current during output transitions (this reduces noise on the power supplies).
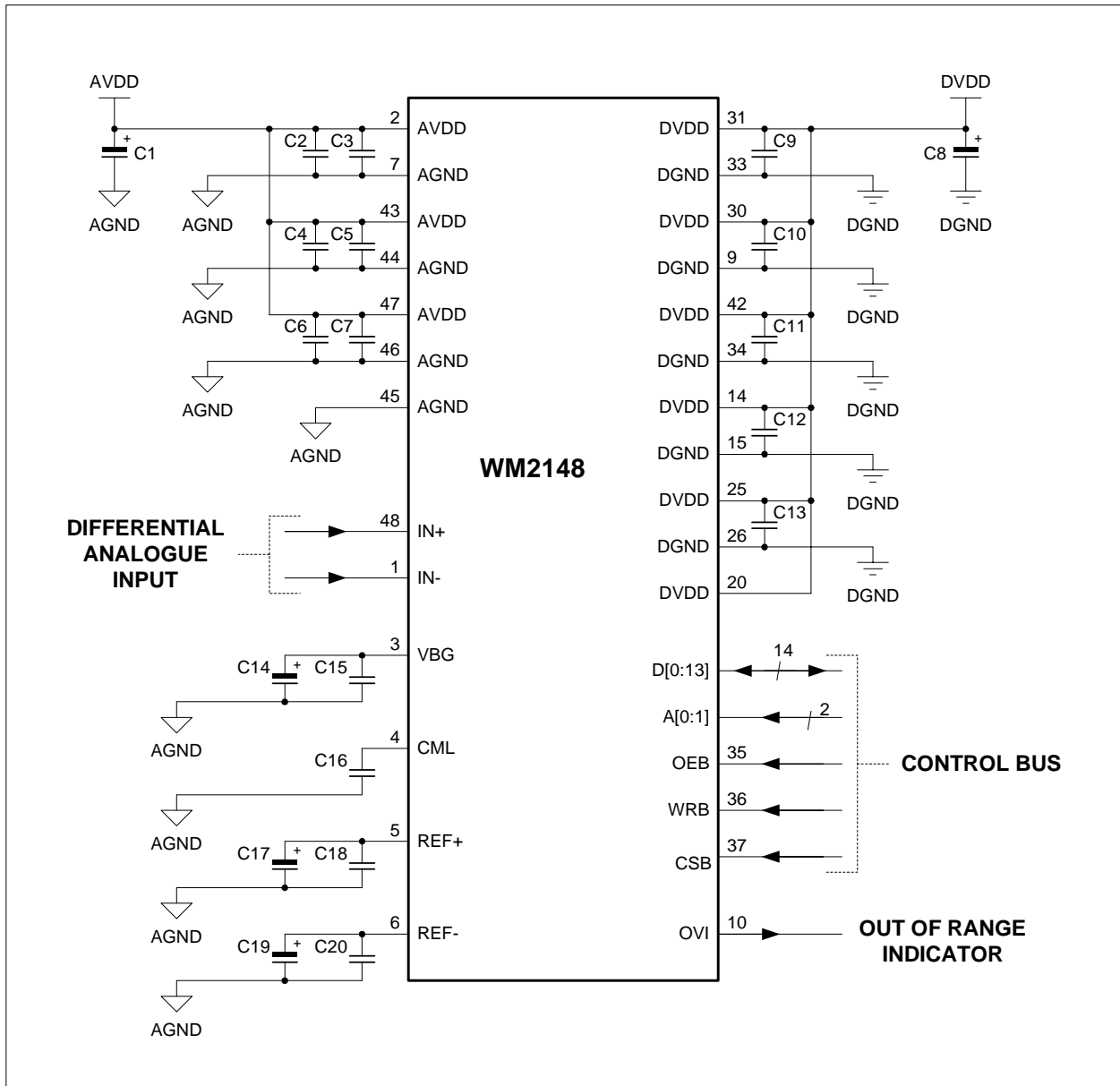
RECOMMENDED EXTERNAL COMPONENTS

Figure 13 External Components Diagram

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	10μF	Analogue Supply Decoupling
C2	0.1μF	Supply Decoupling for Reference Block
C3	470pF	Supply Decoupling for Reference Block - place as close to the IC as possible
C4	0.1μF	Supply Decoupling for ADC
C5	470pF	Supply Decoupling for ADC - place as close to the IC as possible
C6	0.1μF	Supply Decoupling for ADC Op-amps
C7	470pF	Supply Decoupling for ADC Op-amps - place as close to the IC as possible (most critical for ADC performance)
C8	10μF	Digital Supply Decoupling
C9	0.1μF	Supply Decoupling Clock Buffers - place as close to the IC as possible to eliminate clock jitter
C10	0.1μF	Supply Decoupling for Core Logic
C11	0.1μF	Supply Decoupling for Control Block
C12, C13	0.1μF	Supply Decoupling for Output Drivers
C14, C17, C19	10μF	Reference Decoupling
C15, C16, C18, C20	0.1μf	Reference Decoupling - place as close to the IC as possible

Table 6 External Components Values and Description

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm)   **DM004.C**
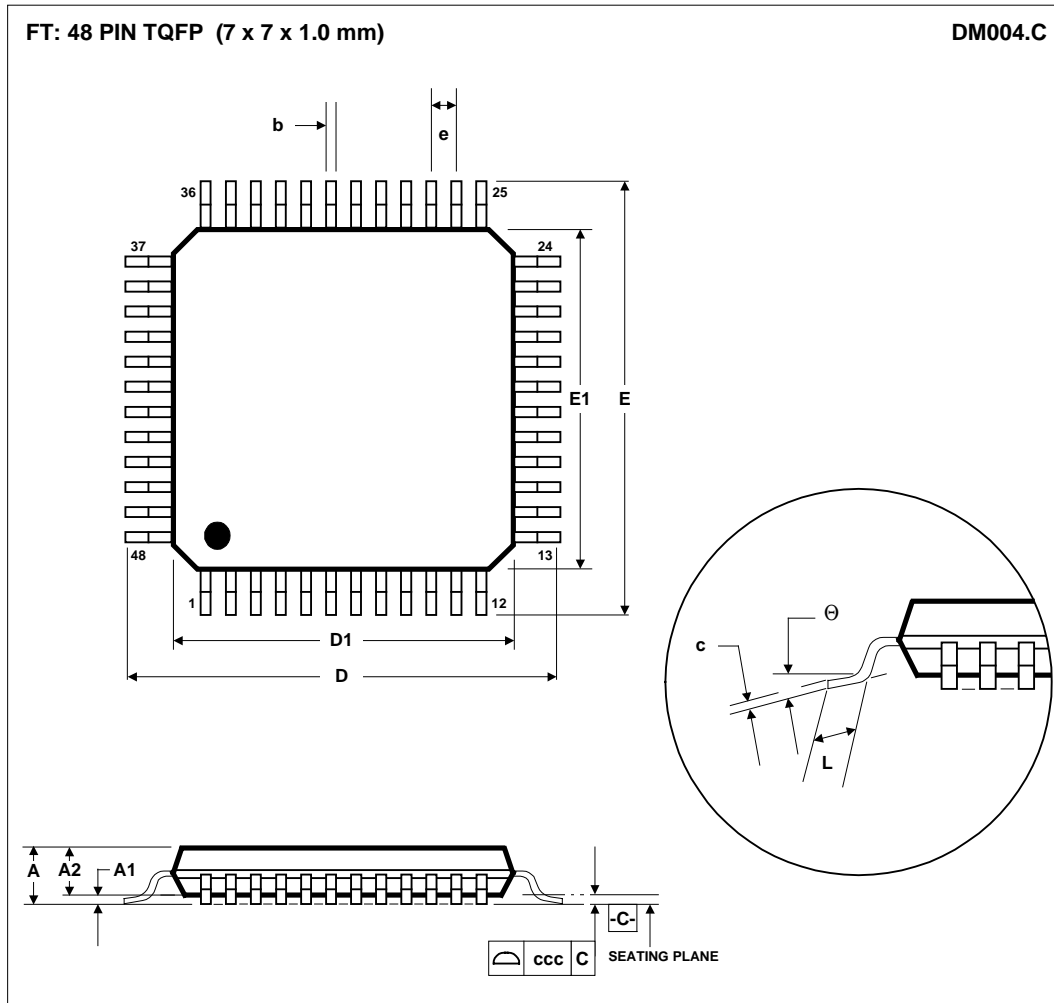
Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A$_1$	0.05	-----	0.15
A$_2$	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D$_1$	7.00 BSC		
E	9.00 BSC		
E$_1$	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
	Tolerances of Form and Position		
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.