WM7230E

Bottom Port Digital Silicon Microphone

DESCRIPTION

The WM7230 is a low-profile silicon digital microphone. It offers high Signal to Noise Ratio (SNR) and low power consumption and is suited to a wide variety of consumer applications.

The WM7230 incorporates Cirrus Logic proprietary CMOS/MEMS membrane technology, offering high reliability and high performance in a miniature, low-profile package. The WM7230 is designed to withstand the high temperatures associated with automated flow solder assembly processes. (Note that conventional microphones can be damaged by this process.)

The WM7230 incorporates a high performance ADC, which outputs a single-bit data stream using Pulse Density Modulation (PDM) encoding. The WM7230 supports selectable left/right channel assignment for a two-channel digital microphone interface, enabling efficient connection of multiple microphones in stereo/array configurations.

The WM7230 offers tight tolerance on the microphone sensitivity, giving reduced variation between parts. This removes the need for in-line production calibration of part-to-part microphone variations.

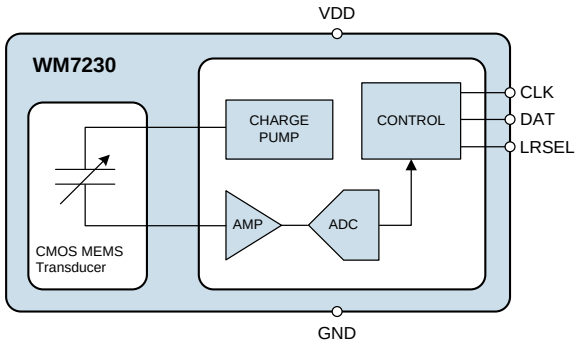
FEATURES

- High SNR (61dB)
- Low variation in sensitivity (±1dB tolerance)
- Low current consumption
  - 2µA (Sleep)
  - 735µA (Normal operation)
- PDM digital audio output
- Stereo/array operation
- Proprietary ADC technology
  - Reduced clock jitter sensitivity
  - Low noise floor
  - Stable in overload condition
- Bottom Port LGA Package
- 1.64V to 3.7V supply

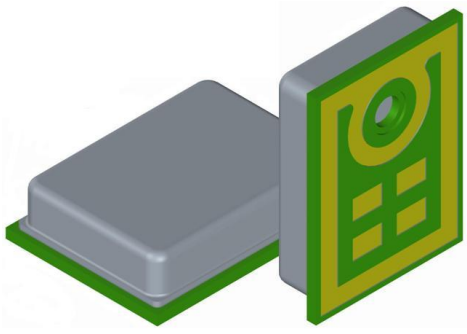
APPLICATIONS

- Mobile telephone handsets
- Portable computers
- Portable media players
- Digital still cameras
- Digital video cameras
- Bluetooth™ headsets
- Portable navigation devices

BLOCK DIAGRAM



3D VIEW



4.00mm x 3.00mm x 1.00mm LGA package

Pre-Production

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product.

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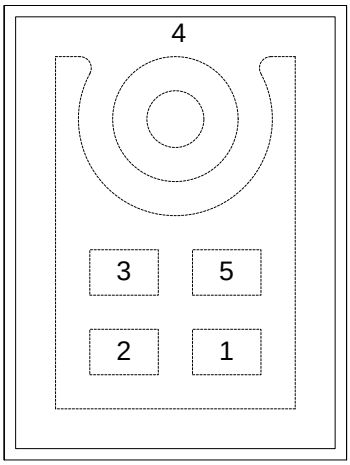
PIN CONFIGURATION



TOP VIEW

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	CLK	Digital Input	Clock input
2	DAT	Digital Output	PDM Data Output
3	VDD	Supply	Power Supply
4	GND	Supply	Ground
5	LRSEL	Digital Input	Channel Select 0 = Data output following falling CLK edge 1 = Data output following rising CLK edge Internal pull-down holds this pin at logic 0 when not connected

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM7230IMSE/RV	-40 to +100°C	LGA (tape and reel)	MSL2A	+260°C

Note:

Reel quantity = 4800

All devices are Pb-free and Halogen free.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL2A = out of bag storage for 4 weeks at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply Voltage (VDD)	-0.3V	+4.2V
Voltage range digital inputs (LRSEL, CLK)	GND - 0.3V	4.0V (see note)
Operating temperature range, T_A	-40°C	+100°C
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-40°C	+100°C

Note:

If VDD is above the minimum recommended operating level, the maximum input voltage is VDD + 0.3V.

IMPORTANT ASSEMBLY GUIDELINES

Do not put a vacuum over the port hole of the microphone. Placing a vacuum over the port hole can damage the device.

Do not board wash the microphone after a re-flow process. Board washing and the associated cleaning agents can damage the device. Do not expose to ultrasonic cleaning methods.

Do not use vapour phase re-flow process. The vapour can damage the device.

Please refer to application note WAN0273 (MEMS MIC Assembly and Handling Guidelines) for further assembly and handling guidelines.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
VDD Supply Range	VDD	1.64		3.7	V
Ground	GND		0		V
Clock Frequency	F_{CLK}	1		3.25	MHz

ACOUSTIC AND ELECTRICAL CHARACTERISTICS

Test Conditions: VDD=1.8V, 1kHz test signal, CLK=2.4MHz, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Directivity			Omni-directional			
Polarity (see note)		Positive sound pressure	Decreasing density of 1s			
Sensitivity	S	94 dB SPL	-27	-26	-25	dBFS
Acoustic Overload		No load, THD < 10%		120		dB SPL
Total Harmonic Distortion	THD	94dB SPL		0.1		%
		114dB SPL		0.5		
		117.5dB SPL		1		
Signal to Noise Ratio	SNR	A-weighted		61		dB
Dynamic Range	DR	A-weighted		84.5		dB
Acoustic Noise Floor		A-weighted		33		dB SPL
Electrical Noise Floor		A-weighted		-87		dBFS
Frequency Response		+3dB high frequency		17000		Hz
Frequency Response Flatness		200Hz to 8kHz	-1		+1	dB
Power Supply Rejection	PSR	217Hz square wave, 100mV (peak-peak)		-75		dBFS
Digital Input / Output						
CLK Input HIGH Level	V_{IH}		0.65 x VDD			V
CLK Input LOW Level	V_{IL}				0.35 x VDD	V
DAT Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9 x VDD			V
DAT Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 x VDD	V
Input capacitance (CLK)				0.5		pF
Input leakage					1	µA
Maximum load capacitance (DAT)	C_{LOAD}				100	pF
Short Circuit Output Current	I_{SC}	DAT connected to GND			10	mA
Miscellaneous						
Current Consumption	I_{VDD}	Active Mode		735		µA
		Sleep Mode		2	10	
Start-up Time		From OFF		10		ms
		From Sleep		10		
CLK Sleep Frequency					1.0	kHz

Note: The WM7230 generates a single-bit digital (PDM) output in response to the acoustic input. A positive sound pressure on the diaphragm generates a decreasing density of 1's in the PDM stream (ie. there is a phase inversion between the acoustic input and the digital output).

TERMINOLOGY

1. Sensitivity (dBFS) – Sensitivity is a measure of the microphone output response to the acoustic pressure of a 1kHz 94dB SPL (1Pa RMS) sine wave. This is referenced to the output Full Scale Range (FSR) of the microphone.
2. Full Scale Range (FSR) - Sensitivity, Electrical Noise Floor and Power Supply Rejection are measured with reference to the output Full Scale Range (FSR) of the microphone. FSR is defined as the amplitude of a 1kHz sine wave output whose positive peak value reaches 100% density of logic 1s and whose negative peak value reaches 0% density of logic 1s. This is the largest 1kHz sine wave that will fit in the digital output range without clipping. Note that, because the definition of FSR is based on a sine wave, it is possible to support a square wave test signal output whose level is +3dBFS.
3. Total Harmonic Distortion (%) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
4. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the output response of a 1kHz 94dB SPL sine wave and the idle noise output.
5. Dynamic Range (dB) – DR is the ratio of the 1% THD microphone output level (in response to a sine wave input) and the idle noise output level.
6. All performance measurements are carried out within a 20Hz to 20kHz bandwidth and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR values than are found in the Acoustic and Electrical Characteristics. The brick wall filter removes out-of-band noise.
7. Sleep Mode is enabled when the CLK input is below the CLK Sleep Frequency noted above. This is a power-saving mode. Normal operation resumes automatically when the CLK input is above the CLK Sleep Frequency. Note that the VDD supply is still required in Sleep mode.

AUDIO INTERFACE TIMING

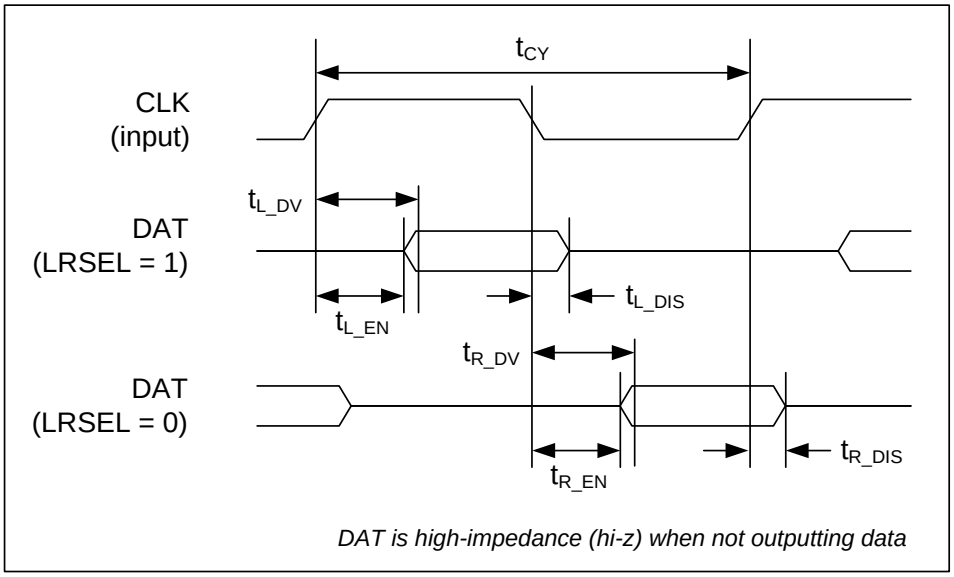


Figure 1 Digital Microphone Interface Timing

Test Conditions

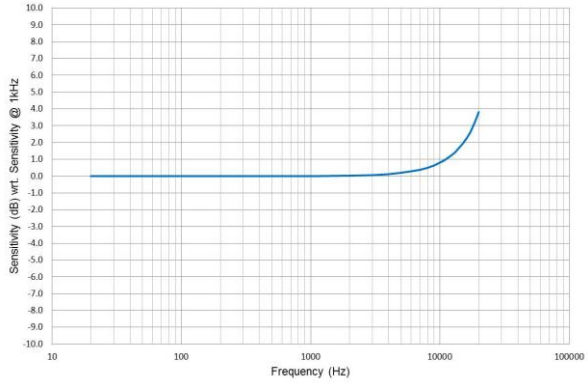
The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
CLK cycle time	t_{CY}	308		1000	ns
CLK duty cycle		60:40		40:60	
CLK rise/fall time				6	ns
DAT enable from rising CLK edge (LRSEL = 1)	t_{L_EN}	14			ns
DAT valid from rising CLK edge (LRSEL = 1)	t_{L_DV}	20		90	ns
DAT disable from falling CLK edge (LRSEL = 1)	t_{L_DIS}			16	ns
DAT enable from falling CLK edge (LRSEL = 0)	t_{R_EN}	14			ns
DAT valid from falling CLK edge (LRSEL = 0)	t_{R_DV}	20		90	ns
DAT disable from rising CLK edge (LRSEL = 0)	t_{R_DIS}			16	ns

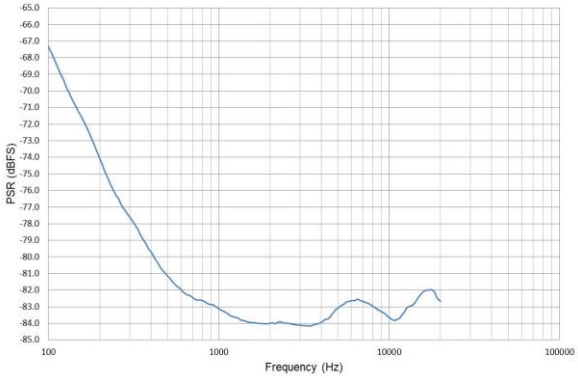
Notes:

1. The DAT output is high-impedance when not outputting data; this enables the outputs of two microphones to be connected together with the data from one microphone interleaved with the data from the other. (The microphones must be configured to transmit on opposite channels in this case.)
2. In a typical configuration, the Left channel is transmitted following the rising CLK edge (LRSEL = 1). In this case, the Left channel should be sampled by the receiving device on the falling CLK edge.
3. Similarly, the Right channel is typically transmitted following the falling CLK edge (LRSEL = 0). In this case, the Right channel should be sampled by the receiving device on the rising CLK edge.
4. The WM7230 operating mode is selected according to the CLK frequency; see “Acoustic and Electrical Characteristics” for further details.

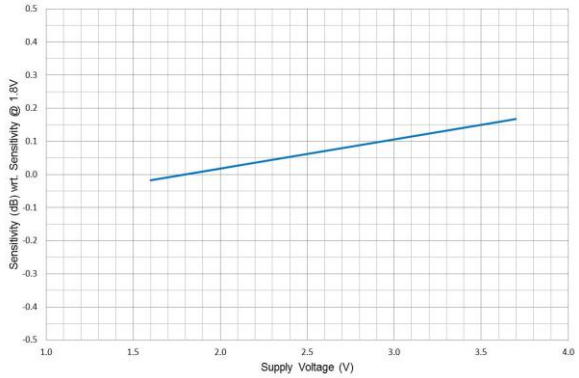
TYPICAL PERFORMANCE



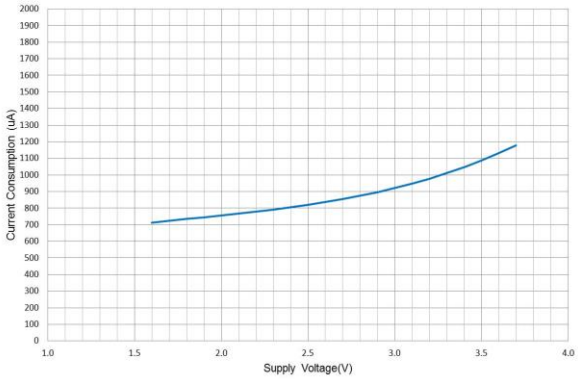
Sensitivity vs. Frequency



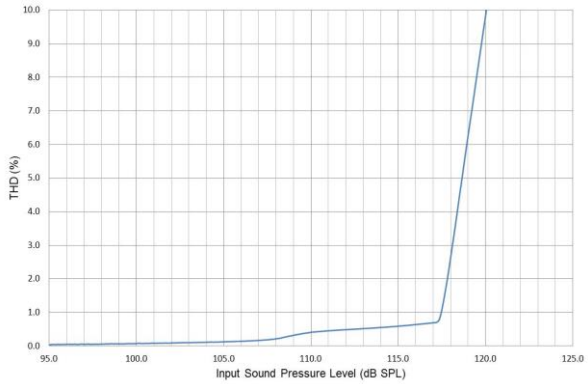
PSR vs. Frequency



Sensitivity vs. Supply Voltage



Current Consumption vs. Supply Voltage



THD vs. Sound Pressure Level

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

It is recommended to connect a 0.1µF decoupling capacitor between the VDD and GND pins of the WM7230. A ceramic 0.1µF capacitor with X7R dielectric or better is suitable. The capacitor should be placed as close to the WM7230 as possible.

OPTIMISED SYSTEM RF DESIGN

For optimised RF design please refer to document WAN0278 (Recommended PCB Layout for Microphone RF Immunity in Mobile Cell Phone Applications) for further information.

CONNECTION TO A CIRRUS LOGIC AUDIO CODEC

Cirrus Logic provides a range of audio CODECs incorporating a digital microphone input interface; these support direction connection to digital microphones such as the WM7230.

Stereo connection of two WM7230 digital microphones is illustrated in Figure 2.

Further information on Cirrus Logic audio CODECs is provided in the respective product datasheet, which is available from the Cirrus Logic website.

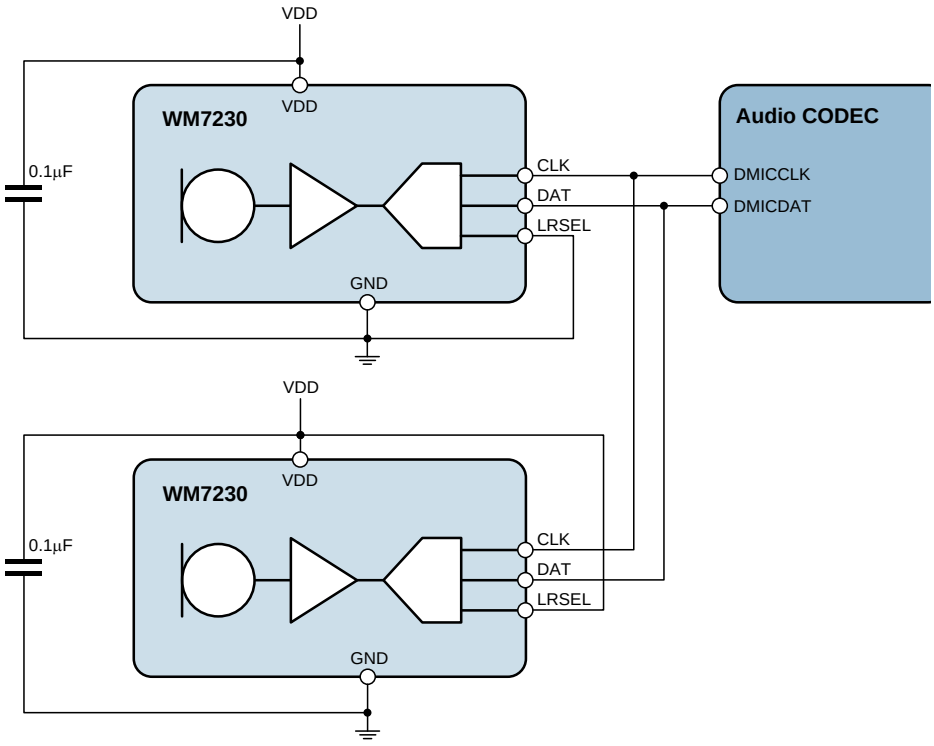


Figure 2 Stereo WM7230 Digital Microphone Connection

PCB LAND PATTERN AND PASTE STENCIL

The recommended PCB Land Pattern and Paste Stencil Pattern for the WM7236 microphone are shown in Figure 3 and Figure 4.

See also Application Note WAN0284 (General Design Considerations for MEMS Microphones) for further details of PCB footprint design.

Full definition of the package dimensions is provided in the “Package Dimensions” section.

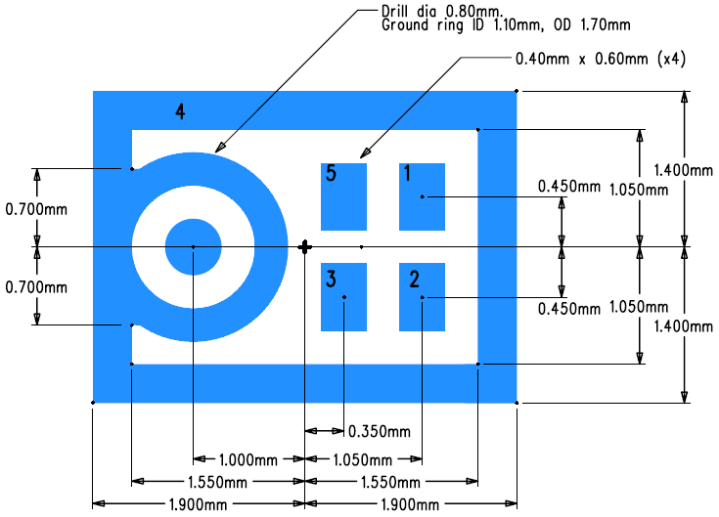


Figure 3 DM089 - PCB Land Pattern, Top View

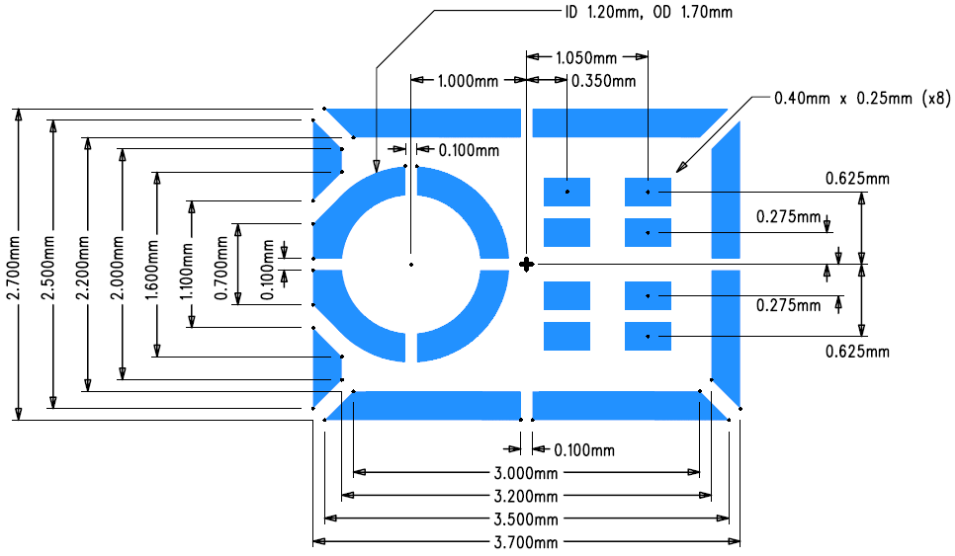
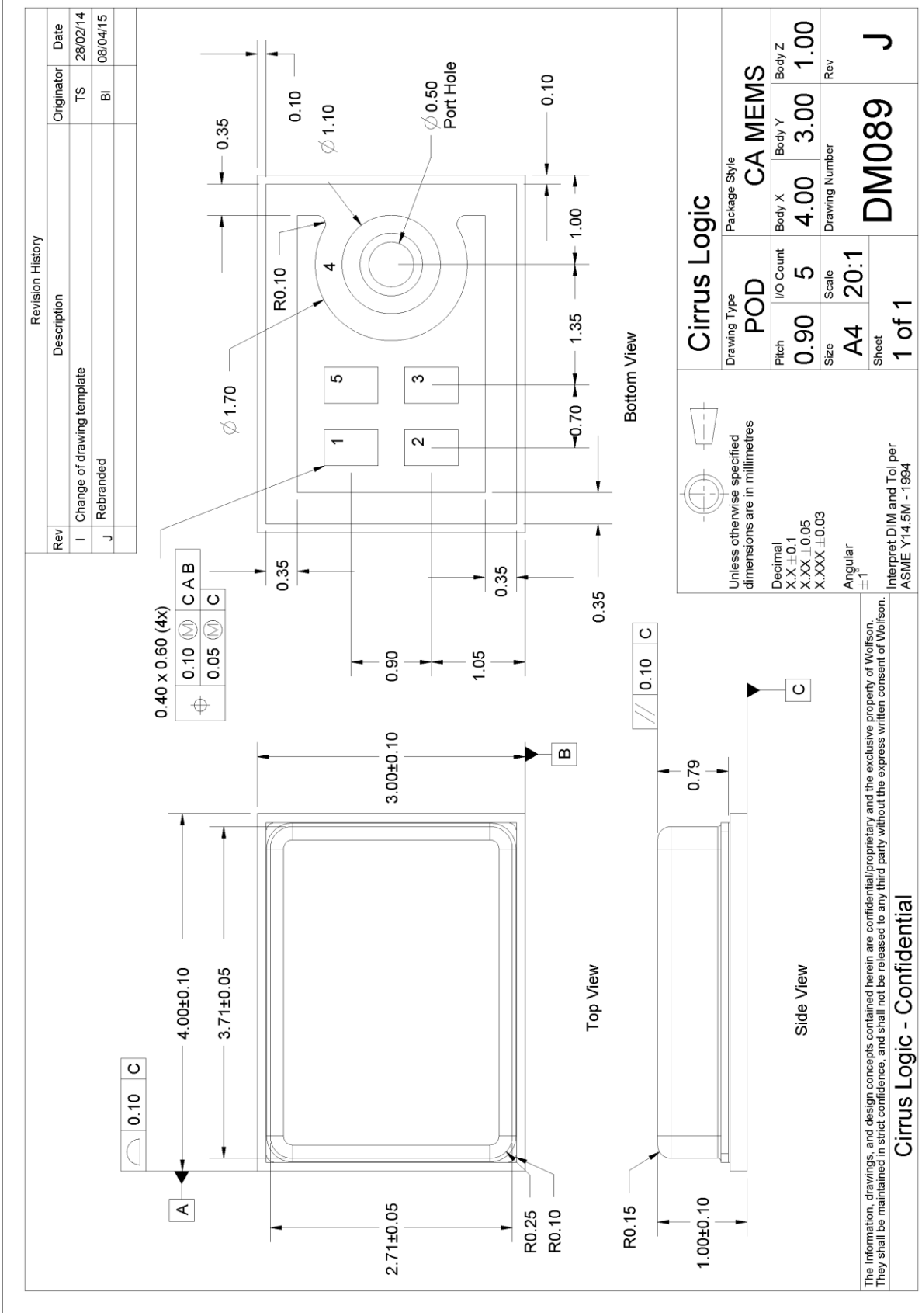


Figure 4 DM089 – Paste Stencil Pattern, Top View

PACKAGE DIMENSIONS



IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
20/10/10	2.0	Front page description and features re-worded. Description of LRSEL pin updated. Electrical Characteristics re-ordered, and terminology updated. Microphone interface timing drawing and descriptions updated. Frequency response graph added. Illustration of external components replaced with text. Connection to Wolfson CODEC text and illustration updated. Recommended PCB land patterns moved to Applications Information.		PH
26/10/10	2.0	Package Diagram DM089.D added		JMacD
23/11/10	2.0	Specification of FSR corrected. Specification for THD corrected Time to data valid changed to minimum		CST
28/01/11	2.0	Reel quantity added to order information		JMacD
06/09/11	2.1	Updated the LRSEL pin description, Timing diagram and notes for the rising and falling clock edges. Sleep mode current updated to 2uA Updated the reel quantity Updated the start up time Updated the new freq response and THD curves Updated +3dB frequency cut off Updated VDD to 1.64V Package Diagram updated to DM089.E. References and dimension letters changed to be consistent with all mems package diagrams. Lid dimensions updated. Swapped dimensions L and E. Added marking area boundary		JMacD
16/12/11	2.2	Introduced E variant with sensitivity +/-1dB Added E variant ordering info Added voltage range digital input Updated the CODEC to WM8994 Added Reference to WAN_0273		KC
22/06/12	2.3	Dynamic Range added, p5 Active mode current changed to 700uA, p1 and p5 CLK cycle time min and max updated, p6 Package Diagram updated to DM089F		MR/JMacD
08/10/12	2.4	Optimised System RF Design added.		JMacD
17/06/13	2.5	Package Diagram updated to DM089.G		JMacD
11/11/13	3.1	Updated to pre-production status. Package Diagram updated – port hole tolerance added. Updated CODEC reference to WM8280.		JMacD
18/12/13	3.1	Acoustic and Electrical Characteristics updated: Polarity added, PSR updated, Note added		MR
29/09/14	3.2	Formatting updates throughout document Electrical Characteristics & Timing Requirements updated Typical Performance graphs added PCB Paste Stencil information & Package Drawing updated	 5-7 8 10-11	PH
11/11/15	3.3	Maximum input voltage updated. Electrical Characteristics updated.	4 5	PH