



Stereo DAC with Integrated Tone Generator and Line/Variable Level Outputs

Advanced Information, May 2000, Rev 1.5

DESCRIPTION

The WM8722 is a high performance stereo DAC designed for audio applications such as digital TV and set top boxes. The WM8722 has two stereo analogue outputs, one at line level and one that includes a digitally controllable mute and attenuator function. An on-board tone generator can be routed through the line or variable outputs.

WM8722 supports data input word lengths from 16-24 bits and sampling rates up to 96kHz. The WM8722 consists of a serial interface port, digital interpolation filter, multi-bit sigma delta modulator and stereo DAC in a small 20-pin SSOP package.

The 3 or 2-wire serial MPU compatible control port provides access to all features including tone generation, on-chip mute, attenuation and phase reversal.

The programmable data input port supports glueless interfaces to popular DSPs, audio decoders and S/PDIF and AES/EBU receivers.

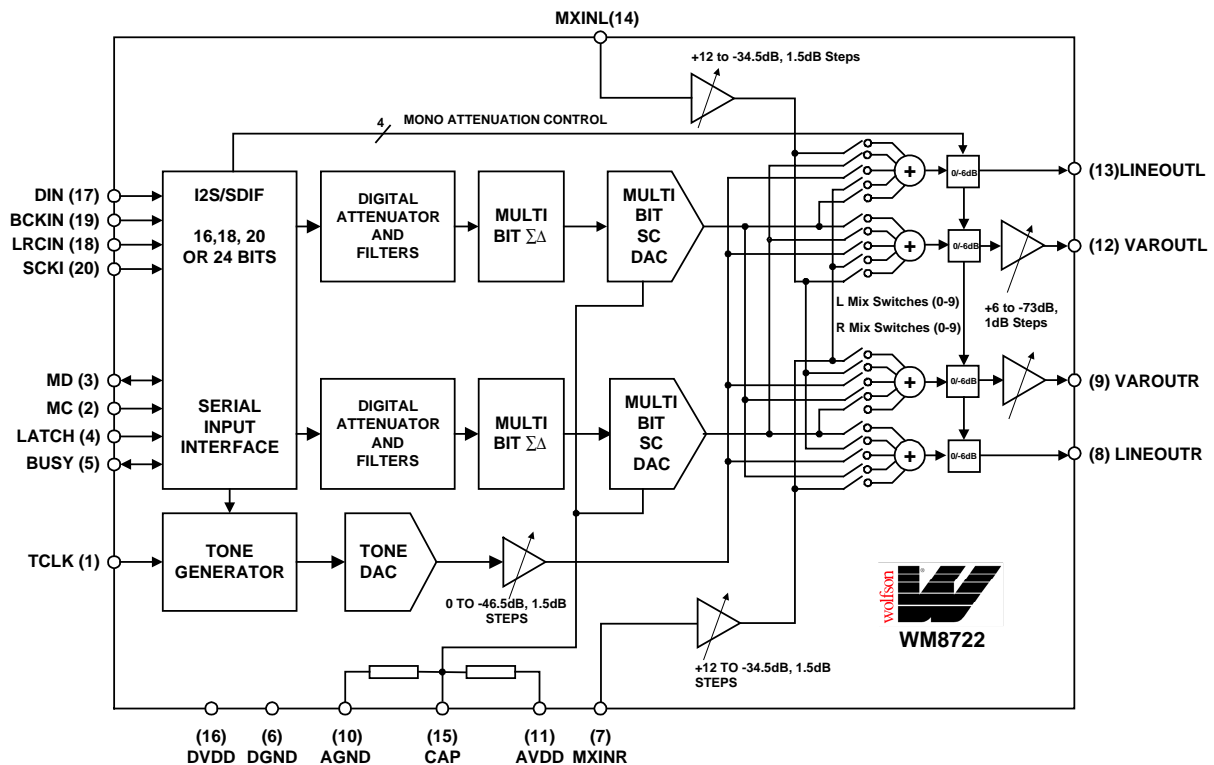
FEATURES

- Performance
 - 102dB SNR ('A' weighted @48kHz)
 - THD+N: -90dB @ F.S.
 - 5V or 3V supply operation
 - Sampling frequency: 8kHz – 96kHz
- 3-wire or 2-wire serial MPU compatible interface for
 - Input data word; 16/20/24-Bit
 - Soft mute
 - De-emphasis
 - Volume control
- On-board tone generator (1Hz – 32kHz, 0.1 – 25.5s)
- Stereo analogue inputs
- 20-pin SSOP package

APPLICATIONS

- Digital TV
- Digital broadcast receivers
- Set top boxes

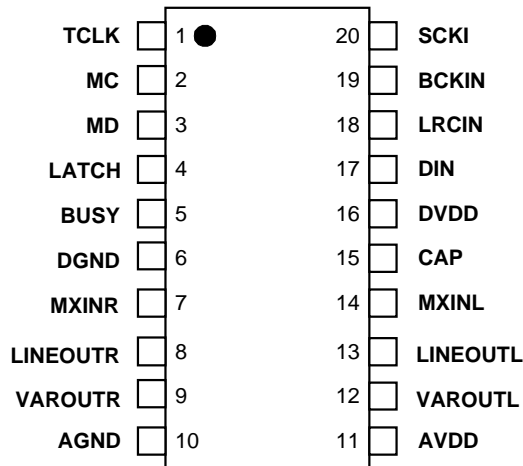
BLOCK DIAGRAM



WOLFSON MICROELECTRONICS LTD
Lutton Court, Bernard Terrace, Edinburgh, EH8 9NX, UK
Tel: +44 (0) 131 667 9386
Fax: +44 (0) 131 667 5176
Email: sales@wolfson.co.uk
http://www.wolfson.co.uk

Advanced Information data sheets contain preliminary data on new products in the preproduction phase of development. Supplementary data will be published at a later date.

PIN CONFIGURATION



ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE |
|------------|--------------|-------------|
| XWM8722EDS | -25 to +85°C | 20-pin SSOP |

PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|-----|----------|-----------------|--|
| 1 | TCLK | Digital input | Tone generator master-clock input. |
| 2 | MC | Digital input | Serial control data clock input (SPI mode) or 2-wire clock input (2-wire mode) |
| 3 | MD | Digital input | Serial control data input (SPI mode) or 2-wire data input (2-wire mode) |
| 4 | LATCH | Digital input | Latch enable (SPI mode) or address select (2-wire mode). |
| 5 | BUSY | Digital I/O | Interface format input pin (0= SPI; 1 = 2-WIRE) or BUSY flag output. |
| 6 | DGND | Supply | Digital ground supply. |
| 7 | MXINR | Analogue input | Analogue mixer input (right channel). |
| 8 | VAROUTR | Analogue output | Right channel mixer output (variable level). |
| 9 | LINEOUTR | Analogue output | Right channel mixer output (line level). |
| 10 | AGND | Supply | Analogue ground supply. |
| 11 | AVDD | Supply | Analogue positive supply. |
| 12 | LINEOUTL | Analogue output | Left channel mixer output (line level). |
| 13 | VAROUTL | Analogue output | Left channel mixer output (variable level). |
| 14 | MXINL | Analogue input | Analogue mixer input (left channel). |
| 15 | CAP | Analogue output | Analogue internal reference. |
| 16 | DVDD | Supply | Digital positive supply. |
| 17 | DIN | Digital input | Serial audio data input. |
| 18 | LRCIN | Digital input | Sample rate clock input. |
| 19 | BCKIN | Digital input | Audio data bit clock input. |
| 20 | SCKI | Digital input | System clock input (256 or 384fs). |

Note: 1. Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

| CONDITION | MIN | MAX |
|---|------------|------------|
| Digital supply voltage | -0.3V | +7V |
| Analogue supply voltage | -0.3V | +7V |
| Voltage range digital inputs | DGND -0.3V | DVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Operating temperature range, T _A | 0°C | +70°C |
| Storage temperature | -65°C | +150°C |
| Package body temperature (soldering 10 seconds) | | +240°C |
| Package body temperature (soldering 2 seconds) | | +183°C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|-------------|-----------------|------|----------|------|------|
| Digital supply range | DVDD | | -10% | 3.3 to 5 | +10% | V |
| Analogue supply range | AVDD | | -10% | 3.3 to 5 | +10% | V |
| Ground | AGND, DGND | | | 0 | | V |
| Difference DGND to AGND | | | -0.3 | 0 | +0.3 | V |
| Analogue supply current | AVDD = 5V | | | 35 | | mA |
| Digital supply current | DVDD = 5V | | | 15 | | mA |
| Analogue supply current | AVDD = 3.3V | | | tba | | mA |
| Digital supply current | DVDD = 3.3V | | | tba | | mA |

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, f_s = 48kHz, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------------|---|-------------|---------|-------------|------------------|
| DAC Circuit Specifications | | | | | | |
| SNR (Note 1 and 2) | | AVDD, DVDD = 5V, f _s = 48kHz | 92 | 102 | | dB |
| | | AVDD, DVDD = 3.3V, f _s = 48kHz | | | | |
| | | AVDD, DVDD = 5V, f _s = 96kHz | | 100 | | dB |
| THD (Note 2) | | 0dB | | -95 | -80 | |
| Dynamic range (Note 2) | | -60dB | | 102 | | dB |
| Passband | | ±0.25dB | 0.4535fs | | | dB |
| Stopband | | -3dB | | 0.491fs | | |
| Passband ripple | | | | ±0.25 | | dB |
| Stopband Attenuation | | f > 0.55fs | | - | | dB |
| Channel Separation | | | | 100 | | dB |
| Gain mismatch channel-to-channel | | | | ±1 | ±5 | %FSR |
| Digital Logic Levels | | | | | | |
| Input LOW level | V _{IL} | | | | 0.8 | V |
| Input HIGH level | V _{IH} | | 2.0 | | | V |
| Output LOW level | V _{OL} | I _{OL} = 2mA | | | AVSS + 0.3V | |
| Output HIGH level | V _{OH} | I _{OH} = 2mA | AVDD - 0.3V | | | |
| Analogue Output Levels | | | | | | |
| Output level | | Into 10kohm, full scale 0dB, (5V supply) | | 1.1 | | V _{rms} |
| | | Into 10kohm, full scale 0dB, (3.3V supply) | | 0.66 | | V _{rms} |
| Minimum resistance load | | To midrail or AC coupled (5V supply) | | 1 | | kohms |
| | | To midrail or AC coupled (3.3V supply) | | 600 | | ohms |
| Maximum capacitance load | | 5V or 3.3V | | 100 | | pF |
| Output DC level | | | | AVDD/2 | | V |
| Reference Levels | | | | | | |
| Potential divider resistance | | AVDD to CAP and CAP to AGND | | 90 | | kohms |
| Voltage at CAP | | | | AVDD/2 | | |
| POR | | | | | | |
| POR threshold | | | 1.2 | 1.6 | 2.0 | V |
| Analogue Mixer Specifications | | | | | | |
| SNR | | | 92 | 100 | | dB |
| THD | | 1V rms output, Into 10kohm, 50pF load | | -96 | -92 | dB |
| Dynamic Range | | | | 100 | | dB |
| Channel Separation | | | | 100 | | dB |
| Output voltage | | Into 10kohm | | | 1.5 | V _{rms} |
| Output current source | | | 2 | 3 | | mA |
| Output current sink | | | 1.5 | 2 | | mA |
| Input voltage, MIXINL/R | | AC coupled | | | 2 | V _{rms} |
| MIXINL/R input resistance | | 0dB | | 50 | | kohm |
| MIXINL/R input resistance | | (at 12dB trim) | | 20 | | kohm |

Test ConditionsAVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------|------------------------|-------|-------|-------|----------|
| Gain mismatch | | Channel to channel | | +/-1% | +/-5% | % of FSR |
| Frequency Bandwidth | | 0dB gain | | 100 | | kHz |
| Master volume max gain | | | 5 | 6 | 7 | dB |
| Master volume min gain | | | -70 | -73 | -76 | dB |
| Master volume step size, codes 0 - 47 | | | 0.7 | 1 | 1.3 | dB |
| Master volume step size, codes 48 – 79 | | | 0.5 | 1 | 1.5 | dB |
| Master volume gain code 80 – 127 (mute) | | | -90 | -100 | | dB |
| Mixer trim max gain | | | 11 | 12 | 13 | dB |
| Mixer trim min gain | | | -32.5 | -34.5 | -36.5 | dB |
| Mixer trim step size | | | 1.3 | 1.5 | 1.7 | dB |
| Tone Generator | | | | | | |
| SINAD (Note 3) | | 1Hz to 1kHz tones | 65 | 75 | | dB |
| SINAD | | 1kHz to 2kHz tones | 60 | 70 | | dB |
| SINAD | | 2kHz to 4kHz tones | 55 | 65 | | dB |
| SINAD | | 4kHz to 32kHz tones | 50 | 60 | | dB |
| Full scale output voltage; trims at | | 0dB | | 2.5 | | V pk-pk |
| Tone Frequency | | TCLK frequency = 27MHz | 1 | | 32767 | Hz |
| Tone Duration | | TCLK frequency = 27MHz | 0.1 | | 25.5 | secs |
| Gain adjust range | | | -46.5 | | 0 | dB |
| Gain adjust step size (4 bit trim) | | | 1.25 | 1.5 | 1.75 | dB |

- Notes:**
- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
 - All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
 - SINAD is ratio of signal to sum of noise, harmonics and spuri, over a bandwidth from 1Hz up to either 127x the tone frequency, or 20kHz, whichever is the lower. (This is to allow for the lower frequency tones having images at 127x and 129x the tone frequency which will fall in the audio band for tones of frequency less than about 20kHz/128).

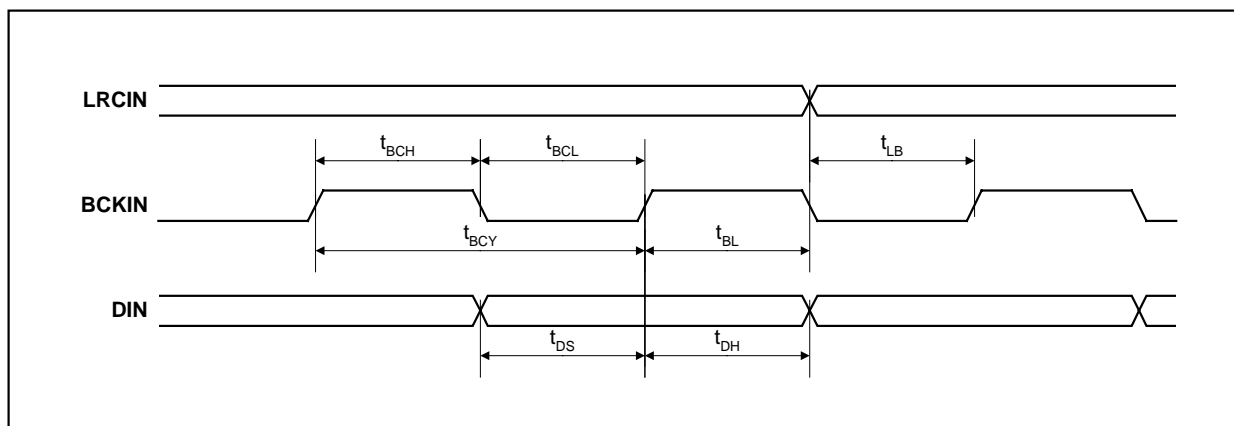


Figure 1. Audio Data Input Timing

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, $T_A = +25^{\circ}\text{C}$, $f_s = 48\text{kHz}$, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------|-----------------|-----|-----|-----|------|
| Audio Data Input Timing Information | | | | | | |
| BCKIN pulse cycle time | t_{BCY} | | 100 | | | ns |
| BCKIN pulse width high | t_{BCH} | | 40 | | | ns |
| BCKIN pulse width low | t_{BCL} | | 40 | | | ns |
| BCKIN rising edge to LRCIN edge | t_{BL} | | 20 | | | ns |
| LRCIN rising edge to BCKIN rising edge | t_{LB} | | 20 | | | ns |
| DIN setup time | t_{DS} | | 20 | | | ns |
| DIN hold time | t_{DH} | | 20 | | | ns |

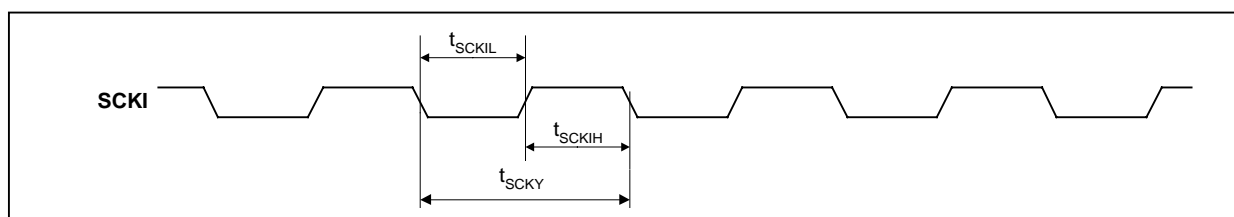


Figure 2. System Clock Timing Requirements

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, $T_A = +25^{\circ}\text{C}$, $f_s = 48\text{kHz}$, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------|-----------------|-----|-----|-----|------|
| System Clock Timing Information | | | | | | |
| System clock pulse width high | t_{SCKIH} | | 10 | | | ns |
| System clock pulse width low | t_{SCKIL} | | 10 | | | ns |
| System clock cycle time | t_{SCKY} | | 27 | | | ns |

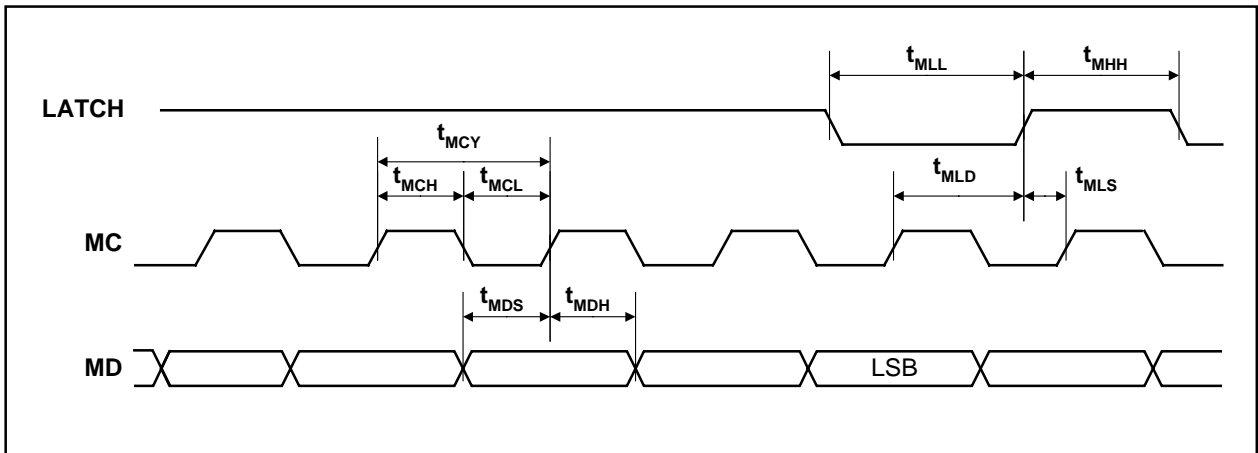


Figure 3. Program Register Input Timing – 3-Wire MPU Serial Control Mode

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, f_s = 48kHz, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------|-----------------|-----|-----|-----|------|
| Program Register Input Information | | | | | | |
| MC pulse cycle time | t _{MCY} | | 100 | | | ns |
| MC pulse width low | t _{MCL} | | 40 | | | ns |
| MD pulse width high | t _{MCH} | | 40 | | | ns |
| MD set-up time | t _{MDS} | | 20 | | | ns |
| MC hold time | t _{MDH} | | 20 | | | ns |
| LATCH pulse width low | t _{MLL} | | 20 | | | ns |
| LATCH pulse width high | t _{MHH} | | 20 | | | ns |
| LATCH set-up time | t _{MLS} | | 20 | | | ns |
| LATCH delay from MC | t _{MLD} | | 20 | | | ns |

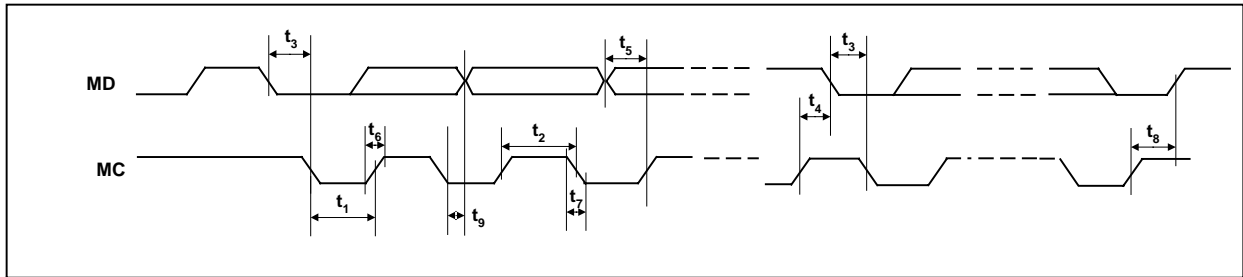


Figure 4. Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, f_s = 48kHz, SCKI = 256fs unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------------|-----------------|-----|-----|-----|------|
| Program Register Input Information | | | | | | |
| MC Frequency | | | 0 | | 400 | kHz |
| MC Low Pulsewidth | t ₁ | | 600 | | | ns |
| MC High Pulsewidth | t ₂ | | 1.3 | | | us |
| Hold Time (Start Condition) | t ₃ | | 600 | | | ns |
| Setup Time (Start Condition) | t ₄ | | 600 | | | ns |
| Data Setup Time | t ₅ | | 100 | | | ns |
| MD, MC Rise Time | t ₆ | | | | 300 | ns |
| MD, MC Fall Time | t ₇ | | | | 300 | ns |
| Setup Time (Stop Condition) | t ₈ | | 600 | | | ns |
| Data Hold Time | t ₉ | | | | 900 | ns |

DEVICE DESCRIPTION

WM8722 is a complete low cost stereo audio DAC, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters. A novel multi-bit sigma-delta DAC design is used, utilising a 64x oversampling rate, to optimise signal-to-noise performance and increase clock jitter tolerance. The WM8722 also provides an analogue mixing function, which allows user-selectable control over mixing of an external analogue input signal (line level sources or microphone output) with the converted output signal. The device provides both line level and variable outputs. The WM8722 contains a high performance sine wave generator circuit, which can be used to generate low distortion sinusoidal waveforms of varying frequency and amplitude. The WM8722 uses a minimum of external components, with the internally generated mid-rail references used to provide DC bias of output signals requiring only a single external capacitor for decoupling purposes.

The WM8722 is controlled through a software serial interface. This allows control of variables such as gain levels through each path, tone frequency and duration, and audio data interface format. The software control interface may be operated using either a 3-wire (SPI compatible) or 2-wire MPU interface. Selection of interface format is achieved by monitoring the state of BUSY pin at power up. In 2-wire mode, the ML pin becomes an address select, allowing two WM8722 devices to be used on the same bus.

Operation using system clock of 256fs or 384fs is provided, selection between clock rates being automatically controlled. Alternatively, the user can select the clock rate through the software interface. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

Tolerance of asynchronous word clock jitter is provided, the internal signal processing of the device re-synching to the external LRCIN clock once the phase difference between left-right and system clocks exceeds half a LRCIN period. During this re-synch period, the oversampling filters either miss an audio sample, or repeat the last sample value, so minimising the audible effects of this operation.

The interface supports normal (Japanese right justified) and I²S (Philips left justified, one bit delayed) interface formats, in both packed and unpacked forms. (Packed has exactly the number of serial clocks corresponding to the number of data bits, per LRCIN period). Additionally the device automatically detects when it is connected to a 16 bit packed data source (32 serial clocks per LRCIN) and switches automatically into 16 bit mode. 44.1kHz de-emphasis is supported, with frequency scaling if other sample rates are used.

The tone generator circuit uses a high quality sine weighted DAC, and sophisticated noise shaping techniques to achieve high quality tones with low noise and spurious tone generation. Using the nominal master tone clock (TCLK) frequency of 27MHz, any frequency from 1Hz to 32kHz may be generated in 1Hz increments. The duration of the tone burst may be programmed from 0.1second to 25.5 seconds. The next tone may be pre-programmed during a current tone burst, and is then loaded, in phase continuous manner at the end of the current tone so allowing continuous generation of varying frequency.

The device is packaged in a small 5.3mm wide 20-pin SSOP package. Single 3V to 5.5V supplies may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption, the low pin count small package and the analogue mixing features, make the WM8722 attractive for many consumer audio applications, including VCD, CD, DVD-Audio, set-top boxes and digital TV. Separate analogue and digital supply pins are provided, allowing 3V operation of digital and 5V operation of analogue circuits.

ANALOGUE MIXER

The analogue mixer circuits comprise signal paths to allow signal switching and gain adjust for each of the mixer line-in, DAC output, and tone generator signals. Additionally, mono signals can be created using the completely flexible switching arrangements, and 6dB attenuation switching circuits. Individual control bits are provided for each of the 5 switch inputs to each summing stage in the mixer, each signal path therefore being individually controllable. Any combination of output signals is therefore permissible. Fixed output level line outputs and volume adjusted variable output level outputs are provided.

TONE GENERATOR DAC

The tone generator comprises a digital frequency synthesiser, which is used to create a clock at 128x the required tone frequency, and a 128 step per cycle, sine weighted DAC, which converts the clock into one of three tone types. An analogue programmable gain stage follows the DAC, allowing gain adjustment of the tone amplitude. Noise shaping techniques are used to create minimal spurious components in the frequency synthesiser.

The WM8722 can generate three different tone types. The default setting is a sinusoidal tone. Square waves are generated by setting the SQR bit. Alternatively, a two-tone output that generates one cycle at the chosen frequency, followed by two cycles at twice that frequency can be selected by setting the F2F bit. This facility may be used in sine or square wave modes.

The frequency of the resulting tone is controllable with 1Hz resolution, over a range of 1Hz to 32.767kHz, based on a TCLK frequency of 27MHz. Alternative tone clock frequencies may be used if required. For example the DAC SCLK frequency may be used, but in these cases the frequency range and resolution will change by the ratio of the clock used, to the nominal 27MHz clock specified.

The duration of the selected tone is programmed via the serial interface. Once both the frequency and the duration have been set to non-zero values, the tone generation commences. Once the tone generator has started running, the next tone frequency and duration may be programmed ready to start as soon as the current tone finishes. Under this condition the tones are phase continuous, and a BUSY flag is set on the BUSY pin, which now becomes a CMOS output, overdriving any pull-up or down resistor placed on the pin to select the interface format at power-up. After a tone frequency of duration has been written, it may be over written with a new value if desired.

At the conclusion of a tone burst, the circuit ensures that at the end of the duration time of the last tone, the tone continues to the next zero crossing point to ensure DC offsets are not created. A control bit (TFIN) is provided which allows selection of the method of completion of the burst: If set to 1, the burst completes at the next zero crossing. If left at 0, the burst completes a whole number of sinusoids, avoiding potential problems with DC levels changing across AC coupling capacitors.

Whilst tones are being generated, writing either new frequency or new duration, will cause the subsequent burst to be generated phase continuously with the current burst. If a duration value of 0 is written during a burst, the current burst will stop immediately (at the next zero cross or full cycle complete point as selected by TFIN).

If the current burst completes, and no new duration or frequency have been set, the tones stop and the duration value is reset to zero. The frequency setting is maintained in volatile memory. If a new duration is programmed, then the tone generator will re-start with the previously programmed frequency. If a new frequency is desired, the frequency is simply programmed before the duration, the tone commencing when the duration is written.

SYSTEM CLOCK

The system clock for the WM8722 must be either 256fs or 384fs where fs is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz, 48kHz or 96kHz. The system clock is used to operate the digital filters and the noise shaping circuits.

WM8722 has system clock detection circuitry that automatically determines the relationship between the system clock frequency and the sampling rate (to within 8 system clocks). If greater than 8 clocks error, then the interface shuts down the DAC and mutes the output. The system clock should be synchronised with LRCIN, but WM8722 is tolerant of phase differences or jitter on this clock. Severe distortion in the phase difference between LRCIN and the system clock (for example caused by too many or too few system clocks received per LRCIN period) will be detected, and cause the device to automatically re-synchronise. If the externally applied LRCIN slips in phase by more than half the internal LRCIN period, which is derived from the master clock, then the interface resynchronises. During re-synchronisation, the WM8722 will either repeat the previous sample or drop the next sample depending on the nature of the phase slip. This will ensure there is no discernible click at the analogue outputs during re-synchronisation.

| SAMPLING RATE (LRCIN) | SYSTEM CLOCK FREQUENCY (MHZ) | |
|-----------------------|------------------------------|---------|
| | 256fs | 384fs |
| 32kHz | 8.192 | 12.288 |
| 44.1kHz | 11.2896 | 16.9340 |
| 48kHz | 12.288 | 18.432 |
| 96kHz | 24.576 | 36.864 |

Table 1 System Clock Frequencies versus Sampling Rate

AUDIO DATA INTERFACE

The serial data interface to WM8722 is fully compatible with both normal (MSB first, right-justified) or I²S interfaces. Data may be packed (number of serial BCLKS per LRCIN period is exactly 2 times the number of data bits, i.e. normally 32 in 16 bit mode) or unpacked (more than 32 BCLKS per LRCIN period).

The WM8722 will automatically detect 16-bit packed data being sent to the device in normal mode, and accept the data in this input format accordingly.

| I ² S MODE | DESCRIPTION |
|-----------------------|---|
| 0 | Normal format (MSB-first, right justified) |
| 1 | I ² S format (Philips serial data protocol) |

Table 2. Serial Interface Formats

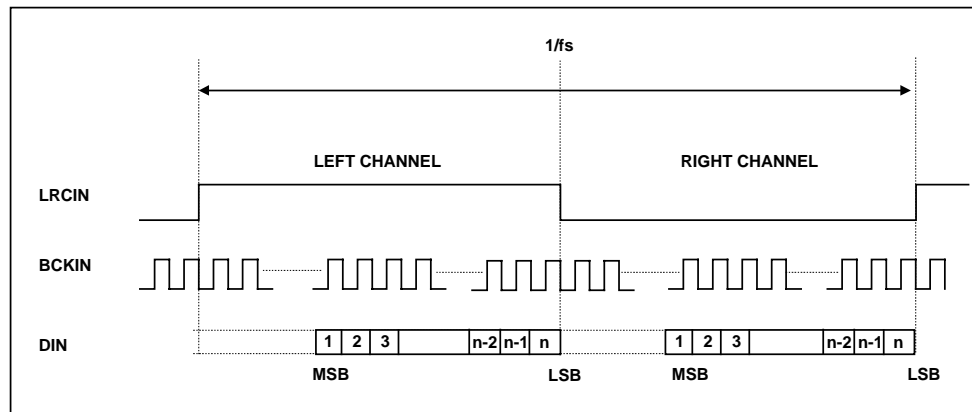


Figure 5. Normal Data Input Timing

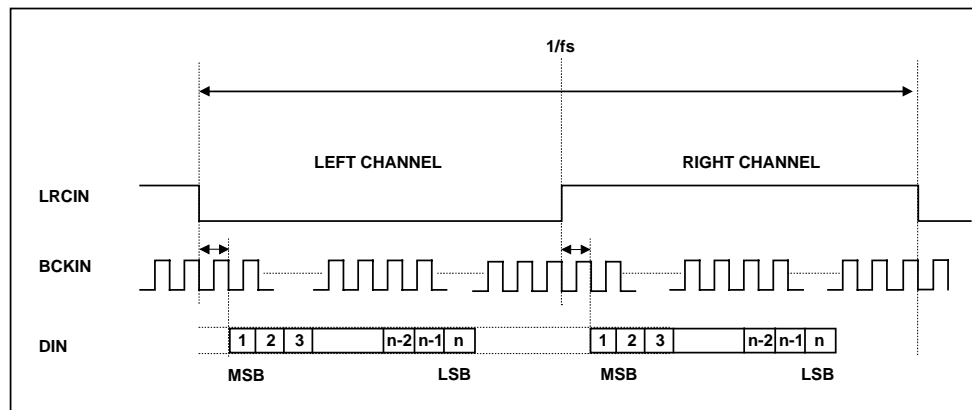


Figure 6. I²S Data Input Timing

MODES OF OPERATION

The software control interface may be operated using either a 3-wire (SPI-compatible) or 2-wire MPU interface. Selection of interface format is achieved by monitoring the state of BUSY pin at power up.

In 3-wire mode, MD is used for the program data, MC is used to clock in the program data and LATCH is used to latch in the program data. In 2-wire mode, MD is used for serial data and MC is used for serial clock. In 2-wire mode, the LATCH pin allows the user to select one of two addresses.

SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the BUSY pin at power-up with a weak, external pull-up or pull-down resistor (typically 10k). This pin is an input at power up, and its state selects the type of input format. The value input at power-up is sampled and stored internally. This allows the BUSY pin to be used as an output when tone generation has been enabled. This stored value is only reset when the device is powered off.

| BUSY PIN (TONE GENERATION NOT ENABLED) | INTERFACE FORMAT |
|--|------------------|
| 0 | 3 wire |
| 1 | 2 wire |

Table 3. Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The WM8722 can be controlled using a 3-wire serial interface. MD is used for the program data, MC is used to clock in the program data and LATCH is used to latch in the program data. The 3-wire interface protocol is shown in Figure 7.

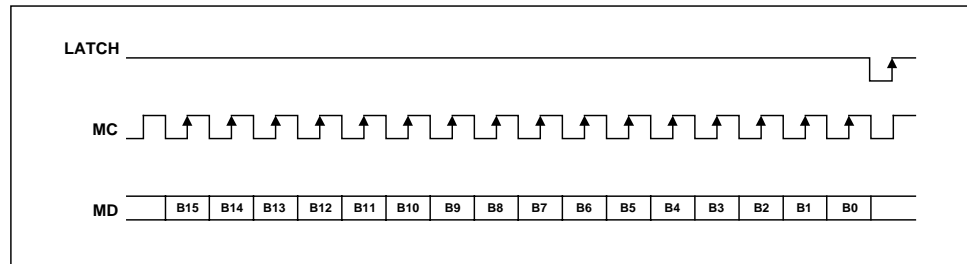


Figure 7. 3-Wire Serial Interface

2-WIRE SERIAL CONTROL MODE

The WM8722 supports a 2-wire MPU serial interface. The device operates as a slave device only. The WM8722 has one of two slave addresses that are selected by setting the state of pin 5, (LATCH).

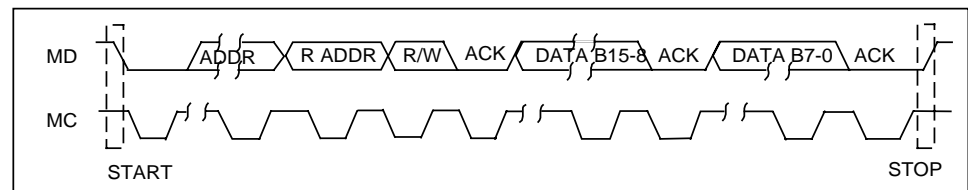


Figure 8. 2-Wire Serial Interface

| LATCH STATE | Address |
|-------------|---------|
| 1 | 1000001 |
| 0 | 1000000 |

To control the WM8722 on the bus, the master must initiate a data transfer by establishing a start condition, defined by a high-to-low transition on MD whilst MC remains high. This indicates that an address and data transfer will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The peripheral that recognises the transmitted address responds by pulling the data line low during the ninth clock pulse (acknowledge bit). All other devices withdraw from the bus and maintain an idle condition once the appropriate peripheral has been recognised. The idle condition is where the device monitors the MD and MC lines waiting for a start condition and the correct transmitted address. The R/W bit determines the direction of data transfer. The WM8722 is a write only device and only responds to the R/W bit indicating a write.

The WM8722 acts as a standard slave device on the bus. The data on the MD is clocked in by MC. The first 6 bits (which must be 100000) are clocked into the WM8722 followed by a programmable address bit to select one of the two available addresses. The eighth bit of the address byte is the R/W bit. The WM8722 checks this bit and responds if it is a write. If the correct address is sent by the master, the WM8722 acknowledges the bus master (ACK) and pulls the bus low. The next byte is the register address. Each subsequent byte of data is separated by an acknowledge bit.

A stop condition is defined when there is a low-to-high transition on MD when MC is high.

If a stop or start condition is detected out of sequence at any point in the data transfer, the device jumps to the idle condition.

SERIAL CONTROL OPERATION

Control of the various modes of operation is software control over the 2 or 3-wire serial interface. The following functions may be controlled via the serial control interface:

| FUNCTION | OPTIONS | SOFTWARE CONTROL DEFAULT VALUE |
|--|--|--|
| Input audio data format | Normal format I ² S format | Normal format (0) |
| Input Word Length | 16 20 24 | 16 bit (0) |
| De-emphasis selection | On Off | Off (0) |
| Operation enable (OPE) (power down) | Enable disable | Enabled (0) |
| Analogue output mode | L, R, mono, Mute | Stereo (1001) |
| Mute | On (Muted) Off (Un-muted) | Off (0) |
| Input LRCIN polarity | Lch/Rch = Hi/Lo Lch/Rch = Lo/Hi | Lch/Rch = Hi/Lo (0) |
| Master Volume Control | Lch, Rch individually Lch, Rch both | 0dB (1111001) Lch, Rch individually (0) |

| FUNCTION | OPTIONS | SOFTWARE CONTROL DEFAULT VALUE |
|------------------------------|--|--|
| DAC digital volume | Lch, Rch individually Lch, Rch common | 0dB (111111) Lch, Rch individually (0) |
| Mixer Volume Control | Lch, Rch individually Lch, Rch both | 0dB (10111) Lch, Rch individually (0) |
| Mixer Output Selection | 5 switches for each of left and right, mix and volume paths, individually controlled, or both together, and with -6dB gain option for mono modes | Normal stereo (11100) MLMX left mux (11100) MLVMX left mux (11100) MRMX right mux (11100) MRVMX right mux M6DB bits all 0 (gain 0dB) |
| Tone amplitude | 0 to -46.5dB in 1.5dB steps plus mute | 0dB (11111) |
| Tone frequency | 1 to 32767Hz in 1Hz steps (based on 27MHz TCLK) | 0 = disabled |
| Tone duration | 0.1 to 25.5secs in 0.1sec steps | 0 = disabled |
| Tone Finish Behaviour (TFIN) | | 1 = Full cycle sine wave 0 = next zero cross |
| Tone Waveform | Sine or square wave | 0 = sine 1 = square wave |
| Tone Burst | f or 2f | 0 = f 1 = 2f |

Table 4. Control Functions

REGISTER MAP

The WM8722 controls the device functions using 15 program registers, each of which is 16-bits long. These registers are all loaded via the serial control interface in either 2 or 3-wire mode.

There are two type of control word; either TFRQ, the tone frequency word, which is a single address bit followed by 15 data bits, or other types, which have 6 address bits, and 10 bits of data. Other types have the lead address bit inverted compared to TFREQ words, allowing use of a single write to load the required frequency.

| REG | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
|-------|-----|----------|----------|-----|-----|-----|-----|----------|-----------|-----------|-------|--------------|-----|-----|-----|-----|--|
| TFREQ | 1 | F[14:0] | | | | | | | | | | | | | | | |
| R0 | 0 | RESERVED | RESERVED | 0 | 0 | 0 | 0 | LDL | DAL [7:0] | | | | | | | | |
| R1 | 0 | | | 0 | 0 | 1 | LDR | DAR[7:0] | | | | | | | | | |
| R2 | 0 | | | 0 | 0 | 1 | 0 | PL[3:0] | | | | IW1 | IW0 | PWD | DE | MU | |
| R3 | 0 | | | 0 | 0 | 1 | 1 | res | res | res | res | res | res | ATC | LRP | I2S | |
| R4 | 0 | | | 0 | 1 | 0 | 0 | BOTH | res | res | MUTE | MTRIML[4:0] | | | | | |
| R5 | 0 | | | 0 | 1 | 0 | 1 | BOTH | res | res | MUTE | MTRIMR[4:0] | | | | | |
| R6 | 0 | | | 0 | 1 | 1 | 0 | BOTH | ZCEN | LVOL[6:0] | | | | | | | |
| R7 | 0 | | | 0 | 1 | 1 | 1 | BOTH | ZCEN | RVOL[6:0] | | | | | | | |
| R8 | 0 | | | 1 | 0 | 0 | 0 | BOTH | res | res | M6DB0 | LMXSEL(4-0) | | | | | |
| R9 | 0 | | | 1 | 0 | 0 | 1 | BOTH | res | res | M6DB1 | RMXSEL(4-0) | | | | | |
| R10 | 0 | | | 1 | 0 | 1 | 0 | BOTH | res | res | M6DB2 | LVMXSEL(4-0) | | | | | |
| R11 | 0 | | | 1 | 0 | 1 | 1 | BOTH | res | res | M6DB3 | RVMXSEL(4-0) | | | | | |
| R12 | 0 | | | 1 | 1 | 0 | 0 | res | TTIM[7:0] | | | | | | | | |
| R13 | 0 | | | 1 | 1 | 0 | 1 | F2F | SQR | TFIN | MUTE | TVOL[4:0] | | | | | |

Table 5. Mapping of Program Registers

| REGISTER NAME | REG ADDRESS | BIT NAME | DESCRIPTION | DEFAULT VALUE |
|---------------|-------------|---|---|--|
| TFREQ | 1 | F[14:0] | Tone frequency value | 000 0000 0000 0000 |
| Register 0 | 000 0000 | DAL[7:0] LDL | DAC attenuation data for left channel Attenuation data load control for left channel | 111 1111 (0dB) 0 |
| Register 1 | 000 0001 | DAR[7:0] LDR | DAC attenuation data for right channel Attenuation data load control for right channel | 111 1111 (0dB) 0 |
| Register 2 | 000 0010 | MU DE PWD IW[1:0] PL[3:0] | Left and right DACs soft mute control De-emphasis control Power off control Input audio data bit length select Output mode select | 0 (not muted) 0 (de-emph off) 0 (power on) 00 (16 bit) 1001 (normal stereo) |
| Register 3 | 000 0011 | I2S LRP ATC | Audio data format select Polarity of LRCIN (pin 7) select Attenuator control | 0 (NORMAL format) 0 0 |
| Register 4 | 000 0100 | MTRIML[4:0] MUTE | Left mixer 1 attenuation data Left mixer mute | 10111 (0dB) 0 (not mute) |
| Register 5 | 000 0101 | MTRIMR[4:0] MUTE | Right mixer 1 attenuation data Right mixer mute | 10111 (0dB) 0 (not mute) |
| Register 6 | 000 0110 | LVOL[6:0] ZCEN BOTH | Left volume 2 attenuation data | 1111 001 (0dB) |
| Register 7 | 000 0111 | RVOL[6:0] ZCEN BOTH | Right volume 2 attenuation data | 1111 001 (0dB) |
| Register 8 | 000 1000 | LMXSEL M6DB0 BOTH | Left mixer output mux control M6DB for left mix output | 11100 (normal stereo) 0 (0dB) |
| Register 9 | 000 1001 | RMXSEL M6DB1 BOTH | Right mixer output mux control M6DB for right mix output | 11100 (normal stereo) 0 (0dB) |
| Register 10 | 000 1010 | LVMXSEL M6DB2 BOTH | Left variable output mux control M6DB for left variable output | 11100 (normal stereo) 0 (0dB) |
| Register 11 | 000 1011 | RVMXSEL M6DB3 BOTH | Right variable output mux control M6DB for right variable output | 11100 (normal stereo) 0 (0dB) |
| Register 12 | 000 1100 | TTIM[7:0] | Tone duration | 000 0000 (no tone) |
| Register 13 | 000 1101 | TVOL[4:0] MUTE TFIN SQR F2F | Tone amplitude Tone mute Tone burst finish on zero cross Tone sine or square wave Tone one cycle at F, two cycle at 2xF | 11111 (max output) 0 (not muted) 0 (finish on full cycle) 0 (sine wave) 0 (normal F) |

Table 6. Internal Register Mapping

REGISTER TFREQ

TONE FREQUENCY

This is the special register of 15 bit length with a single bit address, to allow values for the selected tone frequency from 1Hz to 32767Hz to be written in one word. Writing 0 turns off the tone.

$$F_{\text{TONE}} = (F_{\text{TCLK}} \times T_{\text{FREQ}[15:0]}) / 27 \times 10^6$$

REGISTER 0/1**DAC OUTPUT ATTENUATION**

A digital attenuator is provided to allow the levels of DAC signals to be attenuated in the digital domain.

Register 0 (A[1:0] = 00) is used to control left channel attenuation. Bits 0-7 (AL[7:0]) are used to determine the attenuation level. The level of attenuation is given by:

$$\text{Attenuation} = [20.\log_{10} (\text{Attenuation_Data}/255)] \text{ dB}$$

Bit 8 in register 0 (LDL) is used to control the loading of attenuation data in B[7:0]. When LDL is set to 0, attenuation data will be loaded into AL[7:0], but it will not affect the attenuation level until LDL is set to 1. LDR in register 1 has the same function for right channel attenuation.

Attenuation levels are controlled by setting the register set AL[7:0] (left channel) or AR[7:0] (right channel). Attenuation levels are given in Table 7.

| AX[7:0] | ATTENUATION LEVEL |
|---------|-------------------|
| 00h | - ∞ dB (Mute) |
| 01h | -48.16 dB |
| : | : |
| : | : |
| : | : |
| FEh | -0.034 dB |
| FFh | 0dB |

Table 7. Attenuation Control Levels

Register 1 (A[1:0] = 01) is used to control right channel attenuation in a similar manner.

REGISTER 2**SOFT MUTE**

Soft mute is controlled by setting bit 0 in register 2 (A[1:0]=10). A high level on bit 0 will cause the DAC outputs to be muted, the effect of which is to ramp the signal down in the digital domain so that there is no discernible click.

DIGITAL DE-EMPHASIS

Bit 1 (DE) in register 2 (A[1:0]=10) is used to control digital de-emphasis. A low level on bit 1 disables de-emphasis whilst a high level enables de-emphasis.

POWER OFF CONTROL

Bit 2 (PWD) in register 2 is used for operation control. With PWD = low (default) the device functions normally. With PWD = high the device is disabled and the outputs are held at midrail. Current consumption of the digital section is minimised, but analogue bias sections remain active in order to preserve DC levels.

INPUT WORD RESOLUTION

Bits 3 and 4 of register 2 (IW[1:0]) are used to determine the input word resolution. The WM8722 supports 16-bit, 18-bit, 20-bit and 24-bit word formats.

| BIT 4 (IW1) | BIT 3 (IW0) | INPUT RESOLUTION |
|-------------|-------------|------------------|
| 0 | 0 | 16-bit Data Word |
| 0 | 1 | 20-bit Data Word |
| 1 | 0 | 24-bit Data Word |
| 1 | 1 | 18-bit Data Word |

Table 8. Input Data Resolution

DAC OUTPUT CONTROL

Bits 5, 6, 7 and 8 (PL[3:0]) of register 2 are used to control the output format.

| PL0 | PL1 | PL2 | PL3 | LEFT OUTPUT | RIGHT OUTPUT | NOTE |
|-----|-----|-----|-----|-------------|--------------|--------------------|
| 0 | 0 | 0 | 0 | MUTE | MUTE | Mute Both Channels |
| 0 | 0 | 0 | 1 | MUTE | R | |
| 0 | 0 | 1 | 0 | MUTE | L | |
| 0 | 0 | 1 | 1 | MUTE | (L + R)/2 | |
| 0 | 1 | 0 | 0 | R | MUTE | |
| 0 | 1 | 0 | 1 | R | R | |
| 0 | 1 | 1 | 0 | R | L | Reverse Channels |
| 0 | 1 | 1 | 1 | R | (L + R)/2 | |
| 1 | 0 | 0 | 0 | L | MUTE | |
| 1 | 0 | 0 | 1 | L | R | Stereo Mode |
| 1 | 0 | 1 | 0 | L | L | |
| 1 | 0 | 1 | 1 | L | (L + R)/2 | |
| 1 | 1 | 0 | 0 | (L + R)/2 | MUTE | |
| 1 | 1 | 0 | 1 | (L + R)/2 | R | |
| 1 | 1 | 1 | 0 | (L + R)/2 | L | |
| 1 | 1 | 1 | 1 | (L + R)/2 | (L + R)/2 | Mono Mode |

Table 9. Programmable Output Format

REGISTER 3**AUDIO DATA INPUT FORMAT**

WM8722 allows maximum flexibility over the control of the audio data interface, allowing selection of format type, word length, and sample rates.

DIGITAL AUDIO SERIAL PROTOCOL

A low on bit 0 sets the format to Normal (MSB-first, right justified Japanese format), whilst a high sets the format to I²S (Philips serial data protocol).

AUDIO INTERFACE CLOCKS

Bit 1 (LRP) of register 3 is used to control the polarity of LRCIN (sample rate clock). When bit 1 is low, left channel data is assumed when LRCIN is in a high phase and right channel data is assumed when LRCIN is in a low phase. When bit 1 is high, the polarity assumption is reversed.

ATTENUATOR CONTROL

Bit 2 in register 3 (A1[1:0] = 11) is used to control the attenuator (ATC). When ATC is high, the attenuation data loaded in program register 0 is used for both the left and the right channels. When ATC is low, the attenuation data for each register is applied separately to left and right channels.

REGISTER 4/5**ANALOGUE MIXER TRIM**

Bits 0-4 of register 4, MTRIML[0:4], set the gain level of the first stage of analogue mixing on the left channel. The 5-bit register selects 1.5 dB increments of the MIXINL signal, over a range of +12dB to -34.5dB. A 6th bit, MUTE, controls muting of the signal when set high.

Similarly, bits 0-4 of register 5, MTRIMR[0:4], set the attenuation level of the first stage of analogue mixing on the right channel. The 5-bit register allows 1.5 dB increments of the MIXINR signal, over a range of +12dB to -34.5dB. A 6th bit, MUTE, controls muting of the signal when set high.

BOTH

In register 4 and 5, a further bit BOTH is available: When a write is made to either register 4 or 5 and BOTH is set high, then the same value written to the register will also be written into the other register. This allows both Left and Right channel gains to be updated simultaneously, halving the number of serial writes required, (simplifying gain ramping, for example) provided that the same gain is needed for both channels.

REGISTER 6/7**VOLUME CONTROL**

Bits 0-6 of register 6, LVOL[6:0], control gain applied to the variable level output VAROUTL. This 6-bit register controls 1.0 dB increments of the volume, over a range of +6 dB to -73 dB.

Similarly bits 0-6 of register 7, RVOL[6:0], control the gain applied to the variable level output VAROUTR. Value 1111111 sets maximum, i.e. 6dB gain. Code 48 sets minimum gain. Values less than code 48 apply mute to the gain stage. (i.e. set volume to 000 0000 to achieve mute)

ZCEN

A zero cross detect circuit is provided, so that volume control values are only updated when the input signal to the gain stage is close to the analogue ground level, minimising clicks and zipper noise as the gain values are changed. This circuit has no time out so if DC levels are being applied to the gain stage input, then the gain will not be updated. This zero cross function is enabled when the ZCEN bit is set high during a volume register write. If there is concern that a DC level may have blocked a volume change (one made with ZCEN set high), then a subsequent volume write of the same value, but with the ZCEN bit set low will force a volume update regardless of the DC level.

BOTH

In register 6 and 7, a further bit BOTH is available. When a write is made to either register 6 or 7 and BOTH is set high, then the same value written to the register will also be written into the other register. This allows both Left and Right channel gains to be updated simultaneously, halving the number of serial writes required, provided that the same gain is needed for both channels.

REGISTER 8, 9, 10, 11**ANALOGUE MIXER OUTPUT SELECTION**

The WM8722 allows software controllable selection of signal outputs. The WM8722 allows 2 outputs per channel, with one output at line level, and another output at variable level, according to the LVOL[6:0] and RVOL[6:0] attenuation register settings. In addition, the user may select whether the left or the right signal, converted in the DAC, is mixed with the corresponding mixer input or not.

This switching scheme is detailed in Figure 9, with 10 different select signals per channel, 5 each for each Mux: Each Mux therefore has 5 input signals; DACL, DACR, MIXL, MIXR and TONE. This allows completely flexible selection of signal paths, both mono and stereo outputs, on any output.

| MUX CONTROL BITS MXSEL(4:0) | SIGNAL SELECTED WHEN HIGH IS SET |
|-----------------------------|-----------------------------------|
| 0 | DAC sum enable |
| 1 | MIXIN sum enable |
| 2 | TONE in sum enable |
| 3 | Opposite channel DAC sum enable |
| 4 | Opposite channel MIXIN sum enable |

Table 10. MUX(4:0) mux control switches

If mono outputs are selected, the gain through the summer amplifiers may be reduced by 6dB if required by setting the appropriate M6DB bits. Similarly left and right channels may be completely swapped.

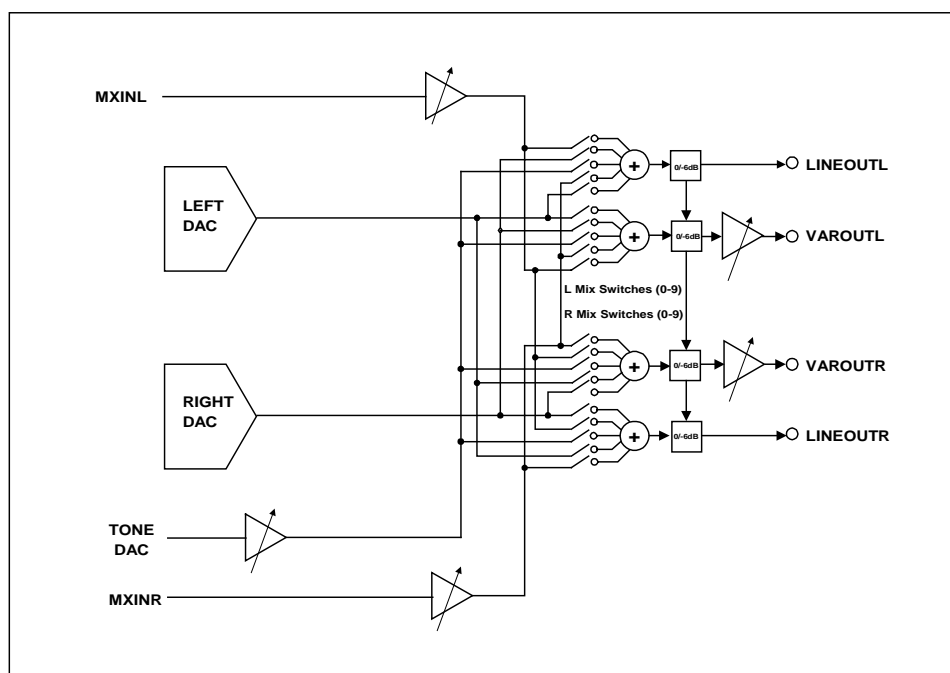


Figure 9. Output Mixer Configuration

M6DB

In each of the 4 MUX control registers there is an M6DB bit relevant to that channel. Setting M6DB high reduces the relevant output signal by 6dB.

BOTH

When a write to any MXSEL register is made with the BOTH bit set high, then the complementary channel MXSEL register for the other channel is updated with the same value. For example, if RVMXSEL is updated and BOTH is set, then LVMXSEL is updated with the same value, but the RMXSEL and LMXSEL registers (the non variable output path muxes) are NOT updated.

REGISTER 12

tone DURATION

Bits 0-7 of register 12 sets the duration of the tone burst. Writing to the register with a non-zero value starts the tone burst. Writing zero to this register stops the tone.

$$T = (2.7 \times 10^6 \times \text{TTIM}[7:0]) / F_{\text{TCLK}}$$

REGISTER 13

tone GENERATOR GAIN CONTROL

Bits 0-4 of register 13 TVOL[0:4] set the gain level of the tones summed into the analogue outputs. Bit 5 of this word controls muting of the tones. Note both mute must be off (0) and the tone input to the relevant mixer summing path must be selected (1). The gain defaults to 0dB (11111) but may be attenuated in 1.5dB steps down to -46.5dB.

tone GENERATOR WAVEFORM CONTROL

TFIN

A control bit (TFIN) is provided which allows selection of the method of completion of the burst. If set to 1, the burst completes at the next zero crossing. If left at 0, the burst completes a whole number of sinusoids, avoiding potential problems with DC levels changing across AC coupling capacitors. At the conclusion of a tone burst, the circuit ensures that at the end of the duration time of the last tone, the tone continues to the next zero crossing point to ensure DC offsets are not created.

SQR

The WM8722 can generate three different tone types. The default setting is a sinusoidal tone. Square waves are generated by setting the SQR bit.

F2F

A two-tone output that generates one cycle at the chosen frequency, followed by two cycles at twice that frequency can be selected by setting the F2F bit. This facility may be used in sine or square wave modes.

SYSTEM DIAGRAM

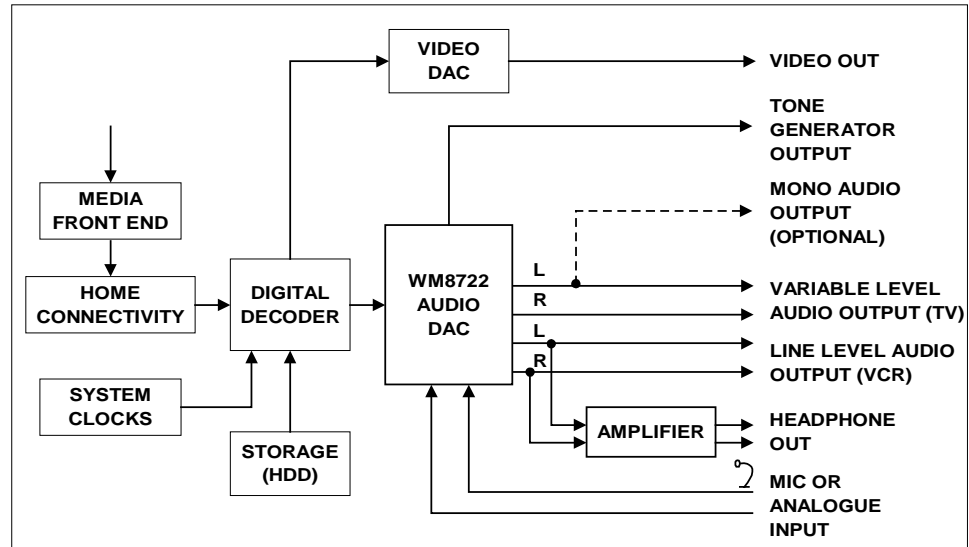


Figure 10. Digital Set Top Box Application

The WM8722 is a complete audio sub-system designed for digital set top box applications. A typical application might require audio outputs to be routed to a VCR and television. The WM8722 allows the user to control the output audio level being sent to the television whilst maintaining a constant volume level to the VCR. The on-board tone generator can be programmed to provide an audible warning signal from the set top box to the television outputs without appearing on the line level outputs. The WM8722 can also directly generate a mono signal for UHF outputs.

The WM8722 contains a stereo analogue input. This signal can be routed or mixed together onto the line and variable outputs. It can be used to control the volume level of an audio output from another audio source such as a games machine or additional set top box. Alternatively, it could be used to provide a karaoke input from a digital effects processor.

RECOMMENDED EXTERNAL COMPONENTS

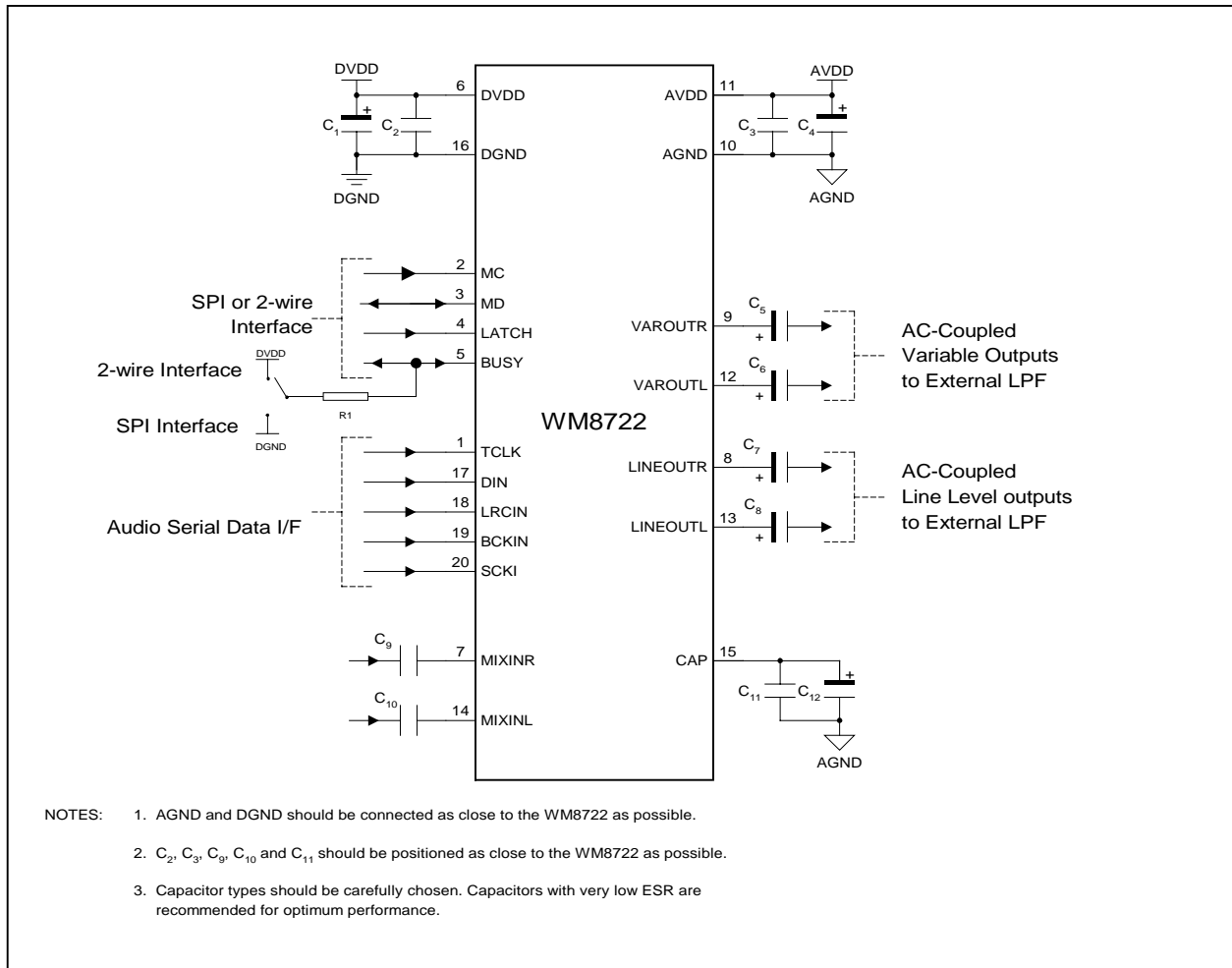


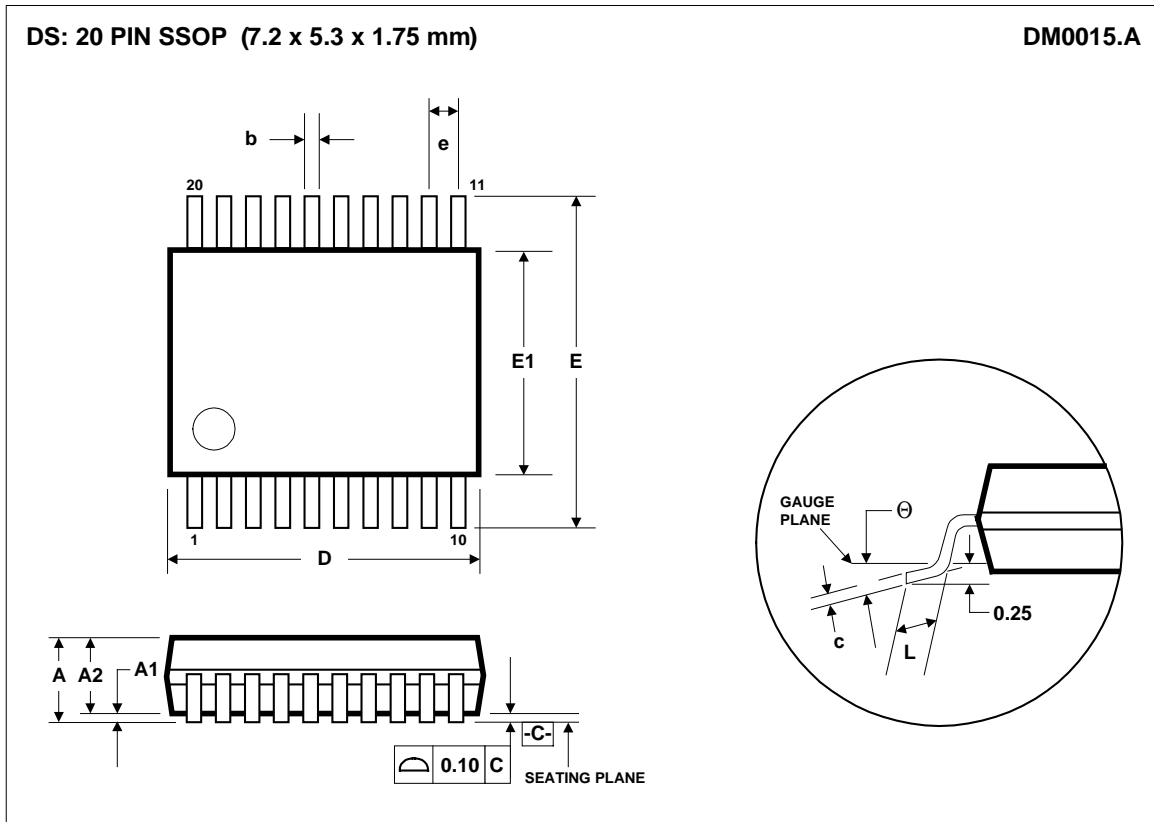
Figure 11. External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION |
|---------------------|-----------------|--|
| C1 and C4 | 10µF | De-coupling for DVDD and AVDD. |
| C2 and C3 | 0.1µF | De-coupling for DVDD and AVDD. |
| C5, C6, C7 and C8 | 10µF | Output AC coupling caps to remove midrail DC level from outputs. |
| C11 | 0.1µF | Reference de-coupling capacitors for CAP pin. |
| C12 | 10µF | |
| R1 | 10kΩ | |
| C9,C10 | 1µF | AC coupling capacitors for setting DC inputs level of analogue |

Table 11. External Components Description

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | |
|----------------------|------------------|-------|-------|
| | MIN | NOM | MAX |
| A | ----- | ----- | 2.0 |
| A₁ | 0.05 | ----- | ----- |
| A₂ | 1.65 | 1.75 | 1.85 |
| b | 0.22 | ----- | 0.38 |
| c | 0.09 | ----- | 0.25 |
| D | 6.90 | 7.20 | 7.50 |
| e | 0.65 BSC | | |
| E | 7.40 | 7.80 | 8.20 |
| E₁ | 5.00 | 5.30 | 5.60 |
| L | 0.55 | 0.75 | 0.95 |
| θ | 0° | 4° | 8° |
| REF: | JEDEC.95, MO-150 | | |

- NOTES:
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
 D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.