WM8736

24-bit, 96kHz 6-Channel DAC with Volume Control

Production Data, January 2001, Rev 2.1

DESCRIPTION

The WM8736 is a high performance 6-channel DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8736 supports data input word lengths from 16 to 24-bits and sampling rates up to 96kHz. The WM8736 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and 6 DACs in a small 28-pin SSOP package. The WM8736 also includes a digitally controllable mute and attenuator function on each channel.

The WM8736 supports a variety of connection schemes for audio DAC control. The SPI-compatible serial port provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available.

The WM8736 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications.

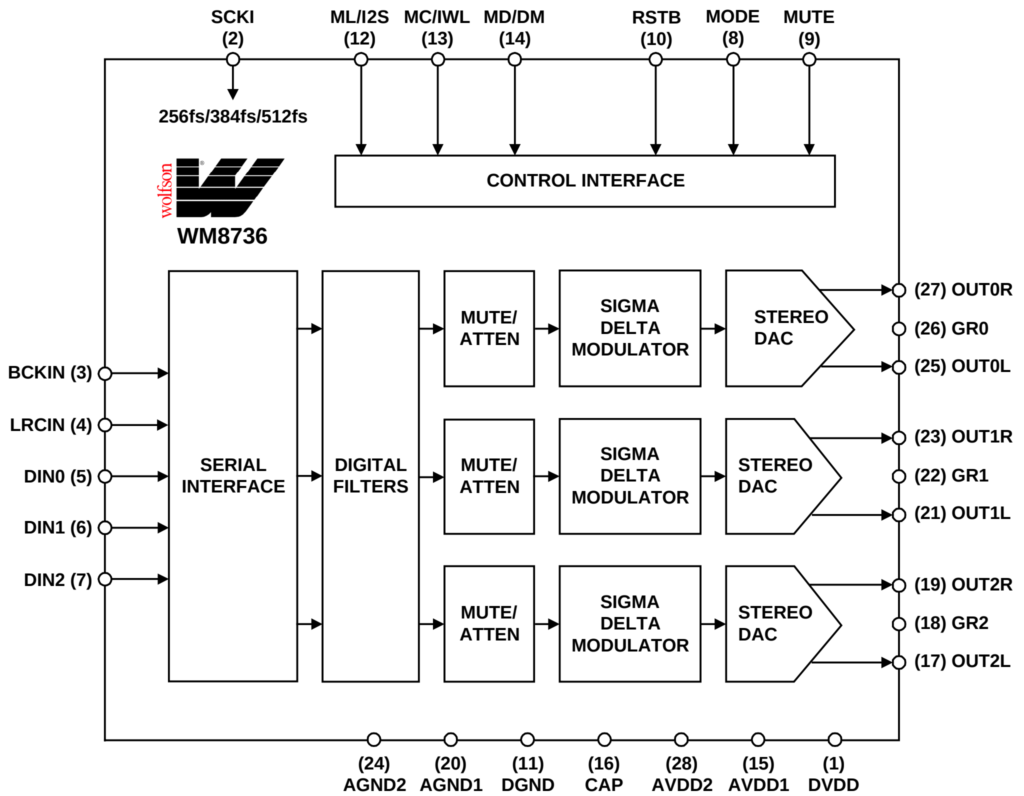
FEATURES

- 6-channel DAC
- Performance:
  - 102dB SNR (‘A’ weighted @ 48kHz), THD+N: -95dB at full scale
- 5V or 3.3V supply operation
- Sampling frequency: 8kHz to 96kHz
- Input data word: 16 to 24-bit
- Hardware or SPI compatible serial port control modes:
  - Hardware mode: system clock, reset, mute
  - Serial control mode: mute, de-emphasis, digital attenuation (256 steps), zero mute, power down

APPLICATIONS

- DVD
- Home theatre systems
- Digital TV
- Digital broadcast receivers

BLOCK DIAGRAM



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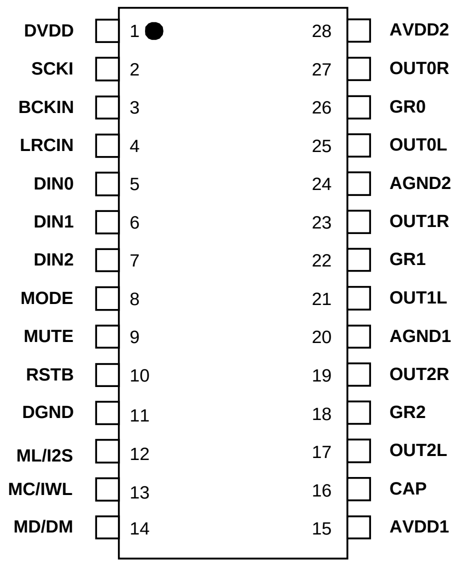
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8736EDS	-25^{o} to 85^{o}C	28-pin SSOP

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7V
Reference input		VDD + 0.3V
Operating temperature range, T_A	-25^{o} C	$+85^{o}$C
Storage temperature	-65^{o} C	$+150^{o}$C
Package body temperature (soldering, 10 seconds)		$+240^{o}$C
Package body temperature (soldering, 2 minutes)		$+183^{o}$C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		-10%	3.3 to 5	+10%	V
Analogue supply range	AVDD		-10%	3.3 to 5	+10%	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current	AVDD = 5V			50		mA
Digital supply current	DVDD = 5V			15		mA
Analogue supply current	AVDD = 3.3V			45		mA
Digital supply current	DVDD = 3.3V			15		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Circuit Specifications						
SNR (See Notes 1 and 2)		AVDD, DVDD = 5V	95	102		dB
		AVDD, DVDD = 3.3V		100		dB
SNR with automute on		AVDD, DVDD = 5V		110		dB
		AVDD, DVDD = 3.3V		108		dB
THD (full-scale) (See Note 2)		0dB		-96	-85	dB
THD+N (Dynamic range) (See Note 2)		-60dB		102		dB
Frequency response			0		20,000	Hz
Pass band ripple				0.125		dB
Transition band			20,000			Hz
Out of band rejection				-40		dB
Channel separation				90		dB
Gain mismatch channel-to-channel				±1		%FSR
Digital Logic Levels						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW level	V_{OL}	I_{OL} = 2mA			GND + 0.3V	
Output HIGH level	V_{OH}	I_{OH} = 2mA	DVDD - 0.3V			
Analogue Output Levels						
Output level		Into 10kohm, full scale 0dB, (5V supply)		1.1		V_{RMS}
		Into 10kohm, full scale 0dB, (3.3V supply)		0.72		V_{RMS}
Minimum resistance load		To midrail or a.c. coupled (5V supply)		1		kohms
		To midrail or a.c. coupled (3.3V supply)		1		kohms
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				AVDD/2		V
Reference Levels						
Potential divider resistance		AVDD to CAP and CAP to AGND		90		kohms
Voltage at CAP				AVDD/2		
POR						
POR threshold				1.8		V

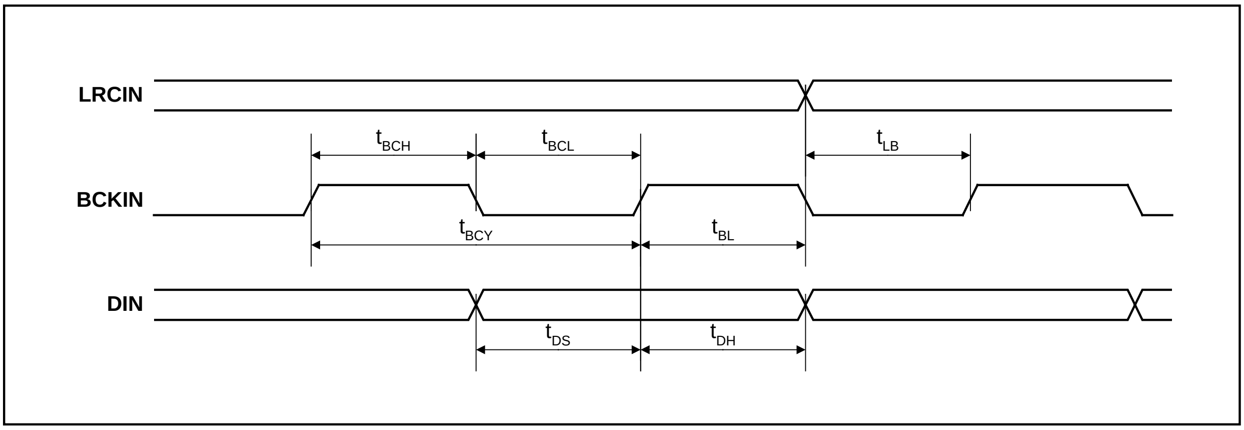


Figure 1 Audio Data Input Timing

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN pulse cycle time	t_{BCY}		100			ns
BCKIN pulse width high	t_{BCH}		50			ns
BCKIN pulse width low	t_{BCL}		50			ns
BCKIN rising edge to LRCIN edge	t_{BL}		30			ns
LRCIN rising edge to BCKIN rising edge	t_{LB}		30			ns
DIN setup time	t_{DS}		30			ns
DIN hold time	t_{DH}		30			ns

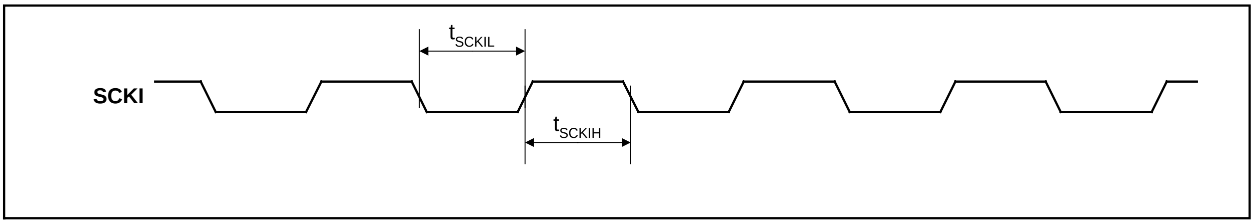


Figure 2 System Clock Timing Requirements

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
SCKI system clock pulse width high	t_{SCKIH}		13			ns
SCKI system clock pulse width low	t_{SCKIL}		13			ns

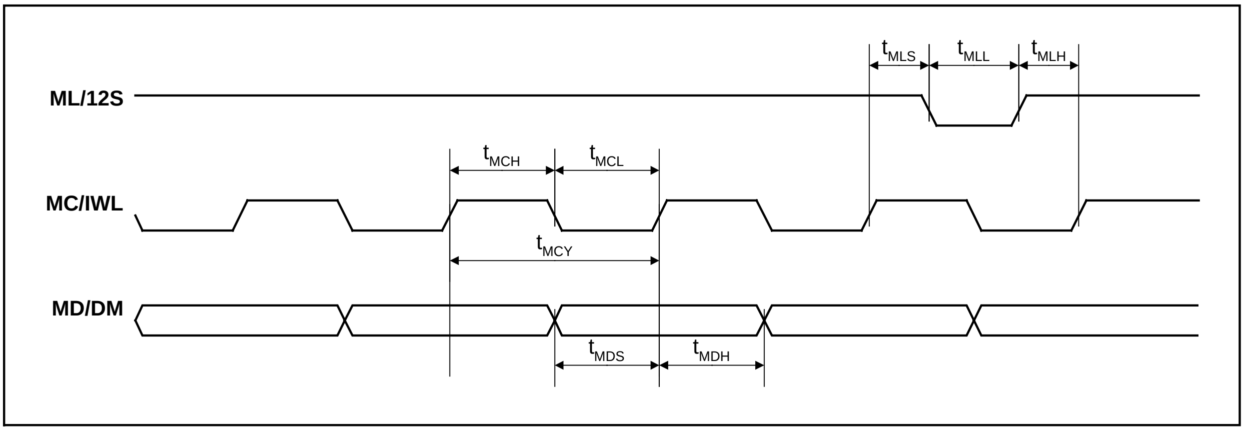


Figure 3 Program Register Input Timing

Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
MC/IWL pulse cycle time	t_{MCY}		100			ns
MC/IWL pulse width low	t_{MCL}		50			ns
MD/DM pulse width high	t_{MCH}		50			ns
MD/DM set-up time	t_{MDS}		30			ns
MC/IWL hold time	t_{MDH}		30			ns
ML/I2S pulse width low	t_{MLL}		30			ns
ML/I2S set-up time	t_{MLS}		30			ns
ML/I2S hold time	t_{MLH}		30			ns

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured “A” weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD	Supply	Digital positive supply.
2	SCKI	Digital input	System clock input (256, 384 or 512fs).
3	BCKIN	Digital input	Audio data bit clock input.
4	LRCIN	Digital input	Left sample rate clock input.
5	DIN0	Digital input	Channel 0 serial audio data input.
6	DIN1	Digital input	Channel 1 serial audio data input.
7	DIN2	Digital input	Channel 2 serial audio data input.
8	MODE	Digital input	Mode select pin. Low is software mode, high is hardware control. Internal pull-down.
9	MUTE	Digital I/O	Mute control pin, input or automute output. Low is not mute, high is mute, Z is automute.
10	RSTB	Digital input	Reset input – active low. Internal pull-up.
11	DGND	Supply	Digital ground supply
12	ML/I2S	Digital input	Latch enable (software mode) or input format selection (hardware mode). Internal pull-up.
13	MC/IWL	Digital input	Serial control data clock input (software mode) or input word length selection (hardware mode). Internal pull-up.
14	MD/DM	Digital input	Serial control data input (software mode) or de-emphasis selection (hardware mode).
15	AVDD1	Supply	Analogue positive supply.
16	CAP	Analogue output	Analogue internal reference.
17	OUT2L	Analogue output	Left channel 2 output.
18	GR2	Analogue input	Channel 2 reference.
19	OUT2R	Analogue output	Right channel 2 output.
20	AGND1	Supply	Analogue ground supply.
21	OUT1L	Analogue output	Left channel 1 output.
22	GR1	Analogue input	Channel 1 reference.
23	OUT1R	Analogue output	Right channel 1 output.
24	AGND2	Supply	Analogue ground supply.
25	OUT0L	Analogue output	Left channel 0 output.
26	GR0	Analogue input	Channel 0 reference.
27	OUT0R	Analogue output	Right channel 0 output.
28	AVDD2	Supply	Analogue positive supply.

Note:

Digital input pins have Schmitt trigger input buffers.

DEVICE DESCRIPTION

WM8736 is a complete 6-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters.

The device is implemented as three separate stereo DACs in a single package and controlled by a single interface. Three separate data input pins are provided for each of the three separate stereo DACs, and LRCIN, BCKIN and SCKI are shared between them.

Control of internal functionality of the device is by either hardware control (pin programmed) or software control (serial interface). The MODE pin selects between hardware and software control. In software control mode, an SPI type interface is used. This interface may be asynchronous to the audio data interface. Control data will be re-synchronized to the audio processing internally.

Operation using system clock of 256fs, 384fs or 512fs is provided, selection between clock rates being automatically controlled in hardware mode, or serial controlled when in software mode. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

The data interface supports normal (Japanese right justified) and I^2S (Philips left justified, one bit delayed) interface formats, in both ‘packed’ and unpacked forms. When in hardware mode, the three serial interface pins become control pins to allow selection of input data format type (I^2S or normal), input word length (16, 18, 20, or 24-bit) and de-emphasis function.

SYSTEM CLOCK

The system clock for WM8736 must be either 256fs, 384fs or 512fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48 or 96kHz. The system clock is used to operate the digital filters and the noise shaping circuits.

WM8736 has a system clock detection circuit that automatically determines what the system clock frequency relative to the sampling rate is (to within +/- 8 system clocks). If greater than 8 clocks error, then the interface shuts down the DAC and mutes the output. The system clock should be synchronised with LRCIN, but WM8736 is tolerant of phase differences or jitter on this clock. Severe distortion in the phase difference between LRCIN and the system clock will be detected, and cause the device to automatically resynchronise. If the externally applied LRCIN slips in phase by more than half the internal LRCIN period, which is derived from master clock, then the interface resynchronises. Such a case would, for example, occur if repeated LRCIN clocks were received with only 252 systems clocks per period. In this case the interface would only resynchronise once every 64 LRCIN periods, even if jitter was present on the LRCIN signal. During resynchronisation, the device will either repeat the previous sample, or drop the next sample, depending on the nature of the phase slip. This will ensure no discernible “click“ at the analogue outputs during resynchronisation. Table 1 shows the typical system clock frequency inputs for the WM8736.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHZ)		
	256fs	384fs	512fs
32kHz	8.192	12.288	16.384
44.1kHz	11.2896	16.9340	22.5792
48kHz	12.288	18.432	24.576
96kHz	24.576	36.864	

Table 1 System Clock Frequencies Versus Sampling Rate

AUDIO DATA INTERFACE

The Serial Data interface to WM8736 is fully compatible with both normal (MSB first, right-justified) or I^2S interfaces. Data may be ‘packed’ (number of serial bit clocks per LRCIN period is exactly 2 times the number of data bits, i.e. normally 32 in 16-bit mode) or unpacked (more than 32 bit clocks per LRCIN period).

The WM8736 will automatically detect 16-bit packed data being sent to the device in normal mode, and accept the data in this input format accordingly.

I^2S MODE	DESCRIPTION
0	Normal format (MSB-first, right Justified)
1	I^2S format (Philips serial data protocol)

Table 2 Serial Interface Formats

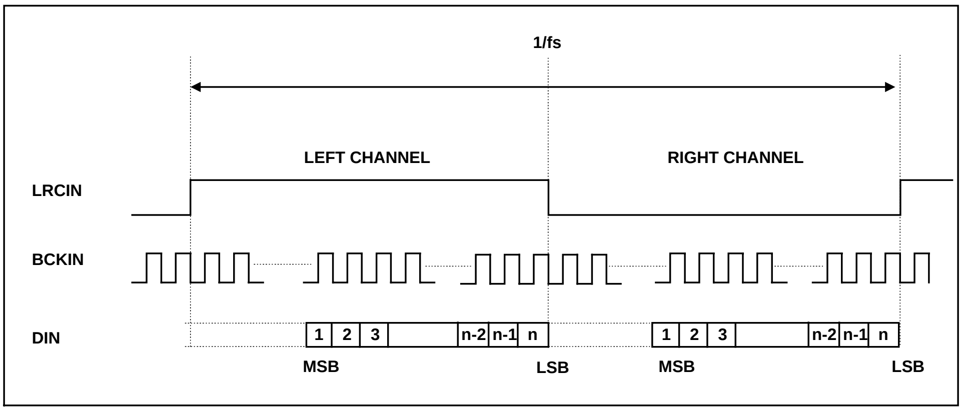


Figure 4 'Normal' Data Input Timing

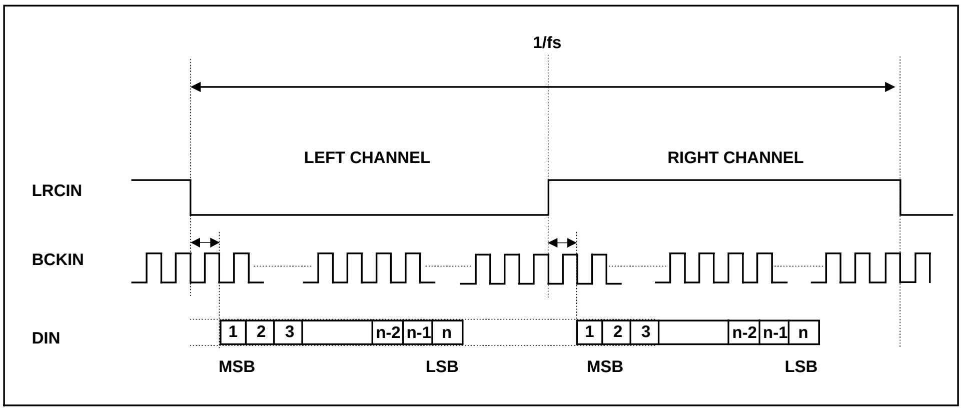


Figure 5 I^2S Data Input Timing

MODES OF OPERATION

Control of the various modes of operation is either by software control over the serial interface, or by hard-wired pin control. Selection of software or hardware mode is via MODE pin. The following functions may be controlled either via the serial control interface or by hard wiring of the appropriate pins.

FUNCTION	OPTIONS	SOFTWARE CONTROL DEFAULT VALUE PIN 8: MODE = 0	HARDWARE CONTROL BEHAVIOUR PIN 8: MODE = 1
Input audio data format	Normal format I^2S format	I^2S = 0 (default) I^2S = 1	Pin 12, 13: ML/I2S, MC/IWL = 00 or 01 or 10 Pin 12, 13: ML/I2S, MC/IWL = 11
Input word length	16 18 20 24	IW[1:0] = 00 (default) IW[1:0] = 11 IW[1:0] = 01 IW[1:0] = 10	Pin 12, 13: ML/I2S, MC/IWL = 00 Pin 12, 13: ML/I2S, MC/IWL = 11 (I^2S only) Pin 12, 13: ML/I2S, MC/IWL = 01 Pin 12, 13: ML/I2S, MC/IWL = 10
De-emphasis selection	On Off	DE = 1 DE = 0 (Default)	Pin 14: MD/DM = 1 Pin 14: MD/DM = 0
Mute	On Off	MU = 1 MU = 0 (default)	Pin 9: MUTE = 1 Pin 9: MUTE = 0
Reset and power down control	WM8736 off WM8736 on	Available from Pin 10: RSTB	Pin 10: RSTB = 0 Pin 10: RSTB = 1
Input LRCIN polarity	Lch/Rch = High/Low Lch/Rch = Low/High	LRP = 0 (default) LRP = 1	Not available in hardware mode, default value set
Volume control	Lch, Rch individually Lch, Rch common	ATC = 0; 0dB (default) ATC = 1	Not available in hardware mode, default 0dB
Infinite zero detect	On Off	IZD = 1 IZD = 0 (default)	Automute function controlled from MUTE pin low = not mute Z = automute enable high = muted
Operation enable (OPE)	Enabled Disabled	OPE = 0 (default) OPE = 1	
DAC output control	See Table 7 for all options	Default is PL[3:0] = 1001, stereo mode	Not available in hardware mode

Table 3 Control Function Summary

HARDWARE CONTROL MODES

When the MODE pin is held high the following hardware modes of operation are available.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes pin 9 (MUTE) controls selection of MUTE directly, and can be used to enable and disable the automute function, or as an output of the automuted signal.

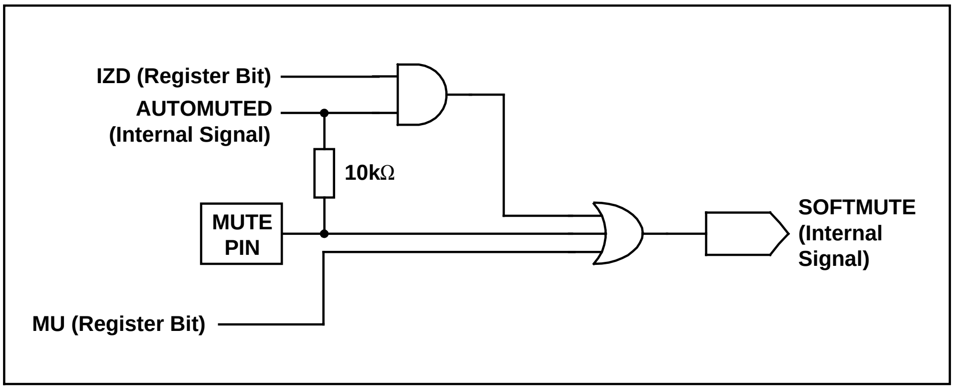


Figure 6 Mute Circuit Operation

The MUTE pin behaves as a bi-directional function, that is, as an input to select MUTE or NOT-MUTE, or as an output indication of automute operation. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of zero value audio samples of 1024 samples long being applied to both left and right channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a 10kohm resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert MUTE.

If MUTE is tied low, AUTOMUTED is overidden and will not mute. If MUTE is driven from a source follower, or diode, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10k source impedance) so can be used to drive external mute circuits.

The automute signal is AND'ed with IZD, this qualified mute signal then being OR'ed into the SOFTMUTE control. Therefore, in software mode, automute operation may be controlled with IZD control bit.

I^{2}S INPUT FORMAT SELECTION AND MC/IWL INPUT FORMAT SELECTION

In hardware mode, pins 12 and 13 become input controls for selection of input data format type and input data word length, see Table 4. I^{2}S mode is designed to support any word length provided enough bit clocks are sent.

I^{2}S	MC/IWL	INPUT DATA MODE
0	0	16-bit normal
0	1	20-bit normal
1	0	24-bit normal
1	1	I^{2}S mode

Table 4 Control of Input Data Format Type and Input Data Word Length

MD/DM DE-EMPHASIS

In hardware mode, pin 14 becomes an input control for selection of de-emphasis filtering to be applied. see Table 5.

MD/DM	0	De-emphasis off
MD/DM	1	De-emphasis on

Table 5 De-emphasis Control

RSTB RESET AND POWER DOWN CONTROL

In both hardware and software modes, this pin resets the entire device when taken low. The device remains powered down while RSTB is held low.

RSTB	0	Device powered down and reset
RSTB	1	Device powered up and active

Table 6 Reset and Power Down Control

SOFTWARE CONTROL INTERFACE

The WM8736 can be controlled using a 3-wire serial interface. MD/DM (pin 6) is used for the program data, MC/IWL (pin 5) is used to clock in the program data and ML/I2S (pin 4) is use to latch in the program data. The 3-wire interface protocol is shown in Figure 7.

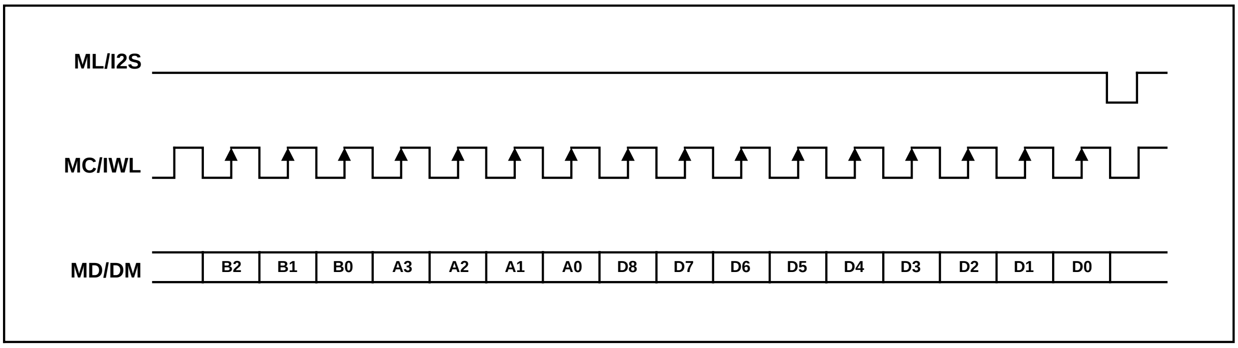


Figure 7 3-Wire Serial Interface

REGISTER MAP

WM8736 controls the special functions using 9 program registers, which are 16-bits long. These registers are all loaded through input pin MD/DM. After the 16 data bits are clocked in, ML/I2S is used to latch in the data to the appropriate register. Table 7 shows the complete mapping of the 9 registers.

	B2	**B1**	**B0**	**A3**	**A2**	**A1**	**A0**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	NOT USED			**ADDRESS**				**DATA**								
M0	-	-	-	0	0	0	0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
M1	-	-	-	0	0	0	1	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
M2	-	-	-	0	0	1	0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DE	MU
M3	-	-	-	0	0	1	1	IZD	-	-	-	-	-	ATC	LRP	I^2S
M4	-	-	-	0	1	0	0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
M5	-	-	-	0	1	0	1	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
M6	-	-	-	0	1	1	0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
M7	-	-	-	0	1	1	1	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
M8	-	-	-	1	0	0	0	LDM	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0

Table 7 Mapping of Program Registers

REGISTER NAME	BIT NAME	DEFAULT	DESCRIPTION
Register M0 A[3:0] = 0000	AL[7:0] LDL	1111 1111 0	Attenuation data for left channel DAC 0 Attenuation data load control for left channel DAC 0
Register M1 A[3:0] = 0001	AR[7:0] LDR	1111 1111 0	Attenuation data for right channel DAC 0 Attenuation data load control for right channel DAC 0
Register M2 A[3:0] = 0010	MU DE OPE IW[1:0] PL[3:0]	0 0 0 00 1001	Left and right DACs soft mute control De-emphasis control Left and right DACs operation control Input audio word resolution DAC output control
Register M3 A[3:0] = 0011	I^2S LRP ATC SF[1:0] IZD	0 0 0 00 0	Audio data format select Polarity of LRCIN (pin 4) Select Attenuator control Sampling rate select Infinite zero detection circuit control and automute control
Register M4 A[3:0] = 0100	AL[7:0] LDL	1111 1111 0	Attenuation data for left channel DAC 1 Attenuation data load control for left channel DAC 1
Register M5 A[3:0] = 0101	AR[7:0] LDR	1111 1111 0	Attenuation data for right channel DAC 1 Attenuation data load control for right channel DAC 1
Register M6 A[3:0] = 0110	AL[7:0] LDL	1111 1111 0	Attenuation data for left channel DAC 2 Attenuation data load control for left channel DAC 2
Register M7 A[3:0] = 0111	AR[7:0] LDR	1111 1111 0	Attenuation data for right channel DAC 2 Attenuation data load control for right channel DAC 2
Register M8 Master Gain A[3:0] = 1000	AM[7:0] LDM	1111 1111 0	DAC attenuation data for all channels Attenuation data load control for all channels

Table 8 Internal Register Mapping

DAC OUTPUT ATTENUATION

Registers M0 and M1 control the left and right channel attenuation of DAC 0. Registers M4 and M5 control the left and right channel attenuation of DAC 1. Registers M6 and M7 control the left and right channel attenuation of DAC 2. Register M8 is a master register that can be used to control attenuation of all channels.

Register M0 (A[3:0] = 0000) is used to control left channel 0 attenuation. Bits 0-7 (AL[7:0]) are used to determine the attenuation level (Table 9). The level of attenuation is given by:

Attenuation = [20.log10 (Attenuation_Data/256)] dB   Eqn. 1

AX[7:0]	ATTENUATION LEVEL
00(hex)	-∞dB (mute)
01(hex)	-48.16dB
:	:
:	:
:	:
FE(hex)	-0.07dB
FF(hex)	0dB

Table 9 Attenuation Control Levels

Bit 8 in register M0 (LDL) is used to control the loading of attenuation data in AL[7:0]. When LDL is set to 0, attenuation data will be loaded into AL[7:0], but it will not affect the attenuation level until LDL is set to 1.

Register M1 (A[1:0] = 01) is used to control right channel attenuation in the same manner. Attenuation of DAC 1 and 2 are similarly controlled.

Bit 2 in register M3 (A[3:0] = 0011) is used to control the attenuator (ATC). When ATC is high, the attenuation data loaded in the left channel program register is used for both the left and the right channels. Therefore, DAC 0 attenuation data for left and right channels is read from register M0, DAC 1 attenuation data for left and right channels is read from register M4 and DAC 2 attenuation data for left and right channels is read from register M6. When ATC is low, attenuation data is read from the individual left and right DAC registers.

The master gain register M8 (A[3:0] = 0110) is used to write a gain value to all channels simultaneously. Bit 8 (LDM) controls the update in the same way as the attenuation registers, and is to be set to 1 for correct operation in this mode.

LEFT AND RIGHT DAC SOFT MUTE CONTROL

Soft mute is controlled by setting bit MU, register M2:bit 0. A high level on MU (MU = 1) will cause the output to be muted, the effect of which is to ramp the signal down in the digital domain so that there is no discernible click. This can be seen in Figure 6 Mute Circuit Operation.

DE-EMPHASIS CONTROL

Bit 1 (DE) in register M2 is used to control digital de-emphasis. A low level on bit 1 (DE = 0) disables de-emphasis whilst a high level enables de-emphasis (DE = 1). De-emphasis applied to the filters shapes the frequency response of the digital filter according to the input sample frequency.

LEFT AND RIGHT DAC OPERATION CONTROL

Bit 2 (OPE) in register M2 is used for operation control. With OPE = 0 (default) the device functions normally. With OPE = 1 the device is disabled and the outputs are held at midrail. Current consumption of the digital section is minimized, but analogue sections remain active in order to preserve d.c. levels.

INPUT AUDIO WORD RESOLUTION

WM8736 allows maximum flexibility over the control of the audio data interface, allowing selection of format type, word length, and sample rates. Bits 3 and 4 of register M2 (IW[1:0]) are used to determine the input word resolution. WM8736 supports 16-bit, 18-bit, 20-bit and 24-bit formats as described in Table 10.

BIT 4 (IW1)	BIT 3 (IW0)	INPUT RESOLUTION
0	0	16-bit data word
0	1	20-bit data word
1	0	24-bit data word
1	1	18-bit data word

Table 10 Input Data Resolution

DAC OUTPUT CONTROL

Bits 5, 6, 7 and 8 (PL[3:0]) of register M2 are used to control the output format as shown in Table 11.

PL3	PL2	PL1	PL0	LEFT OUTPUT	RIGHT OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	Mute both channels
0	0	0	1	L	MUTE	
0	0	1	0	R	MUTE	
0	0	1	1	(L + R)/2	MUTE	
0	1	0	0	MUTE	L	
0	1	0	1	L	L	
0	1	1	0	R	L	Reverse channels
0	1	1	1	(L + R)/2	L	
1	0	0	0	MUTE	R	
1	0	0	1	L	R	Stereo mode
1	0	1	0	R	R	
1	0	1	1	(L + R)/2	R	
1	1	0	0	MUTE	(L + R)/2	
1	1	0	1	L	(L + R)/2	
1	1	1	0	R	(L + R)/2	
1	1	1	1	(L + R)/2	(L + R)/2	Mono mode

Table 11 Programmable Output Format

SERIAL PROTOCOL

Bits 0 (I^2S) and 1 (LRP) of register M3 are used to control the input data format completely. A low on bit 0 ($I^2S = 0$) sets the format to Normal (MSB-first, right justified Japanese format), whilst a high ($I^2S = 1$) sets the format to I^2S (Philips serial data protocol).

POLARITY OF LRCIN SELECT

Bit 1 (LRP) of register M3 is used to control the polarity of LRCIN (sample rate clock). When bit 1 is low (LRP = 0), left channel data is assumed when LRCIN is in a high phase and right channel data is assumed when LRCIN is in a low phase. When bit 1 is high (LRP = 1), the polarity assumption is reversed.

INTERFACE CLOCKS AND SAMPLING RATES

Bits 6 (SF0) and 7 (SF1) of register M3 are used to control the sampling frequency, as shown in Table 12.

SF0	SF1	SAMPLING FREQUENCY	
0	0	44.1kHz group	22.05 / 44.1 / 88.2kHz
0	1	48kHz group	24 / 48 / 96kHz
1	0	32kHz group	16 / 32 / 64kHz
1	1	Reserved	Not defined

Table 12 Sampling Frequencies

INFINITE ZERO DETECTION

Bit 8 (IZD) in register M3 controls operation of the automute function. If IZD (Infinite Zero Detect) is high, 1024 consecutive zero audio samples will force the ouput to zero. See Figure 6. Note that the control of pin MUTE also affects automute operation. To turn off automute, pin MUTE must be held low as well as IZD being low (default).

RECOMMENDED EXTERNAL COMPONENTS

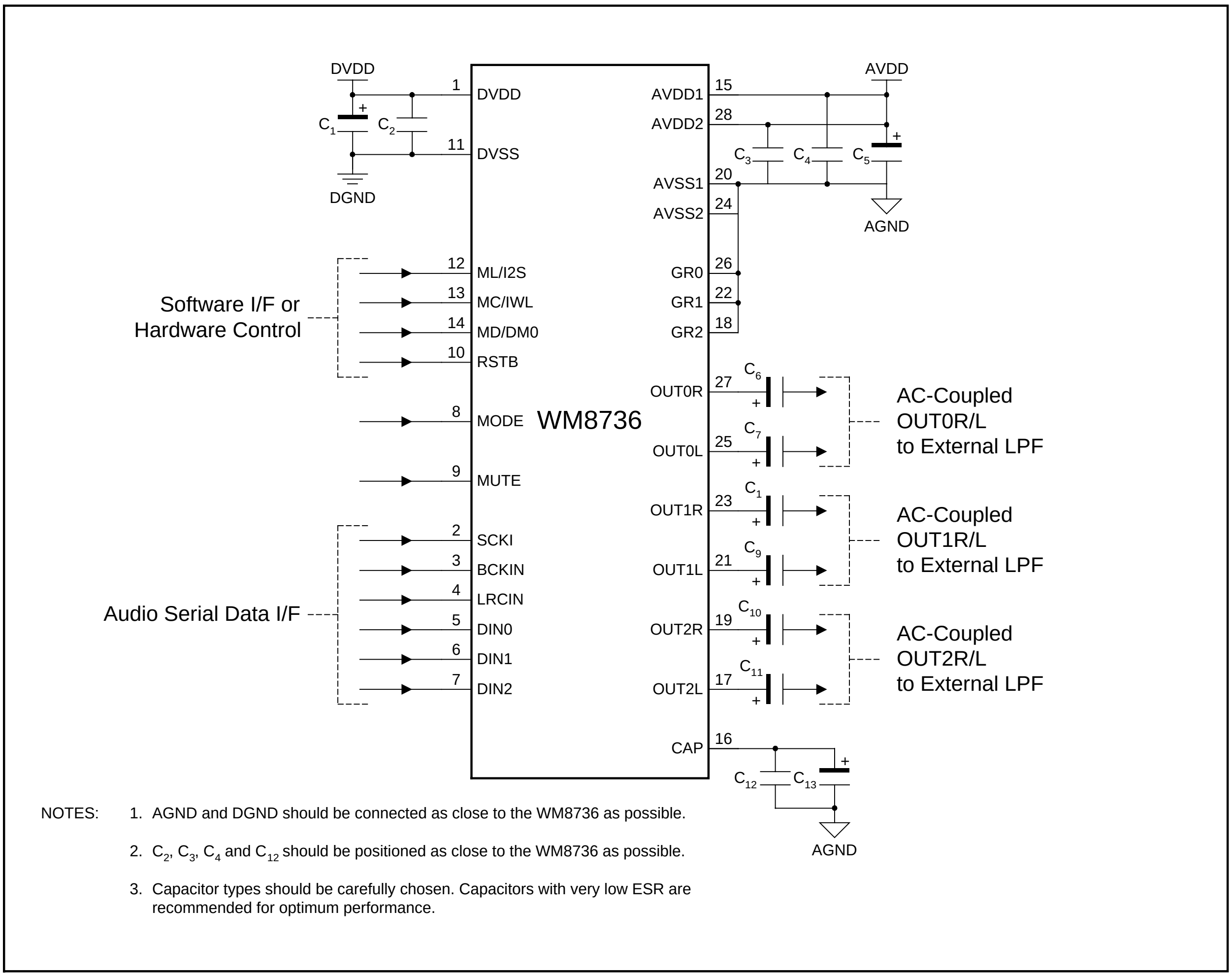


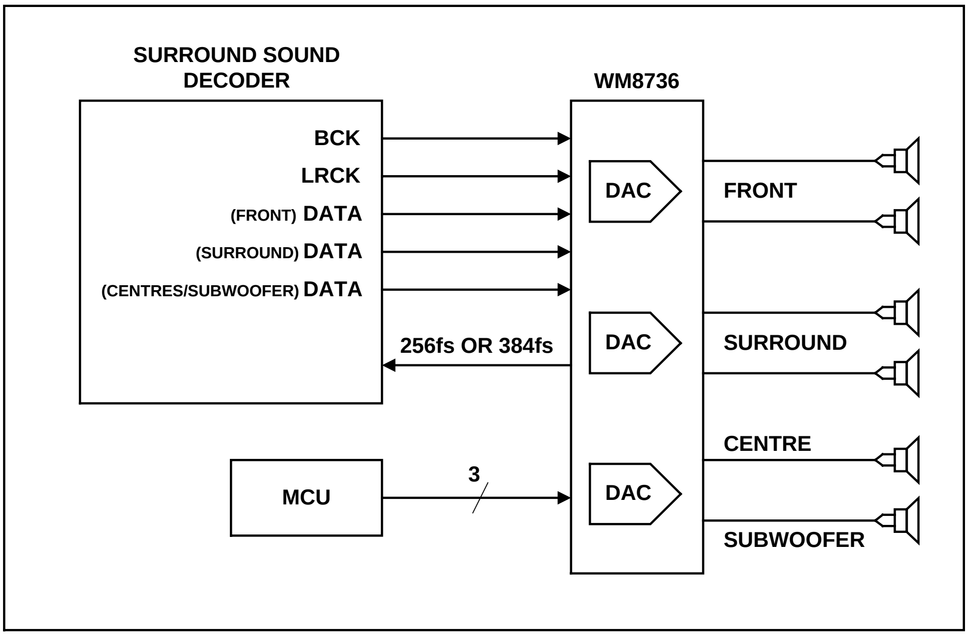
Figure 8 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C5	10µF	De-coupling for DVDD and AVDD.
C2 to C4	0.1µF	De-coupling for DVDD and AVDD.
C6 to C11	10µF	Output AC coupling caps to remove midrail DC level from outputs.
C12	0.1µF	Reference de-coupling capacitors for CAP pin.
C13	10µF	

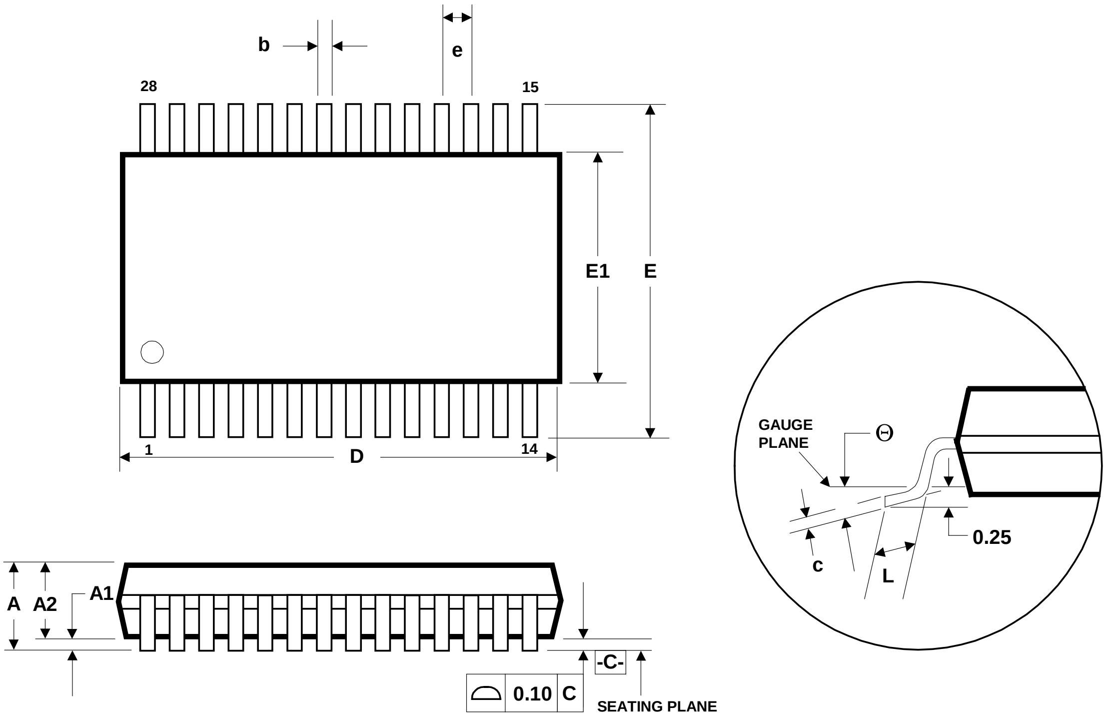
Table 13 External Components Description

APPLICATIONS RECOMMENDED



PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.62	1.75	1.85
b	0.22	-----	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e	0.65 BSC		
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.