WM8850

Multi-Channel High Definition Audio CODEC

DESCRIPTION

The WM8850 is a high performance multi-channel audio CODEC designed for high performance PC audio systems. The device offers full compatibility with the Intel High Definition Audio (HDA) specification revision 1.0, allowing seamless integration with industry-standard HDA controllers.

The WM8850 has three high performance stereo DACs to enable six channels of high definition audio, ideal for 5.1 channel applications. A high-performance ground-referenced stereo headphone amplifier utilises advanced charge pump and DC servo technology to minimise system cost and space without compromise on audio quality. Line outputs provide a high-quality differential connection to speaker amplifiers, enabling common mode noise rejection when these traces are routed across a PCB.

The WM8850 also has two high performance stereo ADCs to provide Hi-Fi quality analogue line-in and microphone input digitisation. A low noise microphone bias with programmable output voltage is provided. Additionally, the CODEC contains a digital microphone interface capable of supporting up to four independent digital microphones. One differential stereo input is provided for line level signals, while one pseudo-differential stereo input with integrated microphone preamplifier is provided.

The WM8850 also contains a S/PDIF transceiver which is fully compatible with IEC-60958-3. The S/PDIF receive and transmit paths each contain a sample rate converter (SRC) to enable asynchronous sample rate conversion between the S/PDIF receive/transmit and HDA interface clock domains. An additional S/PDIF transmitter is provided to allow direct output of a stereo stream from the HDA interface.

The WM8850 is supplied in a small 48-pin QFN package.

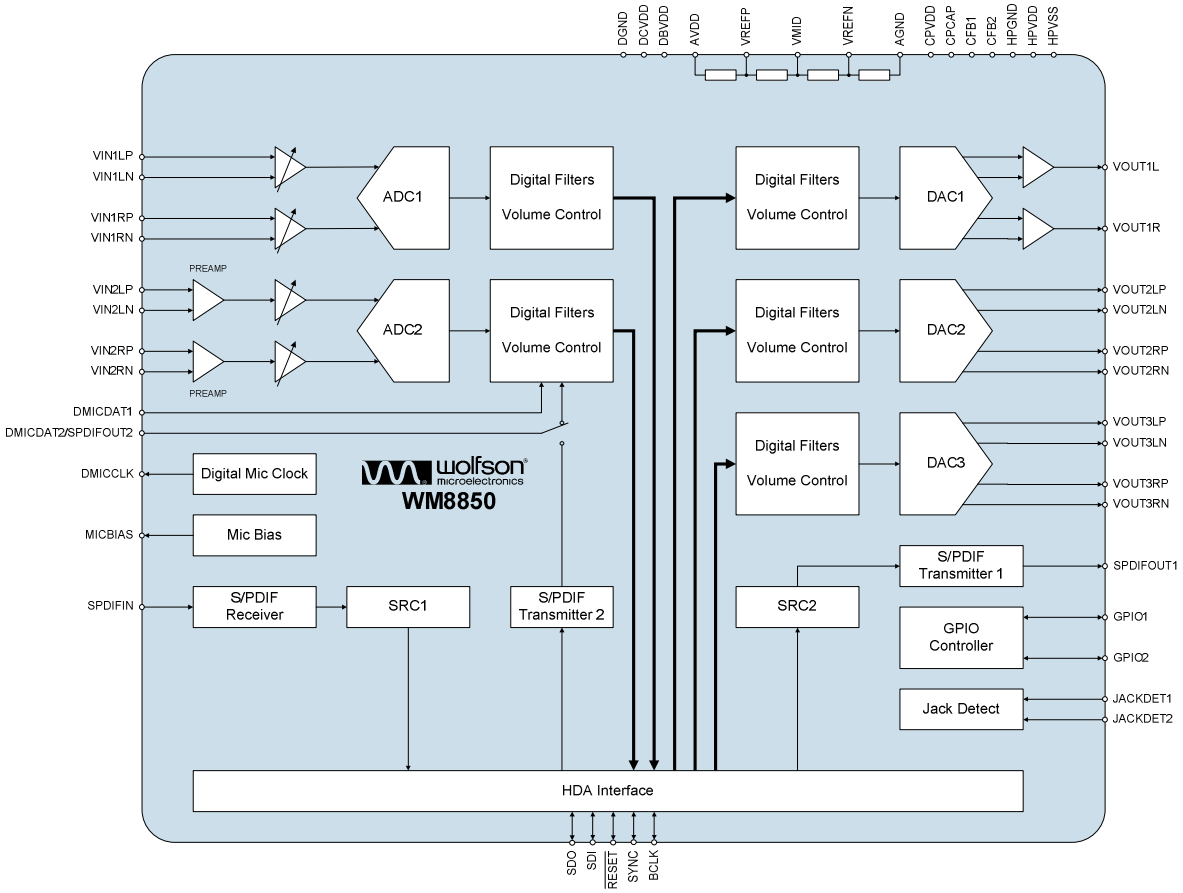
FEATURES

- Multi-channel High Definition Audio CODEC
- Fully compatible with Intel High Definition Audio Revision 1.0
- 6-Channel DAC, 4-channel ADC
- DAC sampling frequency 8kHz - 192kHz
- ADC sampling frequency 8kHz - 96kHz
- DAC Performance:
  - SNR 108 dB ('A' weighted)
  - SNR 105dB (non weighted)
  - THD -96dB (at 0dBFS)
- ADC Performance:
  - SNR 105 dB ('A' weighted)
  - SNR 102dB (non weighted)
  - THD -95dB (at -1dBFS)
- Ground-referenced stereo headphone driver
- Differential line inputs/outputs
- Stereo microphone interface with integrated pre-amp
- Multi-channel digital microphone interface
- IEC-60958-3 compatible S/PDIF transceiver
- Additional IEC-60958-3 compatible S/PDIF transmitter
- Jack detect and load impedance sensing
- Beep generator
- GPIO functionality
- IEEE-754 Single precision 32-bit floating point support
- Power supplies
  - Digital core: 1.62V – 1.98V
  - Digital buffer: 2.97V – 3.63V
  - Analogue: 4.5V – 5.5V
  - Charge pump: 4.5V – 5.5V
- 48-pin 7mm x 7mm QFN package

APPLICATIONS

- High performance PC audio
- All-in-one desktop PC
- Notebook PC

BLOCK DIAGRAM



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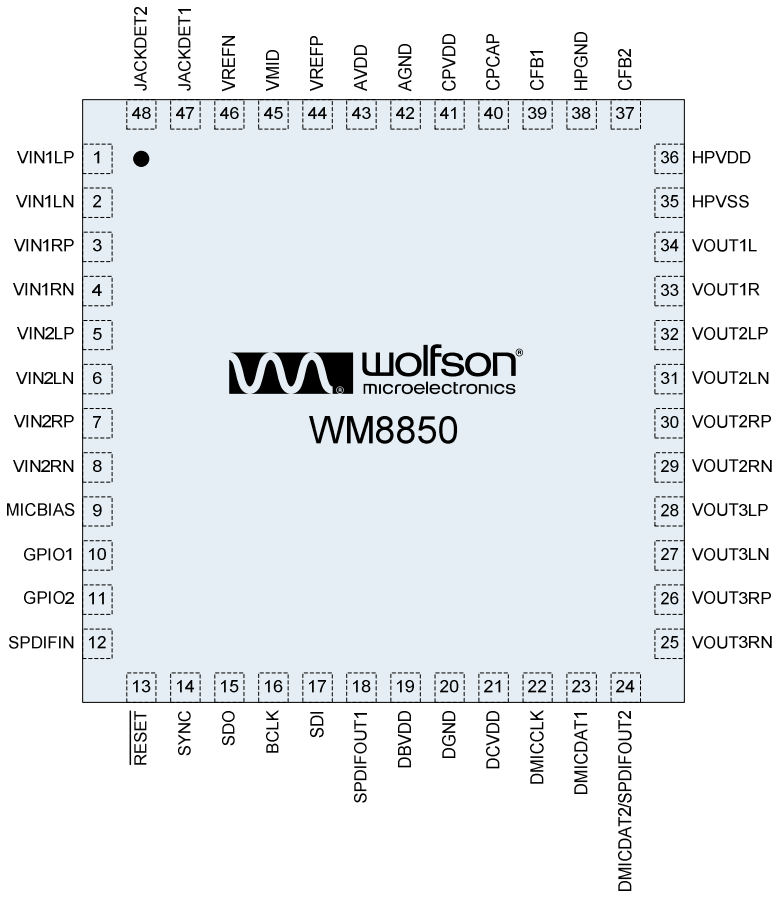
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8850GEFL/V	-40°C to +85°C	48-pin QFN (Pb-free)	MSL3	260°C
WM8850GEFL/RV	-40°C to +85°C	48-pin QFN (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 2200

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	VIN1LP	Analogue input	Left channel 1 positive input
2	VIN1LN	Analogue input	Left channel 1 negative input
3	VIN1RP	Analogue input	Right channel 1 positive input
4	VIN1RN	Analogue input	Right channel 1 negative input
5	VIN2LP	Analogue input	Left channel 2 positive input
6	VIN2LN	Analogue input	Left channel 2 negative input
7	VIN2RP	Analogue input	Right channel 2 positive input
8	VIN2RN	Analogue input	Right channel 2 negative input
9	MICBIAS	Analogue output	Microphone bias output
10	GPIO1	Digital input / output	General purpose digital input/output 1
11	GPIO2	Digital input / output	General purpose digital input/output 2
12	SPDIFIN	Digital input	S/PDIF Input
13	/RESET	Digital input	Global reset (active low)
14	SYNC	Digital input	HDA frame sync, 48kHz
15	SDO	Digital input	Serial data output from HDA controller
16	BCLK	Digital input	HDA Link bit clock, 24MHz
17	SDI	Digital input / output	Serial data input to HDA controller
18	SPDIFOUT1	Digital output	S/PDIF output 1
19	DBVDD	Supply input	Digital buffer supply input
20	DGND	Supply input	Digital ground (return for DBVDD and DCVDD)
21	DCVDD	Supply input	Digital core supply input
22	DMICCLK	Digital output	Digital microphone clock output
23	DMICDAT1	Digital input	Digital microphone data input 1
24	DMICDAT2/ SPDIFOUT2	Digital input / output	Digital microphone data input 2 / S/PDIF output 2
25	VOUT3RN	Analogue output	Right channel 3 negative output
26	VOUT3RP	Analogue output	Right channel 3 positive output
27	VOUT3LN	Analogue output	Left channel 3 negative output
28	VOUT3LP	Analogue output	Left channel 3 positive output
29	VOUT2RN	Analogue output	Right channel 2 negative output
30	VOUT2RP	Analogue output	Right channel 2 positive output
31	VOUT2LN	Analogue output	Left channel 2 negative output
32	VOUT2LP	Analogue output	Left channel 2 positive output
33	VOUT1R	Analogue output	Right channel 1 output
34	VOUT1L	Analogue output	Left channel 1 output
35	HPVSS	Supply output	Charge pump negative supply decoupling point
36	HPVDD	Supply output	Charge pump positive supply decoupling point
37	CFB2	Analogue output	Charge pump flyback capacitor pin 2
38	HPGND	Supply input	Charge pump ground (return path for HPVDD and HPVSS)
39	CFB1	Analogue output	Charge pump flyback capacitor pin 1
40	CPCAP	Supply output	Internally generated regulated charge pump supply decoupling point
41	CPVDD	Supply input	Charge pump supply input
42	AGND	Supply input	Analogue ground (return path for AVDD and CPVDD)
43	AVDD	Supply input	Analogue supply input
44	VREFP	Analogue output	Analogue positive reference decoupling point
45	VMID	Analogue output	Midrail voltage decoupling point
46	VREFN	Analogue output	Analogue negative reference decoupling point
47	JACKDET1	Analogue output	Jack detect sense 1
48	JACKDET2	Analogue output	Jack detect sense 2

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage (AVDD)	-0.3V	+7V
Charge pump supply voltage (CPVDD)	-0.3V	+7V
Digital core supply voltage (DCVDD)	-0.3V	+2.5V
Digtial buffer supply voltage (DBVDD)	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CODEC Power Supplies					
Digital core supply range	DCVDD	1.62	1.8	1.98	V
Digital buffer supply range	DBVDD	2.97	3.3	3.63	V
Analogue supply range	AVDD	4.5	5.0	5.5	V
Charge pump supply range	CPVDD	4.5	5.0	5.5	V
Ground	DGND, AGND, HPGND		0		V

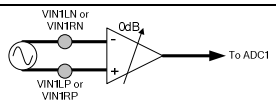
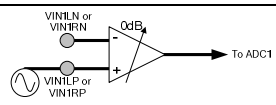
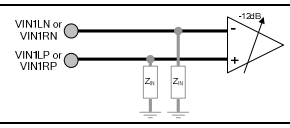
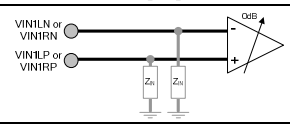
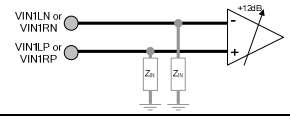
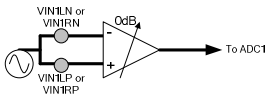
Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).

ELECTRICAL CHARACTERISTICS

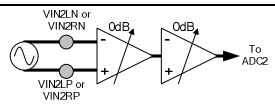
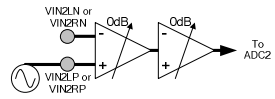
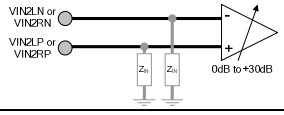
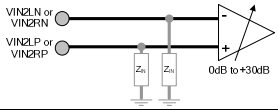
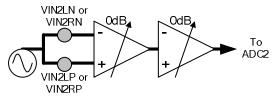
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input 1 (VIN1LP, VIN1LN, VIN1RP, VIN1RN)							
Maximum Differential Input Signal Level	$V_{INDIFF(max)}$	0dB gain			2.25 x AVDD/5		V_{RMS}
Maximum Single-ended Input Signal Level	$V_{INSE(max)}$	0dB gain			1.6 x AVDD/5		V_{RMS}
Input impedance	Z_{IN}	-12dB gain			42		kΩ
		0dB gain			27		kΩ
		+12dB gain			9		kΩ
Common Mode Rejection Ratio	CMRR	20Hz to 20kHz			55		dB
Minimum PGA Gain Setting					-12		dB
Maximum PGA Gain Setting					+12		dB
PGA Gain Step Size		Guaranteed monotonic			0.5		dB

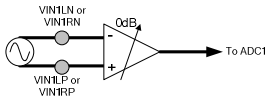
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input 2 (VIN2LP, VIN2LN, VIN2RP, VIN2RN)							
Maximum Differential Input Signal Level	$V_{INDIFF(max)}$	0dB gain			2.25 x AVDD/5		V_{RMS}
Maximum Single-ended Input Signal Level	$V_{INSE(max)}$	0dB gain			1.1 x AVDD/5		V_{RMS}
Input impedance	Z_{IN}	Single-ended or Differential (Inverting)			10		kΩ
		Differential (Non-inverting)			120		kΩ
Common Mode Rejection Ratio	CMRR	20Hz to 20kHz			65		dB
Microphone Preamp Gain Options					0 10 20 30		dB
Minimum PGA Gain Setting					-12		dB
Maximum PGA Gain Setting					+12		dB
PGA Gain Step Size		Guaranteed monotonic			0.5		dB

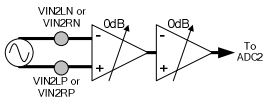
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC1 Performance							
Signal to Noise Ratio	SNR	Unweighted			102		dB
		A-weighted		100	105		dB
		A-weighted fs=96kHz			105		dB
Dynamic Range	DNR	A-weighted -60dBFS			105		dB
Total Harmonic Distortion	THD	-1dBFS			-95	-90	dB
		-1dBFS fs=96kHz			-95		dB
Channel Separation		1kHz			86		dB
		20Hz to 20kHz			86		dB
Channel Level Matching		0dBFS			0.1		dB
Channel Phase Deviation					0.01		°
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD			90		dB
		20Hz to 20kHz, 100mVpp on AVDD			70		dB

Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC2 Performance							
Signal to Noise Ratio	SNR	Unweighted			100		dB
		A-weighted		95	103		dB
		A-weighted fs=96kHz			103		dB
Dynamic Range	DNR	A-weighted -60dBFS			103		dB
Total Harmonic Distortion	THD	-1dBFS			-95	-90	dB
Channel Separation		1kHz			87		dB
		20Hz to 20kHz			84		dB
Channel Level Matching		0dBFS			0.1		dB
Channel Phase Deviation					0.01		°
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD			90		dB
		20Hz to 20kHz, 100mVpp on AVDD			70		dB

Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias Generator						
Output Voltage		VRefEn[2:0] = 001		0.5x AVDD		V
		VRefEn[2:0] = 100		0.8x AVDD		V
Current Source Capability					2.5	mA
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD		100		dB
		20Hz to 20kHz, 100mVpp on AVDD		88		dB

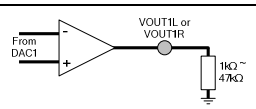
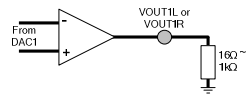
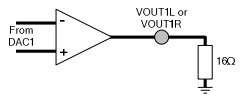
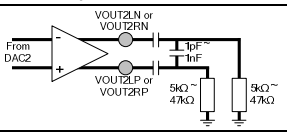
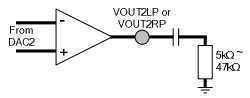
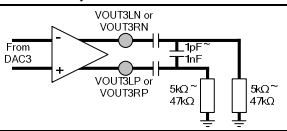
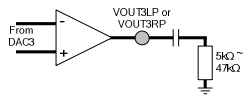
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Interface						
Digital Microphone Clock Frequencies				1.024 1.4112 2.048 2.8224 3.072		MHz
Signal to Noise Ratio	SNR			96		dB
Minimum Digital Gain Setting				-12		dB
Maximum Digital Gain Setting				+32		dB
Digital Gain Step Size				0.5		dB

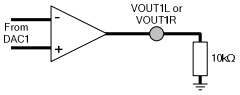
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Output 1 (VOUT1L, VOUT1R)							
Full Scale Output Signal Level	V_{OUT}	R_L = 1kΩ to 47kΩ H-Phn Enable = 0			2 x AVDD/5		V_{RMS}
		R_L = 16Ω to 1kΩ H-Phn Enable = 1			0.8 x AVDD/5		V_{RMS}
Maximum Rated Output Power	$P_{OUT(max)}$	R_L = 16Ω				40	mW
Load Impedance	R_L			16		47k	Ω
Load Capacitance	C_L					1	nF
DC Offset		Measured between VOUT1L/R and AGND with path fully enabled but no signal playing		-1	0	+1	mV
Analogue Output 2 (VOUT2L, VOUT2LN, VOUT2RP, VOUT2RN)							
Differential Full Scale Output Signal Level	V_{OUT}	R_L = 5kΩ to 47kΩ			2 x AVDD/5		V_{RMS}
Single-ended Full Scale Output Signal Level	V_{OUT}	R_L = 5kΩ to 47kΩ			1 x AVDD/5		V_{RMS}
Load Impedance	R_L			5		47	kΩ
Load Capacitance	C_L					1	nF
Analogue Output 3 (VOUT3L, VOUT3LN, VOUT3RP, VOUT3RN)							
Differential Full Scale Output Signal Level	V_{OUT}	R_L = 5kΩ to 47kΩ			2 x AVDD/5		V_{RMS}
Single-ended Full Scale Output Signal Level	V_{OUT}	R_L = 5kΩ to 47kΩ			1 x AVDD/5		V_{RMS}
Load Impedance	R_L			5		47	kΩ
Load Capacitance	C_L					1	nF

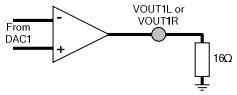
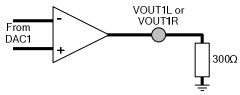
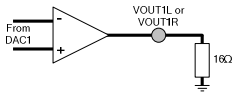
Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC1 Path Performance (VOUT1L and VOUT1R into 10kΩ Line Load)							
Signal to Noise Ratio	SNR	Unweighted			105		dB
		A-weighted		100	108		dB
		A-weighted fs=96kHz			108		dB
Out of Band Signal to Noise Ratio (0.6fs to 150kHz)	OBSNR	Fs > 11.025kHz			80		dB
		Fs <= 11.025kHz			75		dB
Dynamic Range	DNR	A-weighted -60dBFS			108		dB
Total Harmonic Distortion	THD	0dBFS			-96	-85	dB
		0dBFS fs=96kHz			-96	-85	dB
Channel Separation		1kHz			115		dB
		20Hz to 20kHz			110		dB
Channel Level Matching		0dBFS			0.1		dB
Channel Phase Deviation					0.01		°
AVDD Power Supply Rejection Ratio	AVDD PSRR	1kHz, 100mVpp on AVDD			51		dB
		20Hz to 20kHz, 100mVpp on AVDD			50		dB
CPVDD Power Supply Rejection Ratio	CPVDD PSRR	1kHz, 100mVpp on CPVDD			86		dB
		20Hz to 20kHz, 100mVpp on CPVDD			75		dB

Test Conditions

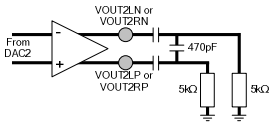
AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

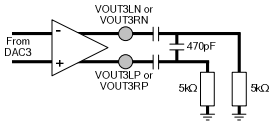
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC1 Path Performance (VOUT1L and VOUT1R into 16Ω Headphone Load)							
Total Harmonic Distortion	THD	P_{OUT} = 30mW R_L = 16Ω			--80	-73	dB
					0.01		%
		P_{OUT} = 10mW R_L = 300Ω			-80		dB
					0.01		%
Idle Channel Noise		R_L = 16Ω A-weighted		90	98		dBV
					12.26		μV_{rms}
Channel Separation		R_L = 16Ω 1kHz			85		dB
		R_L = 16Ω 20Hz to 20kHz			72		dB

Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC2 Path Performance (VOUT2LP, VOUT2LN, VOUT2RP and VOUT2N into 10kΩ Line Load) **DAC3 Path Performance (VOUT3LP, VOUT3LN, VOUT3RP and VOUT3N into 10kΩ Line Load)**							
Signal to Noise Ratio	SNR	Unweighted			103		dB
		A-weighted		100	106		dB
		A-weighted fs=96kHz			106		dB
Out of Band Signal to Noise Ratio (0.6fs to 150kHz)	OBSNR	Fs > 11.025kHz			80		dB
		Fs <= 11.025kHz			75		dB
Dynamic Range	DNR	A-weighted -60dBFS			106		dB
Total Harmonic Distortion	THD	0dBFS			-92		dB
		0dBFS fs=96kHz			-92		dB
Channel Separation		20Hz to 20kHz			102		dB
Channel Level Matching		0dBFS			0.1		dB
Channel Phase Deviation					0.01		°
AVDD Power Supply Rejection Ratio	AVDD PSRR	1kHz, 100mVpp on AVDD			75		dB
		20Hz to 20kHz, 100mVpp on AVDD		55			dB





Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
S/PDIF Receiver Specification						
Input Signal Level		IEC-60958 Compatible Input Mode	200	500		mV_{p-p}
Input Signal Logic High	$V_{IH(S/PDIF)}$	Normal CMOS Compatible Input Mode	0.7 * DBVDD			V
		Low-Amplitude CMOS Compatible Input Mode	0.4 * DBVDD		1.8	V
Input Signal Logic Low	$V_{IL(S/PDIF)}$	Normal CMOS Compatible Input Mode			0.3 * DBVDD	V
		Low-Amplitude CMOS Compatible Input Mode			DBVDD x 0.2	V
Input Pin Bias Voltage		IEC-60958 Compatible Input Mode		0.5 * DCVDD		V
Input Impedance	Z_{IN}	IEC-60958 Compatible Input Mode	7.5			kΩ
		Normal CMOS Compatible Input Mode	100			kΩ
Input Hysteresis		IEC-60958 Compatible Input Mode		50		mV
		Normal CMOS Compatible Input Mode		300		mV
		Low-Amplitude CMOS Compatible Input Mode		150		mV
Input Sample Rate Lock Tolerance		Includes maximum reference clock error of ±0.025% as allowed by HDA Specification			10000	ppm
			-1		+1	%
Lock Delay				3		192 Frame Blocks
S/PDIF Stream Jitter Tolerance		UI = $1/fs_{(in)}$			10	UI
Input Sample Rate Support				32 44.1 48 88.2 96		kHz

Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
S/PDIF Transmitter Specification						
Output Signal Logic High	$V_{OH(S/PDIF)}$		0.9 * DBVDD			V
Output Signal Logic Low	$V_{OL(S/PDIF)}$				0.1 * DBVDD	V
Output Current Source/Sink Capability		DBVDD = 1.8V	7			mA
		DBVDD = 3.63V	15			mA
Output Sample Rate Tolerance		Includes maximum reference clock error of ±0.025% as allowed by HDA Specification			1000	ppm
			-0.1		+0.1	%
Output Sample Rate Support				32 44.1 48 88.2 96 176.4 192		kHz

Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue References						
Positive Voltage Reference	VREFP			0.9 * AVDD		V
Negative Voltage Reference	VREFN			0.1 * AVDD		V
Midrail Voltage Reference	VMID			0.5 * AVDD		V
Charge Pump Cap Level	CPCAP			3.15		V
Midrail Voltage Resistance	R_{VMID}	AVDD to VMID or VMID to AGND VMID_SEL[1:0]=00		12.5		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=01		75		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=10		37.5		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=11		375		kΩ
Digital Input / Output						
Input High Level	V_{IH}		0.65 * DBVDD			V
Input Low Level	V_{IL}				0.35 * DBVDD	V
Output High Level	V_{OH}		0.9 * DBVDD			V
Output Low Level	V_{OL}				0.1 * DBVDD	V
Input Capacitance					7.5	pF
Input Leakage			-0.1		+0.1	µA

INTRODUCTION

The WM8850 is a high performance multi-channel audio CODEC designed for high performance PC audio systems. The device offers full compatibility with the Intel High Definition Audio (HDA) specification revision 1.0, allowing seamless integration with industry-standard HDA controllers.

The WM8850 has three high performance stereo DACs to enable six channels of high definition audio, ideal for 5.1 channel applications. A high-performance ground-referenced stereo headphone amplifier utilises advanced charge pump and DC servo technology to minimise system cost and space without compromise on audio quality. Two stereo pairs of line outputs are also provided. These line outputs may be used at the output of the PC to enable connection to a 5.1 speaker system, or may be used connected to external speaker drivers in a notebook or netbook application.

The WM8850 also has two high performance stereo ADCs to provide Hi-Fi quality analogue line-in and microphone input digitisation. A low noise microphone bias with programmable output voltage is provided, ideally suited as a bias current source for ECM microphones. Additionally, the CODEC contains a digital microphone interface capable of supporting up to four independent digital microphones, allowing high quality microphone array implementations to be realised. One differential stereo input is provided for line level signals, while one pseudo-differential stereo input with integrated microphone preamplifier is provided.

The WM8850 also contains a S/PDIF transceiver which is fully compatible with IEC-60958-3. The S/PDIF receive and transmit paths each contain a sample rate converter (SRC) to enable asynchronous sample rate conversion between the S/PDIF receive/transmit and HDA interface clock domains. An additional S/PDIF transmitter is provided to allow direct output of a stereo stream from the HDA interface.

The WM8850 includes an integrated beep generator allowing system beeps to be played back through the output paths.

This datasheet assumes familiarity with the High Definition Audio Specification Revision 1.0, available from http://www.intel.com/standards/hdaudio/. For those verbs implemented in the WM8850 which are as defined in the High Definition Audio Specification Revision 1.0 there is no detailed text describing their use in this datasheet. However, detailed text describing the function of of vendor-specific verbs is provided. Additionally, a full list of each node and each verb implemented in the WM8850 is provided at the rear of the document.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

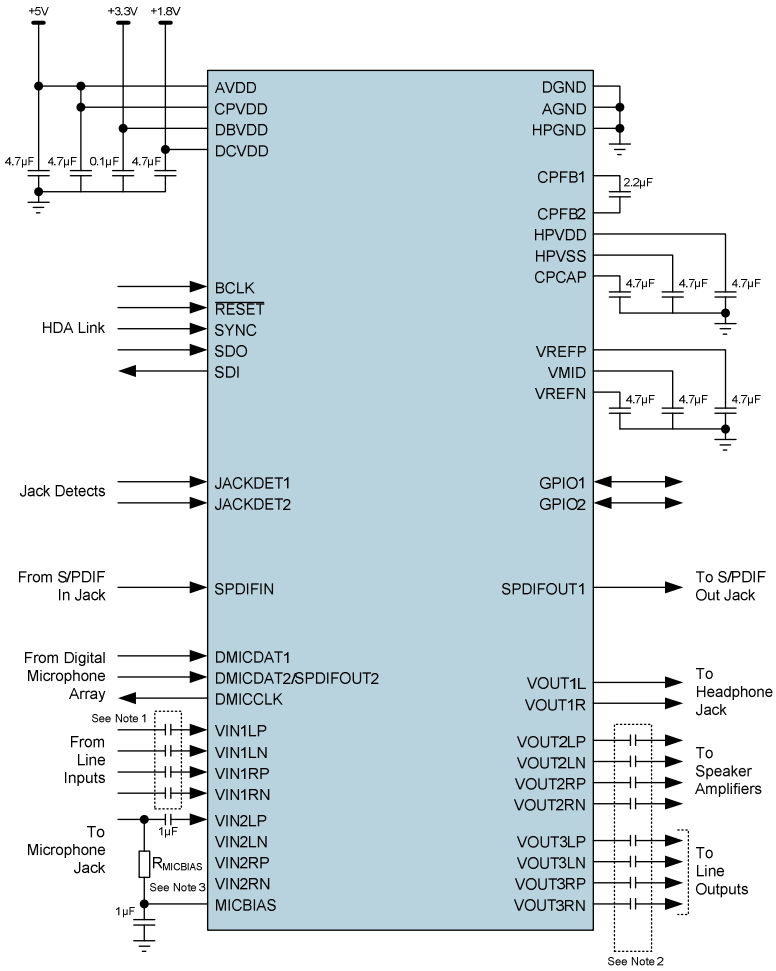


Figure 1 Recommended External Components

Notes:

1. AC-coupling capacitors for inputs may depend on circuitry used prior to WM8850. Typical values between 1µF and 10µF are common – consult any documentation for the exact circuit used
2. AC-coupling capacitors for outputs may depend in circuitry used after WM8850. Typical values between 1µF and 10µF are common – consult any documentation for the exact circuit used
3. A single-ended mono microphone input is shown, but other configurations are equally valid. The value of the microphone bias resistor will vary with the microphone used – a typical value is 2.2kΩ
4. The capacitor between CFB1 and CFB2 must be placed as close as possible to the device pins
5. The decoupling capacitor on CPCAP must also be placed as close as possible to the device pins
6. The decoupling capacitor on CPVDD is next important – it too should be placed as close as possible to the device pins
7. The decoupling capacitors on VREFP, VREFN and VMID are next important, in that order
8. All remaining decoupling capacitors should then be placed as close as possible

REQUIRED JACK DETECT COMPONENTS

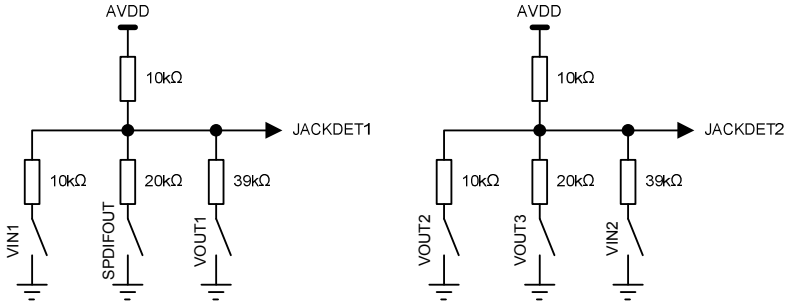
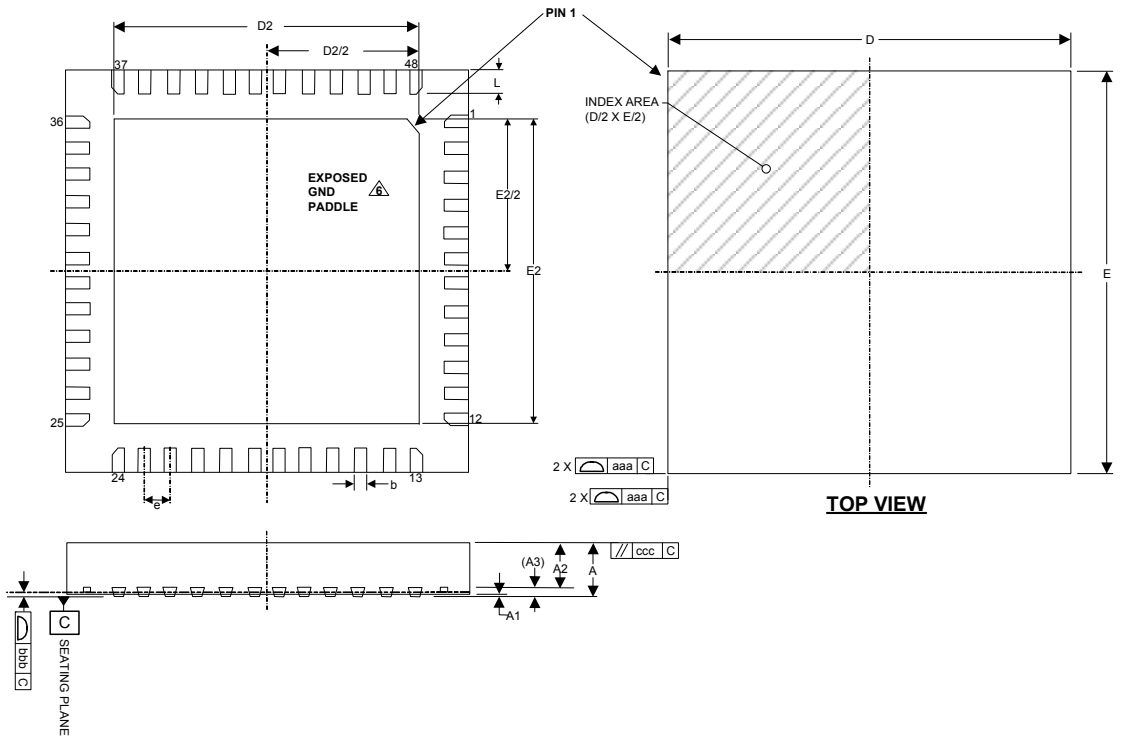


Figure 2 Required Jack Detect Components

The WM8850 supports jack detect on all analogue input and output ports, as well as on the S/PDIF output. This is implemented as per the High Definition Audio Specification Revision 1.0, section 7.4.2 and as such requires the resistor values shown in Figure 2 above. Note that, as per the High Definition Audio Specification, it is a requirement that the tolerance on these resistors is 1% or better.

PACKAGE DIMENSIONS

FL: 48 PIN QFN PLASTIC PACKAGE 7 x 7 x 0.75 mm BODY, 0.50 mm LEAD PITCH **DM079.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.7	0.75	0.8	
A1	0	0.035	0.05	
A2	-	0.55	0.57	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		7.00 BSC		
D2	5.55	5.65	5.75	
E		7.00 BSC		
E2	5.55	5.65	5.75	
e		0.5 BSC		
L	0.35	0.4	0.45	
Tolerances of Form and Position				
aaa	0.10			
bbb	0.08			
ccc	0.10			
REF	JEDEC, MO-220			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION.

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