



# WM8959

## Mobile Multimedia DAC with Dual-Mode Class AB/D Speaker Driver

### DESCRIPTION

The WM8959 is an ultra-low power hi-fi DAC designed for multimedia handsets.

A powerful 1W speaker driver can operate in class D or AB modes, providing total flexibility to the system designer. Low leakage, high PSRR and pop/click suppression enable direct battery connection for the speaker supply.

A flexible input configuration supports two microphone inputs (single-ended or differential), a stereo line input, and a mono differential line input.

Four headphone drivers support fully differential headset drive, providing excellent crosstalk performance and bass response, maximising stereo effects, and allowing the removal of large and expensive headphone capacitors. The headphone outputs can also be configured to drive an ear speaker. A fully differential path to these outputs direct from the input pins is available to maximise signal quality and minimise power consumption.

Stereo 24-bit sigma-delta DACs provide hi-fi quality audio playback, with a flexible digital audio interface supporting most commonly-used clocking schemes. An integrated low power PLL provides additional flexibility.

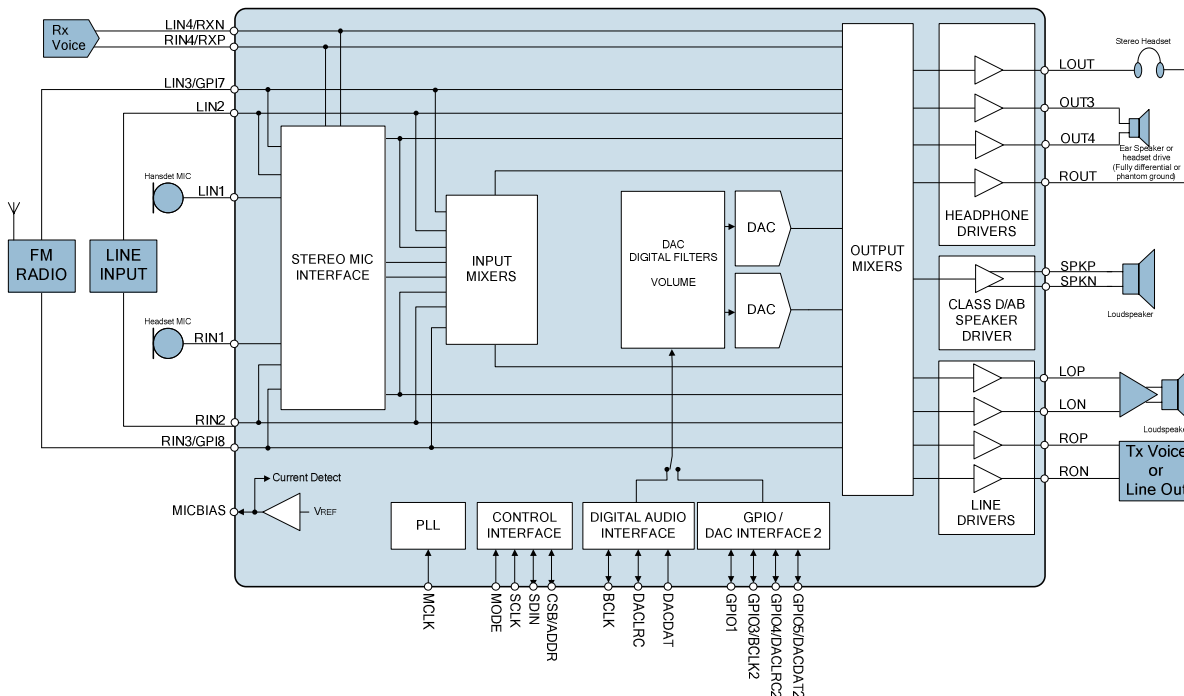
The WM8959 is supplied in very small and thin 42-ball WCSP package, ideal for portable systems.

### FEATURES

- DAC SNR 99dB ('A' weighted), THD -84dB at 48kHz, 3.3V
- Stereo microphone interface
- 1W Speaker driver
  - 1W into 8Ω BTL speaker at <0.1% THD
  - 80dB PSRR @ 217Hz
  - <1uA leakage with direct battery connection
  - Software-selectable class D or AB mode
  - Filterless connection supported
- Headphone / ear speaker drivers
  - 40mW output power into 16Ω at 3.3V
  - Fully differential and capless modes supported
  - Low noise, lower power received voice path
- Stereo or Mono differential line output
- Pop/Click suppression
- Powerful GPIO functions
- Ultra-low power consumption
  - 8.3mW analogue voice call
  - 13.7mW DAC playback to headphones
- On-chip PLL provides flexible clocking scheme
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48kHz
- 42-ball WCSP package (3.226x3.44x0.7mm, 0.5mm pitch)

### APPLICATIONS

- Multimedia phones
- GPS



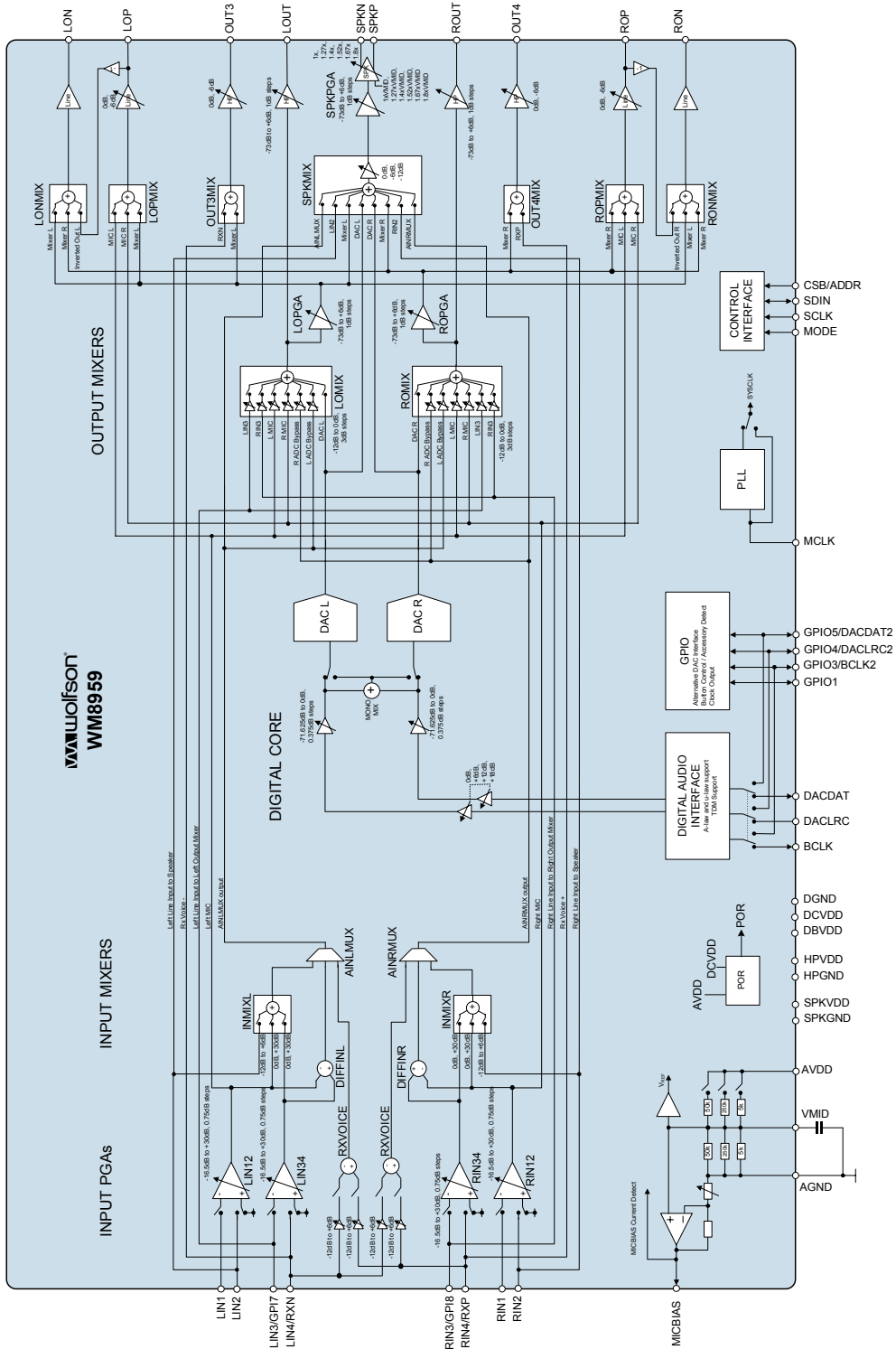
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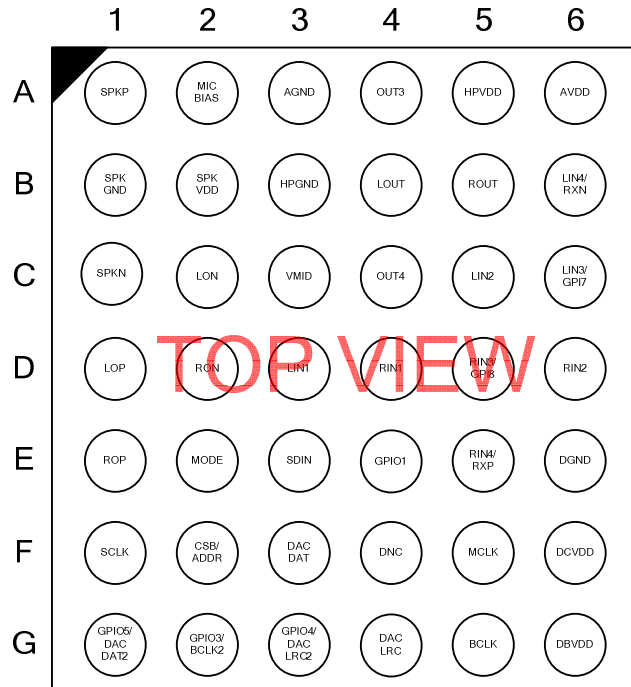
BLOCK DIAGRAM



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## PIN CONFIGURATION



## ORDERING INFORMATION

| ORDER CODE   | TEMPERATURE RANGE | PACKAGE                                  | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|--------------|-------------------|--|----------------------------|----------------------------|
| WM8959ECS/RV | -40°C to +85°C    | 42-ball WCSP<br>(Pb-free, Tape and reel) | MSL3                       | 260°C                      |

**Note:**

Reel quantity = 3500

**PIN DESCRIPTION**

| PIN NO | NAME             | TYPE                              | DESCRIPTION  |
|--------|------------------|-----------------------------------|--|
| A2     | MICBIAS          | Analogue Output                   | Microphone bias  |
| D3     | LIN1             | Analogue Input                    | Left channel single-ended MIC input /<br>Left channel negative differential MIC input  |
| C5     | LIN2             | Analogue Input                    | Left channel line input /<br>Left channel positive differential MIC input  |
| C6     | LIN3 /<br>GPI7   | Analogue Input /<br>Digital Input | Left channel line input /<br>Left channel negative differential MIC input /<br>Accessory or button detect input pin          |
| B6     | LIN4 /<br>RXN    | Analogue Input                    | Left channel line input /<br>Left channel positive differential MIC input /<br>Mono differential negative input (Rx voice -) |
| D4     | RIN1             | Analogue Input                    | Right channel single-ended MIC input /<br>Right channel negative differential MIC input                                      |
| D6     | RIN2             | Analogue Input                    | Right channel line input /<br>Right channel positive differential MIC input  |
| D5     | RIN3 /<br>GPI8   | Analogue Input /<br>Digital Input | Right channel line input /<br>Right channel negative differential MIC input /<br>Accessory or button detect input pin        |
| E5     | RIN4 /<br>RXP    | Analogue Input                    | Left channel line input /<br>Left channel positive differential MIC input /<br>Mono differential positive input (Rx voice +) |
| F6     | DCVDD            | Supply                            | Digital core supply  |
| E6     | DGND             | Supply                            | Digital ground (Return path for both DCVDD and DBVDD)  |
| G6     | DBVDD            | Supply                            | Digital buffer (I/O) supply  |
| A6     | AVDD             | Supply                            | Analogue supply  |
| A3     | AGND             | Supply                            | Analogue ground (Return path for AVDD)   |
| A5     | HPVDD            | Supply                            | Headphone supply   |
| B3     | HPGND            | Supply                            | Headphone ground (Return path for HPVDD)   |
| B2     | SPKVDD           | Supply                            | Supply for speaker driver  |
| B1     | SPKGND           | Supply                            | Ground for speaker driver (Return path from SPKVDD)  |
| F5     | MCLK             | Digital Input                     | Master clock   |
| G5     | BCLK             | Digital Input / Output            | Audio interface bit clock  |
| G4     | DACLRRC          | Digital Input / Output            | Audio interface DAC left / right clock   |
| F3     | DACDAT           | Digital Input                     | DAC digital audio data   |
| E4     | GPIO1            | Digital Input / Output            | GPIO1 pin  |
| E2     | MODE             | Digital Input                     | Selects 2-wire or 3/4 -wire control  |
| F2     | CSB / ADDR       | Digital Input                     | 3/4 -wire chip select or 2-wire address select   |
| F1     | SCLK             | Digital Input                     | Control interface clock input  |
| E3     | SDIN             | Digital Input / Output            | Control interface data input / 2-wire acknowledge output   |
| A1     | SPKP             | Analogue Output                   | Speaker positive output  |
| C1     | SPKN             | Analogue Output                   | Speaker negative output  |
| B4     | LOUT             | Analogue Output                   | Left headphone output  |
| B5     | ROUT             | Analogue Output                   | Right headphone output   |
| A4     | OUT3             | Analogue Output                   | Inverted left headphone output / Mono inverted output  |
| C4     | OUT4             | Analogue Output                   | Inverted right headphone output / Mono non-inverted output   |
| C2     | LON              | Analogue Output                   | Negative left line output / Positive right line output   |
| D1     | LOP              | Analogue Output                   | Positive left line output  |
| D2     | RON              | Analogue Output                   | Negative right line output / Positive left line output   |
| E1     | ROP              | Analogue Output                   | Positive right line output   |
| C3     | VMID             | Analogue Output                   | Midrail voltage decoupling capacitor   |
| G2     | GPIO3 /<br>BCLK2 | Digital Input / Output            | Alternative BCLK / GPIO pin  |

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| <b>PIN NO</b> | <b>NAME</b>        | <b>TYPE</b>            | <b>DESCRIPTION</b>            |
|---------------|--------------------|------------------------|-------------------------------|
| G3            | GPIO4 /<br>DACLRC2 | Digital Input / Output | Alternative DACLRC / GPIO pin |
| G1            | GPIO5 /<br>DACDAT2 | Digital Input / Output | Alternative DACDAT / GPIO pin |
| F4            | DNC                |                        | No Connection                 |

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION                                   | MIN        | MAX         |
|---|------------|-------------|
| Supply voltages (excluding SPKVDD)          | -0.3V      | +4.5V       |
| SPKVDD                                      | -0.3V      | +7V         |
| Voltage range digital inputs                | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs               | AGND -0.3V | AVDD +0.3V  |
| Operating temperature range, T <sub>A</sub> | -40°C      | +85°C       |
| Junction temperature, T <sub>JMAX</sub>     | -40°C      | +150°C      |
| Storage temperature after soldering         | -65°C      | +150°C      |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER                     | SYMBOL                    | MIN  | TYP | MAX | UNIT |
|-------------------------------|---------------------------|------|-----|-----|------|
| Digital supply range (Core)   | DCVDD                     | 1.71 |     | 3.6 | V    |
| Digital supply range (Buffer) | DBVDD                     | 1.71 |     | 3.6 | V    |
| Analogue supplies range       | AVDD, HPVDD               | 2.7  |     | 3.6 | V    |
| Speaker supply range          | SPKVDD                    | 2.7  |     | 5.5 | V    |
| Ground                        | DGND, AGND, HPGND, SPKGND |      | 0   |     | V    |

### Notes:

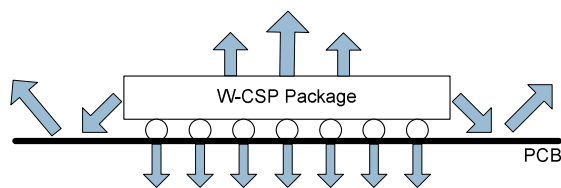
- Analogue, digital and speaker grounds must always be within 0.3V of each other.
- All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
- DCVDD must be less than or equal to AVDD.
- DCVDD must be less than or equal to DBVDD.
- AVDD must be less than or equal to SPKVDD.
- SPKVDD must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is  $AVDD \cdot (DCGAIN + ACGAIN) / 2$ .
- HPVDD must be equal to AVDD

## THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8959 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).



**Figure 1 Heat Transfer Paths**

The temperature rise  $T_R$  is given by  $T_R = P_D * \Theta_{JA}$

- $P_D$  is the power dissipated in the device.
- $\Theta_{JA}$  is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.  $\Theta_{JA}$  is determined with reference to JEDEC standard JESD51-9.

The junction temperature  $T_J$  is given by  $T_J = T_A + T_R$ , where  $T_A$  is the ambient temperature.

| PARAMETER                      | SYMBOL        | MIN | TYP | MAX | UNIT |
|--------------------------------|---------------|-----|-----|-----|------|
| Operating temperature range    | $T_A$         | -40 |     | 85  | °C   |
| Operating junction temperature | $T_J$         | -40 |     | 100 | °C   |
| Thermal Resistance             | $\Theta_{JA}$ |     | 43  |     | °C/W |



### SPEAKER POWER DE-RATING CURVE

The speaker driver has been designed to drive a maximum of 1W into 8Ω with a 5V supply. However, thermal restrictions defined by the W-CSP package  $\Theta_{JA}$  limit the amount of power that can be safely dissipated in the device without exceeding the maximum operating junction temperature. Power dissipated in the device correlates directly with speaker efficiency, hence there are separate de-rating curves for class D and class AB operation.

Under no circumstances should the recommended maximum powers be exceeded.

### CLASS D DE-RATING CURVES

The de-rating curves shown in Figure 2 are based on a full scale sinusoidal input.

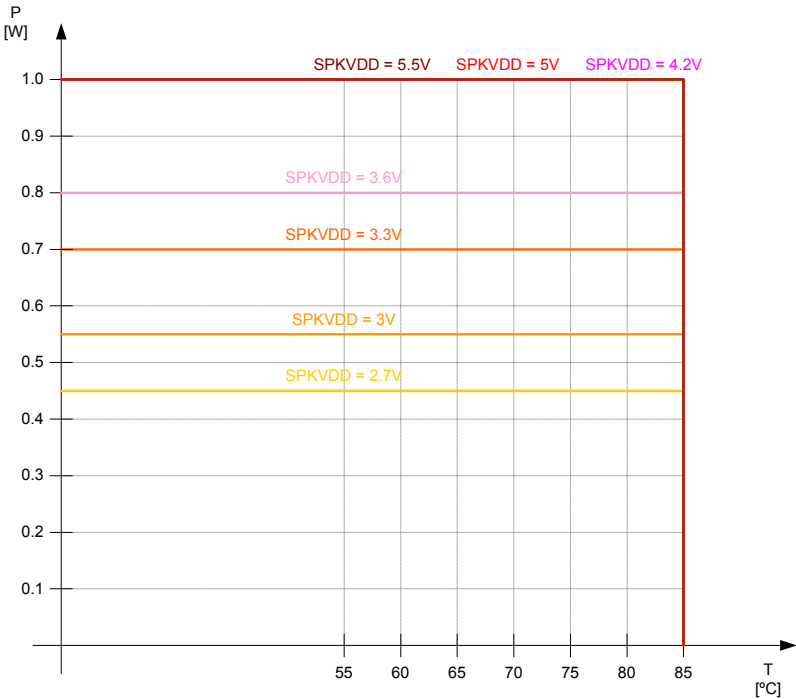
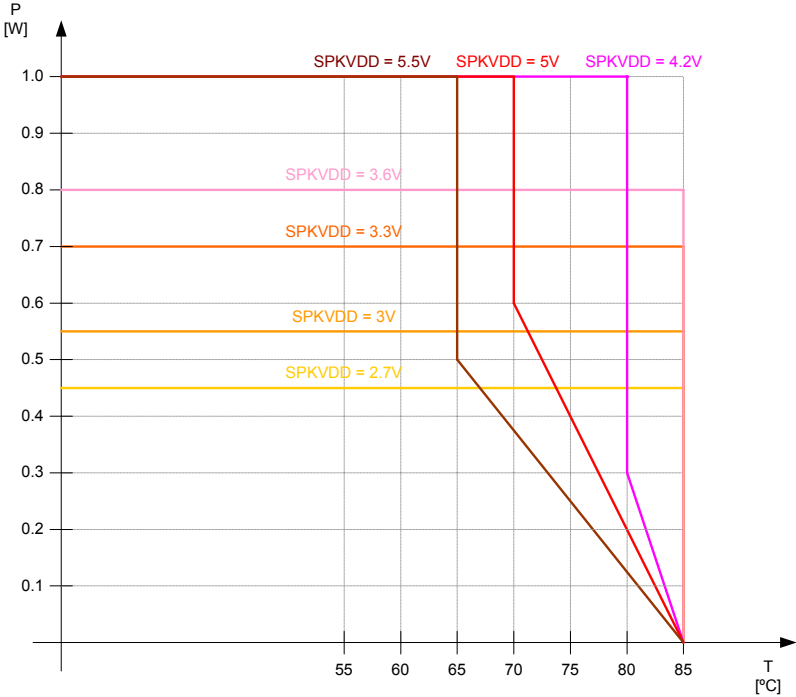


Figure 2 Class D Speaker Power De-Rating Curve

**CLASS AB DE-RATING CURVE**

The de-rating curves shown in Figure 3 are based on a full scale sinusoidal input



**Figure 3 Class AB Speaker Power De-Rating Curve**

## ELECTRICAL CHARACTERISTICS

### Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER  | TEST CONDITIONS   | MIN   | TYP | MAX | UNIT     |             |
|--|---|---|-----|-----|----------|-------------|
| <b>Analogue Input Pin Maximum Signal Levels (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)</b> |   |   |     |     |          |             |
| A1   | Maximum Full-Scale PGA Input Signal Level   | Single-ended PGA input on LIN1, LIN3, RIN1 or RIN3, output to INMIXL or INMIXR                            |     |     | 1.0<br>0 | Vrms<br>dBV |
|  | Note 1: This changes in proportion to AVDD (AVDD/3.3).  | Differential PGA input on LIN1/LIN2, LIN3/LIN4, RIN1/RIN2 or RIN3/RIN4, output to INMIXL or INMIXR        |     |     | 1.0<br>0 | Vrms<br>dBV |
|  | Note 2: When mixing input PGA outputs and line inputs the total signal must not exceed 1Vrms (0dBV).<br><br>Note 3: A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input. | Differential input to two single-ended PGA inputs on LIN1/LIN3 or RIN1/RIN3, output to DIFFINL or DIFFINR |     |     | 1.0<br>0 | Vrms<br>dBV |
| A2   | Maximum Full-Scale Line Input Signal Level  | Line input on LIN2, LIN4, RIN2 or RIN4 to INMIXL or INMIXR  |     |     | 1.0<br>0 | Vrms<br>dBV |
|  | Note 1: This changes in proportion to AVDD (AVDD/3.3).  | Line input on LIN2 or RIN2 to SPKMIX  |     |     | 1.0<br>0 | Vrms<br>dBV |
|  | Note 2: When mixing line inputs, input PGA outputs and DAC outputs the total signal must not exceed 1Vrms (0dBV).   | Line input on LIN3 or RIN3 to LOMIX or ROMIX  |     |     | 1.0<br>0 | Vrms<br>dBV |
|  | Note 3: A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input.   | Differential mono line input on RXP/RXN to RXVOICE  |     |     | 1.0<br>0 | Vrms<br>dBV |
|  |   | Differential mono line input on RXP/RXN to differential output on OUT3/OUT4                               |     |     | 1.0<br>0 | Vrms<br>dBV |

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## Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz,  
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER   | TEST CONDITIONS   |  | MIN | TYP | MAX | UNIT |    |
|---|---|--|-----|-----|-----|------|----|
| <b>Analogue Input Pin Impedances (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)</b> |   |  |     |     |     |      |    |
| B1  | PGA Input Resistance<br><br>Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin  | LIN1, LIN3, RIN1 or RIN3<br>(PGA Gain = -16.5dB)                 |     |     | 57  |      | kΩ |
|   |   | LIN1, LIN3, RIN1 or RIN3<br>(PGA Gain = 0dB)                     |     |     | 33  |      | kΩ |
|   |   | LIN1, LIN3, RIN1 or RIN3<br>(PGA Gain = +30dB)                   |     |     | 2   |      | kΩ |
|   |   | LIN2, LIN4, RIN2 or RIN4<br>(Constant for all gains)             |     |     | 65  |      | kΩ |
| B2  | Line Input Resistance<br><br>Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin | LIN2 or RIN2 to INMIXL or INMIXR (-12dB)                         |     |     | 60  |      | kΩ |
|   |   | LIN2 or RIN2 to INMIXL or INMIXR (0dB)                           |     |     | 15  |      | kΩ |
|   |   | LIN2 or RIN2 to INMIXL or INMIXR (+6dB)                          |     |     | 7.5 |      | kΩ |
|   |   | LIN2 or RIN2 to SPKMIX<br>(SPKATTN = 0dB)                        |     |     | 20  |      | kΩ |
|   |   | LIN2 or RIN2 to SPKMIX<br>(SPKATTN = -12dB)                      |     |     | 20  |      | kΩ |
|   |   | LIN3 or RIN3 to LOMIX or ROMIX (0dB)                             |     |     | 20  |      | kΩ |
|   |   | LIN3 or RIN3 to LOMIX or ROMIX (-21dB)                           |     |     | 224 |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX or AINRMUX<br>(Gain = +6dB)   |     |     | 7.5 |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX or AINRMUX<br>(Gain = 0dB)    |     |     | 15  |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX or AINRMUX<br>(Gain = -12dB)  |     |     | 45  |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX and AINRMUX<br>(Gain = +6dB)  |     |     | 3.8 |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX and AINRMUX<br>(Gain = 0dB)   |     |     | 7.5 |      | kΩ |
|   |   | RXP and RXN via RXVOICE to AINLMUX and AINRMUX<br>(Gain = -12dB) |     |     | 25  |      | kΩ |
|   |   | LIN4 to OUT3 or RIN4 to OUT4 (Gain = -6dB)                       |     |     | 20  |      | kΩ |
|   |   | LIN4 to OUT3 or RIN4 to OUT4 (Gain = 0dB)                        |     |     | 20  |      | kΩ |
| B3  | Input Capacitance   | All analogue input pins  |     | 10  |     | pF   |    |

**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz,  
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER  |   | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT |
|--|---|--|-----|-------|-----|------|
| <b>Input Programmable Gain Amplifiers (PGAs) LIN12, LIN34, RIN12 and RIN34</b>       |   |  |     |       |     |      |
| C1   | Minimum Programmable Gain                   |  |     | -16.5 |     | dB   |
| C2   | Maximum Programmable Gain                   |  |     | 30    |     | dB   |
| C3   | Programmable Gain Step Size                 | Guaranteed monotonic   |     | 1.5   |     | dB   |
| C4   | Mute Attenuation                            | Inputs disconnected  |     | 90    |     | dB   |
| C5   | Common Mode Rejection Ratio<br>(1kHz input) | Single PGA in differential mode, gain = +30dB                                      |     | 60    |     | dB   |
|  |   | Single PGA in differential mode, gain = 0dB  |     | 50    |     |      |
|  |   | Single PGA in differential mode, gain = -16.5dB                                    |     | 50    |     |      |
|  |   | Differential input to DIFFINL or DIFFINR via<br>LIN1/LIN3 or RIN1/RIN3, gain = 0dB |     | 45    |     |      |
| <b>Received Voice (RXP-RXN) Differential to Single-Ended Converter RXVOICE</b>       |   |  |     |       |     |      |
| C6   | Minimum Programmable Gain                   | AINLMODE = 01 or AINRMODE = 01   |     | -12   |     | dB   |
| C7   | Maximum Programmable Gain                   | AINLMODE = 01 or AINRMODE = 01   |     | +6    |     | dB   |
| C8   | Programmable Gain Step Size                 | AINLMODE = 01 or AINRMODE = 01   |     | 3     |     | dB   |
| C9   | Mute Attenuation                            | AINLMODE = 01 or AINRMODE = 01   |     | 95    |     | dB   |
| <b>PGA Output Differential to Single Ended Converters DIFFINL and DIFFINR</b>        |   |  |     |       |     |      |
| C10  | Fixed Gain                                  | AINLMODE = 10 or AINRMODE = 10   |     | 0     |     | dB   |
| C11  | Mute Attenuation                            | AINLMODE = 10 or AINRMODE = 10   |     | 95    |     | dB   |
| <b>Input Mixers INMIXL and INMIXR</b>  |   |  |     |       |     |      |
| C12  | Minimum Programmable Gain                   | PGA Outputs to INMIXL and INMIXR   |     | 0     |     | dB   |
| C13  | Maximum Programmable Gain                   | PGA Outputs to INMIXL and INMIXR   |     | +30   |     | dB   |
| C14  | Programmable Gain Step Size                 | PGA Outputs to INMIXL and INMIXR   |     | 30    |     | dB   |
| C15  | Minimum Programmable Gain                   | Line Inputs and Record path to INMIXL and INMIXR                                   |     | -12   |     | dB   |
| C16  | Maximum Programmable Gain                   | Line Inputs and Record path to INMIXL and INMIXR                                   |     | +6    |     | dB   |
| C17  | Programmable Gain Step Size                 | Line Inputs and Record path to INMIXL and INMIXR                                   |     | 3     |     | dB   |
| C18  | Mute attenuation                            |  |     | 95    |     | dB   |
| <b>Output Programmable Gain Amplifiers (PGAs) SPKPGA, LOPGA, ROPGA, LOU and ROUT</b> |   |  |     |       |     |      |
| C19  | Minimum Programmable Gain                   |  |     | -73   |     | dB   |
| C20  | Maximum Programmable Gain                   |  |     | +6    |     | dB   |
| C21  | Programmable Gain Step Size                 | Guaranteed monotonic   |     | 1     |     | dB   |
| C22  | Mute attenuation                            | LOU and ROUT   |     | 80    |     | dB   |
|  |   | SPKPGA, LOPGA and ROPGA  |     | 70    |     | dB   |
| <b>Output Programmable Gain Amplifiers (PGAs) OUT3, OUT4, LOP and ROP</b>            |   |  |     |       |     |      |
| C23  | Minimum Programmable Gain                   |  |     | -6    |     | dB   |
| C24  | Maximum Programmable Gain                   |  |     | 0     |     | dB   |
| C25  | Programmable Gain Step Size                 |  |     | 6     |     | dB   |
| C26  | Mute attenuation                            | OUT3 and OUT4  |     | 80    |     | dB   |
|  |   | LOP and ROP (also applies to LON and RON)  |     | 100   |     | dB   |
| <b>Speaker Attenuation (SPKATTN)</b>   |   |  |     |       |     |      |
| C27  | Minimum Programmable Gain                   |  |     | -12   |     | dB   |
| C28  | Maximum Programmable Gain                   |  |     | 0     |     | dB   |
| C29  | Programmable Gain Step Size                 |  |     | 6     |     | dB   |
| C30  | Mute attenuation                            |  |     | 80    |     | dB   |

## WM8959

Pre-Production

## Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz,  
 PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| DAC Output Path (Line Outputs 10kΩ / 50pF Load, Headphone Outputs 16Ω Load, Speaker Output 8Ω BTL Load) |                              |   |   |                                  |     |    |    |    |    |    |
|---|------------------------------|---|---|----------------------------------|-----|----|----|----|----|----|
| E1  | SNR (A-weighted)             | DAC to single-ended line out, 0dBFS input, AVDD = 3.3V        |   | 99                               |     | dB |    |    |    |    |
|   | THD                          |   |   | -86                              |     | dB |    |    |    |    |
|   | THD+N                        |   |   | -84                              |     | dB |    |    |    |    |
|   | Crosstalk (L/R)              |   |   | -100                             |     | dB |    |    |    |    |
|   | AVDD PSRR (217Hz)            | 45  |   |                                  | dB  |    |    |    |    |    |
|   | SNR (A-weighted)             | DAC to single-ended line out, 0dBFS input, AVDD = 2.7V        |   | 97                               |     | dB |    |    |    |    |
|   | THD                          |   |   | -89                              |     | dB |    |    |    |    |
| THD+N   | -87                          |   |   | dB                               |     |    |    |    |    |    |
| E2  | SNR (A-weighted)             | DAC to differential line out, 0dBFS input, AVDD = 3.3V        |   | 99                               |     | dB |    |    |    |    |
|   | THD                          |   |   | -86                              |     | dB |    |    |    |    |
|   | THD+N                        |   |   | -84                              |     | dB |    |    |    |    |
|   | Crosstalk (L/R)              |   |   | -100                             |     | dB |    |    |    |    |
|   | AVDD PSRR (217Hz)            | 60  |   |                                  | dB  |    |    |    |    |    |
|   | DC Offset at Load            | 5   |   |                                  | mV  |    |    |    |    |    |
|   | SNR (A-weighted)             | DAC to differential line out, 0dBFS input, AVDD = 2.7V        |   | 97                               |     | dB |    |    |    |    |
| THD   | -90                          |   |   | dB                               |     |    |    |    |    |    |
| THD+N   | -88                          |   |   | dB                               |     |    |    |    |    |    |
| E3  | Minimum Line Out Resistance  | LOP, LON, ROP, RON  | 2 |                                  |     | kΩ |    |    |    |    |
| E4  | Maximum Line Out Capacitance | LOP, LON, ROP, RON  |   | 10                               |     | nF |    |    |    |    |
| E5  | SNR (A-weighted)             | DAC to LOOUT or ROOUT, R <sub>L</sub> =32Ω, AVDD=HPVDD= 3.3V  |   | 32Ω AC-Coupled Headphone Outputs |     |    | 99 |    | dB |    |
|   | THD (P <sub>O</sub> =20mW)   |   |   | -81                              |     | dB |    |    |    |    |
|   | THD+N (P <sub>O</sub> =20mW) |   |   | -79                              |     | dB |    |    |    |    |
|   | THD (P <sub>O</sub> =5mW)    |   |   | -77                              |     | dB |    |    |    |    |
|   | THD+N (P <sub>O</sub> =5mW)  |   |   | -75                              |     | dB |    |    |    |    |
|   | Crosstalk (L/R)              |   |   | -100                             |     | dB |    |    |    |    |
|   | AVDD PSRR (217Hz)            |   |   | 45                               |     | dB |    |    |    |    |
|   | HPVDD PSRR (217Hz)           | 85  |   |                                  | dB  |    |    |    |    |    |
|   | SNR (A-weighted)             | DAC to LOOUT or ROOUT, R <sub>L</sub> =32Ω, AVDD=HPVDD= 2.7V  |   | 97                               |     | dB |    |    |    |    |
|   | THD (P <sub>O</sub> =5mW)    |   |   | -76                              |     | dB |    |    |    |    |
| THD+N (P <sub>O</sub> =5mW)   | -74                          |   |   | dB                               |     |    |    |    |    |    |
| E6  | SNR (A-weighted)             | DAC to LOOUT or ROOUT, R <sub>L</sub> =16Ω, AVDD=HPVDD= 3.3V  |   | 16Ω AC-Coupled Headphone Outputs |     |    | 90 | 99 |    | dB |
|   | THD (P <sub>O</sub> =20mW)   |   |   | -77                              | -72 |    | dB |    |    |    |
|   | THD+N (P <sub>O</sub> =20mW) |   |   | -75                              | -70 |    | dB |    |    |    |
|   | THD (P <sub>O</sub> =5mW)    |   |   | -73                              |     |    | dB |    |    |    |
|   | THD+N (P <sub>O</sub> =5mW)  |   |   | -71                              |     |    | dB |    |    |    |
|   | Crosstalk (L/R)              |   |   | -100                             |     |    | dB |    |    |    |
|   | AVDD PSRR (217Hz)            |   |   | 45                               |     |    | dB |    |    |    |
|   | HPVDD PSRR (217Hz)           | 85  |   |                                  |     | dB |    |    |    |    |
|   | SNR (A-weighted)             | DAC to LOOUT, or ROOUT, R <sub>L</sub> =16Ω, AVDD=HPVDD= 2.7V |   | 97                               |     |    | dB |    |    |    |
|   | THD (P <sub>O</sub> =20mW)   |   |   | -74                              |     |    | dB |    |    |    |
|   | THD+N (P <sub>O</sub> =20mW) |   |   | -72                              |     |    | dB |    |    |    |
|   | THD (P <sub>O</sub> =5mW)    |   |   | -72                              |     |    | dB |    |    |    |
|   | THD+N (P <sub>O</sub> =5mW)  |   |   | -70                              |     |    | dB |    |    |    |
| THD+N (P <sub>O</sub> =5mW)   | -70                          |   |   |                                  | dB  |    |    |    |    |    |

Pre-Production

**WM8959****Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz,  
 PGA gain = 0dB, 24-bit audio data unless otherwise stated.

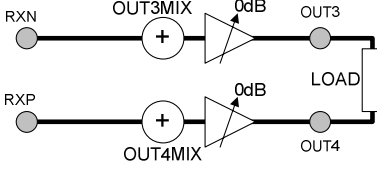
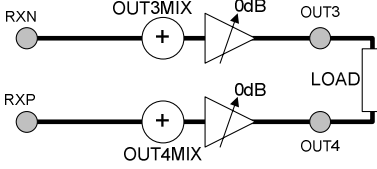
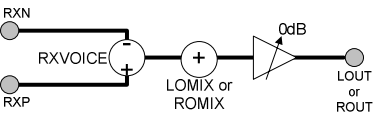
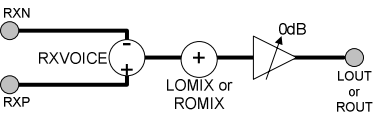
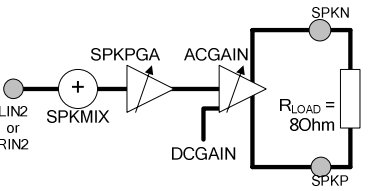
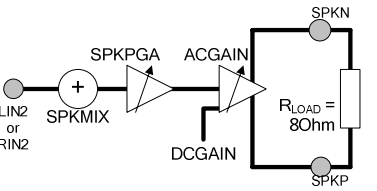
|                              |  |   |    |   |     |    |
|------------------------------|--|---|----|---|-----|----|
| E7                           | SNR (A-weighted)   | DAC to LOUT/OUT3 or ROUT/OUT4, R <sub>L</sub> =16Ω, AVDD=HPVDD=3.3V   |    | 99  |     | dB |
|                              | THD (P <sub>O</sub> =20mW)   |   |    | -71   |     | dB |
|                              | THD+N (P <sub>O</sub> =20mW)   |   |    | -69   |     | dB |
|                              | THD (P <sub>O</sub> =5mW)  |   |    | -67   |     | dB |
|                              | THD+N (P <sub>O</sub> =5mW)  |   |    | -65   |     | dB |
|                              | Crosstalk (L/R)  |   |    | -100  |     | dB |
|                              | AVDD PSRR (217Hz)  |   |    | 60  |     | dB |
|                              | HPVDD PSRR (217Hz)   | 85  |    |   | dB  |    |
|                              | DC Offset at Load  | 5   |    |   | mV  |    |
|                              | SNR (A-weighted)   | DAC to LOUT/OUT3 or ROUT/OUT4, R <sub>L</sub> =16Ω, AVDD=HPVDD=2.7V   |    | 98  |     | dB |
|                              | THD (P <sub>O</sub> =20mW)   |   |    | -70   |     | dB |
|                              | THD+N (P <sub>O</sub> =20mW)   |   |    | -68   |     | dB |
|                              | THD (P <sub>O</sub> =5mW)  |   |    | -66   |     | dB |
|                              | THD+N (P <sub>O</sub> =5mW)  |   |    | -64   |     | dB |
| E8                           |  |   | 99 |   | dB  |    |
| SNR (A-weighted)             | DAC to LOUT or ROUT Capless (OUT3 or 4 as pseudo GND), R <sub>L</sub> =16Ω, AVDD=HPVDD=3.3V  |   |    | -73   |     | dB |
| THD (P <sub>O</sub> =20mW)   |  | -71   |    |   | dB  |    |
| THD+N (P <sub>O</sub> =20mW) |  | -69   |    |   | dB  |    |
| THD (P <sub>O</sub> =5mW)    |  | -67   |    |   | dB  |    |
| THD+N (P <sub>O</sub> =5mW)  |  | -45   |    |   | dB  |    |
| Crosstalk (L/R)              |  | 45  |    |   | dB  |    |
| AVDD PSRR (217Hz)            |  | 85  |    |   | dB  |    |
| HPVDD PSRR (217Hz)           | 97   |   |    | dB  |     |    |
| SNR (A-weighted)             | DAC to LOUT, or ROUT Capless (OUT3 or 4 as pseudo GND), R <sub>L</sub> =16Ω, AVDD=HPVDD=2.7V | -70   |    |   | dB  |    |
| THD (P <sub>O</sub> =20mW)   |  | -68   |    |   | dB  |    |
| THD+N (P <sub>O</sub> =20mW) |  | -67   |    |   | dB  |    |
| THD (P <sub>O</sub> =5mW)    |  | -65   |    |   | dB  |    |
| THD+N (P <sub>O</sub> =5mW)  |  |   |    |   |     |    |
| E9                           |  |   |    | 15  |     | Ω  |
| Minimum Headphone Resistance |  | LOUT, ROUT, OUT3, OUT4  |    |   |     |    |
| E10                          |  |   | 1  |   | uA  |    |
| SPKVDD Leakage Current       | SPKVDD=5.0V,   |   |    |   |     |    |
| E11                          | SNR (A-weighted)   | DAC to Speaker Output (Direct) AVDD=3.3V, SPKVDD=5V, class D, P <sub>O</sub> controlled using DAC volume, ACGAIN=DCGA IN=1.52 |    | 93  |     | dB |
|                              | THD (P <sub>O</sub> =0.5W)   |   |    | -87   |     | dB |
|                              | THD+N (P <sub>O</sub> =0.5W)   |   |    | -85   |     | dB |
|                              | THD (P <sub>O</sub> =1.0W)   |   |    | -76   |     | dB |
|                              | THD+N (P <sub>O</sub> =1.0W)   |   |    | -74   |     | dB |
|                              | SPKVDD PSRR(217Hz)   |   |    | 75  |     | dB |
|                              | SNR (A-weighted)   |   |    | DAC to Speaker Output (Direct) AVDD=3.3V, SPKVDD=5V, class AB, P <sub>O</sub> controlled using DAC volume | 97  |    |
|                              | THD (P <sub>O</sub> =0.5W)   | -78   |    |   | -70 | dB |
|                              | THD+N (P <sub>O</sub> =0.5W)   | -76   |    |   | -68 | dB |
|                              | THD (P <sub>O</sub> =1.0W)   | -76   |    |   | -66 | dB |
|                              | THD+N (P <sub>O</sub> =1.0W)   | -74   |    |   | -64 | dB |
|                              | SPKVDD PSRR(217Hz)   | 75  |    |   |     | dB |
|                              | DC Offset at Load  | 5   |    |   |     | mV |

## WM8959

Pre-Production

## Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz,  
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| Bypass Path Performance (Line Outputs 10kΩ / 50pF load, Headphone Outputs 16Ω load, Speaker Output 8Ω BTL load) |                              |  |  |     |     |    |
|---|------------------------------|--|--|-----|-----|----|
| F1  | SNR (A-weighted)             | Differential Input on RXP/RXN to Differential Output on OUT3/OUT4, AVDD=HPVDD=3.3V |    | 110 |     | dB |
|   | THD (P <sub>O</sub> =20mW)   |  |  | -72 |     | dB |
|   | THD+N (P <sub>O</sub> =20mW) |  |  | -70 |     | dB |
|   | THD (P <sub>O</sub> =5mW)    |  |  | -68 |     | dB |
|   | THD+N (P <sub>O</sub> =5mW)  |  |  | -66 |     | dB |
|   | AVDD PSRR (217Hz)            |  |  | 80  |     | dB |
|   | HPVDD PSRR (217Hz)           |  |  | 90  |     | dB |
|   | DC Offset at Load            |  |  | 5   |     | mV |
|   | SNR (A-weighted)             | Differential Input on RXP/RXN to Differential Output on OUT3/OUT4, AVDD=HPVDD=2.7V |    | 108 |     | dB |
|   | THD (P <sub>O</sub> =20mW)   |  |  | -70 |     | dB |
|   | THD+N (P <sub>O</sub> =20mW) |  |  | -68 |     | dB |
|   | THD (P <sub>O</sub> =5mW)    |  |  | -67 |     | dB |
|   | THD+N (P <sub>O</sub> =5mW)  |  |  | -65 |     | dB |
|   | DC Offset at Load            |  |  | 5   |     | mV |
| F2  | SNR (A-weighted)             | RXVOICE via LOMIX or ROMIX to Headphone Outputs, AVDD=HPVDD=3.3V                   |  | 100 |     | dB |
|   | THD (P <sub>O</sub> =20mW)   |  |  | -77 |     | dB |
|   | THD+N (P <sub>O</sub> =20mW) |  |  | -75 |     | dB |
|   | THD (P <sub>O</sub> =5mW)    |  |  | -73 |     | dB |
|   | THD+N (P <sub>O</sub> =5mW)  |  |  | -71 |     | dB |
|   | AVDD PSRR (217Hz)            |  |  | 45  |     | dB |
|   | HPVDD PSRR (217Hz)           |  |  | 85  |     | dB |
|   | SNR (A-weighted)             | RXVOICE via LOMIX or ROMIX to Headphone Outputs, AVDD=HPVDD=2.7V                   |  | 98  |     | dB |
|   | THD (P <sub>O</sub> =20mW)   |  |  | -74 |     | dB |
|   | THD+N (P <sub>O</sub> =20mW) |  |  | -72 |     | dB |
|   | THD (P <sub>O</sub> =5mW)    |  |  | -72 |     | dB |
|   | THD+N (P <sub>O</sub> =5mW)  |  |  | -70 |     | dB |
|   | AVDD PSRR (217Hz)            |  |  | 45  |     | dB |
|   | HPVDD PSRR (217Hz)           |  |  | 80  |     | dB |
| F3  | SNR (A-weighted)             | Line Input to SPKMIX, AVDD=3.3V, SPKVDD=5V, ACGAIN=DCGAIN=1.52, Class D Mode       |  | 93  |     | dB |
|   | THD (P <sub>O</sub> =0.5W)   |  |  | -87 |     | dB |
|   | THD+N (P <sub>O</sub> =0.5W) |  |  | -85 |     | dB |
|   | THD (P <sub>O</sub> =1.0W)   |  |  | -81 |     | dB |
|   | THD+N (P <sub>O</sub> =1.0W) |  |  | -79 |     | dB |
|   | AVDD PSRR (217Hz)            |  |  | 45  |     | dB |
|   | SPKVDD PSRR(217Hz)           |  |  | 80  |     | dB |
|   | SNR (A-weighted)             | Line Input to SPKMIX, AVDD=3.3V, SPKVDD=5V, Class AB Mode                          |  | 91  | 101 | dB |
|   | THD (P <sub>O</sub> =0.5W)   |  |  | -78 | -70 | dB |
|   | THD+N (P <sub>O</sub> =0.5W) |  |  | -76 | -68 | dB |
|   | THD (P <sub>O</sub> =1.0W)   |  |  | -76 | -66 | dB |
|   | THD+N (P <sub>O</sub> =1.0W) |  |  | -74 | -64 | dB |
|   | AVDD PSRR (217Hz)            |  |  | 45  |     | dB |
|   | SPKVDD PSRR(217Hz)           |  |  | 80  |     | dB |
| DC Offset at Load   | 5                            |  | mV   |     |     |    |



**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

|                              |  |  |     |  |     |     |     |     |     |
|------------------------------|--|--|-----|--|-----|-----|-----|-----|-----|
| F4                           | SNR (A-weighted)   | Input PGA to Differential Line Out, AVDD=3.3V                                      |     | 90   | 101 |     | dB  |     |     |
|                              | THD (0dB output)   |  |     |  |     | -99 | -90 | dB  |     |
|                              | THD+N (0dB output)   |  |     |  |     | -97 | -88 | dB  |     |
|                              | AVDD PSRR (217Hz)  |  |     |  |     | 45  |     | dB  |     |
|                              | DC Offset at Load  |  |     |  |     | 5   |     | mV  |     |
|                              | SNR (A-weighted)   | Input PGA to Differential Line Out, AVDD=2.7V                                      |     |  | 100 |     | dB  |     |     |
|                              | THD (0dB output)   |  |     |  |     |     | -95 | dB  |     |
|                              | THD+N (0dB output)   |  |     |  |     |     | -93 | dB  |     |
|                              | SNR (A-weighted)   |  |     | Input PGA via LOMIX or ROMIX to LOUT or ROUT, R <sub>L</sub> =16Ω, AVDD=HPVDD=3.3V |     | 92  | 102 |     | dB  |
|                              | THD (P <sub>O</sub> =20mW)   |  |     |  |     |     |     | -77 | -72 |
| THD+N (P <sub>O</sub> =20mW) |  |  | -75 |  |     | -70 | dB  |     |     |
| THD (P <sub>O</sub> =5mW)    |  |  | -73 |  |     |     | dB  |     |     |
| THD+N (P <sub>O</sub> =5mW)  |  |  | -71 |  |     |     | dB  |     |     |
| AVDD PSRR (217Hz)            |  |  | 45  |  |     |     | dB  |     |     |
| HPVDD PSRR (217Hz)           |  |  | 85  |  |     |     | dB  |     |     |
| Crosstalk (L/R)              |  |  | -95 |  |     |     | dB  |     |     |
| SNR (A-weighted)             | Input PGA via LOMIX or ROMIX to LOUT or ROUT, R <sub>L</sub> =16Ω, AVDD=HPVDD=2.7V |  | 100 |  |     |     | dB  |     |     |
| THD (P <sub>O</sub> =20mW)   |  |  |     |  |     |     | -74 | dB  |     |
| THD+N (P <sub>O</sub> =20mW) |  |  |     |  | -72 | dB  |     |     |     |
| THD (P <sub>O</sub> =5mW)    |  |  |     |  | -72 | dB  |     |     |     |
| THD+N (P <sub>O</sub> =5mW)  |  |  |     |  | -70 | dB  |     |     |     |
| F6                           | SNR (A-weighted)   | Line Input to Headphones via LOMIX and ROMIX, R <sub>L</sub> =16Ω, AVDD=HPVDD=3.3V |     |  | 104 |     | dB  |     |     |
|                              | THD (P <sub>O</sub> =20mW)   |  |     |  |     | -77 |     | dB  |     |
|                              | THD+N (P <sub>O</sub> =20mW)   |  |     |  |     | -75 |     | dB  |     |
|                              | THD (P <sub>O</sub> =5mW)  |  |     |  |     | -73 |     | dB  |     |
|                              | THD+N (P <sub>O</sub> =5mW)  |  |     |  |     | -71 |     | dB  |     |
|                              | AVDD PSRR (217Hz)  |  |     |  | 70  |     | dB  |     |     |
|                              | HPVDD PSRR (217Hz)   |  |     |  | 85  |     | dB  |     |     |
|                              | Crosstalk (L/R)  |  |     |  | -95 |     | dB  |     |     |
|                              | SNR (A-weighted)   | Line Input to Headphones via LOMIX and ROMIX, R <sub>L</sub> =16Ω, AVDD=HPVDD=2.7V |     |  | 102 |     | dB  |     |     |
|                              | THD (P <sub>O</sub> =20mW)   |  |     |  |     |     | -74 | dB  |     |
| THD+N (P <sub>O</sub> =20mW) |  |  |     |  | -72 | dB  |     |     |     |
| THD (P <sub>O</sub> =5mW)    |  |  |     |  | -72 | dB  |     |     |     |
| THD+N (P <sub>O</sub> =5mW)  |  |  |     |  | -70 | dB  |     |     |     |

WM8959

Pre-Production

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER                            | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |  |    |
|--------------------------------------|---|-----|-----|-----|------|--|----|
| <b>Multi-Path Channel Separation</b> |   |     |     |     |      |  |    |
| G1                                   | <p>Headset Voice Call:<br/>DAC/Headset to Tx Voice Separation</p> <p>1kHz 0dBFS DAC playback to LOOUT and ROOUT; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output</p>  |     |     |     | 85   |  | dB |
| G2                                   | <p>Headset Voice Call:<br/>DAC/Speaker to Tx Voice Separation</p> <p>1kHz 0dBFS DAC playback to speaker, 1W output; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output</p>   |     |     |     | 100  |  | dB |
| G5                                   | <p>Ear Speaker Voice Call:<br/>Tx Voice and Rx Voice Separation</p> <p>1kHz Full scale differential input on RXP/RXN, output to OUT3/OUT4; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output</p>                                  |     |     |     | 70   |  | dB |
| G6                                   | <p>Headset Voice Call:<br/>Tx Voice and Rx Voice Separation</p> <p>1kHz full scale differential input on RXP/RXN via RXVOICE to LOMIX and ROMIX, output to LOOUT and ROOUT; Quiescent input on LIN12 or RIN12 (Gain=+12dB), differential output to LOP/LON or ROP/RON; Measure crosstalk at LOP/LON or ROP/RON output</p> |     |     |     | 75   |  | dB |

**Test Conditions**

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, SPKVDD = 5V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER  | TEST CONDITIONS  | MIN                                     | TYP                                  | MAX       | UNIT                                 |     |
|--|--|---|--------------------------------------|-----------|--------------------------------------|-----|
| <b>Analogue Reference Levels</b>   |  |   |                                      |           |                                      |     |
| H1   | VMID Midrail Reference Voltage                           | -3%                                     | AVDD/2                               | +3%       | V                                    |     |
| <b>Microphone Bias</b>   |  |   |                                      |           |                                      |     |
| H2   | Bias Voltage   | 3mA load current<br>M1BSEL=0 / M2BSEL=0 | -5%                                  | 0.9×AVDD  | +5%                                  | V   |
|  |  | 3mA load current<br>M1BSEL=1 / M2BSEL=1 | -5%                                  | 0.65×AVDD | +5%                                  | V   |
| H3   | Bias Current Source                                      |   |                                      | 3         | mA                                   |     |
| H4   | Output Noise Density                                     | 1kHz to 20kHz                           | 100                                  |           | nV/√Hz                               |     |
| H5   | AVDD PSRR (217Hz)  | 100mV pk-pk @217Hz<br>on AVDD           | 45                                   |           | dB                                   |     |
| <b>Digital Input / Output</b>  |  |   |                                      |           |                                      |     |
| H6   | Input HIGH Level   |   | 0.7×DBVDD                            |           | V                                    |     |
| H7   | Input LOW Level  |   |                                      | 0.3×DBVDD | V                                    |     |
| Note that digital input pins should not be left unconnected / floating.<br>Internal pull-up/pull-down resistors may be enabled on GPIO1, GPIO3, GPIO4 and GPIO5 if required. |  |   |                                      |           |                                      |     |
| H8   | Output HIGH Level  | I <sub>OL</sub> =1mA                    | 0.9×DBVDD                            |           | V                                    |     |
| H9   | Output LOW Level   | I <sub>OH</sub> =-1mA                   |                                      | 0.1×DBVDD | V                                    |     |
| H10  | Input capacitance  |   | 10                                   |           | pF                                   |     |
| H11  | Input leakage  |   | -0.9                                 | 0.9       | µA                                   |     |
| <b>PLL</b>   |  |   |                                      |           |                                      |     |
| H12  | Input Frequency  | PRESCALE = 0b                           | 10                                   |           | 17                                   | MHz |
|  |  | PRESCALE = 1b                           | 20                                   |           | 34                                   | MHz |
| H13  | Lock time  |   | 200                                  |           | µs                                   |     |
| <b>GPIO</b>  |  |   |                                      |           |                                      |     |
| H14  | Clock output duty cycle<br>(Integer OPCLKDIV)            | SYCLK=MCLK;<br>OPCLKDIV=0000            | 35                                   |           | 65                                   | %   |
|  |  | SYCLK=MCLK;<br>OPCLKDIV=1000            | 45                                   |           | 55                                   | %   |
|  |  | SYCLK=PLL output;<br>OPCLKDIV=0000      | 45                                   |           | 55                                   | %   |
|  |  | SYCLK=PLL output;<br>OPCLKDIV=1000      | 45                                   |           | 55                                   | %   |
| H15  | Clock output duty cycle<br>(Non-integer OPCLKDIV)        | SYCLK=MCLK;<br>OPCLKDIV=0100            | 33                                   |           | 66                                   | %   |
|  |  | SYCLK=PLL output;<br>OPCLKDIV=0100      | 33                                   |           | 66                                   | %   |
| H16  | Interrupt response time for accessory /<br>button detect | Input de-bounced                        | 2 <sup>21</sup> / f <sub>SYCLK</sub> |           | 2 <sup>22</sup> / f <sub>SYCLK</sub> | s   |
|  |  | Input de-bounced<br>TOCLKSEL=1          | 2 <sup>19</sup> / f <sub>SYCLK</sub> |           | 2 <sup>20</sup> / f <sub>SYCLK</sub> | s   |
|  |  | Input not de-bounced                    |                                      | 0         |                                      | s   |

## TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. For example, measured signal level on the output of the idle right channel (RIN3 to ROUT via ROMIX) with a full scale signal level at the output of the active left channel (LIN1 to LOUT via LOMIX).
5. Multi-Path Channel Separation (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
7. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

## TYPICAL POWER CONSUMPTION

| Control Register   | Other settings | AVDD | HPVDD | SPKVDD | DBVDD | DCVDD | IAVDD | IHPVDD | ISPKVDD | IDBVDD | IDCVDD | Total Power |       |
|--|----------------|------|-------|--------|-------|-------|-------|--------|---------|--------|--------|-------------|-------|
| Mode   |                | (V)  | (V)   | (V)    | (V)   | (V)   | (mA)  | (mA)   | (mA)    | (mA)   | (mA)   | (mW)        |       |
| OFF<br>(default state at power-up)   | No Clocks      | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 0.028 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.074 |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 0.029 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.086 |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 0.030 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.099 |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 0.031 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.114 |
| OFF<br>(thermal sensor disabled)   | No Clocks      | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 0.008 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.019 |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 0.008 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.024 |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 0.009 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.028 |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 0.009 | 0.000  | 0.000   | 0.000  | 0.000  | 0.000       | 0.035 |
| SLEEP<br>(VMID enabled, thermal sensor enabled)  | With Clocks    | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 0.087 | 0.000  | 0.000   | 0.004  | 0.004  | 0.459       | 1.067 |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 0.096 | 0.000  | 0.000   | 0.008  | 0.008  | 0.694       | 2.043 |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 0.106 | 0.000  | 0.000   | 0.014  | 0.014  | 1.025       | 3.779 |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 0.117 | 0.000  | 0.000   | 0.017  | 0.017  | 1.162       | 4.667 |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>16ohm load   | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.950 | 0.705  | 0.000   | 0.003  | 2.147  | 13.739      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 0.558  | 0.000   | 0.007  | 3.190  | 19.586      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 0.640  | 0.000   | 0.013  | 4.544  | 29.307      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 0.726  | 0.000   | 0.016  | 5.092  | 35.600      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>-20dBV Pink Noise into 16ohm load                            | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.951 | 1.430  | 0.000   | 0.004  | 2.298  | 15.971      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 1.367  | 0.000   | 0.007  | 3.380  | 22.513      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 1.544  | 0.000   | 0.013  | 4.817  | 33.189      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 1.742  | 0.000   | 0.016  | 5.404  | 40.381      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>-30dBV Pink Noise into 16ohm load                            | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.950 | 0.828  | 0.000   | 0.004  | 2.263  | 14.279      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 0.743  | 0.000   | 0.007  | 3.362  | 20.596      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.684 | 0.835  | 0.000   | 0.013  | 4.762  | 30.671      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.056 | 0.937  | 0.000   | 0.016  | 5.344  | 37.270      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>0.1mW/channel into 16ohm load                                | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.950 | 2.563  | 0.000   | 0.004  | 2.251  | 18.943      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 2.476  | 0.000   | 0.007  | 3.323  | 25.698      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 2.508  | 0.000   | 0.014  | 4.736  | 36.103      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 2.556  | 0.000   | 0.016  | 5.304  | 42.951      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>5mW/channel into 16ohm load                                  | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.952 | 15.767 | 0.000   | 0.004  | 2.256  | 54.608      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.316 | 15.789 | 0.000   | 0.007  | 3.343  | 65.690      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 15.675 | 0.000   | 0.013  | 4.762  | 79.640      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 15.836 | 0.000   | 0.016  | 5.329  | 90.850      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>32ohm load   | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.951 | 0.699  | 0.000   | 0.004  | 2.147  | 13.725      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.317 | 0.550  | 0.000   | 0.007  | 3.179  | 19.565      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.684 | 0.629  | 0.000   | 0.013  | 4.543  | 29.268      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 0.711  | 0.000   | 0.016  | 5.089  | 35.536      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>-20dBV Pink Noise into 32ohm load                            | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.951 | 1.019  | 0.000   | 0.004  | 2.302  | 14.868      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 0.915  | 0.000   | 0.007  | 3.359  | 21.105      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.684 | 1.045  | 0.000   | 0.014  | 4.806  | 31.509      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.056 | 1.180  | 0.000   | 0.016  | 5.367  | 38.228      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>-30dBV Pink Noise into 32ohm load                            | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.950 | 0.748  | 0.000   | 0.004  | 2.265  | 14.067      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 0.624  | 0.000   | 0.007  | 3.337  | 20.177      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 0.704  | 0.000   | 0.013  | 4.786  | 30.314      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 0.789  | 0.000   | 0.016  | 5.359  | 36.789      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>0.1mW/channel into 32ohm load                                | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.950 | 1.950  | 0.000   | 0.004  | 2.253  | 17.291      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.315 | 1.868  | 0.000   | 0.007  | 3.327  | 23.883      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.683 | 1.905  | 0.000   | 0.014  | 4.741  | 34.129      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.055 | 1.950  | 0.000   | 0.016  | 5.312  | 40.799      |       |
| Playback to AC Coupled Headphones<br>(DAC to L/ROUT)<br>5mW/channel into 32ohm load                                  | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.955 | 11.421 | 0.000   | 0.004  | 2.267  | 42.901      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.319 | 11.362 | 0.000   | 0.007  | 3.351  | 52.438      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.686 | 11.349 | 0.000   | 0.014  | 4.777  | 65.423      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.057 | 11.406 | 0.000   | 0.016  | 5.342  | 74.956      |       |
| Playback to Line-Out<br>(DAC to ROP/RON)   | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 3.934 | 0.000  | 0.000   | 0.004  | 2.144  | 14.487      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 4.184 | 0.000  | 0.000   | 0.007  | 3.179  | 20.517      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 4.672 | 0.000  | 0.000   | 0.013  | 4.541  | 30.446      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 5.166 | 0.000  | 0.000   | 0.016  | 5.089  | 36.976      |       |
| Playback to Speaker Class D<br>(DAC to SPK)<br>8ohm load   | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 3.621 | 0.000  | 3.070   | 0.004  | 2.138  | 23.763      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 4.080 | 0.000  | 3.652   | 0.007  | 3.167  | 33.322      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 4.548 | 0.000  | 5.154   | 0.013  | 4.530  | 51.648      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 5.021 | 0.000  | 7.223   | 0.016  | 5.073  | 72.511      |       |
| Playback to Speaker Class AB<br>(DAC to SPK)<br>8ohm load  | fs=44.1kHz     | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 3.087 | 0.000  | 2.823   | 0.004  | 2.125  | 21.482      |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 3.470 | 0.000  | 3.307   | 0.007  | 3.146  | 30.198      |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 3.856 | 0.000  | 4.061   | 0.013  | 4.496  | 44.662      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 4.246 | 0.000  | 5.057   | 0.016  | 5.042  | 58.780      |       |
| FM Radio to AC Coupled Headphones<br>(L/RIN3 to L/ROUT bypass via LROMIX)<br>16ohm load                              |                | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 0.442 | 0.697  | 0.000   | 0.000  | 0.000  | 3.074       |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 0.499 | 0.544  | 0.000   | 0.000  | 0.000  | 3.128       |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 0.556 | 0.621  | 0.000   | 0.000  | 0.000  | 3.884       |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 0.613 | 0.702  | 0.000   | 0.000  | 0.000  | 4.735       |       |
| Analogue Voice Call to Handset Ear Speaker<br>(MIC on LIN12 to LOP/LON)<br>(RXP/RXN to OUT3/4 via RXVIOCE & AINLMUX) |                | 2.7  | 2.7   | 3.3    | 1.8   | 1.8   | 2.307 | 0.796  | 0.000   | 0.000  | 0.000  | 8.377       |       |
|  |                | 3.0  | 3.0   | 3.6    | 2.5   | 2.5   | 2.374 | 0.615  | 0.000   | 0.000  | 0.000  | 8.966       |       |
|  |                | 3.3  | 3.3   | 4.2    | 3.3   | 3.3   | 2.660 | 0.703  | 0.000   | 0.000  | 0.000  | 11.097      |       |
|  |                | 3.6  | 3.6   | 5.0    | 3.6   | 3.6   | 2.953 | 0.794  | 0.000   | 0.000  | 0.000  | 13.490      |       |

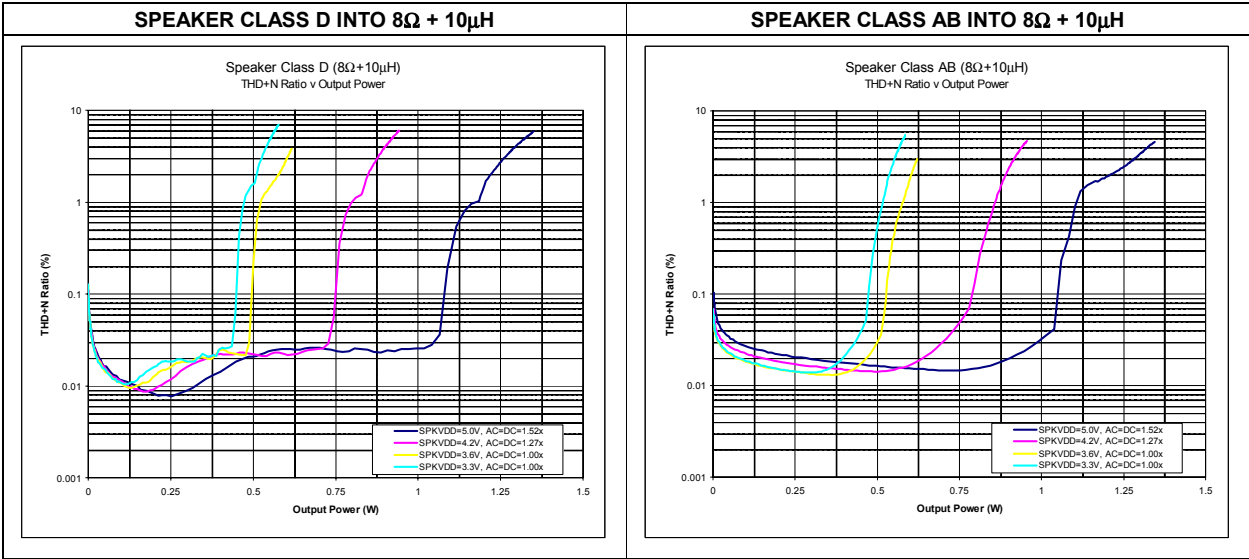
## Notes:

- Power in the load is included.
- All figures are quoted at  $T_A = +25^\circ\text{C}$
- All figures are quoted as quiescent current unless otherwise stated.

### SPEAKER DRIVER PERFORMANCE

Typical speaker driver THD+N performance is shown below for both Class D and Class AB modes. Curves are shown for four typical SPKVDD supply voltage and gain combinations.

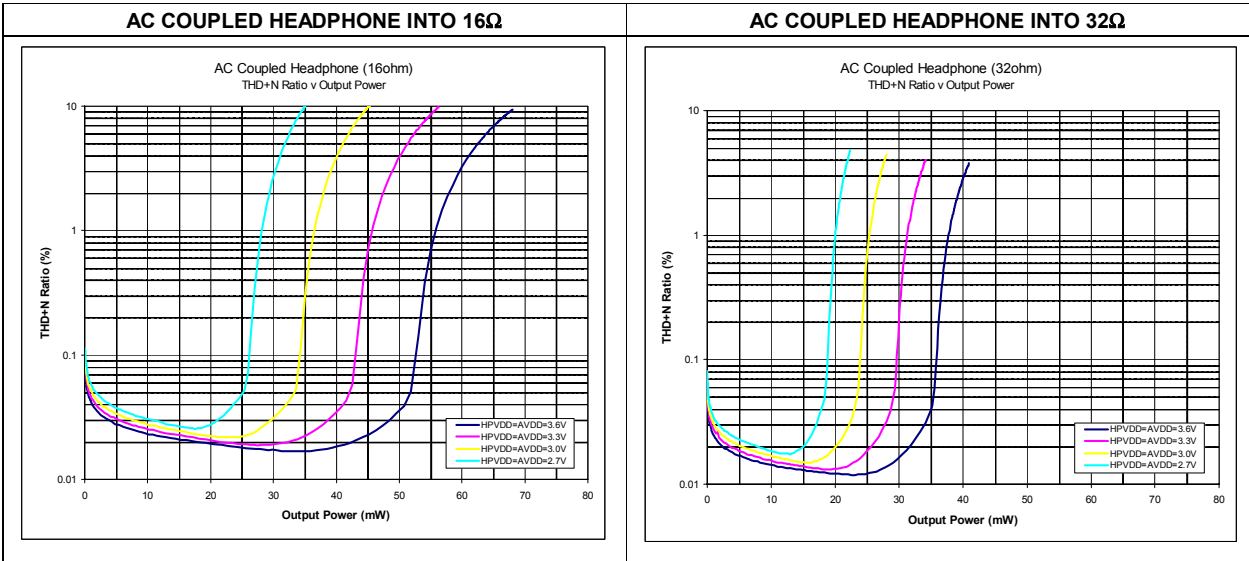
Load  $R_L = 8\Omega + 10\mu H$ , Frequency = 1kHz, +1dB gain in active path.



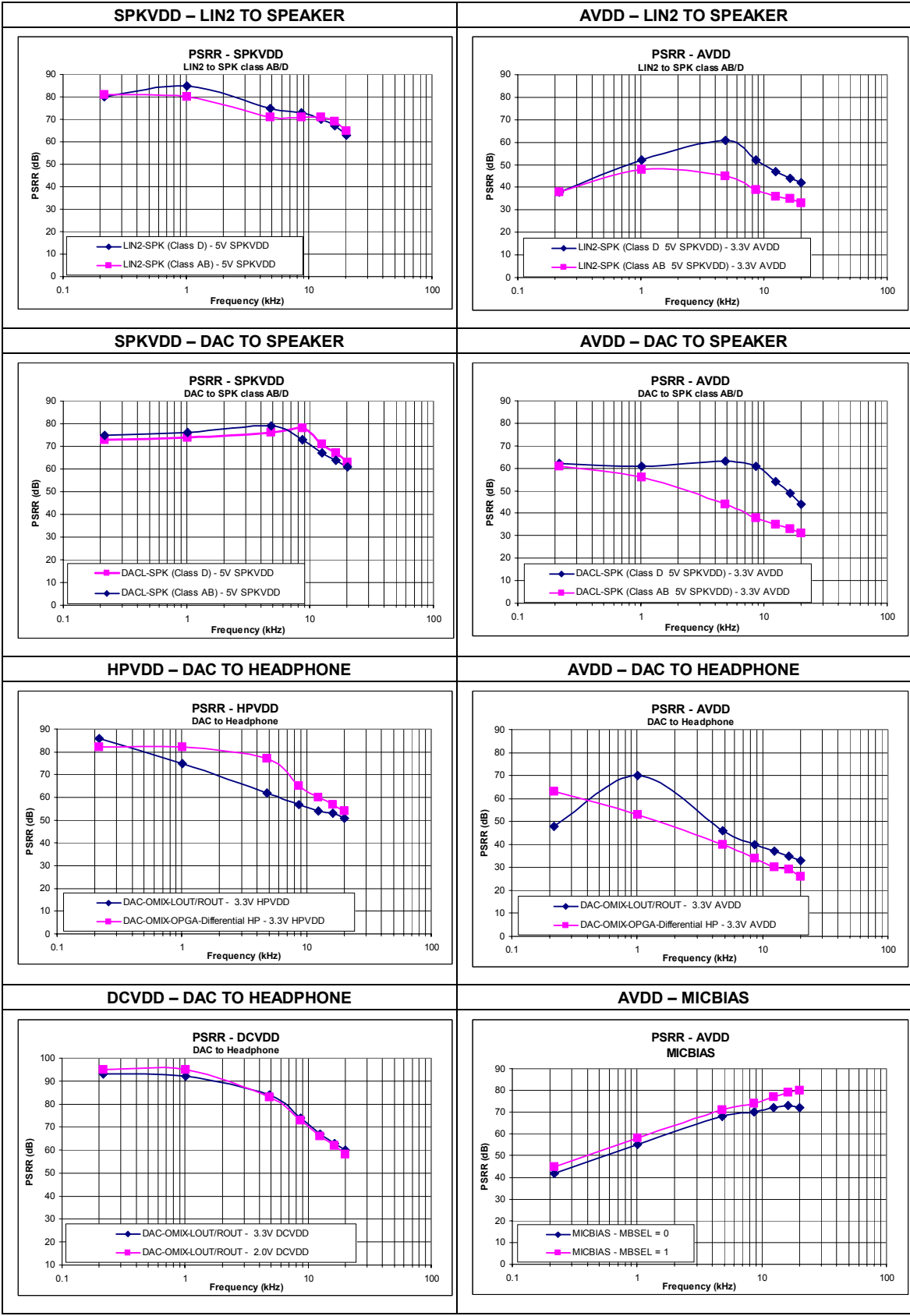
### HEADPHONE DRIVER PERFORMANCE

Typical THD+N performance of the Headphone Drivers is shown below (AC coupled to LOUT/ROUT). Curves are shown for four HPVDD/AVDD supply voltages.

Load  $R_L = 16\Omega$  and  $32\Omega$ , Frequency = 1kHz, +1dB gain in active path.

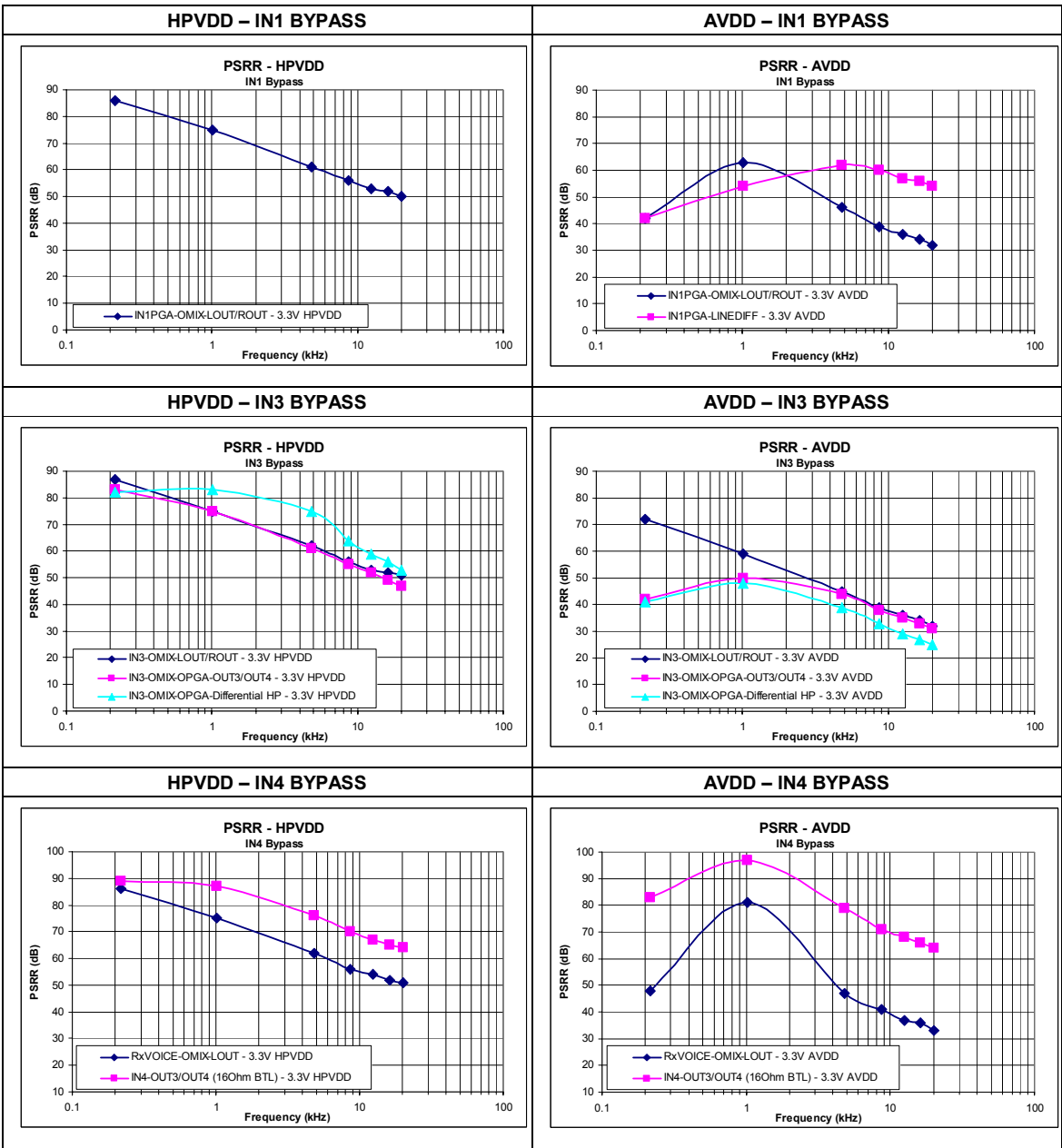


PSRR PERFORMANCE



WM8959

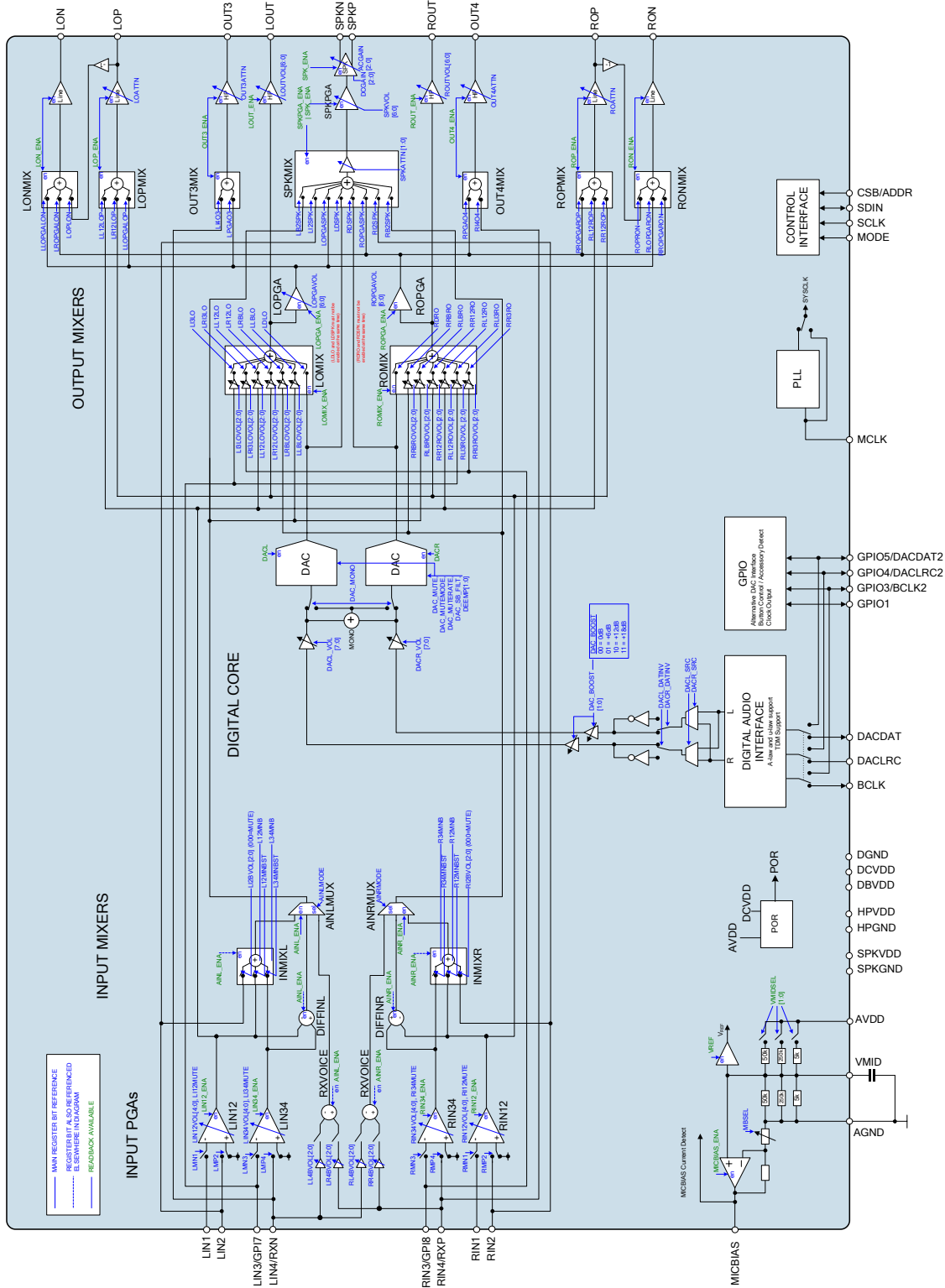
Pre-Production



Note: All figures based on 100mVp-p injected on the supply at the relevant test frequency.



# AUDIO SIGNAL PATHS



**SIGNAL TIMING REQUIREMENTS**

**SYSTEM CLOCK TIMING**

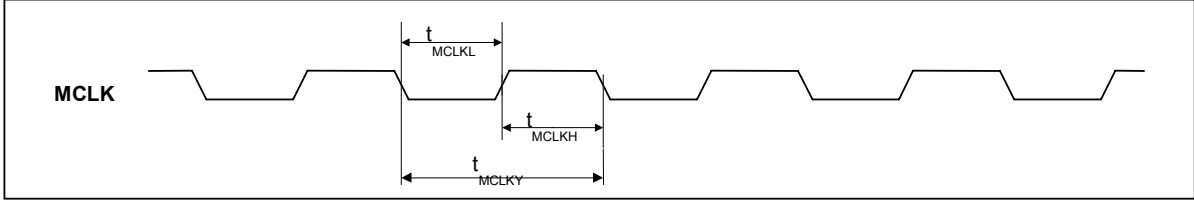


Figure 4 System Clock Timing Requirements

**Test Conditions**

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T<sub>A</sub> = +25°C

| PARAMETER                              | SYMBOL             | CONDITIONS                               | MIN   | TYP | MAX   | UNIT |
|--|--------------------|--|-------|-----|-------|------|
| <b>System Clock Timing Information</b> |                    |  |       |     |       |      |
| MCLK cycle time                        | T <sub>MCLKY</sub> |  | 33.33 |     |       | ns   |
| MCLK duty cycle                        |                    | = T <sub>MCLKH</sub> /T <sub>MCLKL</sub> | 60:40 |     | 40:60 |      |

## AUDIO INTERFACE TIMING – MASTER MODE

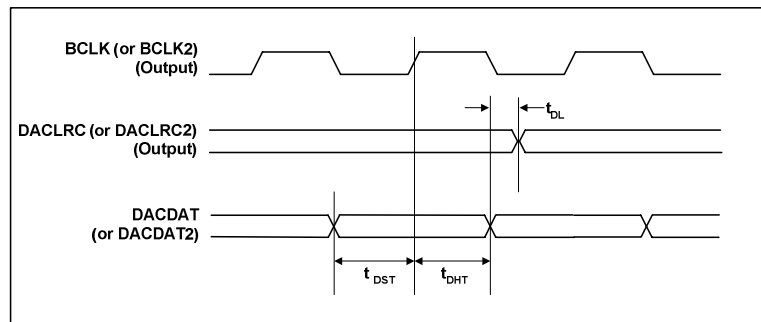


Figure 5 Digital Audio Data Timing – Master Mode (see Control Interface)

### Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V,  $T_A=+25^{\circ}\text{C}$ , Slave Mode,  $f_s=48\text{kHz}$ ,  $MCLK=256\text{fs}$ , data, unless otherwise stated.

| PARAMETER   | SYMBOL    | MIN | TYP | MAX | UNIT |
|---|-----------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b>                              |           |     |     |     |      |
| DACLRC (or DACLRC2) propagation delay from BCLK (or BCLK2) falling edge | $t_{DL}$  |     |     | 20  | ns   |
| DACDAT (or DACDAT2) setup time to BCLK rising edge                      | $t_{DST}$ | 20  |     |     | ns   |
| DACDAT (or DACDAT2) hold time from BCLK rising edge                     | $t_{DHT}$ | 10  |     |     | ns   |

## AUDIO INTERFACE TIMING – SLAVE MODE

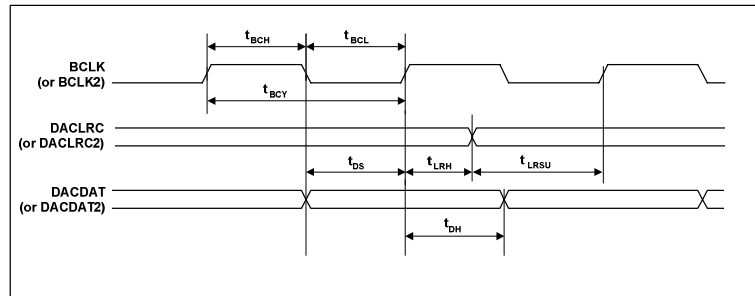


Figure 6 Digital Audio Data Timing – Slave Mode

## Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V,  $T_A=+25^{\circ}\text{C}$ , Slave Mode,  $f_s=48\text{kHz}$ ,  $\text{MCLK}=256f_s$ , 24-bit data, unless otherwise stated.

| PARAMETER  | SYMBOL     | MIN | TYP | MAX | UNIT |
|--|------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b>                     |            |     |     |     |      |
| BCLK (or BCLK2) cycle time                                     | $t_{BCY}$  | 50  |     |     | ns   |
| BCLK (or BCLK2) pulse width high                               | $t_{BCH}$  | 20  |     |     | ns   |
| BCLK (or BCLK2) pulse width low                                | $t_{BCL}$  | 20  |     |     | ns   |
| DACLRC (or DACLRC2) set-up time to BCLK (or BCLK2) rising edge | $t_{LRSU}$ | 20  |     |     | ns   |
| DACLRC (or DACLRC2) hold time from BCLK (or BCLK2) rising edge | $t_{LRH}$  | 10  |     |     | ns   |
| DACDAT (or DACDAT2) hold time from BCLK (or BCLK2) rising edge | $t_{DH}$   | 10  |     |     | ns   |
| DACDAT (or DACDAT2) set-up time to BCLK (or BCLK2) rising edge | $t_{DS}$   | 20  |     |     | ns   |

## Note:

BCLK (or BCLK2) period should always be greater than or equal to MCLK period.

## CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

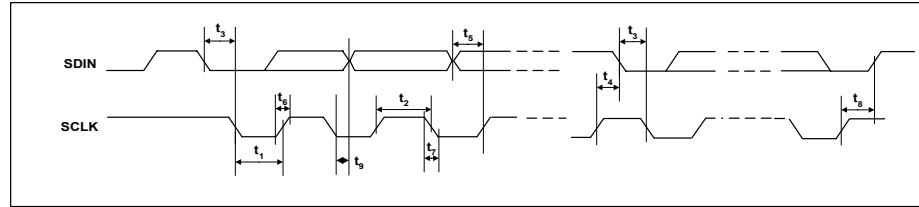


Figure 7 Control Interface Timing – 2-Wire Serial Control Mode

### Test Conditions

DCVDD=1.8V, DBVDD=AVDD=HPVDD=SPKVDD=3.3V, DGND=AGND=HPGND=SPKGND=0V,  $T_A=+25^{\circ}\text{C}$ , Slave Mode,  $f_s=48\text{kHz}$ , MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                     | SYMBOL   | MIN | TYP | MAX | UNIT          |
|---|----------|-----|-----|-----|---------------|
| <b>Program Register Input Information</b>     |          |     |     |     |               |
| SCLK Frequency                                |          |     |     | 526 | kHz           |
| SCLK Low Pulse-Width                          | $t_1$    | 1.3 |     |     | $\mu\text{s}$ |
| SCLK High Pulse-Width                         | $t_2$    | 600 |     |     | ns            |
| Hold Time (Start Condition)                   | $t_3$    | 600 |     |     | ns            |
| Setup Time (Start Condition)                  | $t_4$    | 600 |     |     | ns            |
| Data Setup Time                               | $t_5$    | 100 |     |     | ns            |
| SDIN, SCLK Rise Time                          | $t_6$    |     |     | 300 | ns            |
| SDIN, SCLK Fall Time                          | $t_7$    |     |     | 300 | ns            |
| Setup Time (Stop Condition)                   | $t_8$    | 600 |     |     | ns            |
| Data Hold Time                                | $t_9$    |     |     | 900 | ns            |
| Pulse width of spikes that will be suppressed | $t_{ps}$ | 0   |     | 5   | ns            |

## CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

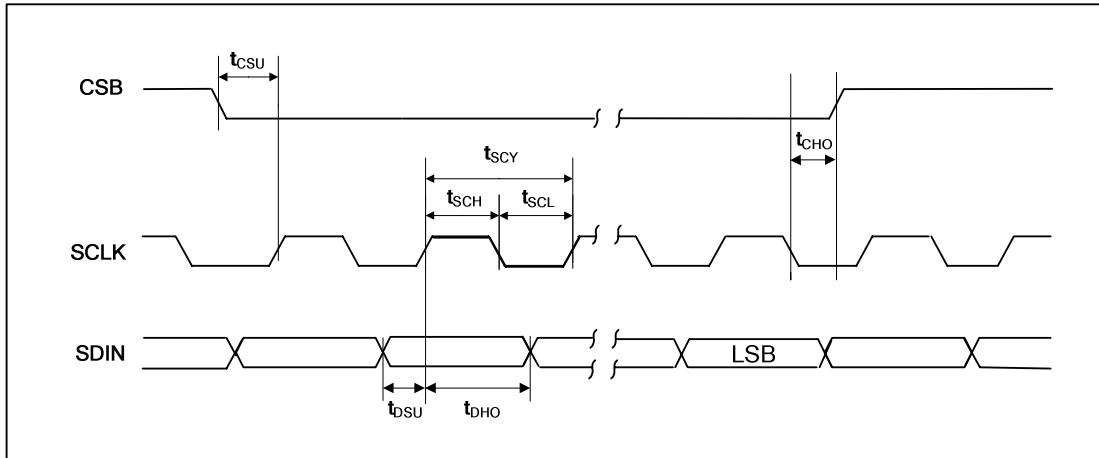


Figure 8 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)

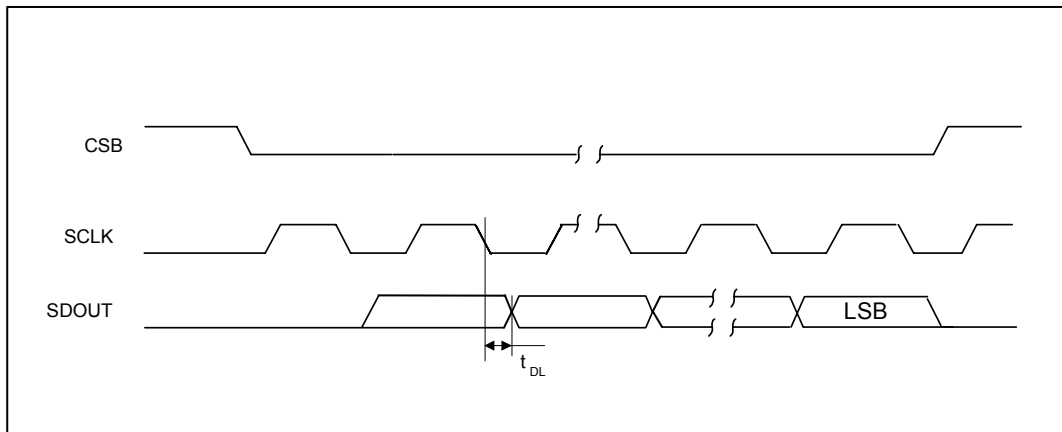


Figure 9 Control Interface Timing – 3-Wire Serial Control Mode (Read Cycle)

### Test Conditions

DCVDD=1.8V, DBVDD=AVDD=HPVDD=SPKVDD=3.3V, DGND=AGND=HPGND=SPKGND=0V,  $T_A=+25^{\circ}\text{C}$ , Slave Mode,  $f_s=48\text{kHz}$ , MCLK=256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                     | SYMBOL    | MIN | TYP | MAX | UNIT |
|---|-----------|-----|-----|-----|------|
| <b>Program Register Input Information</b>     |           |     |     |     |      |
| CSB falling edge to SCLK rising edge          | $t_{CSU}$ | 40  |     |     | ns   |
| SCLK falling edge to CSB rising edge          | $t_{CHO}$ | 40  |     |     | ns   |
| SCLK pulse cycle time                         | $t_{SCY}$ | 200 |     |     | ns   |
| SCLK pulse width low                          | $t_{SCL}$ | 80  |     |     | ns   |
| SCLK pulse width high                         | $t_{SCH}$ | 80  |     |     | ns   |
| SDIN to SCLK set-up time                      | $t_{DSU}$ | 40  |     |     | ns   |
| SDIN to SCLK hold time                        | $t_{DHO}$ | 10  |     |     | ns   |
| Pulse width of spikes that will be suppressed | $t_{ps}$  | 0   |     | 5   | ns   |
| SCLK falling edge to SDOUT transition         | $t_{DL}$  |     |     | 40  | ns   |

## CONTROL INTERFACE TIMING – 4-WIRE MODE

4-wire mode supports readback via SDOOUT which is available as a GPIO pin function.

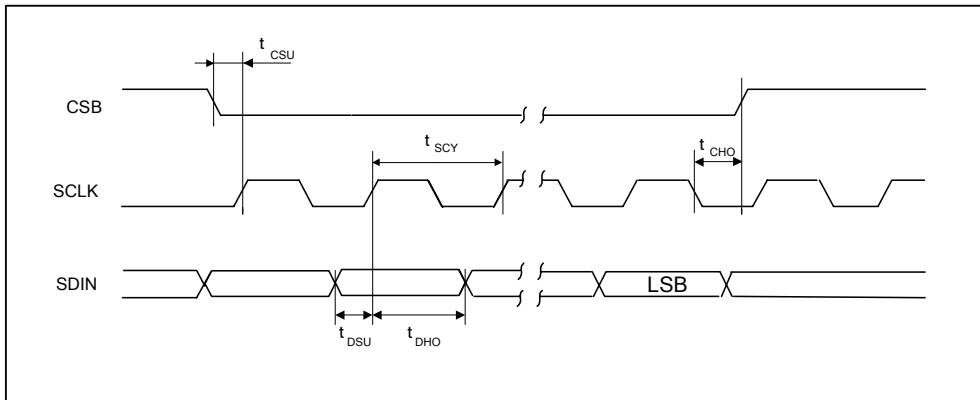


Figure 10 Control Interface Timing – 4-Wire Serial Control Mode (Write Cycle)

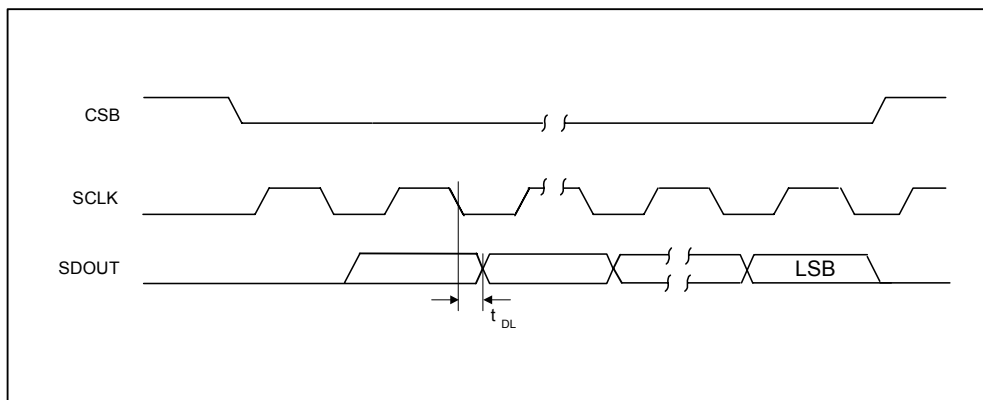


Figure 11 Control Interface Timing – 4-Wire Serial Control Mode (Read Cycle)

### Test Conditions

DCVDD=1.8V, DBVDD=AVDD=HPVDD=SPKVDD=3.3V, DGND=AGND=HPGND=SPKGND=0V, T<sub>A</sub> =+25°C, Slave Mode, f<sub>s</sub>=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

| PARAMETER                                      | SYMBOL           | MIN | TYP | MAX | UNIT |
|--|------------------|-----|-----|-----|------|
| <b>Program Register Input Information</b>      |                  |     |     |     |      |
| SCLK rising edge to CSB falling edge           | t <sub>CSU</sub> | 40  |     |     | ns   |
| SCLK falling edge to CSB rising edge           | t <sub>CHO</sub> | 40  |     |     | ns   |
| SCLK pulse cycle time                          | t <sub>SCY</sub> | 200 |     |     | ns   |
| SCLK pulse width low                           | t <sub>SCL</sub> | 80  |     |     | ns   |
| SCLK pulse width high                          | t <sub>SCH</sub> | 80  |     |     | ns   |
| SDIN to SCLK set-up time                       | t <sub>DSU</sub> | 40  |     |     | ns   |
| SDIN to SCLK hold time                         | t <sub>DHO</sub> | 10  |     |     | ns   |
| SDOOUT propagation delay from SCLK rising edge | t <sub>DL</sub>  |     |     | 10  | ns   |
| Pulse width of spikes that will be suppressed  | t <sub>ps</sub>  | 0   |     | 5   | ns   |
| SCLK falling edge to SDOOUT transition         | t <sub>DL</sub>  |     |     | 40  | ns   |

## INTERNAL POWER ON RESET CIRCUIT

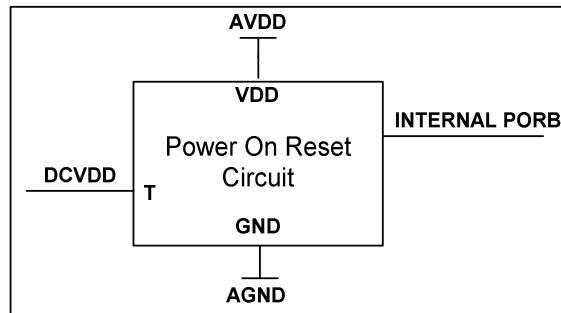


Figure 12 Internal Power on Reset Circuit Schematic

The WM8959 includes an internal Power-On-Reset Circuit, as shown in Figure 12, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

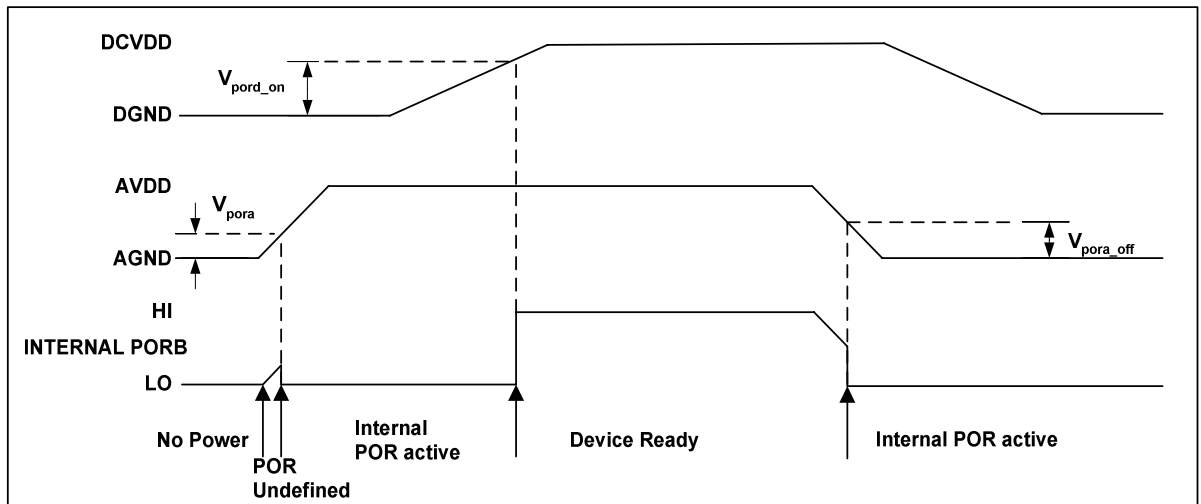


Figure 13 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 13 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to  $V_{pord\_on}$  and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold  $V_{pora\_off}$ .



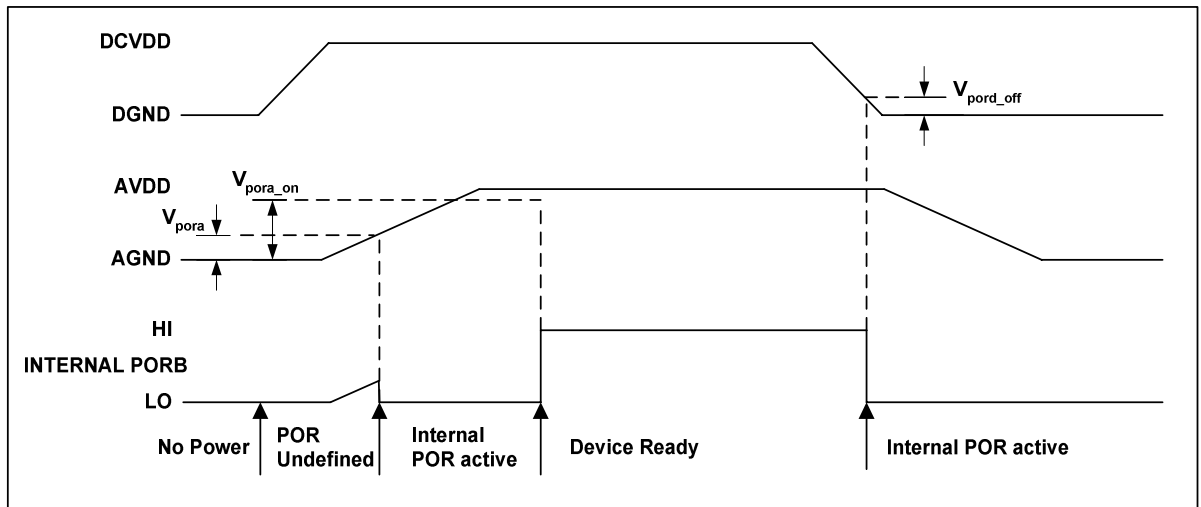


Figure 14 Typical Power up Sequence where DCVDD is powered before AVDD

Figure 14 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to  $V_{pora\_on}$ , PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold  $V_{pord\_off}$ .

| SYMBOL          | MIN | TYP  | MAX | UNIT |
|-----------------|-----|------|-----|------|
| $V_{pora}$      |     | 0.6  |     | V    |
| $V_{pora\_on}$  |     | 1.52 |     | V    |
| $V_{pora\_off}$ |     | 1.5  |     | V    |
| $V_{pord\_on}$  |     | 0.92 |     | V    |
| $V_{pord\_off}$ |     | 0.9  |     | V    |

Table 1 Typical POR Operation (typical values, not tested)

#### Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below  $V_{pora\_off}$  or  $V_{pord\_off}$ ) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below  $V_{pora\_off}$  or  $V_{pord\_off}$ . This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum  $t_{por}$  period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

## DEVICE DESCRIPTION

### INTRODUCTION

The WM8959 is a low power, high quality audio DAC designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small 3.226 x 3.44mm footprint makes it ideal for portable applications such as mobile phones.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs plus multiple stereo or mono line inputs (single-ended or differential). Connections to an external voice CODEC, FM radio, melody IC, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the DAC has been designed for maximum flexibility to support a wide variety of usage modes.

Ten analogue output drivers are integrated, including a high power, high quality speaker driver, capable of providing 1W in class D mode or in class AB mode into 8 $\Omega$  BTL. Four headphone drivers are provided, supporting ear speakers and stereo headsets. Fully differential headphone drive is supported for excellent crosstalk performance and removing the need for large and expensive headphone capacitors. Four line outputs are available for Tx voice output to a voice CODEC, interfacing to an additional speaker driver and single-ended or fully differential line output. All outputs have integrated pop and click suppression. The speaker supply has been designed with low leakage and high PSRR, to support direct connection to a Lithium battery. In addition to the speaker PGA, six AC and DC gain settings allow output signal level to be maximised for many commonly-used SPKVDD/AVDD combinations.

Internal signal routing and amplifier configurations have been optimised to provide the lowest possible power consumption for a number of common usage scenarios such as voice calls and music playback.

The stereo DACs are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. An integrated ultra-low power PLL provides flexible clocking capabilities. DAC soft mute and un-mute is available for pop-free music playback.

The WM8959 has a highly flexible digital audio interface, supporting a number of protocols, including I2S, DSP, MSB-First left/right justified. The interface can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and  $\mu$ -law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. Alternative DAC interface pins are provided to allow connection to an additional processor.

The SYSCLK (system clock) provides clocking for the DACs, DSP, Class D outputs and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via the integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8959 uses a standard 2-wire or 3/4-wire control interface with readback of key registers supported. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications. The device address can be selected using the CSB/ADDR pin.

Versatile GPIO functionality is provided, with support for up to four button/accessory detect inputs with interrupt and status readback and flexible de-bouncing options, clock output, and logic '1' / logic '0' for control of additional external circuitry.

## ANALOGUE INPUT PATH

The WM8959 has eight highly flexible analogue input channels, configurable in many combinations of the following:

1. Up to four pseudo-differential or single-ended microphone inputs
2. Up to eight mono line inputs or 4 stereo line inputs
3. Mono input from external voice CODEC
4. Two fully balanced differential inputs

These inputs may be mixed together or independently routed to different combinations of output drivers. The WM8959 input signal paths and control registers are illustrated in Figure 15.

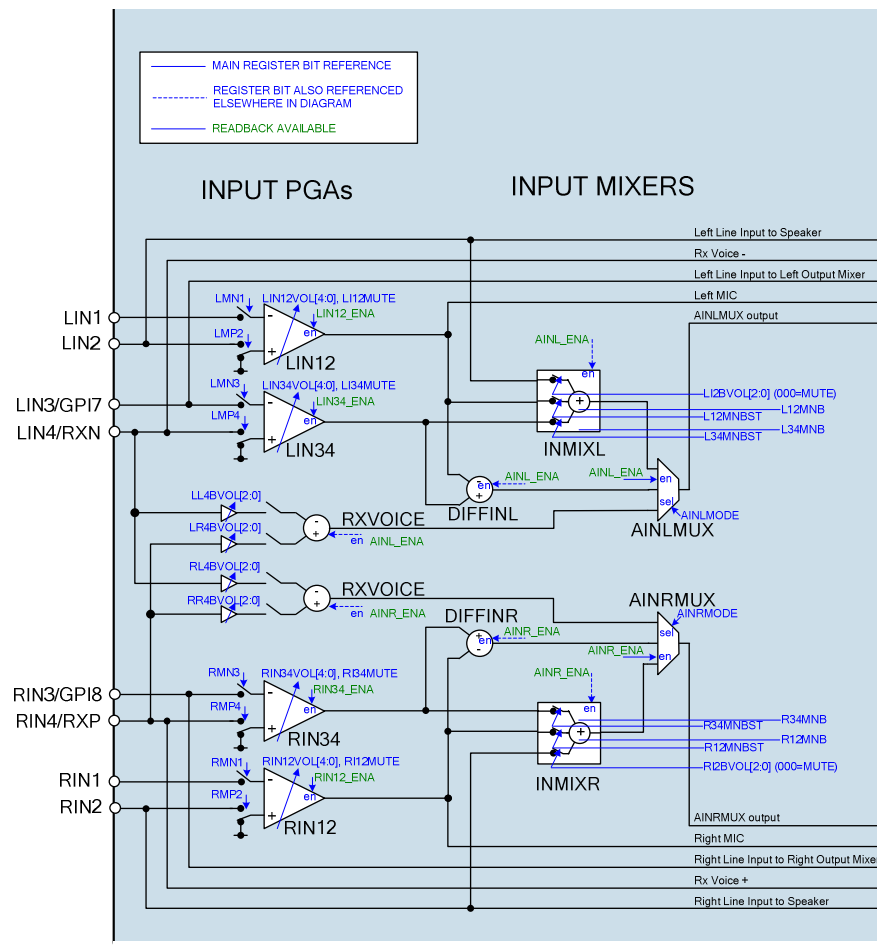


Figure 15 Control Registers for Input Signal Path

## MICROPHONE INPUTS

Up to four microphones can be connected to the WM8959, either in single-ended or pseudo-differential mode. A low noise microphone bias is fully integrated to reduce the need for external components.

In single-ended microphone input configuration, the microphone signal is connected to the inverting input of the PGA (LIN1, LIN3, RIN1 or RIN3). The non-inverting input of the PGAs should be internally connected to VMID in this configuration. This is enabled via the Input PGA configuration register settings. In this configuration, LIN2, LIN4, RIN2 or RIN4 may be free to be used as line input to the Input Mixer or directly to the Speaker Mixer.

In pseudo-differential microphone input configuration, the non-inverted microphone signal is connected to the non-inverting input of the PGA (LIN2, LIN4, RIN2 or RIN4) and the inverted (or noisy ground) signal is connected to the inverting input (LIN1, LIN3, RIN1 or RIN3).

Any PGA input pin that is used in either microphone configuration should not be enabled as a line input path at the same time.

The gain of the input PGAs is controlled via register settings. Note that the input impedance of LIN1, LIN3, RIN1 and RIN3 changes with the input PGA gain setting, as described under "Electrical Characteristics". (Note this does not apply to input paths which bypass the input PGA.) The input impedance of LIN2, LIN4, RIN2 and RIN4 does not change with input PGA gain. The inverting and non-inverting inputs are therefore not matched and the differential configuration is not fully differential.

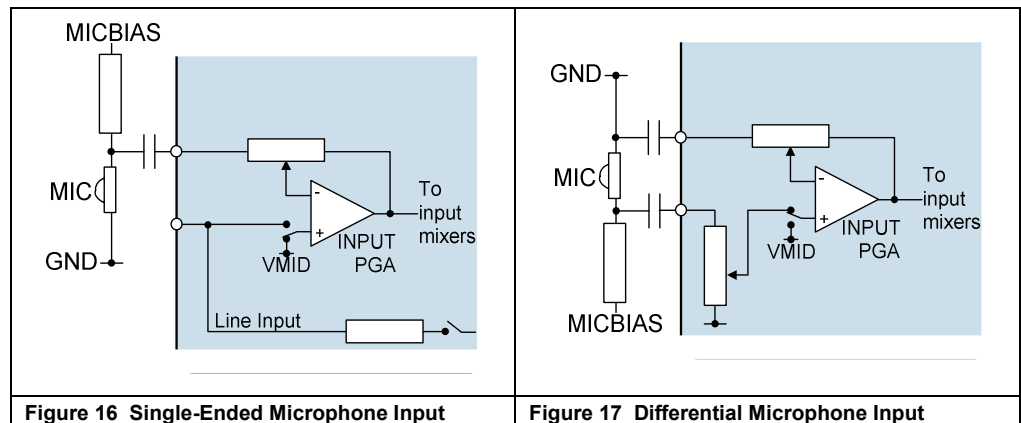


Figure 16 Single-Ended Microphone Input

Figure 17 Differential Microphone Input

## LINE INPUTS

All eight analogue input pins may be configured as line inputs. Various signal paths exist to provide flexibility, high performance and low power consumption for different usage modes.

LIN1 and RIN1 can operate as line inputs to the Input PGAs LIN12 and RIN12 to provide high gain if required for small input signals.

LIN2 and RIN2 can operate as line inputs directly to the input mixers or to the speaker output mixer. Direct routing to the speaker output minimises power consumption by reducing the number of active amplifiers in the signal path.

LIN3 and RIN3 can operate as line inputs to the Input PGAs or as a line input directly to either of the output mixers LOMIX and ROMIX.

LIN1+LIN3 and RIN1+RIN3 can also be used as fully balanced differential inputs via the Input PGAs to one of the input mixers. (Note that these inputs have matched input impedances.)

LIN4/RXN and RIN4/RXP can operate as line inputs directly to the outputs OUT3 and OUT4, providing an ultra-low power stereo or mono differential signal path (e.g. from an external voice CODEC) to an ear speaker. LIN4/RXN and RIN4/RXP can also operate as a mono differential input directly to the output mixer stages.

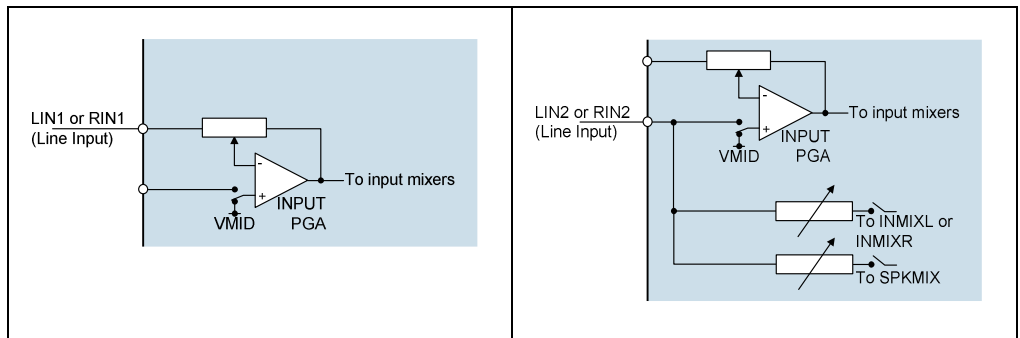


Figure 18 LIN1 or RIN1 as Line Inputs

Figure 19 LIN2 or RIN2 as Line Inputs

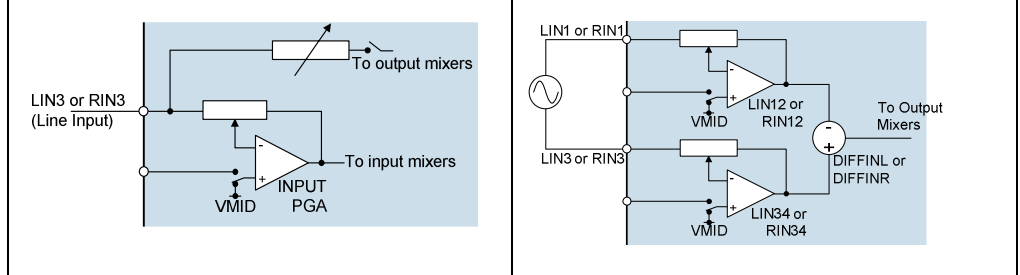


Figure 20 LIN3 or RIN3 as Line Inputs

Figure 21 Fully Balanced Differential Input

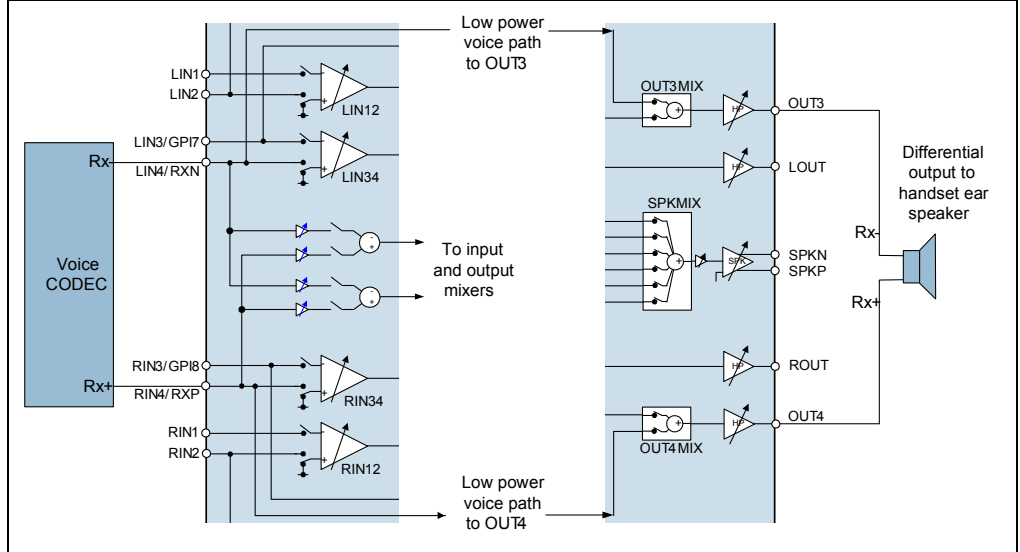


Figure 22 LIN4 and RIN4 as Rx Voice Inputs with Direct Low Power Path to Ear Speaker

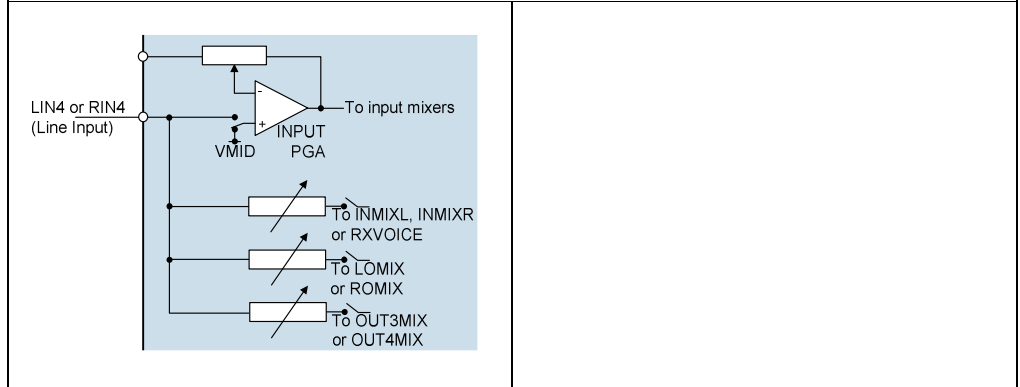


Figure 23 LIN4 or RIN4 as Line Inputs

**INPUT PGA ENABLE**

The Input PGAs are enabled using register bits LIN12\_ENA, LIN34\_ENA, RIN12\_ENA and RIN34\_ENA as described in Table 2.

| REGISTER ADDRESS | BIT | LABEL             | DEFAULT | DESCRIPTION   |
|------------------|-----|-------------------|---------|---|
| R2 (02h)         | 7   | LIN34_ENA<br>(rw) | 0b      | LIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled |
|                  | 6   | LIN12_ENA<br>(rw) | 0b      | LIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled |
|                  | 5   | RIN34_ENA<br>(rw) | 0b      | RIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled |
|                  | 4   | RIN12_ENA<br>(rw) | 0b      | RIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled |

**Table 2 Input PGA Enable**

To enable the input PGAs, the reference voltage VMID and the bias current must also be enabled. See "Power Management" for definitions of the associated controls VMID\_MODE and VREF\_ENA.

**MICROPHONE BIAS CONTROL**

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones via an external resistor. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be enabled or disabled using the MICBIAS\_ENA control bit and the voltage can be selected using the MBSEL register bit as detailed in Table 3.

| REGISTER ADDRESS | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|------------------|-----|---------------------|---------|--|
| R1 (01h)         | 4   | MICBIAS_ENA<br>(rw) | 0b      | Microphone Bias<br>0 = OFF (high impedance output)<br>1 = ON         |
| R58 (3Ah)        | 0   | MBSEL               | 0b      | Microphone Bias Voltage Control<br>0 = 0.9 * AVDD<br>1 = 0.65 * AVDD |

**Table 3 Microphone Bias Control**

Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistance must be large enough to limit the MICBIAS current to 3mA.

**MICROPHONE CURRENT DETECT**

A MICBIAS current detect function allows detection of accessories such as headset microphones. When the MICBIAS load current exceeds one of two programmable thresholds, (e.g. short circuit current or normal operating current), an interrupt or GPIO output can be generated. The current detection circuit is enabled by the MCD bit; the current thresholds are selected by the MCDTHR and MCDSCSTH register fields as described in Table 41 - see "General Purpose Input/Output" for a full description of these fields.

### INPUT PGA CONFIGURATION

Each of the four Input PGAs can be configured in single-ended or pseudo-differential mode.

Single-ended microphone operation of an Input PGA is selected by connecting the input source to the inverting PGA input. The non-inverting PGA input must be connected to VMID by setting the appropriate register bits.

For pseudo-differential microphone operation, the inverting and non-inverting PGA inputs are both connected to the input source and not to VMID.

For any line input or other connection not using the Input PGA, the appropriate PGA input should be disconnected from the external pin and connected to VMID.

Register bits LMN1, LMP2, LMN3, LMP4, RMN1, RMP2, RMN3 and RMP4 control connection of the PGA inputs to the device pins as shown in Table 4. The maximum available attenuation on any of these input paths is achieved using these bits to disable the input path to the applicable PGA.

When not enabled as analogue inputs or as General Purpose inputs, the input pins can be biased to VREF via a 1k $\Omega$  resistor by setting the BUFIOEN bit. See "Pop Suppression Control" for details.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION  |
|------------------|-----|-------|---------|--|
| R40 (28h)        | 7   | LMP4  | 0b      | LIN34 PGA Non-Inverting Input Select<br>0 = LIN4 not connected to PGA<br>1 = LIN4 connected to PGA |
|                  | 6   | LMN3  | 0b      | LIN34 PGA Inverting Input Select<br>0 = LIN3 not connected to PGA<br>1 = LIN3 connected to PGA     |
|                  | 5   | LMP2  | 0b      | LIN12 PGA Non-Inverting Input Select<br>0 = LIN2 not connected to PGA<br>1 = LIN2 connected to PGA |
|                  | 4   | LMN1  | 0b      | LIN12 PGA Inverting Input Select<br>0 = LIN1 not connected to PGA<br>1 = LIN1 connected to PGA     |
|                  | 3   | RMP4  | 0b      | RIN34 PGA Non-Inverting Input Select<br>0 = RIN4 not connected to PGA<br>1 = RIN4 connected to PGA |
|                  | 2   | RMN3  | 0b      | RIN34 PGA Inverting Input Select<br>0 = RIN3 not connected to PGA<br>1 = RIN3 connected to PGA     |
|                  | 1   | RMP2  | 0b      | RIN12 PGA Non-Inverting Input Select<br>0 = RIN2 not connected to PGA<br>1 = RIN2 connected to PGA |
|                  | 0   | RMN1  | 0b      | RIN12 PGA Inverting Input Select<br>0 = RIN1 not connected to PGA<br>1 = RIN1 connected to PGA     |

Table 4 Input PGA Configuration



### INPUT PGA VOLUME CONTROL

Each of the four Input PGAs has an independently controlled gain range of -16.5dB to +30dB in 1.5dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each Input PGA can be independently muted using the PGA mute bits as described in Table 5, with specified mute attenuation achieved by simultaneously disconnecting the corresponding inputs described in Table 4.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK\_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK\_RATE. See "Clocking and Sample Rates" for more information on these fields.

The IPVU bit controls the loading of the input PGA volume data. When IPVU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The LIN12, RIN12, LIN34, RIN34 volume settings are all updated when a 1 is written to IPVU. This makes it possible to update the gain of all input paths simultaneously.

The Input PGA Volume Control register fields are described in Table 5 and Table 6.

| REGISTER ADDRESS | BIT | LABEL          | DEFAULT      | DESCRIPTION  |
|------------------|-----|----------------|--------------|--|
| R24 (18h)        | 8   | IPVU[0]        | N/A          | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34) |
|                  | 7   | LI12MUTE       | 1b           | LIN12 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute  |
|                  | 6   | LI12ZC         | 0b           | LIN12 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only   |
|                  | 4:0 | LIN12VOL [4:0] | 01011b (0dB) | LIN12 Volume<br>(See Table 6 for volume range)   |
| R25 (19h)        | 8   | IPVU[1]        | N/A          | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34) |
|                  | 7   | LI34MUTE       | 1b           | LIN34 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute  |
|                  | 6   | LI34ZC         | 0b           | LIN34 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only   |
|                  | 4:0 | LIN34VOL [4:0] | 01011b (0dB) | LIN34 Volume<br>(See Table 6 for volume range)   |
| R26 (1Ah)        | 8   | IPVU[2]        | N/A          | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34) |
|                  | 7   | RI12MUTE       | 1b           | RIN12 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute  |
|                  | 6   | RI12ZC         | 0b           | RIN12 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only   |

| REGISTER ADDRESS | BIT | LABEL             | DEFAULT         | DESCRIPTION   |
|------------------|-----|-------------------|-----------------|---|
|                  | 4:0 | RIN12VOL<br>[4:0] | 01011b<br>(0dB) | RIN12 Volume<br>(See Table 6 for volume range)  |
| R27 (1Bh)        | 8   | IPVU[3]           | N/A             | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input<br>PGA volumes to be updated<br>simultaneously (LIN12, LIN34, RIN12 and<br>RIN34) |
|                  | 7   | RI34MUTE          | 1b              | RIN34 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute   |
|                  | 6   | RI34ZC            | 0b              | RIN34 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|                  | 4:0 | RIN34VOL<br>[4:0] | 01011b<br>(0dB) | RIN34 Volume<br>(See Table 6 for volume range)  |

Table 5 Input PGA Volume Control

| LIN12VOL[4:0], LIN34VOL[4:0],<br>RIN12VOL[4:0], RIN34VOL[4:0] | VOLUME<br>(dB) |
|---|----------------|
| 00000   | -16.5          |
| 00001   | -15.0          |
| 00010   | -13.5          |
| 00011   | -12.0          |
| 00100   | -10.5          |
| 00101   | -9.0           |
| 00110   | -7.5           |
| 00111   | -6.0           |
| 01000   | -4.5           |
| 01001   | -3.0           |
| 01010   | -1.5           |
| 01011   | 0              |
| 01100   | +1.5           |
| 01101   | +3.0           |
| 01110   | +4.5           |
| 01111   | +6.0           |
| 10000   | +7.5           |
| 10001   | +9.0           |
| 10010   | +10.5          |
| 10011   | +12.0          |
| 10100   | +13.5          |
| 10101   | +15.0          |
| 10110   | +16.5          |
| 10111   | +18.0          |
| 11000   | +19.5          |
| 11001   | +21.0          |
| 11010   | +22.5          |
| 11011   | +24.0          |
| 11100   | +25.5          |
| 11101   | +27.0          |
| 11110   | +28.5          |
| 11111   | +30.0          |

Table 6 Input PGA Volume Range

**INPUT MIXER ENABLE**

The WM8959 has two analogue input mixers which allow the Input PGAs and Line Inputs to be combined in a number of ways and fed to the Output Mixers.

The input mixers INMIXL and INMIXR are enabled by the AINL\_ENA and AINR\_ENA register bits, as described in Table 7. These control bits also enable the Input Multiplexers and Differential Input drivers, described in the following section.

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|------------------|-----|------------------|---------|---|
| R2 (02h)         | 9   | AINL_ENA<br>(rw) | 0b      | Left Input Path Enable<br>(Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX)<br>0 = Input Path disabled<br>1 = Input Path enabled  |
|                  | 8   | AINR_ENA<br>(rw) | 0b      | Right Input Path Enable<br>(Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX)<br>0 = Input Path disabled<br>1 = Input Path enabled |

**Table 7 Input Mixer Enable**

**INPUT MIXER CONFIGURATION**

The left and right channel input multiplexers AINLMUX and AINRMUX select one of three input sources for the Left and Right channels independently. The three input sources are as follows:

1. INMIXL or INMIXR output (a combination of Input PGAs and line inputs).
2. RXVOICE (a differential to single-ended conversion of RXP and RXN inputs).
3. DIFFINL or DIFFINR output (a differential to single-ended conversion of two Input PGAs).

The input source for the multiplexers is controlled by register bits AINLMODE and AINRMODE as described in Table 8.

| REGISTER ADDRESS | BIT | LABEL             | DEFAULT | DESCRIPTION  |
|------------------|-----|-------------------|---------|--|
| R39 (27h)        | 3:2 | AINLMODE<br>[1:0] | 00b     | AINLMUX Input Source<br>00 = INMIXL (Left Input Mixer)<br>01 = RXVOICE (RXP - RXN)<br>10 = DIFFINL (LIN12 PGA - LIN34 PGA)<br>11 = (Reserved)  |
|                  | 1:0 | AINRMODE<br>[1:0] | 00b     | AINRMUX Input Source<br>00 = INMIXR (Right Input Mixer)<br>01 = RXVOICE (RXP - RXN)<br>10 = DIFFINR (RIN12 PGA - RIN34 PGA)<br>11 = (Reserved) |

**Table 8 Input Mixer Configuration**

The Input Mixer configuration is described for each of the three modes in the following sections. Note that the Left and Right multiplexer (mode) settings can be set independently.

In Mixer Mode (AINLMODE=00, AINRMODE=00), adjustable gain control is available on the input mixers INMIXL and INMIXR for all available input signals (PGA outputs, line inputs and record paths). This configuration is illustrated in Figure 24. The applicable register settings are shown in Table 9.

| CONFIGURATION                                   | REGISTER SETTINGS   |   |
|---|---|---|
| Left Channel Mixer Mode<br>(INMIXL to AINLMUX)  | 1. Select Mixer Mode  | AINLMODE = 00   |
|   | 2. Enable input paths as required<br><br>(see Table 5 and Table 12 for full definitions of the applicable settings listed here) | L12MNB, L12MNBST<br>LIN12VOL, LIN12MUTE<br>L34MNB, L34MNBST<br>LIN34VOL, LIN34MUTE<br>LI2BVOL |
| Right Channel Mixer Mode<br>(INMIXR to AINRMUX) | 1. Select Mixer Mode  | AINRMODE = 00   |
|   | 2. Enable input paths as required<br><br>(see Table 5 and Table 13 for full definitions of the applicable settings listed here) | R12MNB, R12MNBST<br>RIN12VOL, RIN12MUTE<br>R34MNB, R34MNBST<br>RIN34VOL, RIN34MUTE<br>RI2BVOL |

Table 9 Mixer Mode Register Settings

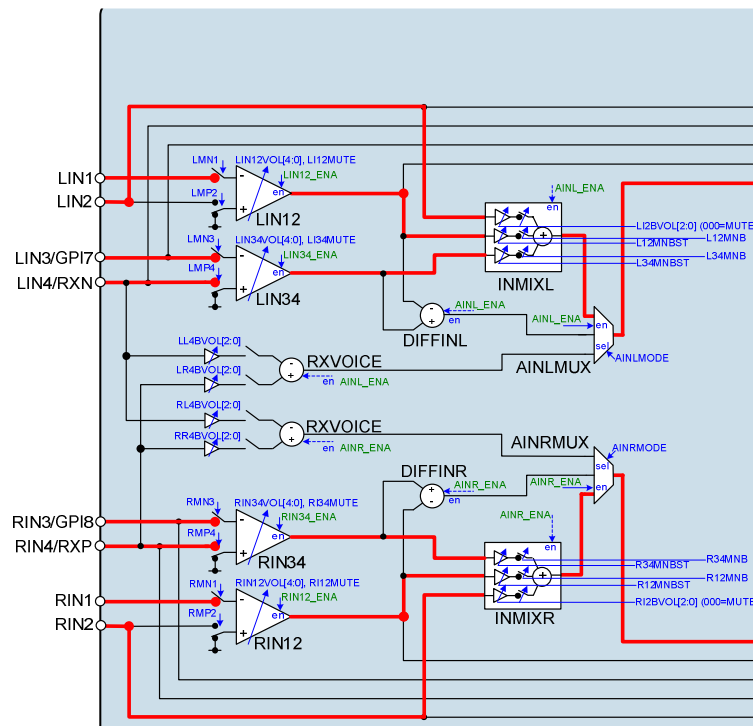


Figure 24 Mixer Mode Signal Paths

In Rx Voice Mode (AINLMODE=01, AINRMODE=01), adjustable gain control is available for the RXVOICE output by use of the LR4BVOL[2:0] and LL4BVOL[2:0] register fields on the left channel and by RL4BVOL[2:0] and RR4BVOL[2:0] on the right channel. Both Volume fields for the desired channel(s) must be be set to the same value for true Differential input characteristics. This configuration is illustrated in Figure 25. The applicable register settings are shown in Table 10.

| CONFIGURATION                                       | REGISTER SETTINGS  |                    |
|---|--|--------------------|
| Left Channel Rx Voice Mode<br>(RXVOICE to AINLMUX)  | 1. Select Rx Voice Mode  | AINLMODE = 01      |
|   | 2. Enable Rx Voice input as required<br>Important: These two register fields must be set to the same value. See Table 12 for full definitions of these fields. | LL4BVOL<br>LR4BVOL |
| Right Channel Rx Voice Mode<br>(RXVOICE to AINRMUX) | 1. Select Rx Voice Mode  | AINRMODE = 01      |
|   | 2. Enable Rx Voice input as required<br>Important: These two register fields must be set to the same value. See Table 13 for full definitions of these fields. | RL4BVOL<br>RR4BVOL |

Table 10 RxVoice Mode Register Settings

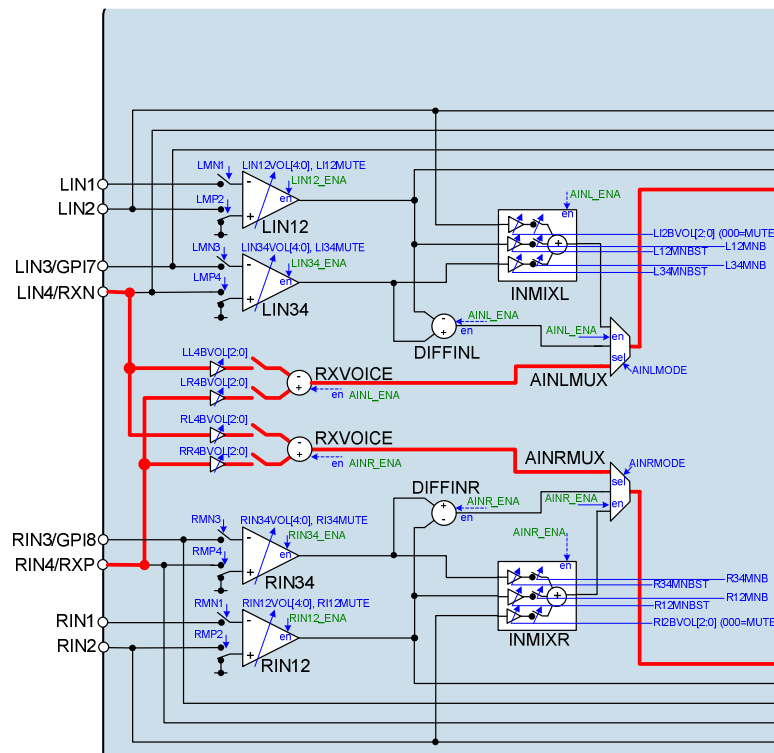


Figure 25 RxVoice Mode Signal Paths

In Differential Mode (AINLMODE=10, AINRMODE=10), no additional volume control is available in the input signal path, but the Input PGA volume control can be used to adjust the signal level as with other modes. Both PGAs on the desired channel(s) must be enabled, and the PGA volumes of each set to the same value for true Differential input characteristics. The PGA Output (LIN12 or RIN12) to Mixer (INMIXL or INMIXR) path must also be enabled on the desired channel(s) by use of register bit L12MNB or R12MNB. This configuration is illustrated in Figure 26. The applicable register settings are shown in Table 11.

| CONFIGURATION   | REGISTER SETTINGS   |  |
|---|---|--|
| Left Channel Differential Mode<br>(DIFFINL to AINLMUX)  | 1. Select Differential Mode   | AINLMODE = 10                              |
|   | 2. Enable LIN12 input path  | L12MNB = 1                                 |
|   | 3. Set channel volume as required. Important: The LIN12 and LIN34 volume and mute settings must be set to the same value. See Table 5 for full definitions of these fields. | LIN12VOL, LIN12MUTE<br>LIN34VOL, LIN34MUTE |
| Right Channel Differential Mode<br>(DIFFINR to AINRMUX) | 1. Select Differential Mode   | AINRMODE = 10                              |
|   | 2. Enable RIN12 input path  | R12MNB = 1                                 |
|   | 3. Set channel volume as required. Important: The RIN12 and RIN34 volume and mute settings must be set to the same value. See Table 5 for full definitions of these fields. | RIN12VOL, RIN12MUTE<br>RIN34VOL, RIN34MUTE |

Table 11 Differential Mode Register Settings

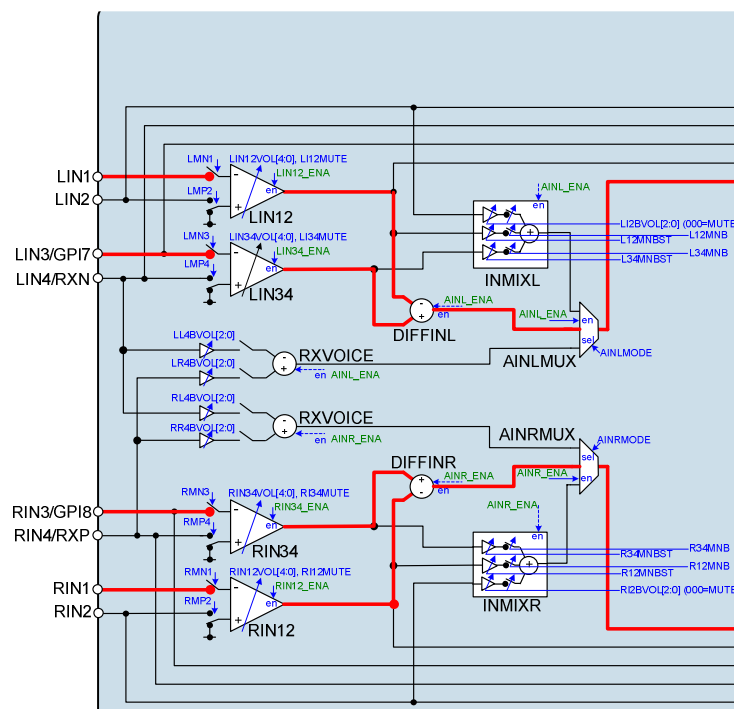


Figure 26 Differential Mode Signal Paths

**INPUT MIXER VOLUME CONTROL**

The Input Mixer volume controls are described in Table 12 for the Left Channel and Table 13 for the Right Channel. The Input PGA levels may be set to Mute, 0dB or 30dB boost. The other gain controls provide adjustment from -12dB to +6dB in 3dB steps.

To prevent pop noise it is recommended that gain and mute controls for the input mixers are not modified while the signal paths are active. If volume control is required on the input signal path it is recommended that the input PGA volume controls are used instead of the input mixer gain registers.

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT        | DESCRIPTION  |
|------------------|-----|------------------|----------------|--|
| R41 (29h)        | 8   | L34MNB           | 0b             | LIN34 PGA Output to INMIXL Mute<br>0 = Mute<br>1 = Un-Mute   |
|                  | 7   | L34MNBST         | 0b             | LIN34 PGA Output to INMIXL Gain<br>0 = 0dB<br>1 = +30dB  |
|                  | 5   | L12MNB           | 0b             | LIN12 PGA Output to INMIXL Mute<br>0 = Mute<br>1 = Un-Mute   |
|                  | 4   | L12MNBST         | 0b             | LIN12 PGA Output to INMIXL Gain<br>0 = 0dB<br>1 = +30dB  |
| R43 (2Bh)        | 8:6 | LI2BVOL<br>[2:0] | 000b<br>(Mute) | LIN2 Pin to INMIXL Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB   |
|                  | 5:3 | LR4BVOL<br>[2:0] | 000b<br>(Mute) | RXVOICE to AINLMUX Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB   |
|                  | 2:0 | LL4BVOL<br>[2:0] | 000b<br>(Mute) | RXVOICE to INMIXL Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB<br><br>Note - LR4BVOL must be set to the same value as LL4BVOL when AINLMODE=01. |

**Table 12 Left Input Mixer Volume Control**



| REGISTER ADDRESS | BIT | LABEL            | DEFAULT        | DESCRIPTION  |
|------------------|-----|------------------|----------------|--|
| R42 (2A)         | 8   | R34MNB           | 0b             | RIN34 PGA Output to INMIXR Mute<br>0 = Mute<br>1 = Un-Mute   |
|                  | 7   | R34MNBST         | 0b             | RIN34 PGA Output to INMIXR Gain<br>0 = 0dB<br>1 = +30dB  |
|                  | 5   | R12MNB           | 0b             | RIN12 PGA Output to INMIXR Mute<br>0 = Mute<br>1 = Un-Mute   |
|                  | 4   | R12MNBST         | 0b             | RIN12 PGA Output to INMIXR Gain<br>0 = 0dB<br>1 = +30dB  |
| R44 (2Ch)        | 8:6 | RI2BVOL<br>[2:0] | 000b<br>(Mute) | RIN2 Pin to INMIXR Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB   |
|                  | 5:3 | RL4BVOL<br>[2:0] | 000b<br>(Mute) | RXVOICE to AINRMUX Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB   |
|                  | 2:0 | RR4BVOL<br>[2:0] | 000b<br>(Mute) | RXVOICE to INMIXR Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB<br>Note - RL4BVOL must be set to the same value as RR4BVOL when AINRMODE=01. |

Table 13 Right Input Mixer Volume Control

DIGITAL INPUT PATH

The DAC input data can be manipulated in various ways to support a range of different usage modes. Data from either of the digital audio interface channels can be routed to either the left or the right DAC. Mono mixing and digital volume control is also possible. See "Digital Audio Interface" for more information on the audio interface.

DIGITAL MIXING PATHS

Figure 27 shows the digital mixing paths available in the WM8959 digital core.

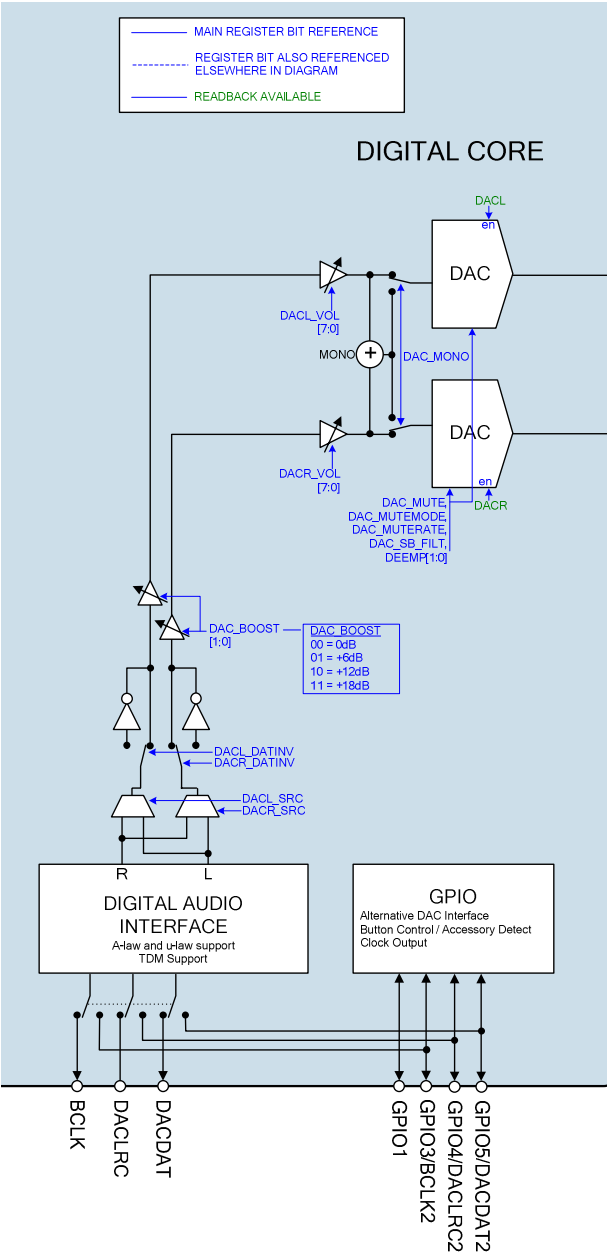


Figure 27 Digital Mixing Paths

The input data source for each DAC can be changed under software control using register bits DACL\_SRC and DACR\_SRC. The polarity of each DAC input may also be modified using register bits DACL\_DATINV and DACR\_DATINV. These register bits are described in Table 14.

| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION   |
|------------------|-----|-------------|---------|---|
| R5 (05h)         | 15  | DACL_SRC    | 0b      | Left DAC Data Source Select<br>0 = Left DAC outputs left channel data<br>1 = Left DAC outputs right channel data    |
|                  | 14  | DACR_SRC    | 1b      | Right DAC Data Source Select<br>0 = Right DAC outputs left channel data<br>1 = Right DAC outputs right channel data |
| R10 (0Ah)        | 1   | DACL_DATINV | 0b      | Left DAC Invert<br>0 = Left DAC output not inverted<br>1 = Left DAC output inverted                                 |
|                  | 0   | DACR_DATINV | 0b      | Right DAC Invert<br>0 = Right DAC output not inverted<br>1 = Right DAC output inverted                              |

**Table 14 DAC Routing and Control**

#### DAC INTERFACE VOLUME BOOST

A digital gain function is available at the audio interface to boost the DAC volume when a small signal is received on DACDAT. This is controlled using register bits DAC\_BOOST[1:0]. To prevent clipping at the DAC input, this function should not be used when the boosted DAC data is expected to be greater than 0dBFS.

| REGISTER ADDRESS | BIT   | LABEL              | DEFAULT | DESCRIPTION   |
|------------------|-------|--------------------|---------|---|
| R5 (05h)         | 11:10 | DAC_BOOST<br>[1:0] | 00b     | DAC Input Volume Boost<br>00 = 0dB<br>01 = +6dB (Input data must not exceed -6dBFS)<br>10 = +12dB (Input data must not exceed -12dBFS)<br>11 = +18dB (Input data must not exceed -18dBFS) |

**Table 15 DAC Interface Volume Boost**

## DIGITAL TO ANALOGUE CONVERTER (DAC)

The WM8959 DACs receive digital input data from the DACDAT pin. The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The analogue outputs from the DACs can then be mixed with other analogue inputs using the output mixers LOMIX, ROMIX and the speaker output mixer SPKMIX.

The DACs are enabled by the DACL\_ENA and DACR\_ENA register bits.

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|------------------|-----|------------------|---------|---|
| R3 (03h)         | 1   | DACL_ENA<br>(rw) | 0b      | Left DAC Enable<br>0 = DAC disabled<br>1 = DAC enabled  |
|                  | 0   | DACR_ENA<br>(rw) | 0b      | Right DAC Enable<br>0 = DAC disabled<br>1 = DAC enabled |

**Table 16 DAC Enable Control**

### DAC DIGITAL VOLUME CONTROL

The output level of each DAC can be controlled digitally over a range from -71.625dB to 0dB in 0.375dB steps. The level of attenuation for an eight-bit code X is given by:

$$0.375 \times (X-192) \text{ dB for } 1 \leq X \leq 192; \quad \text{MUTE for } X = 0 \quad 0\text{dB for } 192 \leq X \leq 255$$

The DAC\_VU bit controls the loading of digital volume control data. When DAC\_VU is set to 0, the DACL\_VOL or DACR\_VOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC\_VU. This makes it possible to update the gain of both channels simultaneously.

| REGISTER ADDRESS | BIT | LABEL             | DEFAULT             | DESCRIPTION  |
|------------------|-----|-------------------|---------------------|--|
| R11 (0Bh)        | 8   | DAC_VU            | N/A                 | DAC Volume Update<br>Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously |
|                  | 7:0 | DACL_VOL<br>[7:0] | 1100_0000b<br>(0dB) | Left DAC Digital Volume<br>(See Table 18 for volume range)   |
| R12 (0Ch)        | 8   | DAC_VU            | N/A                 | DAC Volume Update<br>Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously |
|                  | 7:0 | DACR_VOL<br>[7:0] | 1100_0000b<br>(0dB) | Right DAC Digital Volume<br>(See Table 18 for volume range)  |

**Table 17 DAC Digital Volume Control**

Pre-Production

**WM8959**

| DACL_VOL or<br>DACR_VOL | Volume (dB) | DACL_VOL or<br>DACR_VOL | Volume (dB) | DACL_VOL or<br>DACR_VOL | Volume (dB) | DACL_VOL or<br>DACR_VOL | Volume (dB) |
|-------------------------|-------------|-------------------------|-------------|-------------------------|-------------|-------------------------|-------------|
| 0h                      | MUTE        | 40h                     | -48.000     | 80h                     | -24.000     | C0h                     | 0.000       |
| 1h                      | -71.625     | 41h                     | -47.625     | 81h                     | -23.625     | C1h                     | 0.000       |
| 2h                      | -71.250     | 42h                     | -47.250     | 82h                     | -23.250     | C2h                     | 0.000       |
| 3h                      | -70.875     | 43h                     | -46.875     | 83h                     | -22.875     | C3h                     | 0.000       |
| 4h                      | -70.500     | 44h                     | -46.500     | 84h                     | -22.500     | C4h                     | 0.000       |
| 5h                      | -70.125     | 45h                     | -46.125     | 85h                     | -22.125     | C5h                     | 0.000       |
| 6h                      | -69.750     | 46h                     | -45.750     | 86h                     | -21.750     | C6h                     | 0.000       |
| 7h                      | -69.375     | 47h                     | -45.375     | 87h                     | -21.375     | C7h                     | 0.000       |
| 8h                      | -69.000     | 48h                     | -45.000     | 88h                     | -21.000     | C8h                     | 0.000       |
| 9h                      | -68.625     | 49h                     | -44.625     | 89h                     | -20.625     | C9h                     | 0.000       |
| Ah                      | -68.250     | 4Ah                     | -44.250     | 8Ah                     | -20.250     | CAh                     | 0.000       |
| Bh                      | -67.875     | 4Bh                     | -43.875     | 8Bh                     | -19.875     | CBh                     | 0.000       |
| Ch                      | -67.500     | 4Ch                     | -43.500     | 8Ch                     | -19.500     | CCh                     | 0.000       |
| Dh                      | -67.125     | 4Dh                     | -43.125     | 8Dh                     | -19.125     | CDh                     | 0.000       |
| Eh                      | -66.750     | 4Eh                     | -42.750     | 8Eh                     | -18.750     | CEh                     | 0.000       |
| Fh                      | -66.375     | 4Fh                     | -42.375     | 8Fh                     | -18.375     | CFh                     | 0.000       |
| 10h                     | -66.000     | 50h                     | -42.000     | 90h                     | -18.000     | D0h                     | 0.000       |
| 11h                     | -65.625     | 51h                     | -41.625     | 91h                     | -17.625     | D1h                     | 0.000       |
| 12h                     | -65.250     | 52h                     | -41.250     | 92h                     | -17.250     | D2h                     | 0.000       |
| 13h                     | -64.875     | 53h                     | -40.875     | 93h                     | -16.875     | D3h                     | 0.000       |
| 14h                     | -64.500     | 54h                     | -40.500     | 94h                     | -16.500     | D4h                     | 0.000       |
| 15h                     | -64.125     | 55h                     | -40.125     | 95h                     | -16.125     | D5h                     | 0.000       |
| 16h                     | -63.750     | 56h                     | -39.750     | 96h                     | -15.750     | D6h                     | 0.000       |
| 17h                     | -63.375     | 57h                     | -39.375     | 97h                     | -15.375     | D7h                     | 0.000       |
| 18h                     | -63.000     | 58h                     | -39.000     | 98h                     | -15.000     | D8h                     | 0.000       |
| 19h                     | -62.625     | 59h                     | -38.625     | 99h                     | -14.625     | D9h                     | 0.000       |
| 1Ah                     | -62.250     | 5Ah                     | -38.250     | 9Ah                     | -14.250     | DAh                     | 0.000       |
| 1Bh                     | -61.875     | 5Bh                     | -37.875     | 9Bh                     | -13.875     | DBh                     | 0.000       |
| 1Ch                     | -61.500     | 5Ch                     | -37.500     | 9Ch                     | -13.500     | DCh                     | 0.000       |
| 1Dh                     | -61.125     | 5Dh                     | -37.125     | 9Dh                     | -13.125     | DDh                     | 0.000       |
| 1Eh                     | -60.750     | 5Eh                     | -36.750     | 9Eh                     | -12.750     | DEh                     | 0.000       |
| 1Fh                     | -60.375     | 5Fh                     | -36.375     | 9Fh                     | -12.375     | DFh                     | 0.000       |
| 20h                     | -60.000     | 60h                     | -36.000     | A0h                     | -12.000     | E0h                     | 0.000       |
| 21h                     | -59.625     | 61h                     | -35.625     | A1h                     | -11.625     | E1h                     | 0.000       |
| 22h                     | -59.250     | 62h                     | -35.250     | A2h                     | -11.250     | E2h                     | 0.000       |
| 23h                     | -58.875     | 63h                     | -34.875     | A3h                     | -10.875     | E3h                     | 0.000       |
| 24h                     | -58.500     | 64h                     | -34.500     | A4h                     | -10.500     | E4h                     | 0.000       |
| 25h                     | -58.125     | 65h                     | -34.125     | A5h                     | -10.125     | E5h                     | 0.000       |
| 26h                     | -57.750     | 66h                     | -33.750     | A6h                     | -9.750      | E6h                     | 0.000       |
| 27h                     | -57.375     | 67h                     | -33.375     | A7h                     | -9.375      | E7h                     | 0.000       |
| 28h                     | -57.000     | 68h                     | -33.000     | A8h                     | -9.000      | E8h                     | 0.000       |
| 29h                     | -56.625     | 69h                     | -32.625     | A9h                     | -8.625      | E9h                     | 0.000       |
| 2Ah                     | -56.250     | 6Ah                     | -32.250     | AAh                     | -8.250      | EAh                     | 0.000       |
| 2Bh                     | -55.875     | 6Bh                     | -31.875     | ABh                     | -7.875      | EBh                     | 0.000       |
| 2Ch                     | -55.500     | 6Ch                     | -31.500     | ACh                     | -7.500      | ECh                     | 0.000       |
| 2Dh                     | -55.125     | 6Dh                     | -31.125     | ADh                     | -7.125      | EDh                     | 0.000       |
| 2Eh                     | -54.750     | 6Eh                     | -30.750     | AEh                     | -6.750      | EEh                     | 0.000       |
| 2Fh                     | -54.375     | 6Fh                     | -30.375     | AFh                     | -6.375      | EFh                     | 0.000       |
| 30h                     | -54.000     | 70h                     | -30.000     | B0h                     | -6.000      | F0h                     | 0.000       |
| 31h                     | -53.625     | 71h                     | -29.625     | B1h                     | -5.625      | F1h                     | 0.000       |
| 32h                     | -53.250     | 72h                     | -29.250     | B2h                     | -5.250      | F2h                     | 0.000       |
| 33h                     | -52.875     | 73h                     | -28.875     | B3h                     | -4.875      | F3h                     | 0.000       |
| 34h                     | -52.500     | 74h                     | -28.500     | B4h                     | -4.500      | F4h                     | 0.000       |
| 35h                     | -52.125     | 75h                     | -28.125     | B5h                     | -4.125      | F5h                     | 0.000       |
| 36h                     | -51.750     | 76h                     | -27.750     | B6h                     | -3.750      | F6h                     | 0.000       |
| 37h                     | -51.375     | 77h                     | -27.375     | B7h                     | -3.375      | F7h                     | 0.000       |
| 38h                     | -51.000     | 78h                     | -27.000     | B8h                     | -3.000      | F8h                     | 0.000       |
| 39h                     | -50.625     | 79h                     | -26.625     | B9h                     | -2.625      | F9h                     | 0.000       |
| 3Ah                     | -50.250     | 7Ah                     | -26.250     | BAh                     | -2.250      | FAh                     | 0.000       |
| 3Bh                     | -49.875     | 7Bh                     | -25.875     | BBh                     | -1.875      | FBh                     | 0.000       |
| 3Ch                     | -49.500     | 7Ch                     | -25.500     | BCh                     | -1.500      | FCh                     | 0.000       |
| 3Dh                     | -49.125     | 7Dh                     | -25.125     | BDh                     | -1.125      | FDh                     | 0.000       |
| 3Eh                     | -48.750     | 7Eh                     | -24.750     | BEh                     | -0.750      | FEh                     | 0.000       |
| 3Fh                     | -48.375     | 7Fh                     | -24.375     | BFh                     | -0.375      | FFh                     | 0.000       |

Table 18 DAC Digital Volume Range

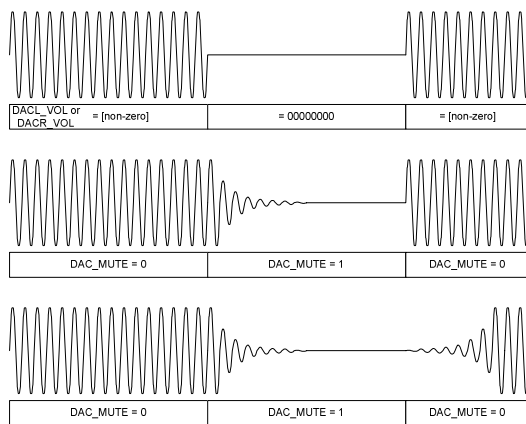
### DAC SOFT MUTE AND SOFT UN-MUTE

The WM8959 has a soft mute function which, when enabled, gradually attenuates the volume of the DAC output. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DAC\_MUTEMODE register bit.

The DAC is soft-muted by default (DAC\_MUTE = 1). To play back an audio signal, this function must first be disabled by setting DAC\_MUTE to 0.

Soft Mute Mode would typically be enabled (DAC\_MUTEMODE = 1) when using DAC\_MUTE during playback of audio data so that when DAC\_MUTE is subsequently disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

Soft Mute Mode would typically be disabled (DAC\_MUTEMODE = 0) when un-muting at the start of a music file, in order that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).



DAC muting and un-muting using volume control bits DACL\_VOL and DACR\_VOL.

DAC muting and un-muting using soft mute bit DAC\_MUTE.

Soft Mute Mode not enabled (DAC\_MUTEMODE = 0).

DAC muting and un-muting using soft mute bit DAC\_MUTE.

Soft Mute Mode enabled (DAC\_MUTEMODE = 1).

Figure 28 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DAC\_MUTERATE bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 19. The ramp rate determines the rate at which the volume will be increased or decreased. The actual ramp time depends on the extent of the difference between the muted and un-muted volume settings.

| REGISTER ADDRESS | BIT | LABEL        | DEFAULT | DESCRIPTION   |
|------------------|-----|--------------|---------|---|
| R10 (0Ah)        | 7   | DAC_MUTERATE | 0b      | DAC Soft Mute Ramp Rate<br>0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k)<br>1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)   |
|                  | 6   | DAC_MUTEMODE | 0b      | DAC Soft Mute Mode<br>0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings<br>1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings |
|                  | 2   | DAC_MUTE     | 1b      | DAC Soft Mute Control<br>0 = DAC Un-mute<br>1 = DAC Mute  |

Table 19 DAC Soft-Mute Control

**DAC MONO MIX**

A DAC digital mono-mix mode can be enabled using the DAC\_MONO register bit. This mono mix will be output on the enabled DACs. To prevent clipping, a -6dB attenuation is automatically applied to the mono mix.

| REGISTER ADDRESS | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|------------------|-----|----------|---------|--|
| R10 (0Ah)        | 9   | DAC_MONO | 0b      | DAC Mono Mix<br>0 = Stereo<br>1 = Mono (Mono mix output on enabled DACs) |

Table 20 DAC Mono Mix

**DAC DE-EMPHASIS**

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz. See "Digital Filter Characteristics" section for details of de-emphasis filter characteristics.

| REGISTER ADDRESS         | BIT | LABEL          | DEFAULT | DESCRIPTION  |
|--------------------------|-----|----------------|---------|--|
| R10 (0Ah)<br>DAC Control | 5:4 | DEEMP<br>[1:0] | 00b     | DAC De-Emphasis Control<br>00 = No de-emphasis<br>01 = 32kHz sample rate<br>10 = 44.1kHz sample rate<br>11 = 48kHz sample rate |

Table 21 DAC De-Emphasis Control

**DAC SLOPING STOPBAND FILTER**

Two DAC filter types are available, selected by the register bit DAC\_SB\_FILTER. When operating at lower sample rates (e.g. during voice communication) it is recommended that the sloping stopband filter type is selected (DAC\_SB\_FILTER=1) to reduce out-of-band noise which can be audible at low DAC sample rates. See "Digital Filter Characteristics" for details of DAC filter characteristics.

| REGISTER ADDRESS         | BIT | LABEL         | DEFAULT | DESCRIPTION  |
|--------------------------|-----|---------------|---------|--|
| R10 (0Ah)<br>DAC Control | 8   | DAC_SB_FILTER | 0b      | Selects DAC filter characteristics<br>0 = Normal mode<br>1 = Sloping stopband mode |

Table 22 DAC Sloping Stopband Filter

### OUTPUT SIGNAL PATH

The WM8959 output routing and mixers provide a high degree of flexibility, allowing operation of many simultaneous signal paths through the device to various analogue outputs. The outputs provide many combinations of headphone, loudspeaker and single-ended line drivers. See "Analogue Outputs" for further details of these outputs.

The WM8959 output signal paths and control registers are illustrated in Figure 29.

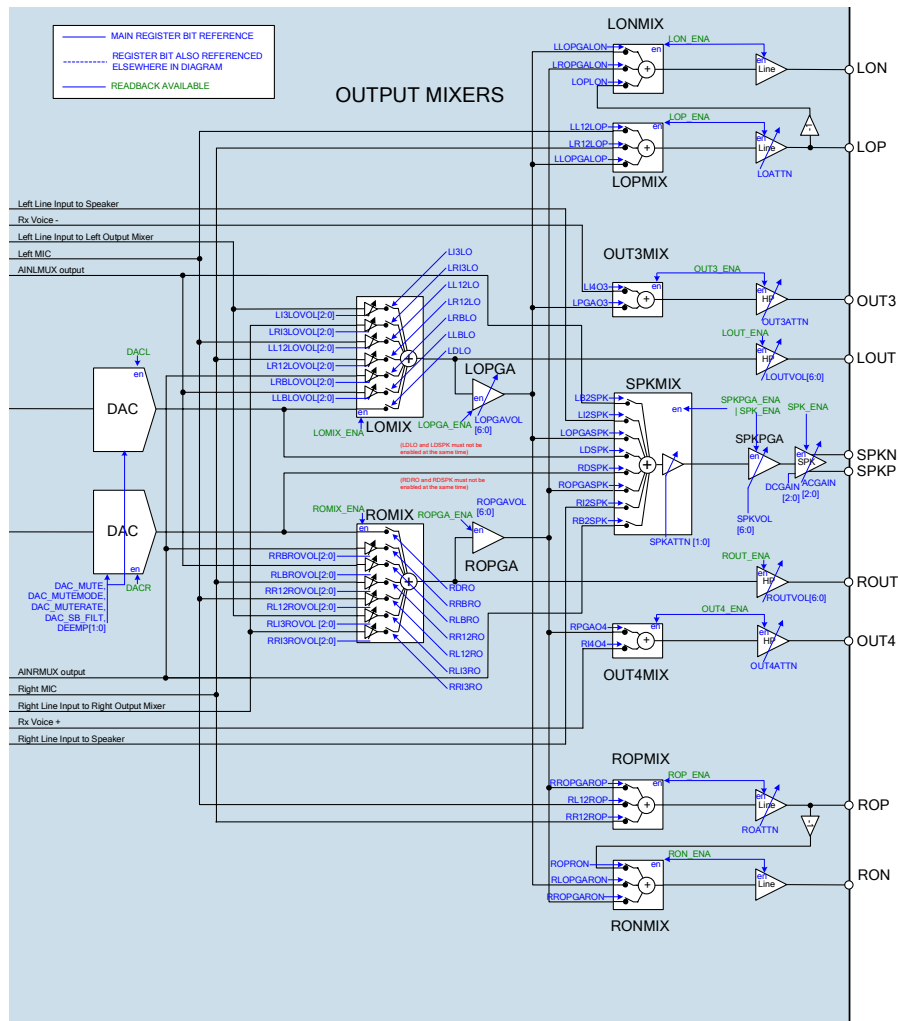


Figure 29 Control Registers for Output Signal Path



**OUTPUT SIGNAL PATHS ENABLE**

The output mixers and drivers can be independently enabled and disabled as described in Table 23.

Note that the headphone outputs LOUT and ROUT have dedicated volume controls. As a result, the output PGAs LOPGA and ROPGA do not need to be enabled to provide volume control for the LOUT and ROUT outputs.

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   |
|------------------|-----|--------------------|---------|---|
| R3 (03h)         | 13  | LON_ENA<br>(rw)    | 0b      | LON Line Out and LONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 12  | LOP_ENA<br>(rw)    | 0b      | LOP Line Out and LOPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 11  | RON_ENA<br>(rw)    | 0b      | RON Line Out and RONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 10  | ROP_ENA<br>(rw)    | 0b      | ROP Line Out and ROPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 8   | SPKPGA_ENA<br>(rw) | 0b      | SPKMIX Mixer and Speaker PGA Enable<br>0 = disabled<br>1 = enabled<br>Note that SPKMIX and SPKPGA are also enabled when SPK_ENA is set. |
|                  | 7   | LOPGA_ENA<br>(rw)  | 0b      | LOPGA Left Volume Control Enable<br>0 = disabled<br>1 = enabled   |
|                  | 6   | ROPGA_ENA<br>(rw)  | 0b      | ROPGA Right Volume Control Enable<br>0 = disabled<br>1 = enabled  |
|                  | 5   | LOMIX_ENA<br>(rw)  | 0b      | LOMIX Left Output Mixer Enable<br>0 = disabled<br>1 = enabled   |
|                  | 4   | ROMIX_ENA<br>(rw)  | 0b      | ROMIX Right Output Mixer Enable<br>0 = disabled<br>1 = enabled  |
| R1 (01h)         | 12  | SPK_ENA<br>(rw)    | 0b      | SPKMIX Mixer, Speaker PGA and Speaker Output Enable<br>0 = disabled<br>1 = enabled  |
|                  | 11  | OUT3_ENA<br>(rw)   | 0b      | OUT3 and OUT3MIX Enable<br>0 = disabled<br>1 = enabled  |
|                  | 10  | OUT4_ENA<br>(rw)   | 0b      | OUT4 and OUT4MIX Enable<br>0 = disabled<br>1 = enabled  |
|                  | 9   | LOUT_ENA<br>(rw)   | 0b      | LOUT (Left Headphone Output) Enable<br>0 = disabled<br>1 = enabled  |
|                  | 8   | ROUT_ENA<br>(rw)   | 0b      | ROUT (Right Headphone Output) Enable<br>0 = disabled<br>1 = enabled   |

**Table 23 Output Signal Paths Enable**

**OUTPUT MIXER CONTROL**

The Output Mixer volume controls are described in Table 24 for the Left Channel and Table 25 for the Right Channel. The gain of each of analogue input paths may be controlled independently in the range described in Table 26. The DAC input levels may be controlled by the DAC digital volume control - see "Digital to Analogue Converter (DAC)" for further details of this control.

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|------------------|-----|--------------------|---------|--|
| R45 (2Dh)        | 5   | LRI3LO             | 0b      | RIN3 to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
| R45 (2Dh)        | 4   | LLI3LO             | 0b      | LIN3 to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
| R49 (31h)        | 8:6 | LRI3LOVOL<br>[2:0] | 000b    | RIN3 to LOMIX Volume<br>(See Table 26 for Volume Range)                                    |
| R47 (2Fh)        | 8:6 | LLI3LOVOL<br>[2:0] | 000b    | LIN3 to LOMIX Volume<br>(See Table 26 for Volume Range)                                    |
| R45 (2Dh)        | 2   | LL12LO             | 0b      | LIN12 PGA Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute                                  |
| R47 (2Fh)        | 2:0 | LL12LOVOL<br>[2:0] | 000b    | LIN12 PGA Output to LOMIX Volume<br>(See Table 26 for Volume Range)                        |
| R45 (2Dh)        | 3   | LR12LO             | 0       | RIN12 PGA Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute                                  |
| R47 (2Fh)        | 5:3 | LR12LOVOL<br>[2:0] | 000b    | RIN12 PGA Output to LOMIX Volume<br>(See Table 26 for Volume Range)                        |
| R45 (2Dh)        | 7   | LRBLO              | 0b      | AINRMUX Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute                                    |
| R49 (31h)        | 5:3 | LRBLOVOL<br>[2:0]  | 000b    | AINRMUX Output to LOMIX Volume<br>(See Table 26 for Volume Range)                          |
| R45 (2Dh)        | 6   | LLBLO              | 0b      | AINLMUX Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute                                    |
| R49 (31h)        | 2:0 | LLBLOVOL<br>[2:0]  | 000b    | AINLMUX Output to LOMIX Volume<br>(See Table 26 for Volume Range)                          |
| R45 (2Dh)        | 0   | LDLO               | 0b      | Left DAC to LOMIX Mute<br>0 = Mute<br>1 = Un-mute<br>Note: LDLO must be muted when LDSPK=1 |

**Table 24 Left Output Mixer (LOMIX) Volume Control**

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|------------------|-----|--------------------|---------|--|
| R46 (2Eh)        | 5   | RLI3RO             | 0b      | LIN3 to ROMIX Mute<br>0 = Mute<br>1 = Un-mute  |
| R46 (2Eh)        | 4   | RRI3RO             | 0b      | RIN3 to ROMIX Mute<br>0 = Mute<br>1 = Un-mute  |
| R50 (32h)        | 8:6 | RLI3ROVOL<br>[2:0] | 000b    | LIN3 to ROMIX Volume<br>(See Table 26 for Volume Range)  |
| R48 (30h)        | 8:6 | RRI3ROVOL<br>[2:0] | 000b    | RIN3 to ROMIX Volume<br>(See Table 26 for Volume Range)  |
| R46 (2Eh)        | 3   | RL12RO             | 0b      | LIN12 PGA Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute                                      |
| R48 (30h)        | 5:3 | RL12ROVOL<br>[2:0] | 000b    | LIN12 PGA Output to ROMIX Volume<br>(See Table 26 for Volume Range)                            |
| R46 (2Eh)        | 2   | RR12RO             | 0b      | RIN12 PGA Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute                                      |
| R48 (30h)        | 2:0 | RR12ROVOL<br>[2:0] | 000b    | RIN12 PGA Output to ROMIX Volume<br>(See Table 26 for Volume Range)                            |
| R46 (2Eh)        | 7   | RLBRO              | 0b      | AINLMUX Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute  |
| R50 (32h)        | 5:3 | RLBROVOL<br>[2:0]  | 000b    | AINLMUX Output to ROMIX Volume<br>(See Table 26 for Volume Range)                              |
| R46 (2Eh)        | 6   | RRBRO              | 0b      | AINRMUX Output to ROMIX<br>0 = Mute<br>1 = Un-mute   |
| R50 (32h)        | 2:0 | RRBROVOL<br>[2:0]  | 000b    | AINRMUX Output to ROMIX Volume<br>(See Table 26 for Volume Range)                              |
| R46 (2Eh)        | 0   | RDRO               | 0b      | Right DAC to ROMIX Mute<br>0 = Mute<br>1 = Un-mute<br>Note: RDRO must be muted when<br>RDSPK=1 |

Table 25 Right Output Mixer (ROMIX) Volume Control

| VOLUME SETTING | VOLUME (dB) |
|----------------|-------------|
| 000            | 0           |
| 001            | -3          |
| 010            | -6          |
| 011            | -9          |
| 100            | -12         |
| 101            | -15         |
| 110            | -18         |
| 111            | -21         |

Table 26 LOMIX and ROMIX Volume Range

### OUTPUT SIGNAL PATH VOLUME CONTROL

The output drivers LOPGA, ROPGA, LOOUT and ROUT can be independently controlled as shown in Table 27 and Table 28.

To minimise pop noise it is recommended that only the LOPGAVOL, ROPGAVOL, LOOUTVOL and ROUTVOL are modified while the output signal path is active. Other gain controls are provided in the output signal path to provide appropriate relative scaling of signals from different sources, and to prevent clipping when multiple signals are mixed. To prevent pop noise, only the gain controls noted above should be modified while playback is active.

To prevent "zipper noise", a zero-cross function is provided on these output paths, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK\_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK\_RATE. See "Clocking and Sample Rates" for more information on these fields.

The OPVU bit controls the loading of the output driver volume data. When OPVU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The LOPGA, ROPGA, LOOUT and ROUT volume settings are all updated when a 1 is written to OPVU. This makes it possible to update the gain of all output paths simultaneously.

Note that the headphone outputs LOOUT and ROUT have dedicated volume controls. As a result, the output PGAs LOPGA and ROPGA do not need to be enabled to provide volume control for the LOOUT and ROUT outputs.

| REGISTER ADDRESS | BIT | LABEL          | DEFAULT    | DESCRIPTION  |
|------------------|-----|----------------|------------|--|
| R32 (20h)        | 8   | OPVU[2]        | N/A        | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOOUTVOL and ROUTVOL volumes simultaneously. |
|                  | 7   | LOPGAZC        | 0b         | LOPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled   |
|                  | 6:0 | LOPGAVOL [6:0] | 79h (0dB)  | LOPGA Volume<br>(See Table 28 for output PGA volume control range)   |
| R33 (21h)        | 8   | OPVU[3]        | N/A        | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOOUTVOL and ROUTVOL volumes simultaneously. |
|                  | 7   | ROPGAZC        | 0b         | ROPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled   |
|                  | 6:0 | ROPGAVOL [6:0] | 79h (0dB)  | ROPGA Volume<br>(See Table 28 for output PGA volume control range)   |
| R28 (1Ch)        | 8   | OPVU[0]        | N/A        | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOOUTVOL and ROUTVOL volumes simultaneously. |
|                  | 7   | LOZC           | 0b         | LOOUT (Left Headphone Output) Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled                       |
|                  | 6:0 | LOOUTVOL [6:0] | 00h (mute) | LOOUT (Left Headphone Output) Volume<br>(See Table 28 for output PGA volume control range)                                 |

| REGISTER ADDRESS | BIT | LABEL         | DEFAULT    | DESCRIPTION  |
|------------------|-----|---------------|------------|--|
| R29 (1Dh)        | 8   | OPVU[1]       | N/A        | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOUVOL and ROUTVOL volumes simultaneously. |
|                  | 7   | ROZC          | 0b         | ROUT (Right Headphone Output) Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled                     |
|                  | 6:0 | ROUTVOL [6:0] | 00h (mute) | ROUT (Right Headphone Output) Volume<br>(See Table 28 for output PGA volume control range)                               |

**Table 27 LOPGA, ROPGA, LOUVOL and ROUT Volume Control**

| LOPGAVOL,<br>ROPGAVOL,<br>LOUTVOL,<br>ROUTVOL or<br>SPKVOL | Volume<br>(dB) | LOPGAVOL,<br>ROPGAVOL,<br>LOUTVOL,<br>ROUTVOL or<br>SPKVOL | Volume<br>(dB) |
|--|----------------|--|----------------|
| 0h   | MUTE           | 40h  | -57            |
| 1h   | MUTE           | 41h  | -56            |
| 2h   | MUTE           | 42h  | -55            |
| 3h   | MUTE           | 43h  | -54            |
| 4h   | MUTE           | 44h  | -53            |
| 5h   | MUTE           | 45h  | -52            |
| 6h   | MUTE           | 46h  | -51            |
| 7h   | MUTE           | 47h  | -50            |
| 8h   | MUTE           | 48h  | -49            |
| 9h   | MUTE           | 49h  | -48            |
| Ah   | MUTE           | 4Ah  | -47            |
| Bh   | MUTE           | 4Bh  | -46            |
| Ch   | MUTE           | 4Ch  | -45            |
| Dh   | MUTE           | 4Dh  | -44            |
| Eh   | MUTE           | 4Eh  | -43            |
| Fh   | MUTE           | 4Fh  | -42            |
| 10h  | MUTE           | 50h  | -41            |
| 11h  | MUTE           | 51h  | -40            |
| 12h  | MUTE           | 52h  | -39            |
| 13h  | MUTE           | 53h  | -38            |
| 14h  | MUTE           | 54h  | -37            |
| 15h  | MUTE           | 55h  | -36            |
| 16h  | MUTE           | 56h  | -35            |
| 17h  | MUTE           | 57h  | -34            |
| 18h  | MUTE           | 58h  | -33            |
| 19h  | MUTE           | 59h  | -32            |
| 1Ah  | MUTE           | 5Ah  | -31            |
| 1Bh  | MUTE           | 5Bh  | -30            |
| 1Ch  | MUTE           | 5Ch  | -29            |
| 1Dh  | MUTE           | 5Dh  | -28            |
| 1Eh  | MUTE           | 5Eh  | -27            |
| 1Fh  | MUTE           | 5Fh  | -26            |
| 20h  | MUTE           | 60h  | -25            |
| 21h  | MUTE           | 61h  | -24            |
| 22h  | MUTE           | 62h  | -23            |
| 23h  | MUTE           | 63h  | -22            |
| 24h  | MUTE           | 64h  | -21            |
| 25h  | MUTE           | 65h  | -20            |
| 26h  | MUTE           | 66h  | -19            |
| 27h  | MUTE           | 67h  | -18            |
| 28h  | MUTE           | 68h  | -17            |
| 29h  | MUTE           | 69h  | -16            |
| 2Ah  | MUTE           | 6Ah  | -15            |
| 2Bh  | MUTE           | 6Bh  | -14            |
| 2Ch  | MUTE           | 6Ch  | -13            |
| 2Dh  | MUTE           | 6Dh  | -12            |
| 2Eh  | MUTE           | 6Eh  | -11            |
| 2Fh  | MUTE           | 6Fh  | -10            |
| 30h  | -73            | 70h  | -9             |
| 31h  | -72            | 71h  | -8             |
| 32h  | -71            | 72h  | -7             |
| 33h  | -70            | 73h  | -6             |
| 34h  | -69            | 74h  | -5             |
| 35h  | -68            | 75h  | -4             |
| 36h  | -67            | 76h  | -3             |
| 37h  | -66            | 77h  | -2             |
| 38h  | -65            | 78h  | -1             |
| 39h  | -64            | 79h  | 0              |
| 3Ah  | -63            | 7Ah  | 1              |
| 3Bh  | -62            | 7Bh  | 2              |
| 3Ch  | -61            | 7Ch  | 3              |
| 3Dh  | -60            | 7Dh  | 4              |
| 3Eh  | -59            | 7Eh  | 5              |
| 3Fh  | -58            | 7Fh  | 6              |

Table 28 LOPGA, ROPGA, LOUT, ROUT and SPKVOL Volume Range

The speaker mixer SPKMIX, the speaker PGA SPKPGA and the outputs SPKN and SPKP are controlled as described in Table 29. Care should be taken to avoid clipping when enabling more than one path to the speaker mixer.

Register bits SPKATTN control the speaker output attenuation and can be used to avoid clipping when more than one full scale signal is input to the mixer. Fine adjustment of the speaker output can be made using the SPKVOL register field.

To prevent "zipper noise" when adjusting the SPKVOL, a zero-cross function is provided so that, when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOCLK\_ENA register bit), the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout period is set by TOCLK\_RATE. See "Clocking and Sample Rates" for more information on these fields.

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT      | DESCRIPTION  |
|------------------|-----|------------------|--------------|--|
| R54 (36h)        | 7   | LB2SPK           | 0b           | AINLMUX Output to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                  | 6   | RB2SPK           | 0b           | AINRMUX Output to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                  | 5   | LI2SPK           | 0b           | LIN2 to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                  | 4   | RI2SPK           | 0b           | RIN2 to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                  | 3   | LOPGASPK         | 0b           | LOPGA to SPKMIX<br>0 = Mute<br>1 = Un-mute   |
|                  | 2   | ROPGASPK         | 0b           | ROPGA to SPKMIX<br>0 = Mute<br>1 = Un-mute   |
|                  | 1   | LDSPK            | 0b           | Left DAC to SPKMIX<br>0 = Mute<br>1 = Un-mute<br>Note: LDSPK must be muted when LDLO=1         |
|                  | 0   | RDSPK            | 0b           | Right DAC to SPKMIX<br>0 = Mute<br>1 = Un-mute<br>Note: RDSPK must be muted when RDRO=1        |
| R34 (22h)        | 1:0 | SPKATTN<br>[1:0] | 11b          | Speaker Output Attenuation (SPKN and SPKP)<br>00 = 0dB<br>01 = -6dB<br>10 = -12dB<br>11 = mute |
| R38 (26h)        | 7   | SPKZC            | 0b           | SPKPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled                  |
|                  | 6:0 | SPKVOL<br>[6:0]  | 79h<br>(0dB) | SPKPGA Volume<br>(see Table 28 for SPKPGA volume control range)                                |

Table 29 Speaker Output Volume Control

The output mixers OUT3MIX and OUT4MIX and their outputs OUT3 and OUT4 are controlled as described in Table 30. Care should be taken to avoid clipping when enabling more than one path to OUT3 or OUT4. The OUT3ATTN and OUT4ATTN attenuation controls can be used to prevent clipping when more than one full scale signal is input to the mixers.

| REGISTER ADDRESS | BIT | LABEL    | DEFAULT | DESCRIPTION  |
|------------------|-----|----------|---------|--|
| R31 (1Fh)        | 5   | OUT3MUTE | 1b      | OUT3 Mute<br>0 = Un-mute<br>1 = Mute               |
|                  | 4   | OUT3ATTN | 0b      | OUT3 Attenuation<br>0 = 0dB<br>1 = -6dB            |
|                  | 1   | OUT4MUTE | 1b      | OUT4 Mute<br>0 = Un-mute<br>1 = Mute               |
|                  | 0   | OUT4ATTN | 0b      | OUT4 Attenuation<br>0 = 0dB<br>1 = -6dB            |
| R51 (33h)        | 5   | LI4O3    | 0b      | LIN4/RXN Pin to OUT3MIX<br>0 = Mute<br>1 = Un-mute |
|                  | 4   | LPGA03   | 0b      | LOPGA to OUT3MIX<br>0 = Mute<br>1 = Un-mute        |
|                  | 1   | RI4O4    | 0b      | RIN4/RXP Pin to OUT4MIX<br>0 = Mute<br>1 = Un-mute |
|                  | 0   | RPGA04   | 0b      | ROPGA to OUT4MIX<br>0 = Mute<br>1 = Un-mute        |

Table 30 OUT3 and OUT4 Volume Control



The output mixers LOPMIX and LONMIX and their outputs LOP and LON are controlled as described in Table 31. Care should be taken to avoid clipping when enabling more than one path to LOP or LON. The LOATTN attenuation control can be used to prevent clipping when more than one full scale signal is input to the LOP mixer.

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|------------------|-----|-----------|---------|--|
| R30 (1Eh)        | 6   | LONMUTE   | 1b      | LON Line Output Mute<br>0 = Un-mute<br>1 = Mute          |
|                  | 5   | LOPMUTE   | 1b      | LOP Line Output Mute<br>0 = Un-mute<br>1 = Mute          |
|                  | 4   | LOATTN    | 0b      | LOP Attenuation<br>0 = 0dB<br>1 = -6dB                   |
| R52 (34h)        | 6   | LLOPGALON | 0b      | LOPGA to LONMIX<br>0 = Mute<br>1 = Un-mute               |
|                  | 5   | LROPGALON | 0b      | ROPGA to LONMIX<br>0 = Mute<br>1 = Un-mute               |
|                  | 4   | LOPLON    | 0b      | Inverted LOP Output to LONMIX<br>0 = Mute<br>1 = Un-mute |
|                  | 2   | LR12LOP   | 0b      | RIN12 PGA Output to LOPMIX<br>0 = Mute<br>1 = Un-mute    |
|                  | 1   | LL12LOP   | 0b      | LIN12 PGA Output to LOPMIX<br>0 = Mute<br>1 = Un-mute    |
|                  | 0   | LLOPGALOP | 0b      | LOPGA to LOPMIX<br>0 = Mute<br>1 = Un-mute               |

**Table 31 LOP and LON Volume Control**

The output mixers ROPMIX and RONMIX and their outputs ROP and RON are controlled as described in Table 32. Care should be taken to avoid clipping when enabling more than one path to ROP or RON. The ROATTN attenuation control can be used to prevent clipping when more than one full scale signal is input to the ROP mixer.

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|------------------|-----|-----------|---------|--|
| R30 (1Eh)        | 2   | RONMUTE   | 1b      | RON Line Output Mute<br>0 = Un-mute<br>1 = Mute          |
|                  | 1   | ROPMUTE   | 1b      | ROP Line Output Mute<br>0 = Un-mute<br>1 = Mute          |
|                  | 0   | ROATTN    | 0b      | ROP Attenuation<br>0 = 0dB<br>1 = -6dB                   |
| R53 (35h)        | 6   | RROPGARON | 0b      | ROPGA to RONMIX<br>0 = Mute<br>1 = Un-mute               |
|                  | 5   | RLOPGARON | 0b      | LOPGA to RONMIX<br>0 = Mute<br>1 = Un-mute               |
|                  | 4   | ROPRON    | 0b      | Inverted ROP Output to RONMIX<br>0 = Mute<br>1 = Un-mute |
|                  | 2   | RL12ROP   | 0b      | LIN12 PGA Output to ROPMIX<br>0 = Mute<br>1 = Un-mute    |
|                  | 1   | RR12ROP   | 0b      | RIN12 PGA Output to ROPMIX<br>0 = Mute<br>1 = Un-mute    |
|                  | 0   | RROPGAROP | 0b      | ROPGA to ROPMIX<br>0 = Mute<br>1 = Un-mute               |

Table 32 ROP and RON Volume Control

## ANALOGUE OUTPUTS

The speaker, headphone and line outputs are highly configurable and may be used in many different ways.

### SPEAKER OUTPUT CONFIGURATIONS

The speaker outputs SPKP and SPKN are driven by the speaker mixer SPKMIX, and speaker volume control SPKPGA, which can output a mix that is any combination of the following signals:

- Left DAC and Right DAC outputs
- LOMIX and ROMIX outputs via volume controls LOPGA and ROPGA
- Line inputs LIN2 and RIN2
- Output from left and right input mixers (AINLMUX & AINRMUX)

The speaker mixer is controlled as described under "Output Signal Path". The speaker mixer output can be attenuated to avoid clipping when mixing multiple signal inputs. Fine adjustment of the speaker output can be made by the speaker volume control SPKPGA.

The speaker outputs SPKP and SPKN operate in a BTL configuration in Class AB and Class D amplifier modes. The mode is selected by register bit CDMODE. The outputs are capable of driving 1W into an 8Ω BTL load (or 500mW in class AB mode for thermal reasons) at room temperature. For performance at higher temperatures, see **Error! Reference source not found.** in the "Recommended Operating Conditions" section. Ultra-low leakage and high PSRR allow the speaker supply SPKVDD to be directly connected to a lithium battery.

Six levels of AC and DC signal boost are provided in order to deliver maximum output power for many commonly-used SPKVDD/AVDD combinations. These boost options are available in both Class AB and Class D modes. The AC and DC gain levels from 1.0x to 1.8x are selected using register bits ACGAIN and DCGAIN. To prevent pop noise, DCGAIN and ACGAIN should not be modified while the speaker outputs are enabled.

Note that an appropriate SPKVDD supply voltage must be provided to prevent waveform clipping when speaker boost is used.

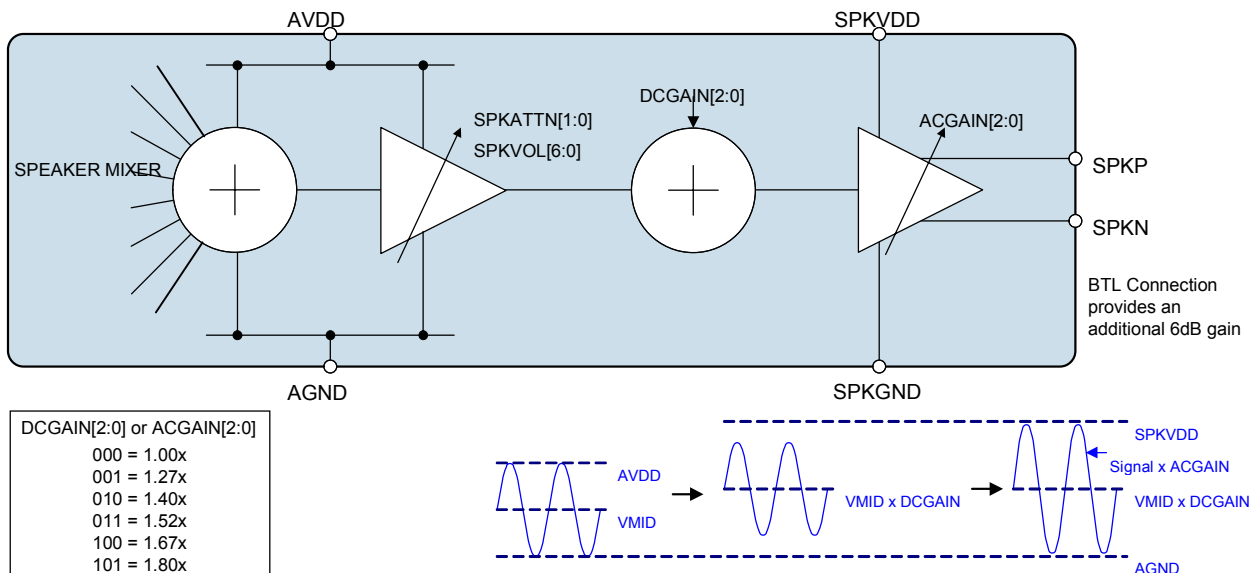


Figure 30 Speaker Boost Operation

| REGISTER ADDRESS | BIT | LABEL           | DEFAULT        | DESCRIPTION   |
|------------------|-----|-----------------|----------------|---|
| R35 (23h)        | 8   | CDMODE          | 0b             | Speaker Class D Mode Enable<br>0 = Class D mode<br>1 = Class AB mode  |
| R37 (25h)        | 5:3 | DCGAIN<br>[2:0] | 000b<br>(1.0x) | DC Speaker Boost<br>000 = 1.00x boost (+0dB)<br>001 = 1.27x boost (+2.1dB)<br>010 = 1.40x boost (+2.9dB)<br>011 = 1.52x boost (+3.6dB)<br>100 = 1.67x boost (+4.5dB)<br>101 = 1.80x boost (+5.1dB)<br>110 to 111 = Reserved |
|                  | 2:0 | ACGAIN<br>[2:0] | 000b<br>(1.0x) | AC Speaker Boost<br>000 = 1.00x boost (+0dB)<br>001 = 1.27x boost (+2.1dB)<br>010 = 1.40x boost (+2.9dB)<br>011 = 1.52x boost (+3.6dB)<br>100 = 1.67x boost (+4.5dB)<br>101 = 1.80x boost (+5.1dB)<br>110 to 111 = Reserved |

Table 33 Speaker Boost Control

### HEADPHONE OUTPUT CONFIGURATIONS

The headphone outputs LOUT, ROUT, OUT3 and OUT4 are each driven by different output mixers as described below.

The LOUT and ROUT pins output the LOMIX and ROMIX outputs respectively.

OUT3 is the output of mixer OUT3MIX, whose inputs are:

- LIN4/RXN
- LOMIX output via volume control LOPGA

OUT4 is the output of mixer OUT4MIX, whose inputs are:

- RIN4/RXP
- ROMIX output via volume control ROPGA

Full volume control is available on LOUT and ROUT. 0dB and -6dB attenuation is available on OUT3 and OUT4, with full volume control available using LOPGA and ROPGA for the LOMIX and ROMIX signals.

The outputs LOUT, ROUT, OUT3 and OUT4 are capable of driving 40mW into 16Ω loads such as stereo headsets, headphones, and/or a handset ear speaker. AC-coupled, capless mode and fully differential headphone drive modes are available.

AC-coupled output is possible on each of LOUT, ROUT, OUT3 and OUT4 simultaneously.

Capless headphone output is possible on LOUT and ROUT by using either OUT3 or OUT4 as the common return path. (This is achieved by muting OUT3 or OUT4 as required.)

If RXP and RXN are a mono differential input (e.g. a connection to an external voice CODEC), then OUT3 and OUT4 may be used as a differential output capable of driving a handset ear speaker. The signal paths from RXP to OUT4 and from RXN to OUT3 are direct, and do not pass through any additional amplifiers. This reduces standby and active power consumption and improves signal quality.

When driving a handset ear speaker using OUT3 and OUT4 from LOMIX and ROMIX, the required phase difference may be provided by inverting one of the DAC outputs. Alternatively, the phase difference can be achieved by mixing Left and Right channels through LOMIX to OUT3 and by muting OUT4. Similarly, the phase difference can be achieved by mixing Left and Right channels through ROMIX to OUT4 and by muting OUT3.

Note that a differential output will provide an additional 6dB gain at the output pins. Register bits OUT3ATTN and OUT4ATTN can be used to compensate for this gain if required.

Fully differential headphone drive is possible between LOUT and OUT3 and between ROUT and OUT4. Routing LOPGA to OUT3 and ROPGA to OUT4 results in a phase inversion at LOUT with respect to OUT3 and at ROUT with respect to OUT4. This allows fully differential headset drive, with greatly improved crosstalk performance, improved bass response, increased noise immunity and removing the need for large and expensive DC-blocking capacitors.

To ensure fully balanced differential operation, LOUT and OUT3 must be set to the same gain as each other, and ROUT and OUT4 must be set to the same gain as each other. This is best achieved by setting OUT3ATTN and OUT4ATTN to 0dB, whilst setting volume controls LOPGAVOL and LOUTVOL at matching levels and setting volume controls ROPGAVOL and ROUTVOL at matching levels.

Some example headphone output configurations are shown below.

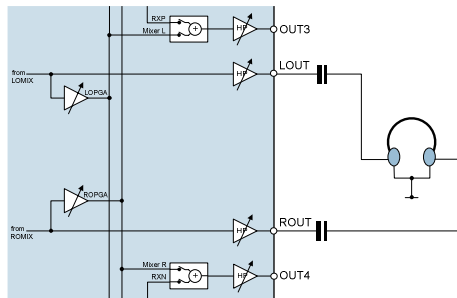


Figure 31 AC-Coupled Headphone Drive

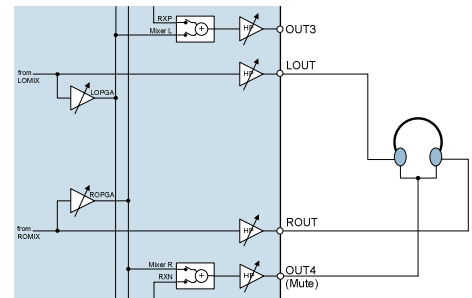


Figure 32 Capless Mode Headphone Drive

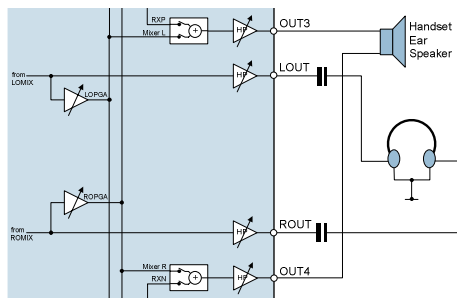


Figure 33 Headphone and Ear Speaker Drive

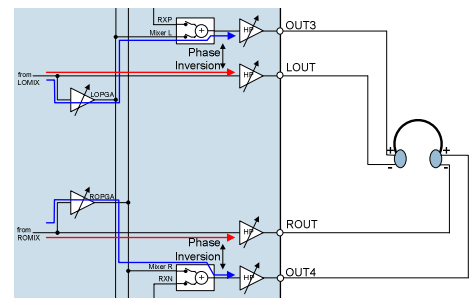


Figure 34 Fully Differential Headphone Drive

## LINE OUTPUT CONFIGURATIONS

The line outputs LON, LOP, RON and ROP are each driven by different output mixers as described below.

The LOP and ROP pins output a mix of LIN12 input PGA, RIN12 input PGA and either LOMIX or ROMIX outputs.

The LON output is a mix of ROMIX, LOMIX and a phase-inverted copy of LOP.

The RON output is a mix of LOMIX, ROMIX and a phase-inverted copy of ROP.

Volume control of LOMIX and ROMIX is available in all cases above via LOPGA and ROPGA. An additional -6dB attenuation option is provided on LOP and ROP outputs.

The outputs LON, LOP, RON and ROP are capable of driving line loads only. Single ended output is possible on all these output simultaneously. Differential output is also possible between LOP and LON and between ROP and RON.

Typical applications for the line outputs (single-ended or differential) are:

- Handset or headset microphone output to external voice CODEC
- Stereo line output
- Output to external speaker driver(s) to support stereo loudspeakers

Some example line output configurations are shown below.

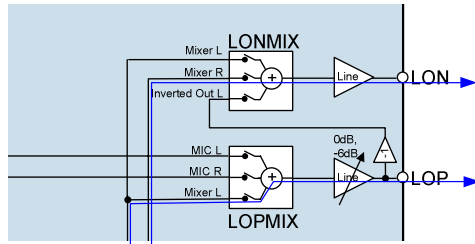


Figure 35 Stereo Line Out (A)

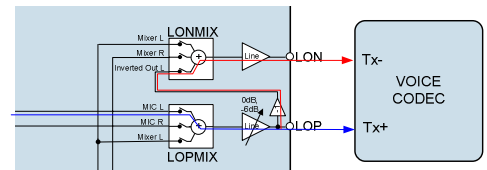


Figure 36 Differential Output of MIC PGA

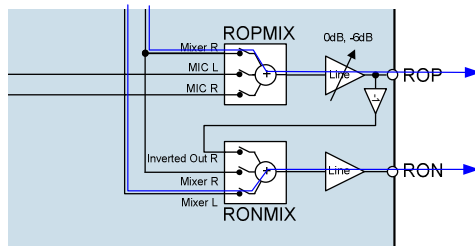


Figure 37 Stereo Line Out (B)

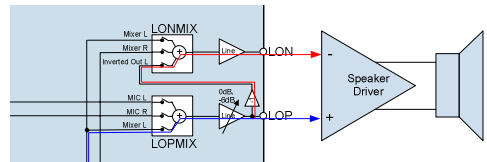


Figure 38 Differential Output to Speaker Driver

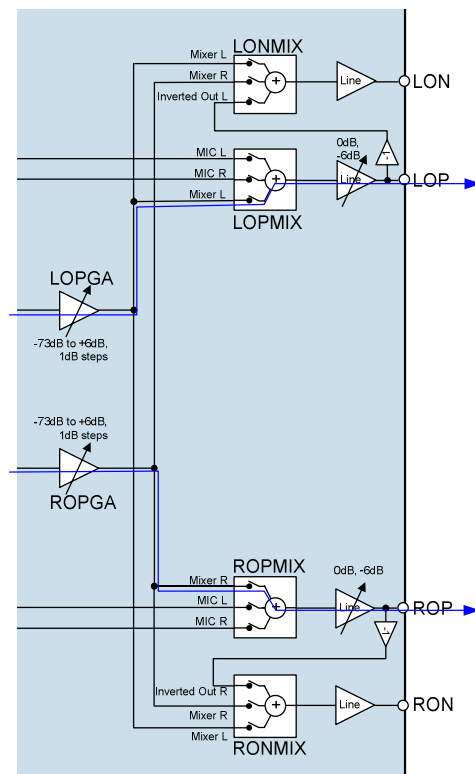


Figure 39 Stereo Line Out (C)

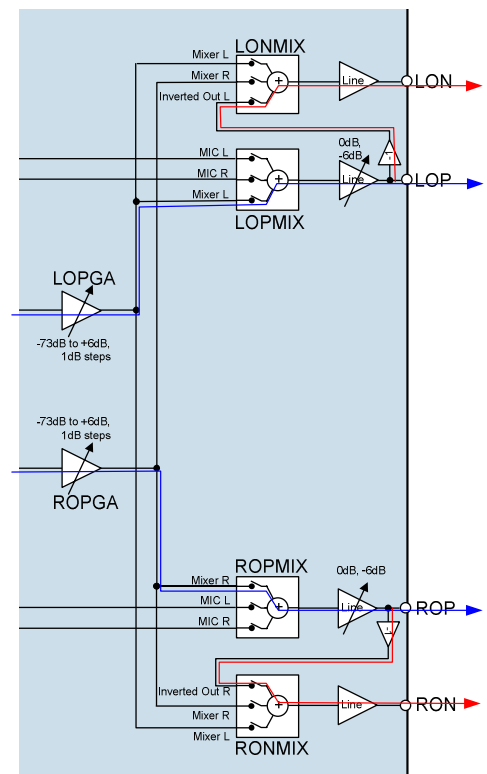


Figure 40 Stereo Differential Line Out

### DISABLED OUTPUTS

Whenever an analogue output is disabled, it can be connected to VREF through a resistor; this feature is enabled by setting the BUFIOEN bit – see “Pop Suppression Control”. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using register bit VROI. By default, a high resistance is used - 20kΩ for Headphone outputs (LOUT, ROUT, OUT3 and OUT4) and 10kΩ for Line outputs (LON, LOP, RON and ROP). If a low impedance is desired for disabled outputs, VROI can then be set to 1, decreasing the resistance to about 500Ω in all cases.

Note that a disabled output may be used as a common ground connection for a capless headphone output as described earlier.

| REGISTER ADDRESS                | BIT | LABEL | DEFAULT | DESCRIPTION  |
|---------------------------------|-----|-------|---------|--|
| R55 (37h)<br>Additional Control | 0   | VROI  | 0       | VREF to Analogue Output Resistance (Disabled Outputs)<br>0 = 20kΩ (Headphone) or 10kΩ (Line Out) from buffered VMID to output<br>1 = 500Ω from buffered VMID to output |

Table 34 Disabled Outputs to VREF Resistance

### THERMAL SHUTDOWN

The speaker and headphone outputs can drive very large currents. To protect the WM8959 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 150°C and the thermal shutdown circuit is enabled (TSHUT\_ENA = 1; TSHUT\_OPDIS = 1) the speaker and headphone amplifiers (LOUT, ROUT, SPKP, SPKN, OUT3 and OUT4) will be disabled.

TSHUT\_ENA must be set to 1 to enable the temperature sensor when using the TSHUT\_OPDIS thermal shutdown function. The output of the temperature sensor can also be output to the GPIO pins.

| REGISTER ADDRESS | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|------------------|-----|---------------------|---------|--|
| R2 (02h)         | 14  | TSHUT_ENA<br>(rw)   | 1b      | Thermal Sensor Enable<br>0 = Thermal sensor disabled<br>1 = Thermal sensor enabled   |
|                  | 13  | TSHUT_OPDIS<br>(rw) | 1b      | Thermal Shutdown Enable (Requires thermal sensor to be enabled)<br>0 = Thermal shutdown disabled<br>1 = Thermal shutdown enabled |

Table 35 Thermal Shutdown

When the speaker driver is operating in class AB mode the internal power dissipation of the WM8959 is likely to be significantly higher than when operating in class D mode.

Note: To prevent potential pops and clicks TSHUT\_ENA and TSHUT\_OPDIS need to be configured while the speaker and headphone outputs are off, i.e. LOUT\_ENA, ROUT\_ENA, OUT3\_ENA, OUT4\_ENA and SPK\_ENA are 0 (see also Table 70).

## GENERAL PURPOSE INPUT/OUTPUT

The WM8959 provides a number of versatile GPIO functions to enable features such as mobile TV support, Wi-Fi voice call recording, button and accessory detection and clock output.

The WM8959 has six multi-purpose pins for these functions.

- GPIO1, GPIO3, GPIO4 and GPIO5: Dedicated GPIO pins.
- LIN3/GPI7 and RIN3/GPI8: Analogue inputs or button/accessory detect inputs.

The following functions are available on some or all of the GPIO pins.

- Alternative DAC interface (DACDAT, DACLRC, BCLK)
- Button detect (latched with programmable de-bounce)
- MICBIAS / Accessory current or short circuit detect
- Clock output
- Temperature sensor output
- PLL lock output
- Logic '1' and logic '0' output
- Interrupt event output
- Serial data output (register readback)

The functions available on each of the GPIO pins are identified in Table 36.

| GPIO PIN FUNCTION               | GPIO PINS |       |       |       |      |      |
|---------------------------------|-----------|-------|-------|-------|------|------|
|                                 | GPIO1     | GPIO3 | GPIO4 | GPIO5 | GPI7 | GPI8 |
| BCLK2                           |           | Y     |       |       |      |      |
| DACLRC2                         |           |       | Y     |       |      |      |
| DACDAT2                         |           |       |       | Y     |      |      |
| Button/Accessory Detect Input   | Y         | Y     | Y     | Y     | Y    | Y    |
| Clock Output                    | Y         | Y     | Y     | Y     |      |      |
| Temperature OK                  | Y         | Y     | Y     | Y     |      |      |
| PLL Lock                        | Y         | Y     | Y     | Y     |      |      |
| Logic 1 and Logic 0             | Y         | Y     | Y     | Y     |      |      |
| Interrupt                       | Y         | Y     | Y     | Y     |      |      |
| SDOUT (Readback Data)           | Y         | Y     | Y     | Y     |      |      |
| Pull-up and Pull-down Available | Y         | Y     | Y     | Y     |      |      |

**Table 36 Functions Available on GPIO Pins**

The GPIO pins are configured by a combination of register settings described in Table 37 to Table 40 in the following section. The order of precedence for the control of the GPIO pins is as listed below.

1. Pin pull-up or pull-down (GPIO<sub>n</sub>\_PU, GPIO<sub>n</sub>\_PD)
2. Audio Interface and GPIO Tristate (AIF\_TRIS)
3. Pin configuration (AIFSEL and GPIO1\_ENA)
4. GPIO functionality (GPIO<sub>n</sub>\_SEL)



### GPIO CONTROL REGISTERS

Table 37 shows how the dual-function GPIO pins are configured to operate in their different modes. Note that the order of precedence described earlier applies.

Register field AIF\_SEL selects the function of GPIO3, GPIO4 and GPIO5 between Audio Interface 2 and GPIO functions. Register field GPIO1\_ENA enables the GPIO functionality on GPIO1. Register bit AIF\_TRIS, when set, takes precedence over AIF\_SEL and GPIO1 and tri-states all GPIO pins.

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION   |
|------------------|-----|-----------|---------|---|
| R8 (08h)         | 13  | AIF_SEL   | 0b      | Audio Interface Select<br>0 = Audio interface 1<br>1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)                      |
| R9 (09h)         | 15  | GPIO1_ENA | 0b      | GPIO1 Enable<br>0 = GPIO1 not enabled<br>1 = GPIO1 enabled  |
|                  | 13  | AIF_TRIS  | 0b      | Audio Interface and GPIO Tristate<br>0 = Audio interface and GPIO pins operate normally<br>1 = Tristate all audio interface and GPIO pins |

**Table 37 GPIO and GPI Pin Function Select**

The GPIO pins and the GPIO Register behaviour are also controlled by the register fields described in Table 38. Note the order of precedence described earlier applies.

Pull-up and pull-down resistors may be enabled on any of GPIO1, GPIO3, GPIO4 and GPIO5. If enabled, these settings take precedence over all other GPIO selections for that pin. Note that, by default, the pull-down resistors on GPIO3, GPIO4 and GPIO5 are enabled.

When the GPIO pins are used as inputs, de-bounce and interrupt masking may be controlled on all GPIO pins (including GPI7 and GPI8) using GPION\_DEB\_ENA and GPION\_IRQ\_ENA bits as shown in Table 39.

For each of GPIO1 and GPIO3 to GPIO5, the register field GPION\_SEL is used to select the pin functions of the individual GPIO pins as shown in Table 39. Note that this control has the lowest precedence and is only effective when GPION\_PU, GPION\_PD, AIF\_TRIS, AIFSEL and GPIO1\_ENA are set to allow GPIO functionality on that GPIO pin.

| REGISTER ADDRESS | BIT       | LABEL          | DEFAULT        | DESCRIPTION                                    |  |
|------------------|-----------|----------------|----------------|--|--|
| R19 (13h)        | 7         | GPIO1_DEB_ENA  | 0b             | See Table 39 for GPIO1 control bit description |  |
|                  | 6         | GPIO1_IRQ_ENA  | 0b             |  |  |
|                  | 5         | GPIO1_PU       | 0b             |  |  |
|                  | 4         | GPIO1_PD       | 0b             |  |  |
|                  | 3:0       | GPIO1_SEL[3:0] | 0000b          |  |  |
| R20 (14h)        | 15        | GPIO4_DEB_ENA  | 0b             | See Table 39 for GPIO4 control bit description |  |
|                  | 14        | GPIO4_IRQ_ENA  | 0b             |  |  |
|                  | 13        | GPIO4_PU       | 0b             |  |  |
|                  | 12        | GPIO4_PD       | 1b             |  |  |
|                  | 11:8      | GPIO4_SEL[3:0] | 0000b          |  |  |
|                  | R20 (14h) | 7              | GPIO3_DEB_ENA  | 0b   | See Table 39 for GPIO3 control bit description |
|                  |           | 6              | GPIO3_IRQ_ENA  | 0b   |  |
|                  |           | 5              | GPIO3_PU       | 0b   |  |
|                  |           | 4              | GPIO3_PD       | 1b   |  |
|                  |           | 3:0            | GPIO3_SEL[3:0] | 0000b  |  |
| R21 (15h)        | 7         | GPIO5_DEB_ENA  | 0b             | See Table 39 for GPIO5 control bit description |  |
|                  | 6         | GPIO5_IRQ_ENA  | 0b             |  |  |
|                  | 5         | GPIO5_PU       | 0b             |  |  |
|                  | 4         | GPIO5_PD       | 1b             |  |  |
|                  | 3:0       | GPIO5_SEL[3:0] | 0000b          |  |  |
| R22 (16h)        | 7         | GPI8_DEB_ENA   | 0b             | See Table 39 for GPI n control bit description |  |
|                  | 6         | GPI8_IRQ_ENA   | 0b             |  |  |
|                  | 4         | GPI8_ENA       | 0b             |  |  |
|                  | R22 (16h) | 3              | GPI7_DEB_ENA   | 0b   | See Table 39 for GPI n control bit description |
|                  |           | 2              | GPI7_IRQ_ENA   | 0b   |  |
|                  |           | 0              | GPI7_ENA       | 0b   |  |

Table 38 GPIO and GPI Control

The following table describes the coding of the fields listed in Table 38.

| REGISTER ADDRESS   | LABEL                                     | DEFAULT         | DESCRIPTION  |
|--|---|-----------------|--|
| Registers<br>R19 (13h)<br>to<br>R21 (15h)<br>(See Table<br>38) | GPIOn_DEB_ENA<br>(n = 1, 3, 4, 5, 7 or 8) | 0b              | De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and<br>TOCLK_ENA = 1)   |
|  | GPIOn_IRQ_ENA<br>(n = 1, 3, 4, 5, 7 or 8) | 0b              | IRQ Enable<br>0 = disabled<br>1 = enabled  |
|  | GPIOn_PU<br>(n = 1, 3, 4 or 5)            | 0b              | GPIO Pull-Up Resistor Enable<br>0 = Pull-up disabled<br>1 = Pull-up enabled (Approx 150kΩ)   |
|  | GPIOn_PD<br>(n = 1, 3, 4 or 5)            | See<br>Table 38 | GPIO Pull-Down Resistor Enable<br>0 = Pull-down disabled<br>1 = Pull-down enabled (Approx 150kΩ)   |
|  | GPIOn_SEL[3:0]<br>(n = 1, 3, 4 or 5)      | 0000b           | GPIO Pin Function Select<br>0000 = Input pin<br>0001 = Clock output (SYSCLK/OPCLKDIV)<br>0010 = Logic '0'<br>0011 = Logic '1'<br>0100 = PLL Lock output<br>0101 = Temperature OK output<br>0110 = SDOOUT data output<br>0111 = IRQ output<br>1000 = MIC Detect<br>1001 = MIC Short Circuit Detect<br>1010 to 1111 = Reserved |
|  | GPIIn_ENA<br>(n = 7 or 8)                 | 0b              | GPIIn Input Pin Enable<br>0 = pin disabled as GPIIn input<br>1 = pin enabled as GPIIn input  |

**Table 39 GPIO Function Control Bits**

The polarity of GPIO/GPI inputs may be configured using the GPIO\_POL register bits. This is described in Table 40.

| REGISTER ADDRESS | BIT | LABEL                     | DEFAULT | DESCRIPTION   |
|------------------|-----|---------------------------|---------|---|
| R23 (17h)        | 7:0 | GPIO_POL<br>[7:0]<br>(rw) | 00h     | GPIO Input Polarity<br>0 = Non-inverted<br>1 = Inverted<br>GPIO_POL[7] = GPI8 polarity<br>GPIO_POL[6] = GPI7 polarity<br>GPIO_POL[5] = Reserved<br>GPIO_POL[4] = GPIO5 polarity<br>GPIO_POL[3] = GPIO4 polarity<br>GPIO_POL[2] = GPIO3 polarity<br>GPIO_POL[1] = Reserved<br>GPIO_POL[0] = GPIO1 polarity |

**Table 40 GPIO Polarity**

Each of the available GPIO functions is described in turn in the following sections.

### ALTERNATIVE DAC INTERFACE

The WM8959 may be configured to select between two different audio interfaces, providing the capability to receive DAC input data via BCLK2, DACLRC2 and DACDAT2 instead of BCLK, DACLRC and DACDAT. This selection is made by register bit AIF\_SEL, as described in Table 37.

To use the alternative DAC interface, the following register settings are required:

- AIF\_TRIS = 0
- AIF\_SEL = 1
- GPIO3\_PU = 0, GPIO4\_PU = 0, GPIO5\_PU = 0
- GPIO3\_PD = 0, GPIO4\_PD = 0, GPIO5\_PD = 0

Note that additional devices can also be connected to the main interface pins using the TDM mode. See "Digital Audio Interface" section for further details on controlling the audio interface pins.

The alternative DAC interface connection is illustrated in Figure 41.

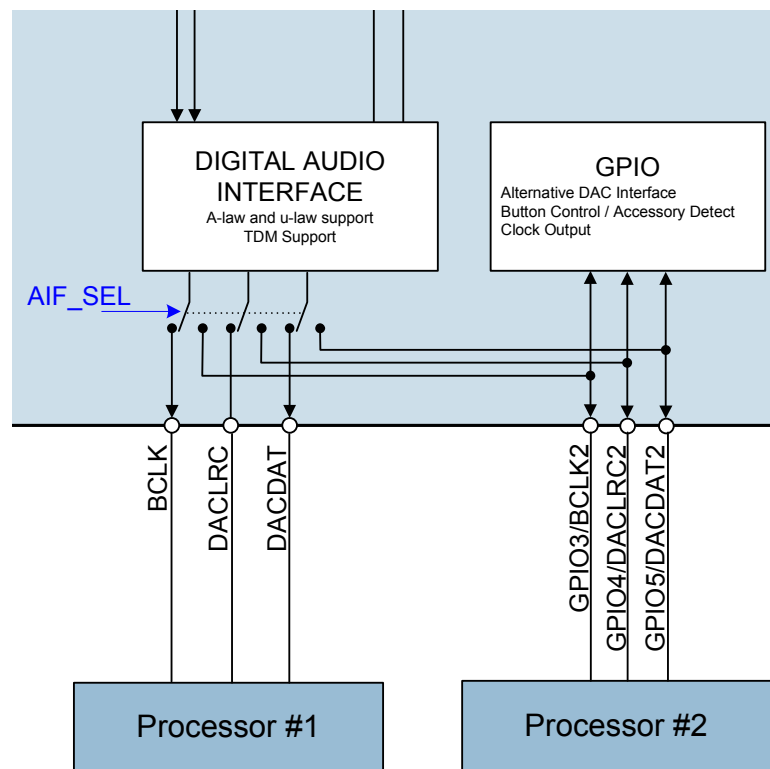


Figure 41 Alternative DAC Interface

## BUTTON CONTROL

The WM8959 GPIO supports button control detection with full status readback for up to six inputs (or five inputs and one IRQ output). All inputs are latched at the IRQ Register, with de-bounce available for normal operation. De-bouncing may be disabled in order to allow the device to respond to wake-up events while the processor is disabled and is unable to provide a clock for de-bouncing.

To enable button control and accessory detection, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- LMN3 = 0, LLI3LO = 0 and RLI3LO = 0 (only required if using GPI7)
- RMN3 = 0, RRI3LO = 0 and RI3RO = 0 (only required if using GPI8)
- AIF\_TRIS = 0
- GPIO<sub>n</sub>\_SEL = 0000 for each required GPIO button input

Programmable pull-up and pull-down resistors are available on GPIO1 and GPIO3 to GPIO5. These should be set according to the external circuit configuration. Note that pull-up and pull-down resistors are not available on the GPI7 and GPI8 input pins. Note that the analogue input paths to GPI7 and GPI8 must be disabled as described above when using these as digital inputs.

In this application, one or more of the GPIO pins may be configured as an Interrupt event if desired. This is controlled by the GPIO<sub>n</sub>\_IRQ\_ENA bits described in Table 38. The GPIO Pin status fields contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 47 for more details of the Interrupt function.

An example configuration of the button control GPIO function is illustrated in Figure 42.

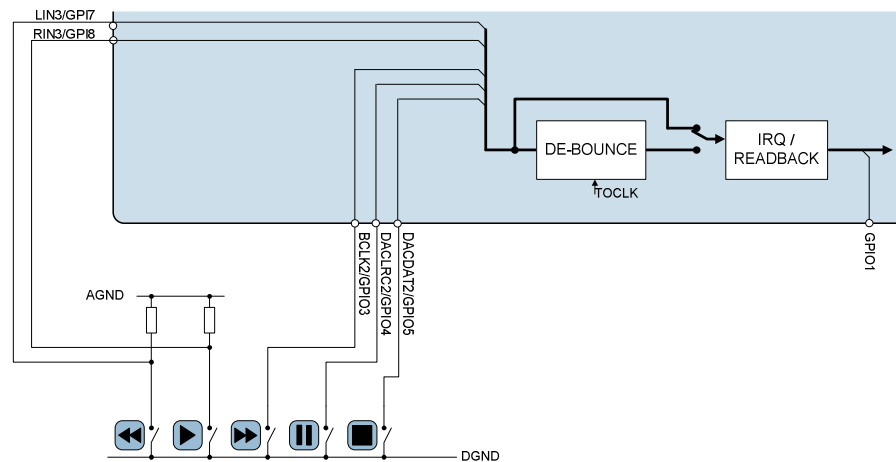


Figure 42 Example of Button Control Using GPIO Pins

### Note:

- The GPIOs 1, 3, 4 and 5 are referenced to DBVDD
- The GPIs 7 and 8 are referenced to AVDD

**MICBIAS CURRENT AND ACCESSORY DETECT**

A MICBIAS current detect function is provided for accessory detection. When a microphone current is detected (e.g. when a headset is inserted), an interrupt event can be generated and the microphone status read back via the control interface.

The MICBIAS current detect threshold is programmable. A short-circuit current detection is also available, with a programmable threshold. These functions are enabled by register bit MCD; the thresholds are programmable via register fields MCDTHR and MCDSTR as shown in Table 41.

The polarity of the current detect GPIO signals may be controlled by register bits MICDET\_POL and MICSHRT\_POL. Note that these polarity inversion bits apply to the Interrupt register behaviour only; they do not affect the direct GPIO output of the Current Detect functions. The respective interrupt events may be masked or enabled by register bits MICDET\_IRQ\_ENA and MICSHRT\_IRQ\_ENA. The MICBIAS current threshold status bits contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 47 for more details of the Interrupt function.

If direct output of the MICBIAS current detect function is required to the external pins of the WM8959, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO\_n\_SEL = 1000 for the selected GPIO MICBIAS Current Detect output pin
- GPIO\_n\_SEL = 1001 for the selected GPIO MICBIAS Short Circuit Detect output pin
- GPIO\_n\_PU = 0 for the selected GPIO MICBIAS output pin or pins
- GPIO\_n\_PD = 0 for the selected GPIO MICBIAS output pin or pins

The register fields used to configure the MICBIAS Current Detect function are described in Table 41.

| REGISTER ADDRESS | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|------------------|-----|---------------------|---------|--|
| R58 (3Ah)        | 7:6 | MCDSTR<br>[1:0]     | 00b     | MICBIAS Short Circuit Detect Threshold<br>00 = 600uA<br>01 = 1200uA<br>10 = 1800uA<br>11 = 2400uA<br>These values are for AVDD=3.3V and scale proportionally with AVDD.  |
|                  | 5:3 | MCDTHR<br>[2:0]     | 000b    | MICBIAS Current Detect Threshold<br>000 = 200uA<br>001 = 350uA<br>010 = 500uA<br>011 = 650uA<br>100 = 800uA<br>101 = 950uA<br>110 = 1100uA<br>111 = 1250uA<br>These values are for AVDD=3.3V and scale proportionally with AVDD. |
|                  | 2   | MCD                 | 0b      | MICBIAS Current and Short Circuit Detect Enable<br>0 = disabled<br>1 = enabled   |
| R23 (17h)        | 10  | MICSHRT_POL<br>(rw) | 0b      | MICBIAS short circuit detect polarity<br>0 = Non-inverted<br>1 = Inverted  |

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION  |
|------------------|-----|--------------------|---------|--|
|                  | 9   | MICDET_POL<br>(rw) | 0b      | MICBIAS current detect polarity<br>0 = Non-inverted<br>1 = Inverted    |
| R22 (16h)        | 10  | MICSHRT_IRQ_ENA    | 0b      | MICBIAS short circuit detect IRQ Enable<br>0 = disabled<br>1 = enabled |
|                  | 9   | MICDET_IRQ_ENA     | 0b      | MICBIAS current detect IRQ Enable<br>0 = disabled<br>1 = enabled       |

Table 41 MICBIAS Current Detect Control

The current detect function operates according to the following the truth table:

| LABEL                    | VALUE | DESCRIPTION                             |
|--------------------------|-------|---|
| Mic Short Circuit Detect | 0     | MCDSCPTH current threshold not exceeded |
| Mic Short Circuit Detect | 1     | MCDSCPTH current threshold exceeded     |
| Mic Current Detect       | 0     | MCDTHR current threshold not exceeded   |
| Mic Current Detect       | 1     | MCDTHR current threshold exceeded       |

Table 42 Truth Table for GPIO Output of MICBIAS Current Detect Function

### CLOCK OUTPUT

A clock output (OPCLK) derived from SYSCLK may be output via GPIO1 and GPIO3 to GPIO5. SYSCLK is derived from MCLK (either directly, or in conjunction with the PLL), and is used to provide all internal clocking for the WM8959 (see "Clocking and Sample Rates" section for more information).

A programmable clock divider OPCLKDIV controls the frequency of the OPCLK output. This clock is enabled by register bit OPCLK\_ENA. See "Clocking and Sample Rates" for a definition of this register field.

To enable clock output via one or more GPIO pins, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO<sub>n</sub>\_SEL = 0001 for the selected GPIO clock output pin
- GPIO<sub>n</sub>\_PU = 0 for the selected GPIO clock output pin
- GPIO<sub>n</sub>\_PD = 0 for the selected GPIO clock output pin

### TEMPERATURE SENSOR OUTPUT

The WM8959 output drivers can generate a large amount of heat. To protect the device from overheating a thermal shutdown function is provided (see "Thermal Shutdown" section for more information).

The polarity of the Thermal Shutdown sensor may be controlled by register bit TEMPOK\_POL. Note that this polarity inversion bit applies to the Interrupt register behaviour only; it does not affect the direct GPIO output of the Temperature Sensor function. The associated interrupt event may be masked or enabled by register bit TEMPOK\_IRQ\_ENA. The Temperature status bit contained in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 47 for more details of the Interrupt function.

If direct output of the Temperature status bit is required to the external pins of the WM8959, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIOOn\_SEL = 0101 for the selected GPIO Temperature status output pin
- GPIOOn\_PU = 0 for the selected GPIO Temperature status output pin
- GPIOOn\_PD = 0 for the selected GPIO Temperature status output pin

The register fields used to configure the Temperature Sensor GPIO function are described in Table 43.

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   |
|------------------|-----|--------------------|---------|---|
| R23 (17h)        | 11  | TEMPOK_POL<br>(rw) | 1b      | Temperature Sensor polarity<br>0 = Non-inverted<br>1 = Inverted |
| R22 (16h)        | 11  | TEMPOK_IRQ_ENA     | 0b      | Temperature Sensor IRQ Enable<br>0 = disabled<br>1 = enabled    |

**Table 43 Temperature Sensor GPIO Control**

The temperature sensor function operates according to the following truth table:

| LABEL                     | VALUE | DESCRIPTION                       |
|---------------------------|-------|-----------------------------------|
| Temperature Sensor output | 0     | Overheat temperature exceeded     |
| Temperature Sensor output | 1     | Overheat temperature not exceeded |

**Table 44 Truth Table for GPIO Output of Temperature Sensor Function**



### PLL LOCK OUTPUT

An internal signal used to indicate the lock status of the PLL can be output to a GPIO pin or used to trigger an Interrupt event. The polarity of the PLL Lock indication may be controlled by register bit PLL\_LCK\_POL. Note that this polarity inversion bit applies to the Interrupt register behaviour only; it does not affect the direct GPIO output of the PLL Lock function. The associated interrupt event may be masked or enabled by register bit PLL\_LCK\_IRQ\_ENA. The PLL Lock status bit in the IRQ Register (R18) may be read at any time or else in response to an Interrupt event. See Table 47 for more details of the Interrupt function.

If direct output of the PLL Lock status bit is required to the external pins of the WM8959, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO<sub>n</sub>\_SEL = 0100 for the selected PLL Lock status output pin
- GPIO<sub>n</sub>\_PU = 0 for the selected PLL Lock status output pin
- GPIO<sub>n</sub>\_PD = 0 for the selected PLL Lock status output pin

The register fields used to configure the PLL Lock GPIO function are described in Table 45.

| REGISTER ADDRESS | BIT | LABEL               | DEFAULT | DESCRIPTION   |
|------------------|-----|---------------------|---------|---|
| R23 (17h)        | 8   | PLL_LCK_POL<br>(rw) | 0b      | PLL Lock polarity<br>0 = Non-inverted<br>1 = Inverted |
| R22 (16h)        | 8   | PLL_LCK_IRQ_ENA     | 0b      | PLL Lock IRQ Enable<br>0 = disabled<br>1 = enabled    |

**Table 45 PLL Lock GPIO Control**

The PLL Lock function operates according to the following truth table:

| LABEL           | VALUE | DESCRIPTION    |
|-----------------|-------|----------------|
| PLL Lock output | 0     | PLL not Locked |
| PLL Lock output | 1     | PLL Locked     |

**Table 46 Truth Table for GPIO Output of PLL Lock function**

### LOGIC '1' AND LOGIC '0' OUTPUT

The GPIO pins can be programmed to drive a logic high or logic low signal. The following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO<sub>n</sub>\_SEL = 0010 for each Logic '0' output pin
- GPIO<sub>n</sub>\_SEL = 0011 for each Logic '1' output pin
- GPIO<sub>n</sub>\_PU = 0 for each Logic '0' or Logic '1' GPIO pin
- GPIO<sub>n</sub>\_PD = 0 for each Logic '0' or Logic '1' GPIO pin

## INTERRUPT EVENT OUTPUT

An interrupt can be generated by any of the following events described earlier:

- Button Control input (on GPIO1, GPIO3 to GPIO5, GPI7 and GPI8)
- MICBIAS current / short circuit / accessory detect
- PLL Lock
- Temperature Sensor

The interrupt status flag IRQ is asserted when any un-masked Interrupt input is asserted. It is the OR'd combination of all the un-masked Interrupt inputs. If required, this flag may be inverted using the IRQ\_INV register bit. The GPIO pins can be configured to output the IRQ signal.

The interrupt behaviour is driven by level detection (not edge detection) of the un-masked inputs. Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt status flag IRQ will be triggered again even though no transition has occurred. If edge detection is required (eg. confirming that the input has been de-asserted), then the polarity inversion may be used after each event in order to detect each rising and falling edge separately. This is described further in the "GPIO Summary" section.

The status of the IRQ flag may be read back via the control interface. The status of each GPIO pin and the internal signals PLL\_LCK, TEMPOK, MICSHRT and MICDET may also be read back in the same way.

The IRQ register (R18) is described in Table 47. The status of the GPIO pins or other Interrupt inputs can be read back via the read/write bits R18[11:0]. The Interrupt inputs are latched once set. Each input may be reset by writing a 1 to the appropriate bit. The IRQ bit cannot be reset; it is the OR'd combination of all other registers and will reset only if R18[11:0] are all 0.

If direct output of the Interrupt signal is required to external pins of the WM8959, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO\_n\_SEL = 0111 for the selected Interrupt (IRQ) output pin
- GPIO\_n\_PU = 0 for the selected Interrupt (IRQ) output pin
- GPIO\_n\_PD = 0 for the selected Interrupt (IRQ) output pin

The IRQ register (R18) is described in Table 47.

| REGISTER ADDRESS                 | BIT | LABEL                        | DEFAULT       | DESCRIPTION   |
|----------------------------------|-----|------------------------------|---------------|---|
| R18 (12h)                        | 12  | IRQ<br>(ro)                  | Read Only     | IRQ Readback<br>(Allows polling of IRQ status)  |
|                                  | 11  | TEMPOK<br>(rr)               | Read or Reset | Temperature OK status<br>Read-<br>0 = Device temperature NOT ok<br>1 = Device temperature ok<br>Write -<br>1 = Reset TEMPOK latch   |
|                                  | 10  | MICSHRT<br>(rr)              | Read or Reset | MICBIAS short status<br>Read-<br>0 = MICBIAS ok<br>1 = MICBIAS shorted<br>Write-<br>1 = Reset MICSHRT latch   |
|                                  | 9   | MICDET<br>(rr)               | Read or Reset | MICBIAS detect status<br>MICBIAS microphone detect Readback<br>Read-<br>0 = No Microphone detected<br>1 = Microphone detected<br>Write-<br>1 = Reset MICDET latch   |
|                                  | 8   | PLL_LCK<br>(rr)              | Read or Reset | PLL Lock status<br>Read-<br>0 = PLL NOT locked<br>1 = PLL locked<br>Write-<br>1 = Reset PLL_LCK latch   |
|                                  | 7:0 | GPIO_STATUS<br>[7:0]<br>(rr) | Read or Reset | GPIO and GPI Input Pin Status<br>GPIO_STATUS[7] = GPI8 pin status<br>GPIO_STATUS[6] = GPI7 pin status<br>GPIO_STATUS[5] = Reserved<br>GPIO_STATUS[4] = GPIO5 status<br>GPIO_STATUS[3] = GPIO4 status<br>GPIO_STATUS[2] = GPIO3 status<br>GPIO_STATUS[1] = Reserved<br>GPIO_STATUS[0] = GPIO1 status |
| R23 (17h)<br>GPIO<br>Control (2) | 12  | IRQ_INV<br>(rw)              | 0b            | IRQ Invert<br>0 = IRQ output active high<br>1 = IRQ output active low   |

Table 47 GPIO Interrupt and Status Readback

**SERIAL DATA OUTPUT (REGISTER READBACK)**

The GPIO pins can be configured to output serial data during register readback in 3-wire (open-drain) or 4-wire mode. The readback mode is configured using the register bits RD\_3W\_ENA and MODE\_3W4W as described in Table 48.

Setting the RD\_3W\_ENA bit to 1 enables 3-wire readback using the SDIN pin in open-drain mode. Setting the RD\_3W\_ENA bit to 0 requires the use of a GPIO pin as SDOUT. To enable SDOUT on a GPIO pin, the following register settings are required:

- GPIO1\_ENA = 1 (only required if using GPIO1)
- AIF\_SEL = 0 (only required if using GPIO3, GPIO4 or GPIO5)
- AIF\_TRIS = 0
- GPIO<sub>n</sub>\_SEL = 0110 for the selected SDOUT output pin
- GPIO<sub>n</sub>\_PU = 0 for the selected SDOUT output pin
- GPIO<sub>n</sub>\_PD = 0 for the selected SDOUT output pin

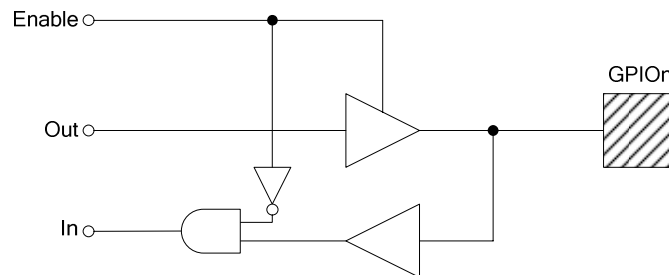
The register fields used to configure SDOUT on the GPIO pins are described in Table 48. Refer to "Control Interface" for more details of 3-wire and 4-wire interfacing.

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|------------------|-----|-----------|---------|--|
| R22 (16h)        | 15  | RD_3W_ENA | 1b      | 3- / 4-wire readback configuration<br>1 = 3-wire mode<br>0 = 4-wire mode, using GPIO pin     |
|                  | 14  | MODE_3W4W | 0b      | 3-wire mode<br>0 = push 0/1<br>1 = open-drain<br>4-wire mode<br>0 = push 0/1<br>1 = wired-OR |

**Table 48 GPIO 3-Wire Readback Enable**



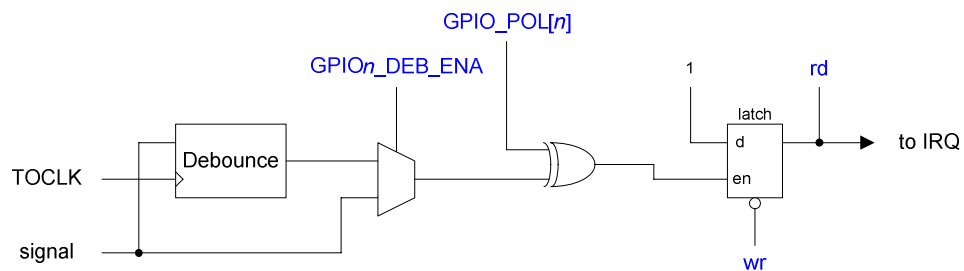
Details of the GPIO implementation are shown below. In order to avoid GPIO loops if a GPIO is configured as an output the corresponding input is disabled, as shown in Figure 44 below.



**Figure 44 GPIO Pad**

The GPIO register, i.e. latch structure, is shown in Figure 45 below. The de-bounce Control fields `GPIO n_DEB_ENA` determine whether the signal is de-bounced or not. (Note that `TOCLK` (via `SYCLK`) needs to be present in order for the debounce circuit to work.) The polarity bits `GPIO_POL[7:0]` control whether an interrupt is triggered by a logic 1 level (for `GPIO_POL[n] = 0`) or a logic 0 level (for `GPIO_POL[n] = 1`). The latch will cause the interrupt to be stored until it is reset by writing to the Interrupt Register. The latched signal is processed by the IRQ circuit, shown in Figure 43 above. The interrupt status bits can be read at any time from Register R18 (see Table 47) and are reset by writing a "1" to the applicable bit in Register R18.

Note that the interrupt behaviour is driven by level detection (not edge detection). Therefore, if an input remains asserted after the interrupt register has been reset, then the interrupt event will be triggered again even though no transition has occurred. If edge detection is required, this may be implemented as described in the following paragraphs.



**Figure 45 GPIO Function**

Three typical scenarios are presented in the following Figure 46, Figure 47 and Figure 48. The examples are:

- Latch a GPIO input (Figure 46)
- Debounce and latch a GPIO input (Figure 47)
- Use the `GPIO n_POL` bit to implement an IRQ edge detect function (Figure 48)

The GPIO input or internal Interrupt event (eg. MICBIAS current detect) is latched as illustrated below:

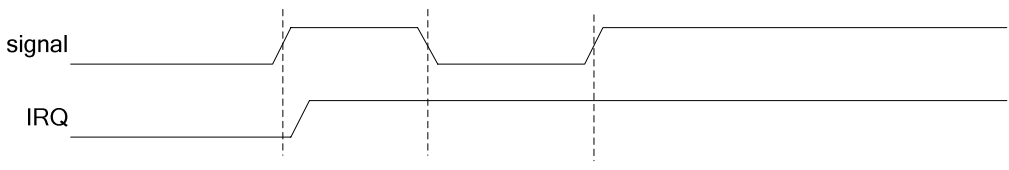


Figure 46 GPIO Latch

The de-bounce function on the GPIO input pins enables transient behaviour to be filtered as illustrated below:

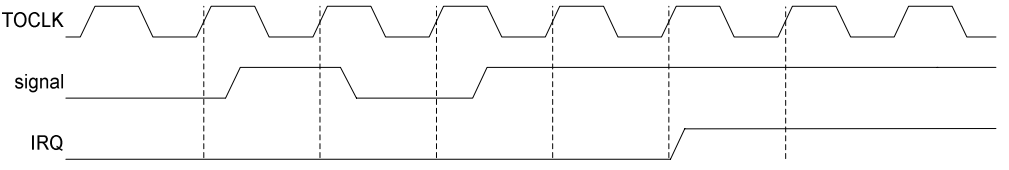


Figure 47 GPIO De-bounce

To implement an edge detect function on a GPIO input, the GPIO<sub>n</sub>\_POL bits may be used to alternate the GPIO polarity after each edge transition. For example, after a logic 1 has caused an Interrupt event, the polarity may be inverted prior to resetting the Interrupt register bit. In this way, the next interrupt event generated by this GPIO will occur when it returns to the logic 0 state. The GPIO<sub>n</sub>\_POL bit must be reversed after every GPIO edge transition, as illustrated below:

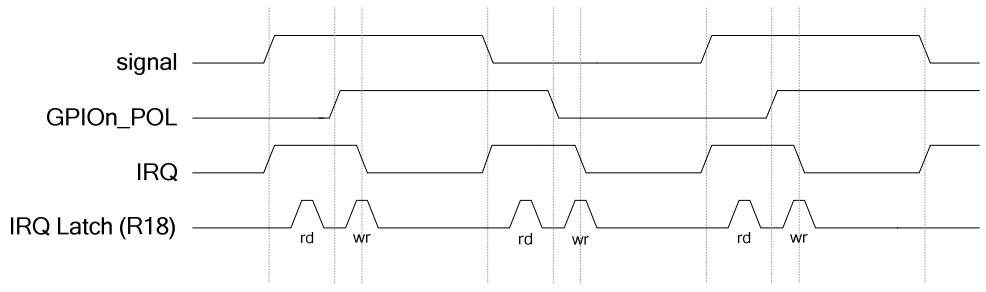


Figure 48 GPIO Edge Detect

**GPIO IRQ HANDLING**

In the following diagram Figure 49 a typical IRQ scenario is illustrated.

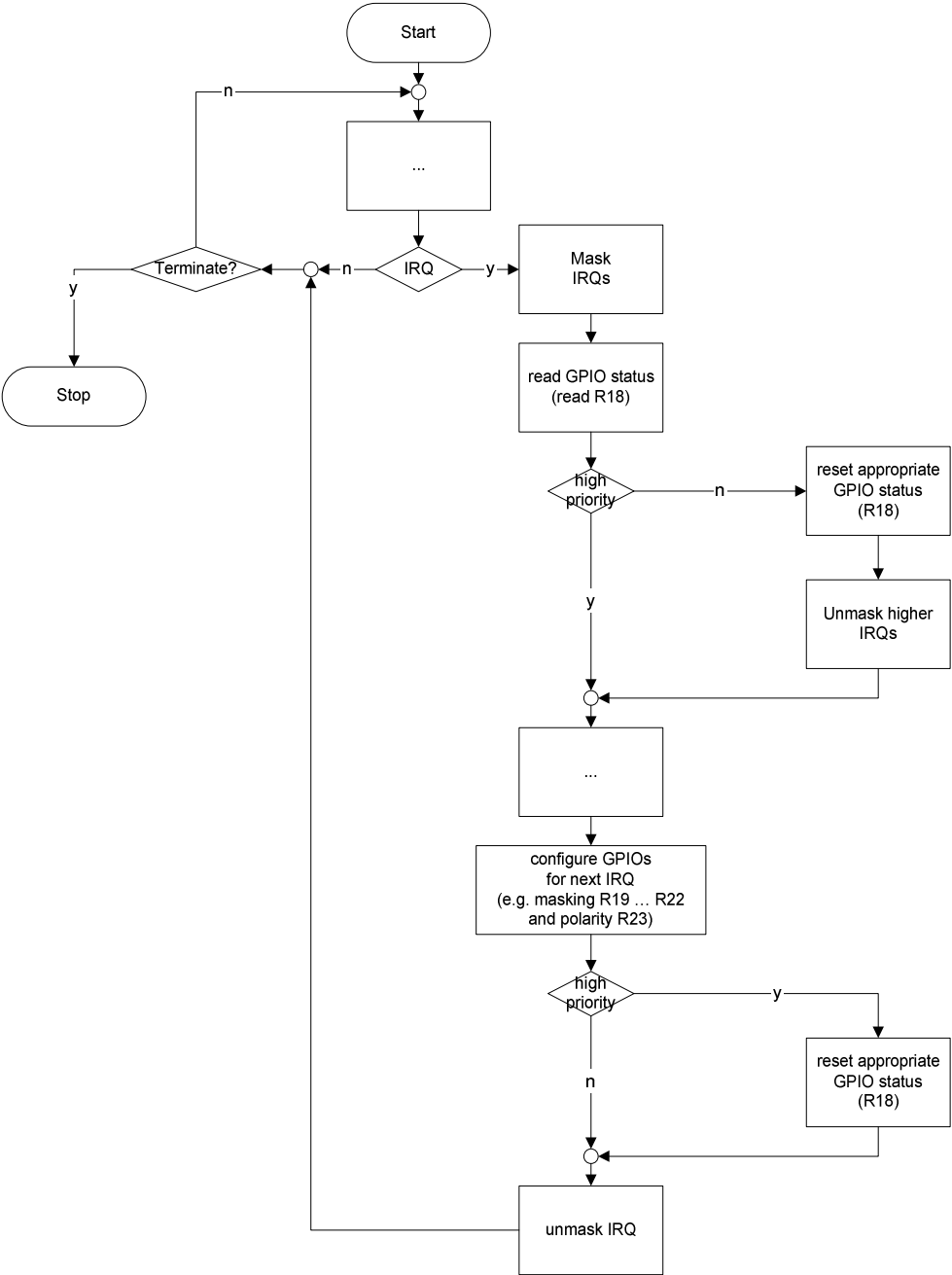


Figure 49 GPIO IRQ Handling



## DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data to the WM8959. It uses three pins:

- DACDAT: DAC data input
- DACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

DACDAT, DACLRC and BCLK functions can also be supported using alternative GPIO pins.

The clock signals BCLK and DACLRC can be outputs when the WM8959 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I<sup>2</sup>S
- DSP mode

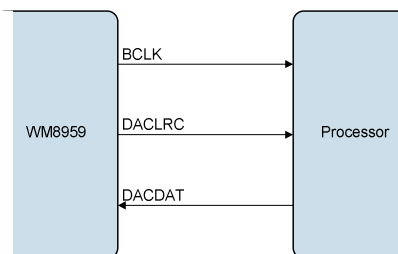
All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the "Electrical Characteristics" section for timing information.

Time Division Multiplexing (TDM) is available in all four data format modes. The WM8959 can be programmed to send and receive data in one of two time slots.

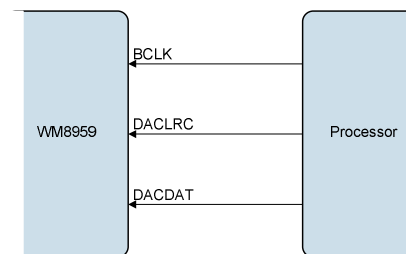
PCM operation is supported using the DSP mode.

## MASTER AND SLAVE MODE OPERATION

The WM8959 digital audio interface can operate as a master or slave as shown in Figure 50 and Figure 51.



**Figure 50 Master Mode**



**Figure 51 Slave Mode**

## OPERATION WITH ALTERNATIVE DAC INTERFACE

To allow data to be input to the WM8959 DACs from two separate sources, the GPIO[5:3] pins can be configured as an alternative DAC interface (BCLK2, DACLRC2, DACDAT2) as shown in Figure 52 to Figure 57.

WM8959

Pre-Production

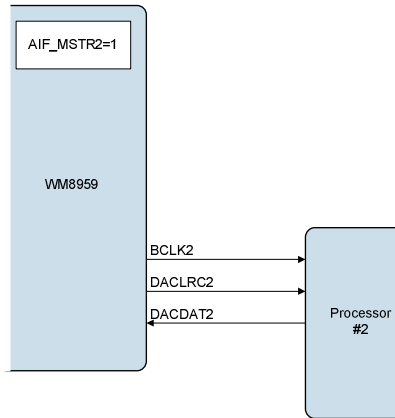


Figure 52 Interface 2 = Master

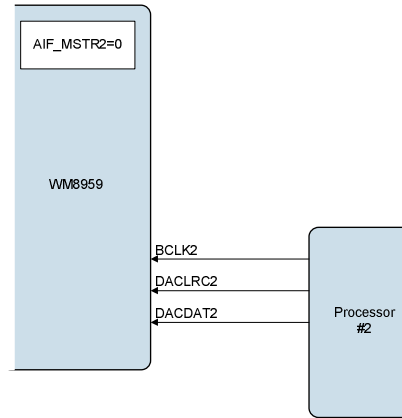


Figure 53 Interface 2 = Slave

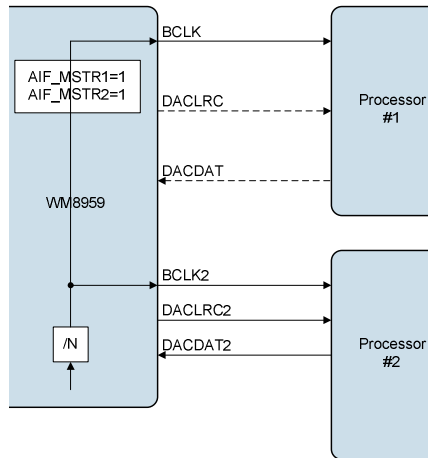


Figure 54 Interface 1 = Master, Interface 2 = Master

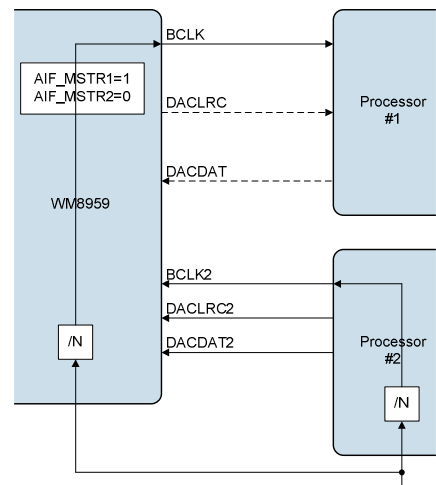


Figure 55 Interface 1 = Master, Interface 2 = Slave

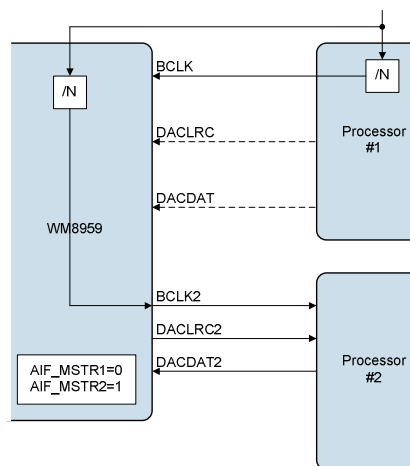


Figure 56 Interface 1 = Slave, Interface 2 = Master

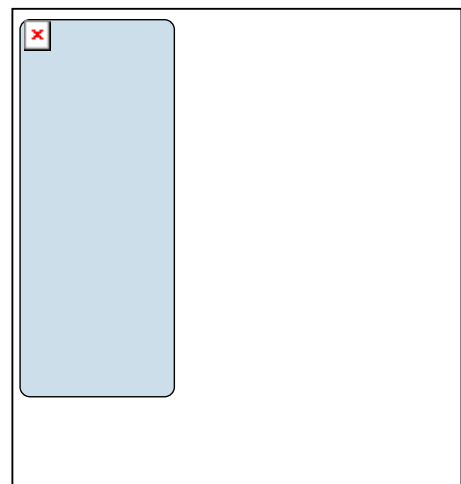


Figure 57 Interface 1 = Slave, Interface 2 = Slave

The dual Audio Interface approach of the WM8959 has been implemented in such a way that it gives the user and application as much flexibility as possible, without any restrictions built into the WM8959.

This means that the application has to be carefully analysed and the WM8959 configured accordingly. In the following Figure 58 and Figure 59, the Audio Interface input flow and the output controls are illustrated.

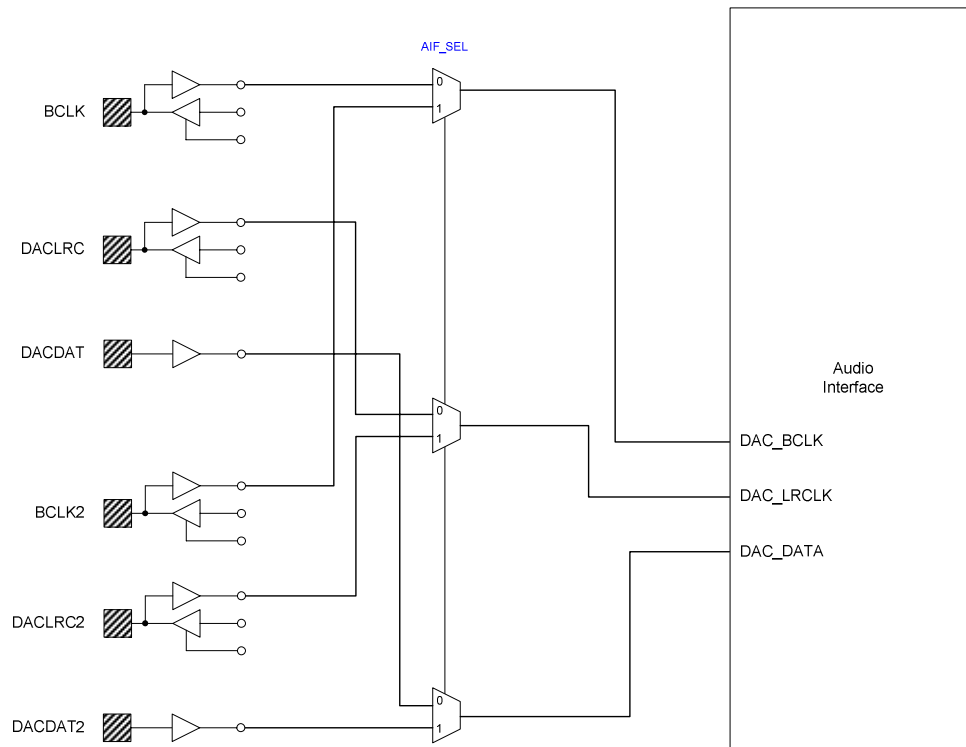


Figure 58 Audio Interface Input Flow

The Audio Interface input flow illustrated above is controlled only by the AIF\_SEL register bit.

| REGISTER ADDRESS | BIT | LABEL   | DEFAULT | DESCRIPTION  |
|------------------|-----|---------|---------|--|
| R8 (08h)         | 13  | AIF_SEL | 0b      | Audio Interface Select<br>0 = Audio interface 1<br>1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2) |

Table 49 Audio Interface Pin Function Select

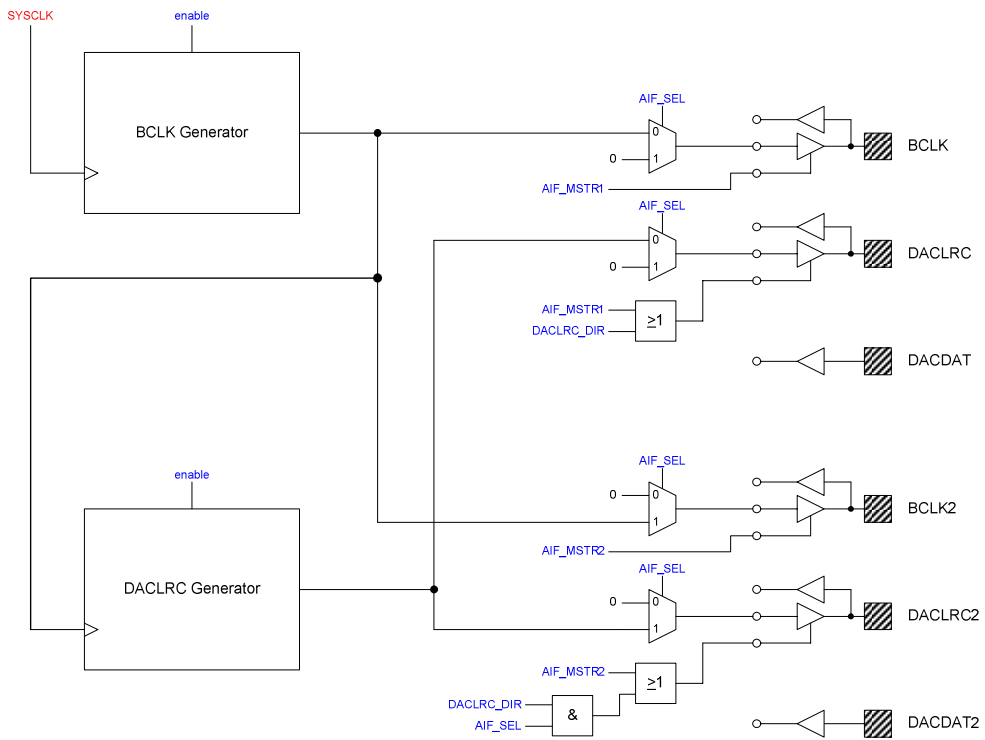


Figure 59 Audio Interface Output Control

The Audio Interface output control is illustrated above. The master mode control registers AIF\_MSTR1 and AIF\_MSTR2 as well as the left-right clock control register DACLRC\_DIR determine whether the WM8959 generates the required clocks and the AIF\_SEL control field determines which pins these clocks are provided from.

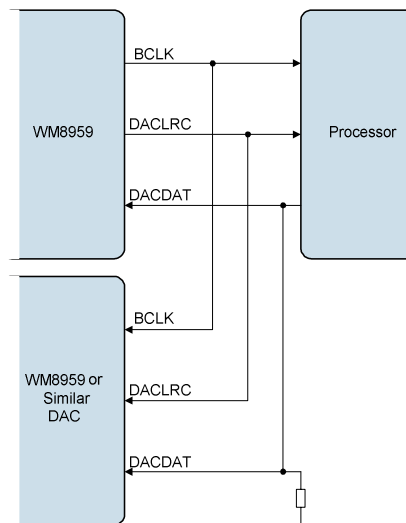
These registers are described in Table 50 below.

| REGISTER ADDRESS | BIT | LABEL      | DEFAULT | DESCRIPTION  |
|------------------|-----|------------|---------|--|
| R8 (08h)         | 15  | AIF_MSTR1  | 0b      | Audio Interface 1 Master Mode Select<br>0 = Slave mode<br>1 = Master mode  |
|                  | 14  | AIF_MSTR2  | 0b      | Audio Interface 2 Master Mode Select<br>0 = Slave mode<br>1 = Master mode  |
|                  | 13  | AIF_SEL    | 0b      | Audio Interface Select<br>0 = Audio interface 1<br>1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)                   |
| R9 (09h)         | 11  | DACLRC_DIR | 0b      | DACLRC Direction<br>(Forces DACLRC clock to be output in slave mode)<br>0 = DACLRC normal operation<br>1 = DACLRC clock output enabled |

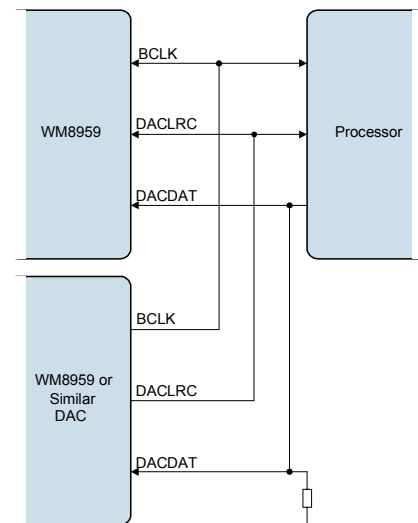
**Table 50 Audio Interface Output Function Control**

### OPERATION WITH TDM

Time division multiplexing (TDM) allows multiple devices to transfer data simultaneously on the same bus. The WM8959 DACs support TDM in master and slave modes, on both interfaces, and for all data formats and word lengths. TDM is enabled using register bit AIFDAC\_TDM. The TDM data slot is programmed using register bit AIFDAC\_TDM\_CHAN.



**Figure 60 TDM with WM8959 as Master**



**Figure 61 TDM with Other DAC as Master**

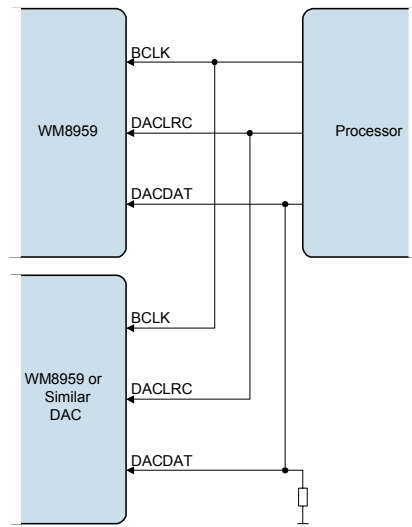


Figure 62 TDM with Processor as Master

**Note:** The WM8959 is a 24-bit device. If the user operates the WM8959 in 32-bit mode then the 8 LSBs will be ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the DACDAT line in TDM mode.

**BCLK DIVIDE**

The BCLK frequency is controlled by BCLK\_DIV. Internal clock divide and phase control mechanisms ensure that the BCLK and DACLRC edges will occur in a predictable and repeatable position relative to each other and relative to the data for a given combination of DAC sample rate and BCLK\_DIV settings.

See “Clocking and Sample Rates” section for more information.

**AUDIO DATA FORMATS (NORMAL MODE)**

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a DACLRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each DACLRC transition.

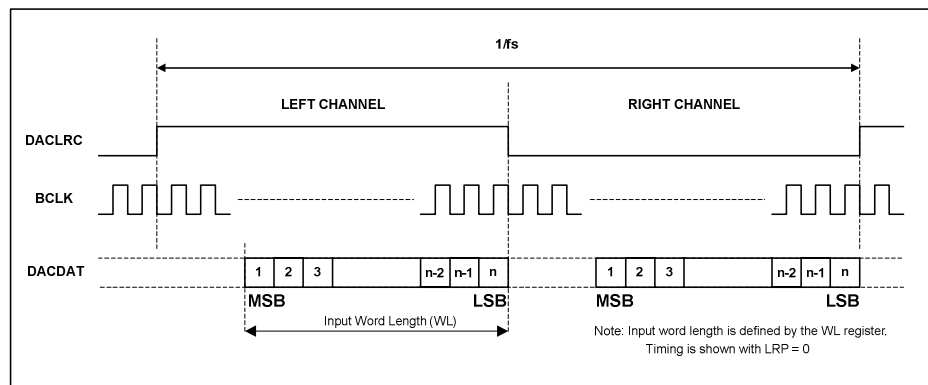


Figure 63 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a DACLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each DACLRC transition.

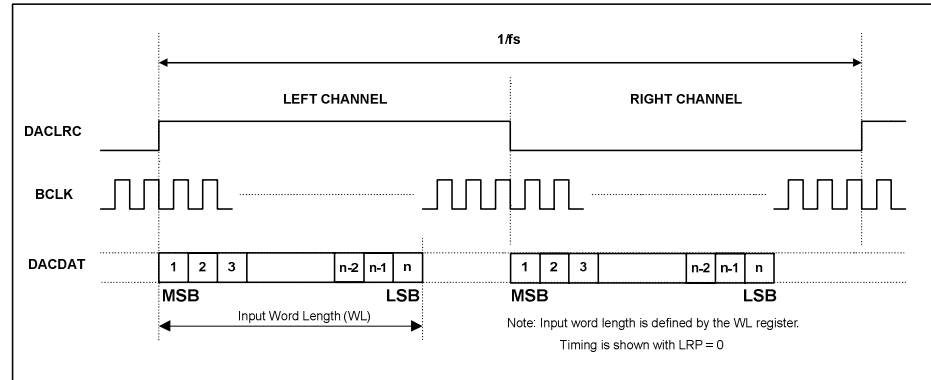


Figure 64 Left Justified Audio Interface (assuming n-bit word length)

In I<sup>2</sup>S mode, the MSB is available on the second rising edge of BCLK following a DACLRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

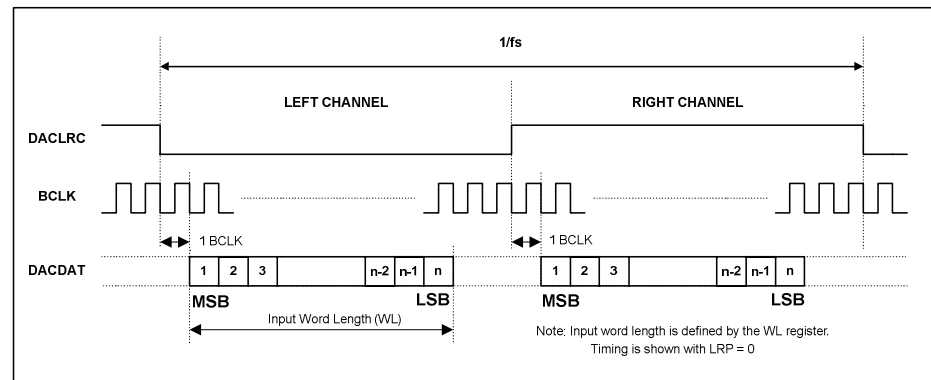


Figure 65 I<sup>2</sup>S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1<sup>st</sup> (mode B) or 2<sup>nd</sup> (mode A) rising edge of BCLK (selectable by AIF\_LRCLK\_INV) following a rising edge of DACLRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 66 and Figure 67. In device slave mode, Figure 68 and Figure 69, it is possible to use any length of frame pulse less than  $1/f_s$ , providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

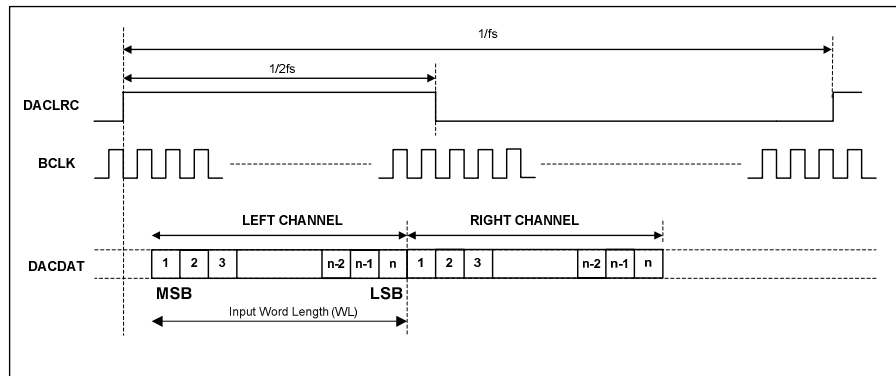


Figure 66 DSP Mode Audio Interface (mode A, AIF\_LRCLK\_INV=0, Master)

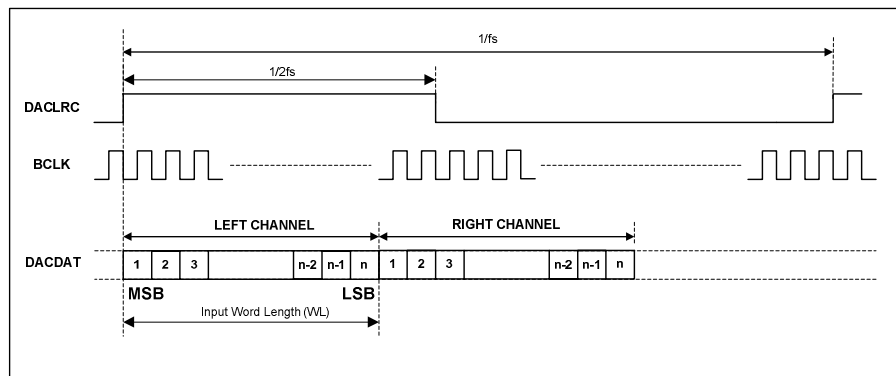


Figure 67 DSP Mode Audio Interface (mode B, AIF\_LRCLK\_INV=1, Master)

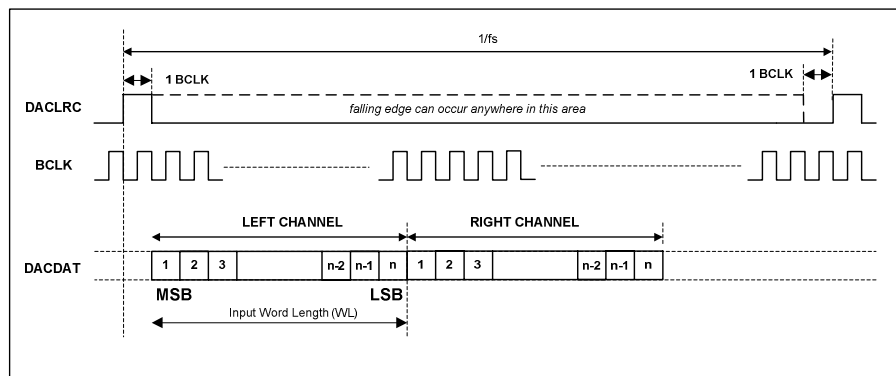


Figure 68 DSP Mode Audio Interface (mode A, AIF\_LRCLK\_INV=0, Slave)



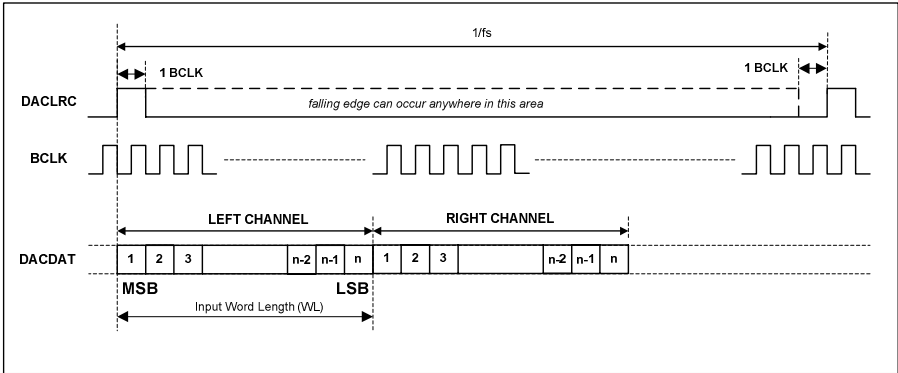


Figure 69 DSP Mode Audio Interface (mode B, AIF\_LRCLK\_INV=1, Slave)

PCM operation is supported in DSP interface mode. Mono PCM data received by the WM8959 will be treated as Left Channel data. This data may be routed to the Left/Right DACs as described in the "Digital Input Path" section.

**AUDIO DATA FORMATS (TDM MODE)**

TDM is supported in master and slave mode and is enabled by register bit AIF\_DAC\_TDM. All audio interface data formats support time division multiplexing (TDM) for DAC data.

Two time slots are available (Slot 0 and Slot 1), selected by register bit AIFDAC\_TDM\_CHAN which selects the time slot for the DAC data.

When TDM is enabled, BCLK frequency must be high enough to allow data from both time slots to be transferred. The relative timing of Slot 0 and Slot 1 depends upon the selected data format as shown in Figure 70 to Figure 74.

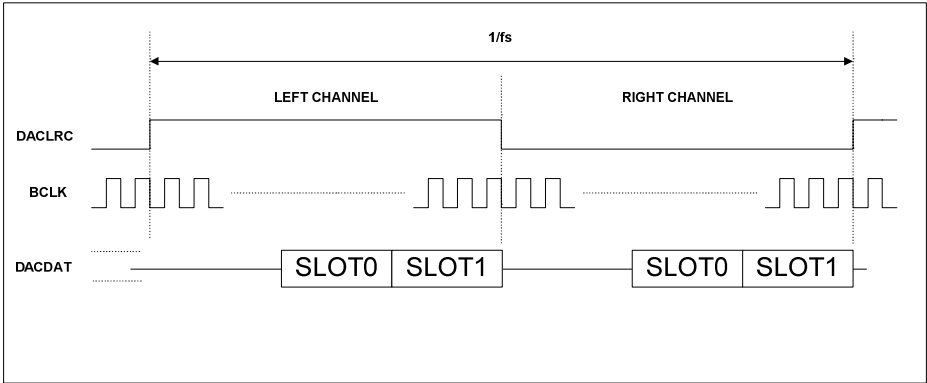


Figure 70 TDM in Right-Justified Mode

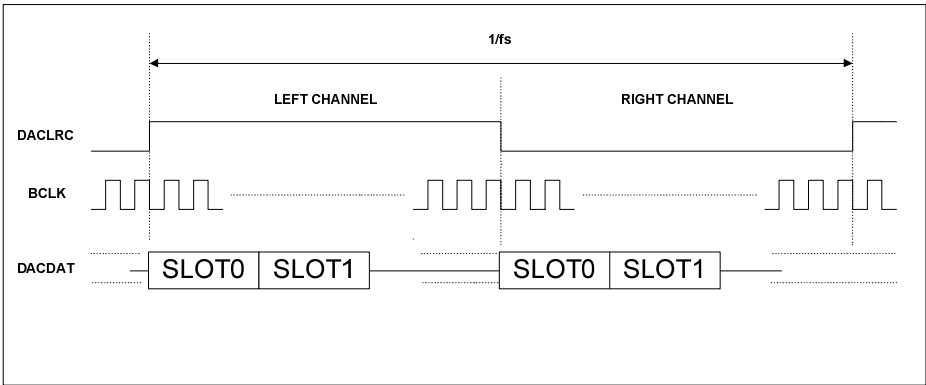


Figure 71 TDM in Left-Justified Mode

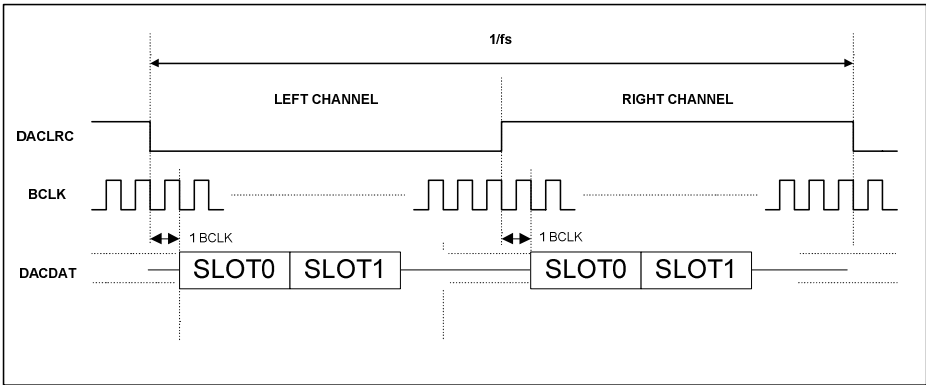


Figure 72 TDM in I<sup>2</sup>S Mode

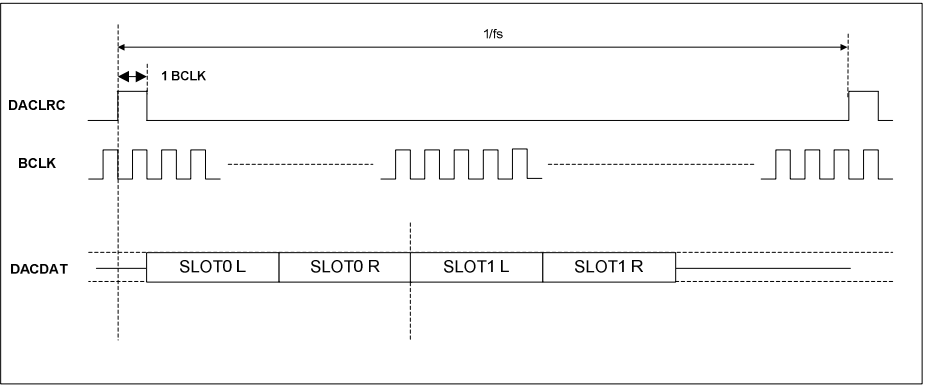


Figure 73 TDM in DSP Mode A

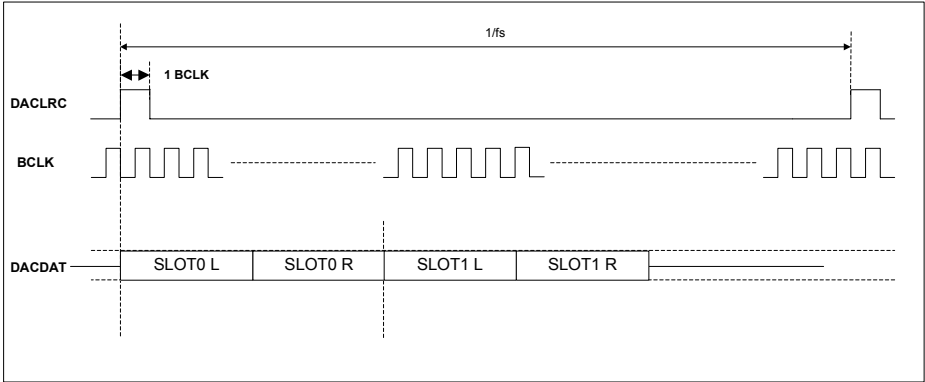


Figure 74 TDM in DSP Mode B

## DIGITAL AUDIO INTERFACE CONTROL

The register bits controlling audio data format, word length, left/right channel data source and TDM are summarised in Table 51.

| REGISTER ADDRESS | BIT | LABEL           | DEFAULT | DESCRIPTION  |
|------------------|-----|-----------------|---------|--|
| R4 (04h)         | 8   | AIF_BCLK_INV    | 0b      | BCLK Invert<br>0 = BCLK not inverted<br>1 = BCLK inverted  |
|                  | 7   | AIF_LRCLK_INV   | 0b      | Right, left and I <sup>2</sup> S modes – DACLRC polarity<br>0 = normal DACLRC polarity<br>1 = invert DACLRC polarity<br><br>DSP Mode – mode A/B select<br>0 = MSB is available on 2nd BCLK rising edge after DACLRC rising edge (mode A)<br>1 = MSB is available on 1st BCLK rising edge after DACLRC rising edge (mode B) |
|                  | 6:5 | AIF_WL [1:0]    | 10b     | Digital Audio Interface Word Length<br>00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits<br>11 = 32 bits<br>Note - see "Companding" for the selection of 8-bit mode   |
|                  | 4:3 | AIF_FMT [1:0]   | 10b     | Digital Audio Interface Format<br>00 = Right justified<br>01 = Left justified<br>10 = I <sup>2</sup> S Format<br>11 = DSP Mode   |
| R5 (05h)         | 15  | DACL_SRC        | 0b      | Left DAC Data Source Select<br>0 = Left DAC outputs left channel data<br>1 = Left DAC outputs right channel data   |
|                  | 14  | DACR_SRC        | 1b      | Right DAC Data Source Select<br>0 = Right DAC outputs left channel data<br>1 = Right DAC outputs right channel data  |
|                  | 12  | AIFDAC_TDM      | 0b      | DAC TDM Enable<br>0 = Normal DACDAT operation<br>1 = TDM enabled on DACDAT   |
|                  | 13  | AIFDAC_TDM_CHAN | 0b      | DACDAT TDM Channel Select<br>0 = DACDAT data input on slot 0<br>1 = DACDAT data input on slot 1  |

Table 51 Audio Data Format Control

## AUDIO INTERFACE OUTPUT AND GPIO TRISTATE

Register bit AIF\_TRIS can be used to tristate the audio interface and GPIO pins as described in Table 52.

All GPIO pins and digital audio interface pins will be tristated by this function, regardless of the state of other registers which control these pin configurations.

| REGISTER ADDRESS | BIT | LABEL    | DEFAULT | DESCRIPTION   |
|------------------|-----|----------|---------|---|
| R9 (09h)         | 13  | AIF_TRIS | 0       | Audio Interface and GPIO Tristate<br>0 = Audio interface and GPIO pins operate normally<br>1 = Tristate all audio interface and GPIO pins |

Table 52 Tri-stating the Audio Interface and GPIO Pins

### MASTER MODE BCLK AND DACLRC ENABLE

The main audio interface pins (BCLK, DACLRC and DACDAT) and the alternative interface pins (BCLK2, DACLRC2, DACDAT2) can be independently programmed to operate in master mode or slave mode using register bits AIF\_MSTR1 and AIF\_MSTR2.

When the main audio interface is operating in slave mode, the BCLK and DACLRC clock outputs to these pins are by default disabled to allow the digital audio source to drive these pins. Similarly, when the alternative audio interface is operating in slave mode, the BCLK2 and DACLRC2 clock outputs to these pins are by default disabled.

It is possible to force the DACLRC or DACLRC2 to be output using register bit DACLRC\_DIR, allowing mixed master and slave modes on the active audio interface. The active audio interface is selected by register bit AIF\_SEL. Enabled clock outputs on the de-selected audio interface will output logic 0.

The clock generators for the audio interface are enabled according to the control signals shown in Figure 75.

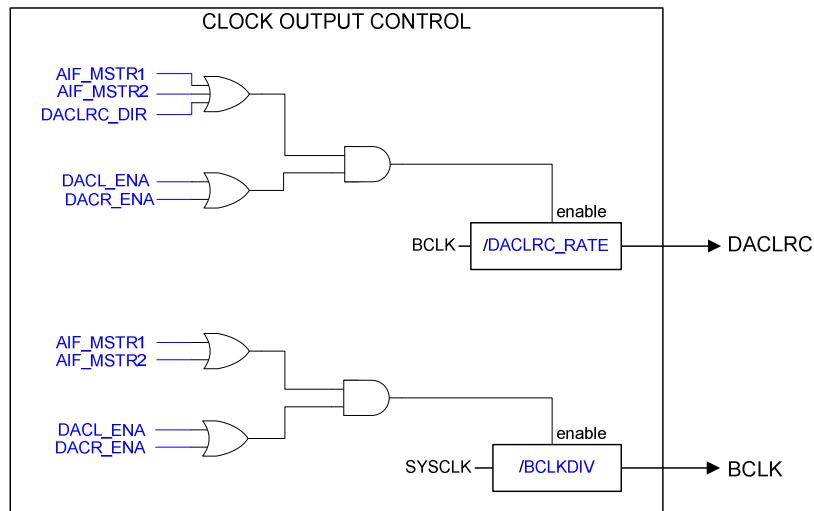


Figure 75 Clock Output Control

| REGISTER ADDRESS | BIT | LABEL      | DEFAULT | DESCRIPTION  |
|------------------|-----|------------|---------|--|
| R8 (08h)         | 15  | AIF_MSTR1  | 0b      | Audio Interface 1 Master Mode Select<br>0 = Slave mode<br>1 = Master mode  |
|                  | 14  | AIF_MSTR2  | 0b      | Audio Interface 2 Master Mode Select<br>0 = Slave mode<br>1 = Master mode  |
|                  | 13  | AIF_SEL    | 0b      | Audio Interface Select<br>0 = Audio interface 1<br>1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)                   |
| R9 (09h)         | 11  | DACLRC_DIR | 0b      | DACLRC Direction<br>(Forces DACLRC clock to be output in slave mode)<br>0 = DACLRC normal operation<br>1 = DACLRC clock output enabled |

| REGISTER ADDRESS | BIT  | LABEL                 | DEFAULT | DESCRIPTION   |
|------------------|------|-----------------------|---------|---|
|                  | 10:0 | DACLRC_RATE<br>[10:0] | 040h    | DACLRC Rate<br>DACLRC clock output = BCLK /<br>DACLRC_RATE<br><br>Integer (LSB = 1)<br>Valid from 8..2047 |

Table 53 Digital Audio Interface Clock Output Control

### COMPANDING

The WM8959 supports A-law and  $\mu$ -law companding as shown in Table 54.

| REGISTER ADDRESS | BIT | LABEL        | DEFAULT | DESCRIPTION  |
|------------------|-----|--------------|---------|--|
| R5 (05h)         | 4   | DAC_COMP     | 0b      | DAC Companding Enable<br>0 = disabled<br>1 = enabled |
|                  | 3   | DAC_COMPMODE | 0b      | DAC Companding Type<br>0 = $\mu$ -law<br>1 = A-law   |

Table 54 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

$\mu$ -law (where  $\mu=255$  for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad -1 \leq x \leq 1$$

A-law (where  $A=87.6$  for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \text{for } x \leq 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \text{for } 1/A \leq x \leq 1$$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for  $\mu$ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSBs of data.

Companding converts 13 bits ( $\mu$ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low amplitude signals than for high amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization. The companded signal is an 8-bit word comprising sign (1 bit), exponent (3 bits) and mantissa (4 bits).

8-bit mode is selected whenever DAC\_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per LRC frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting DAC\_COMPMODE=1 and DAC\_COMP=0.

| BIT7 | BIT[6:4] | BIT[3:0] |
|------|----------|----------|
| SIGN | EXPONENT | MANTISSA |

Table 55 8-bit Companded Word Composition

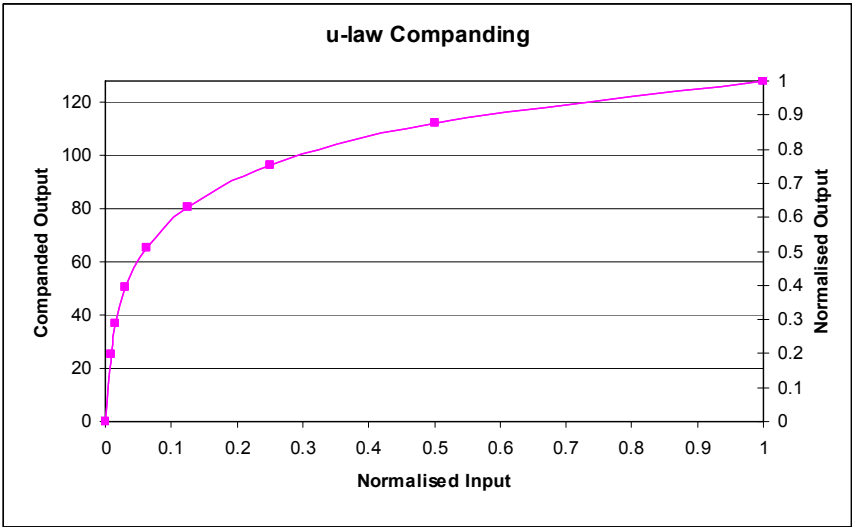


Figure 76  $\mu$ -Law Companding

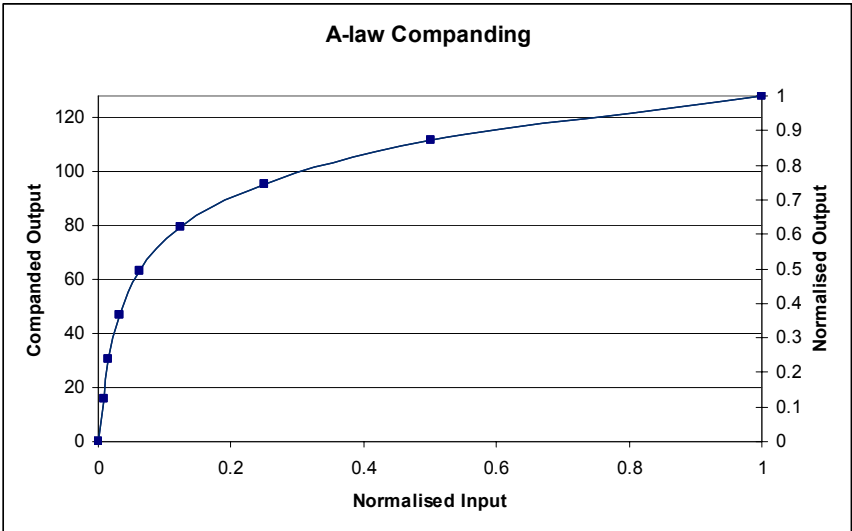


Figure 77 A-Law Companding

## CLOCKING AND SAMPLE RATES

The internal clocks for the DACs, DSP core functions, digital audio interface and Class D switching amplifier are all derived from a common internal clock source, SYSCLK.

SYSCLK can either be derived directly from MCLK, or may be generated from a PLL using MCLK as an external reference. Many commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the PLL provides additional flexibility for a wide range of MCLK frequencies. All clock configurations must be set up before enabling playback to avoid glitches.

The DAC sample rate is selectable, relative to SYSCLK by setting register field DAC\_CLKDIV. This field must be set according to the required sampling frequency and depending on the selected clocking mode (AIF\_LRCLKRATE).

In master mode, BCLK is also derived from SYSCLK via a programmable division set by BCLK\_DIV. The DACLRRC signal does not automatically match the DAC sample rates; this must be configured using DACLRRC\_RATE as described under "Digital Audio Interface Control".

A clock (OPCLK) derived from SYSCLK can be output on the GPIO pins to provide clocking for other parts of the system. This clock is enabled by OPCLK\_ENA and its frequency is set by OPCLKDIV.

A slow clock (TOCLK) derived from SYSCLK can be used to de-bounce the button/accessory detect inputs, and to set the timeout period for volume updates when zero-cross detect is used. This clock is enabled by TOCLK\_ENA and its frequency is set by TOCLK\_RATE.

The Class D switching amplifier requires a clock; this is derived from SYSCLK via a programmable divider DCLKDIV.

Table 56 to Table 62 show the clocking and sample rate controls for MCLK input, BCLK output (in master mode), DACs, class D outputs and GPIO clock output.

The overall clocking scheme for the WM8959 is illustrated in Figure 78.

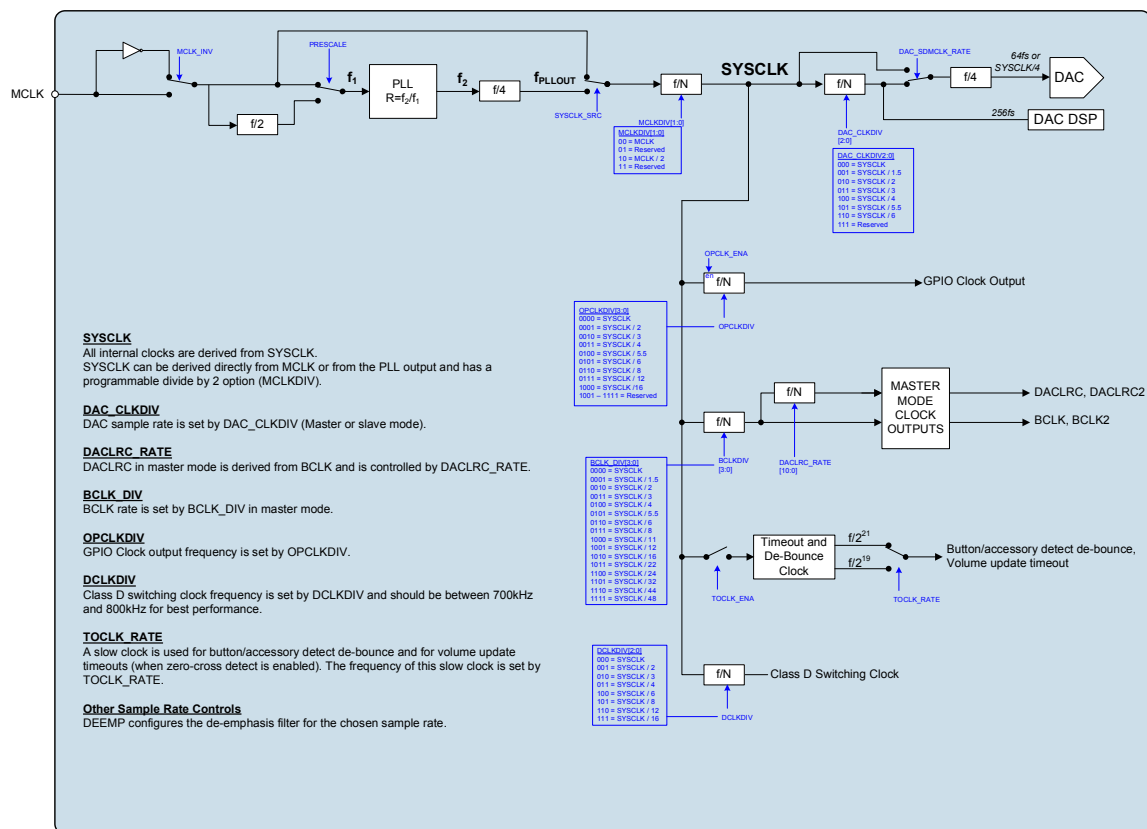


Figure 78 Clocking Scheme



**SYSCLK CONTROL**

MCLK may be inverted by setting register bit MCLK\_INV. Note that it is not recommended to change the control bit MCLK\_INV while the WM8959 is processing data as this may lead to clock glitches and signal pop and clicks.

The SYSCLK\_SRC bit is used to select the source for SYSCLK. The source may be either MCLK or the PLL output. The selected source is divided by the SYSCLK pre-divider MCLK\_DIV to generate SYSCLK. The selected source may also be adjusted by the MCLK\_DIV divider. These register fields are described in Table 56. See "PLL" for more details of the Phase Locked Loop clock generator.

The WM8959 supports glitch-free SYSCLK source selection. When both clock sources are running and SYSCLK\_SRC is modified to select one of these clocks, a glitch-free clock transition will take place. The de-glitching circuit will ensure that the minimum pulse width will be no less than the pulse width of the faster of the two clock sources.

When the initial clock source is to be disabled before changing to the new clock source, the CLK\_FORCE bit must also be used to force the clock source transition to take place. In this case, glitch-free operation cannot be guaranteed.

| REGISTER ADDRESS | BIT   | LABEL          | DEFAULT | DESCRIPTION   |
|------------------|-------|----------------|---------|---|
| R7 (07h)         | 14    | SYSCLK_SRC     | 0b      | SYSCLK Source Select<br>0 = MCLK<br>1 = PLL output  |
|                  | 13    | CLK_FORCE      | 0b      | Forces Clock Source Selection<br>0 = Existing SYSCLK source (MCLK or PLL output) must be active when changing to a new clock source.<br>1 = Allows existing MCLK source to be disabled before changing to a new clock source. |
|                  | 12:11 | MCLK_DIV [1:0] | 00b     | SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK.<br>00 = Divide SYSCLK by 1<br>01 = Reserved<br>10 = Divide SYSCLK by 2<br>11 = Reserved                               |
|                  | 10    | MCLK_INV       | 0b      | MCLK Invert<br>0 = Master clock not inverted<br>1 = Master clock inverted   |

**Table 56 MCLK and SYSCLK Control**

### DAC SAMPLE RATES

The DAC sample rate is selectable, relative to SYSCLK, by setting the register field DAC\_CLKDIV. This field must be set according to the SYSCLK frequency, and according to the selected clocking mode.

Two clocking modes are provided - Normal Mode (AIF\_LRCLKRATE = 0) allows selection of the commonly used sample rates from typical audio system clocking frequencies (eg. 12.288MHz); USB Mode (AIF\_LRCLKRATE = 1) allows many of these sample rates to be generated from a 12MHz USB clock. Depending on the available clock sources, the USB mode may be used to save power by supporting 44.1kHz operation without requiring the PLL.

The AIF\_LRCLKRATE field must be set as described in Table 57 to ensure correct operation of internal functions according to the SYSCLK / Fs ratio. Table 58 describes the available sample rates using four different common MCLK frequencies.

In Normal mode, the programmable division set by DAC\_CLKDIV must ensure that a  $256 * \text{DAC } F_s$  clock is generated for the DAC DSP.

In USB mode, the programmable division set by DAC\_CLKDIV must ensure that a  $272 * \text{DAC } F_s$  clock is generated for the DAC DSP.

Note that in USB mode, the DAC sample rate does not match exactly with the commonly used sample rates (e.g. 44.118 kHz instead of 44.100 kHz). At most, the difference is less than 0.5%. Data recorded at 44.100 kHz sample rate and replayed at 44.118 kHz will experience a slight (sub 0.5%) pitch shift as a result of this difference. Note also the USB mode cannot be used to generate a 48kHz samples rate from a 12MHz MCLK. The PLL should be used in this case.

In low sample rate modes (eg. 8kHz voice), the SNR is liable to be degraded if the typical 64fs DAC clocking rate is used (see Figure 28). In this case, it may be possible to improve the SNR by raising the DAC clocking rate by setting the DAC\_SDMCLK\_RATE register field, causing the DAC clocking rate to be set equal to  $\text{SYSCLK}/4$ . The DAC\_CLKDIV field must still be set as described above to derive the correct clock for the DAC DSP. In 8kHz voice applications, in systems where  $\text{SYSCLK} > 256f_s$  (or  $272f_s$  when applicable), setting DAC\_SDMCLK\_RATE will result in the SNR performance being improved. Note that setting DAC\_SDMCLK\_RATE will result in an increase in power consumption.

| REGISTER ADDRESS | BIT | LABEL               | DEFAULT | DESCRIPTION  |
|------------------|-----|---------------------|---------|--|
| R7 (07h)         | 4:2 | DAC_CLKDIV<br>[2:0] | 000b    | DAC Sample Rate Divider<br>000 = $\text{SYSCLK} / 1.0$<br>001 = $\text{SYSCLK} / 1.5$<br>010 = $\text{SYSCLK} / 2.0$<br>011 = $\text{SYSCLK} / 3.0$<br>100 = $\text{SYSCLK} / 4.0$<br>101 = $\text{SYSCLK} / 5.5$<br>110 = $\text{SYSCLK} / 6.0$<br>111 = Reserved |
| R10 (0Ah)        | 12  | DAC_SDMCLK_RATE     | 0b      | DAC clocking rate<br>0 = Normal operation (64fs)<br>1 = $\text{SYSCLK}/4$  |
|                  | 10  | AIF_LRCLKRATE       | 0b      | LRCLK Rate<br>0 = Normal mode ( $256 * f_s$ )<br>1 = USB mode ( $272 * f_s$ )  |

Table 57 DAC Sample Rate Control

| SYCLK       | SAMPLE RATE DIVIDER | CLOCKING MODE          | SAMPLE RATE |
|-------------|---------------------|------------------------|-------------|
| 12.288 MHz  | 000 = SYCLK / 1     | Normal<br>(256 * Fs)   | 48 kHz      |
|             | 001 = SYCLK / 1.5   |                        | 32 kHz      |
|             | 010 = SYCLK / 2     |                        | 24 kHz      |
|             | 011 = SYCLK / 3     |                        | 16 kHz      |
|             | 100 = SYCLK / 4     |                        | 12 kHz      |
|             | 101 = SYCLK / 5.5   |                        | Not used    |
|             | 110 = SYCLK / 6     |                        | 8 kHz       |
|             | 111 = Reserved      |                        | Reserved    |
| 11.2896 MHz | 000 = SYCLK / 1     | Normal<br>(256 * Fs)   | 44.1 kHz    |
|             | 001 = SYCLK / 1.5   |                        | Not used    |
|             | 010 = SYCLK / 2     |                        | 22.05 kHz   |
|             | 011 = SYCLK / 3     |                        | Not used    |
|             | 100 = SYCLK / 4     |                        | 11.025 kHz  |
|             | 101 = SYCLK / 5.5   |                        | 8.018 kHz   |
|             | 110 = SYCLK / 6     |                        | Not used    |
|             | 111 = Reserved      |                        | Reserved    |
| 12 MHz      | 000 = SYCLK / 1     | USB Mode<br>(272 * Fs) | 44.118 kHz  |
|             | 001 = SYCLK / 1.5   |                        | Not used    |
|             | 010 = SYCLK / 2     |                        | 22.059 kHz  |
|             | 011 = SYCLK / 3     |                        | Not used    |
|             | 100 = SYCLK / 4     |                        | 11.029 kHz  |
|             | 101 = SYCLK / 5.5   |                        | 8.021 kHz   |
|             | 110 = SYCLK / 6     |                        | Not used    |
|             | 111 = Reserved      |                        | Reserved    |
| 2.048 MHz   | 000 = SYCLK / 1     | Normal<br>(256 * Fs)   | 8 kHz       |
|             | 001 = SYCLK / 1.5   |                        | Not used    |
|             | 010 = SYCLK / 2     |                        | Not used    |
|             | 011 = SYCLK / 3     |                        | Not used    |
|             | 100 = SYCLK / 4     |                        | Not used    |
|             | 101 = SYCLK / 5.5   |                        | Not used    |
|             | 110 = SYCLK / 6     |                        | Not used    |
|             | 111 = Reserved      |                        | Reserved    |

Table 58 DAC Sample Rates

**BCLK CONTROL**

In Master Mode, BCLK is derived from SYSCLK via a programmable division set by BCLK\_DIV, as described in Table 59. BCLK\_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words to the DACs.

In Slave Mode, BCLK is generated externally and appears as an input to the DAC. The host device must provide sufficient BCLK cycles to transfer complete data words to the DACs.

| REGISTER ADDRESS | BIT | LABEL             | DEFAULT | DESCRIPTION  |
|------------------|-----|-------------------|---------|--|
| R6 (06h)         | 4:1 | BCLK_DIV<br>[3:0] | 0100b   | BCLK Frequency (Master Mode)<br>0000 = SYSCLK<br>0001 = SYSCLK / 1.5<br>0010 = SYSCLK / 2<br>0011 = SYSCLK / 3<br>0100 = SYSCLK / 4<br>0101 = SYSCLK / 5.5<br>0110 = SYSCLK / 6<br>0111 = SYSCLK / 8<br>1000 = SYSCLK / 11<br>1001 = SYSCLK / 12<br>1010 = SYSCLK / 16<br>1011 = SYSCLK / 22<br>1100 = SYSCLK / 24<br>1101 = SYSCLK / 32<br>1110 = SYSCLK / 44<br>1111 = SYSCLK / 48 |

Table 59 BCLK Control

**OPCLK CONTROL**

A clock output (OPCLK) derived from SYSCLK may be output via GPIO1 or GPIO3 to GPIO5. This clock is enabled by register bit OPCLK\_ENA, and its frequency is controlled by OPCLKDIV.

This output of this clock is also dependent upon the GPIO register settings described under "General Purpose Input/Output".

| REGISTER ADDRESS | BIT  | LABEL             | DEFAULT | DESCRIPTION   |
|------------------|------|-------------------|---------|---|
| R6 (06h)         | 12:9 | OPCLKDIV<br>[3:0] | 0000b   | GPIO Output Clock Divider<br>0000 = SYSCLK<br>0001 = SYSCLK / 2<br>0010 = SYSCLK / 3<br>0011 = SYSCLK / 4<br>0100 = SYSCLK / 5.5<br>0101 = SYSCLK / 6<br>0110 = SYSCLK / 8<br>0111 = SYSCLK / 12<br>1000 = SYSCLK / 16<br>1001 to 1111 = Reserved |
| R2 (02h)         | 11   | OPCLK_ENA<br>(rw) | 0b      | GPIO Clock Output Enable<br>0 = disabled<br>1 = enabled   |

Table 60 OPCLK Control

**CLASS D SWITCHING CLOCK**

The Class D switching clock is derived from SYSCLK as determined by register field DCLKDIV as described in Table 61. This clock should be set to between 700kHz and 800kHz for optimum performance. The class D switching clock should not be disabled when the speaker output is active, as this will prevent the speaker outputs from functioning. The class D switching clock frequency should not be altered while the speaker output is active as this may generate an audible click.

| REGISTER ADDRESS | BIT | LABEL            | DEFAULT | DESCRIPTION   |
|------------------|-----|------------------|---------|---|
| R6 (06h)         | 8:6 | DCLKDIV<br>[2:0] | 111b    | Class D Clock Divider<br>000 = SYSCLK<br>001 = SYSCLK / 2<br>010 = SYSCLK / 3<br>011 = SYSCLK / 4<br>100 = SYSCLK / 6<br>101 = SYSCLK / 8<br>110 = SYSCLK / 12<br>111 = SYSCLK / 16 |

Table 61 DCLK Control

**TOCLK CONTROL**

A slow clock (TOCLK) is derived from SYSCLK to enable input de-bouncing and volume update timeout functions. This clock is enabled by register bit TOCLK\_ENA, and its frequency is controlled by TOCLK\_RATE, as described in Table 62.

| REGISTER ADDRESS | BIT | LABEL      | DEFAULT | DESCRIPTION   |
|------------------|-----|------------|---------|---|
| R6 (06h)         | 15  | TOCLK_RATE | 0b      | Timeout Clock Rate<br>(Selects clock to be used for volume update timeout and GPIO input de-bounce)<br>0 = SYSCLK / 2 <sup>21</sup> (Slower Response)<br>1 = SYSCLK / 2 <sup>19</sup> (Faster Response) |
|                  | 14  | TOCLK_ENA  | 0b      | Timeout Clock Enable<br>(This clock is required for volume update timeout and GPIO input de-bounce)<br>0 = disabled<br>1 = enabled  |

Table 62 TOCLK Control

**USB MODE**

It is possible to reduce power consumption by disabling the PLL in some applications. One such application is when SYSCLK is generated from a 12MHz USB clock source. Setting the AIF\_LRCLKRATE bit as described earlier (see "DAC Sample Rates") allows a sample rate close to 44.1kHz to be generated with no additional PLL power consumption.

In this configuration, SYSCLK must be driven directly from MCLK (or MCLK2) and by disabling the PLL. This is achieved by setting SYSCLK\_SRC=0, PLL\_ENA=0.

| REGISTER ADDRESS | BIT | LABEL         | DEFAULT | DESCRIPTION   |
|------------------|-----|---------------|---------|---|
| R10 (0Ah)        | 10  | AIF_LRCLKRATE | 0b      | LRCLK Rate<br>0 = Normal mode (256 * fs)<br>1 = USB mode (272 * fs) |

Table 63 USB Mode Control

## PLL

The integrated PLL can be used to generate SYSCLK for the WM8959 from a wide range of MCLK reference frequencies. The PLL is enabled by the PLL\_ENA register bit. If required, the input reference clock can be divided by 2 by setting the register bit PRESCALE.

The PLL frequency ratio R is equal to  $f_2/f_1$  (see Figure 78). This ratio is the real number represented by register fields PLLN and PLLK, where PLLN is an integer (LSB = 1) and PLLK is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field SDM. De-selection of fractional mode results in lower power consumption.

For PLL stability, input frequencies and divisions must be chosen so that  $5 \leq \text{PLLN} \leq 13$ . Best performance is achieved for  $7 \leq N \leq 9$ . Also, the PLL performs best when  $f_2$  is set between 90MHz and 100MHz.

If PLLK is regarded as a 16-bit integer (instead of a fractional quantity), then PLLN and PLLK may be determined as follows:

- $\text{PLLN} = \text{int } R$
- $\text{PLLK} = \text{int } (2^{16} (R - \text{PLLN}))$

The PLL Control register settings are described in Table 64.

| REGISTER ADDRESS | BIT | LABEL           | DEFAULT | DESCRIPTION   |
|------------------|-----|-----------------|---------|---|
| R2 (02h)         | 15  | PLL_ENA<br>(rw) | 0       | PLL Enable<br>0 = disabled<br>1 = enabled                               |
| R60 (3Ch)        | 7   | SDM             | 0       | Enable PLL Integer Mode<br>0 = Integer mode<br>1 = Fractional mode      |
|                  | 6   | PRESCALE        | 0b      | Divide MCLK by 2 at PLL input<br>0 = Divide by 1<br>1 = Divide by 2     |
|                  | 3:0 | PLLN [3:0]      | 8h      | Integer (N) part of PLL frequency ratio.                                |
| R61 (3Dh)        | 7:0 | PLLK [15:8]     | 31h     | Fractional (K) part of PLL frequency ratio.<br>(Most significant bits)  |
| R62 (3Eh)        | 7:0 | PLLK [7:0]      | 26h     | Fractional (K) part of PLL frequency ratio.<br>(Least significant bits) |

**Table 64 PLL Control**

## EXAMPLE PLL CALCULATION

To generate 12.288MHz SYSCLK from a 12MHz reference clock:

There is a fixed divide by 4 at the PLL output (see Figure 78) followed by a selectable divide by 2 in the same path. PLL output  $f_2$  should be set in the range 90MHz - 100MHz. Enabling the divide by 2 (MCLK\_DIV = 10b) sets the required  $f_2 = 4 \times 2 \times 12.288\text{MHz} = 98.304\text{MHz}$ .

There is a selectable pre-scale (divide MCLK by 2) at the PLL input ( $f_1$  - see Figure 75). The PLL frequency ratio  $f_2/f_1$  must be set in the range 5 - 13. Disabling the MCLK pre-scale (PRESCALE = 0b) sets the required ratio  $f_2/f_1 = 8.192$ .

The required settings for this example are:

- MCLK\_DIV = 10b
- PRESCALE = 0b
- PLL\_ENA = 1
- SDM = 1
- PLLN = 8 = 8h
- PLLK = 0.192 = 3126h

#### EXAMPLE PLL SETTINGS

Table 65 provides example PLL settings for generating common SYSCLK frequencies from a variety of MCLK reference frequencies.

| MCLK (MHZ) | SYSCLK (MHZ) | MCLKDIV | F2<br>= SYSCLK *<br>4 * MCLKDIV | PRESCALE | F1<br>= MCLK/<br>PRESCALE | R<br>= F2/F1 | N  | K     |
|------------|--------------|---------|---------------------------------|----------|---------------------------|--------------|----|-------|
| 12         | 11.2896      | 2       | 90.3168                         | 1        | 12                        | 7.5264       | 7h | 86C2h |
| 12         | 12.288       | 2       | 98.304                          | 1        | 12                        | 8.192        | 8h | 3126h |
| 13         | 11.2896      | 2       | 90.3168                         | 1        | 13                        | 6.947446     | 6h | F28Bh |
| 13         | 12.288       | 2       | 98.304                          | 1        | 13                        | 7.561846     | 7h | 8FD5h |
| 14.4       | 11.2896      | 2       | 90.3168                         | 1        | 14.4                      | 6.272        | 6h | 45A1h |
| 14.4       | 12.288       | 2       | 98.304                          | 1        | 14.4                      | 6.826667     | 6h | D3A0h |
| 19.2       | 11.2896      | 2       | 90.3168                         | 2        | 9.6                       | 9.408        | 9h | 6872h |
| 19.2       | 12.288       | 2       | 98.304                          | 2        | 9.6                       | 10.24        | Ah | 3D70h |
| 19.68      | 11.2896      | 2       | 90.3168                         | 2        | 9.84                      | 9.178537     | 9h | 2DB4h |
| 19.68      | 12.288       | 2       | 98.304                          | 2        | 9.84                      | 9.990243     | 9h | FD80h |
| 19.8       | 11.2896      | 2       | 90.3168                         | 2        | 9.9                       | 9.122909     | 9h | 1F76h |
| 19.8       | 12.288       | 2       | 98.304                          | 2        | 9.9                       | 9.929697     | 9h | EE00h |
| 24         | 11.2896      | 2       | 90.3168                         | 2        | 12                        | 7.5264       | 7h | 86C2h |
| 24         | 12.288       | 2       | 98.304                          | 2        | 12                        | 8.192        | 8h | 3126h |
| 26         | 11.2896      | 2       | 90.3168                         | 2        | 13                        | 6.947446     | 6h | F28Bh |
| 26         | 12.288       | 2       | 98.304                          | 2        | 13                        | 7.561846     | 7h | 8FD5h |
| 27         | 11.2896      | 2       | 90.3168                         | 2        | 13.5                      | 6.690133     | 6h | B0ACh |
| 27         | 12.288       | 2       | 98.304                          | 2        | 13.5                      | 7.281778     | 7h | 4822h |

Table 65 PLL Frequency Examples

## CONTROL INTERFACE

The WM8959 is controlled by writing to its control registers. Readback is available for certain registers, including device ID, power management registers and some GPIO status bits. The control interface can operate as either a 2-, 3- or 4-wire control interface, with additional variants as detailed below:

1. 2-wire
  - open-drain
2. 3-wire
  - push 0/1
  - open drain
3. 4-wire
  - push 0/1
  - wired-OR

Readback is provided on the bi-directional pin SDIN in 2-/3-wire modes and on a GPIO pin in 4-wire mode.

### SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS

MODE pin determines the 2- or 3-/4-wire mode as shown in Table 66.

| MODE | INTERFACE FORMAT |
|------|------------------|
| Low  | 2 wire           |
| High | 3- or 4- wire    |

**Table 66 Control Interface Mode Selection**

### 2-WIRE SERIAL CONTROL MODE

The WM8959 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 24 bits. The first 8 bits (B23 to B16) are address bits that select which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 8-bit address of each register in the WM8959). The default device address is 0011010 (0x34h).

The WM8959 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8959, then the WM8959 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8959 returns to the idle condition and wait for a new start condition and valid address.

The WM8959 supports a multitude of read and write operations, which are:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment



These modes are shown in the section below. Terminology used in the following figures:

| TERMINOLOGY | DESCRIPTION     |                       |
|-------------|-----------------|-----------------------|
| S           | Start Condition |                       |
| Sr          | Repeated start  |                       |
| A           | Acknowledge     |                       |
| P           | Stop Condition  |                       |
| R $\bar{W}$ | ReadNotWrite    | 0 = Write<br>1 = Read |

Table 67 Terminology

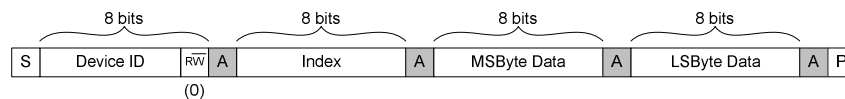


Figure 79 2-Wire Serial Control Interface (single write)

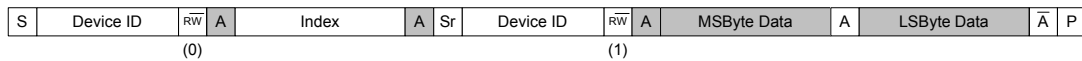


Figure 80 2-Wire Serial Control Interface (single read)

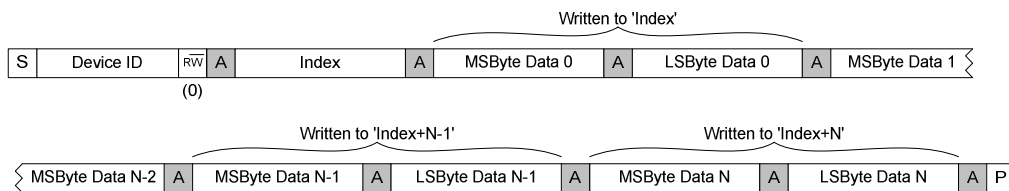


Figure 81 2-Wire Serial Control Interface (multiple write using auto-increment)

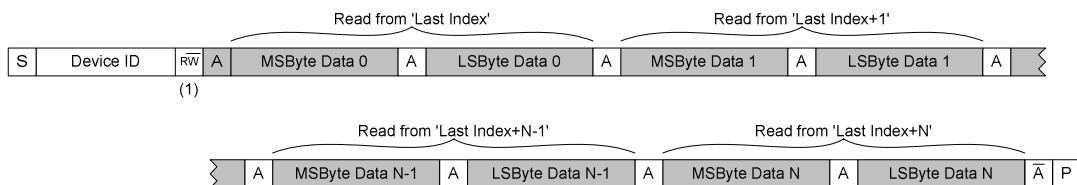


Figure 82 2-Wire Serial Control Interface (multiple read using auto-increment)

In 2-wire mode, the WM8959 has two possible device addresses, which can be selected using the CSB/ADDR pin.

| CSB/ADDR STATE | DEVICE ADDRESS    |
|----------------|-------------------|
| Low            | 0011010 (0 x 34h) |
| High           | 0011011 (0 x 36h) |

Table 68 2-Wire Control Interface Address Selection

### 3-WIRE / 4-WIRE SERIAL CONTROL MODES

The WM8959 is controlled by writing to registers through a 3- or 4-wire serial control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/W), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

The 3- or 4-wire modes are selected by the RD\_3W\_ENA register bit. Additionally the MODE\_3W4W control bit can be used to select between push 0/1 and open-drain or wired-OR modes, as described in Table 69 below.

| REGISTER ADDRESS | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|------------------|-----|-----------|---------|--|
| R22 (16h)        | 15  | RD_3W_ENA | 1b      | 3- / 4-wire readback configuration<br>1 = 3-wire mode<br>0 = 4-wire mode, using GPIO pin     |
|                  | 14  | MODE_3W4W | 0b      | 3-wire mode<br>0 = push 0/1<br>1 = open-drain<br>4-wire mode<br>0 = push 0/1<br>1 = wired-OR |

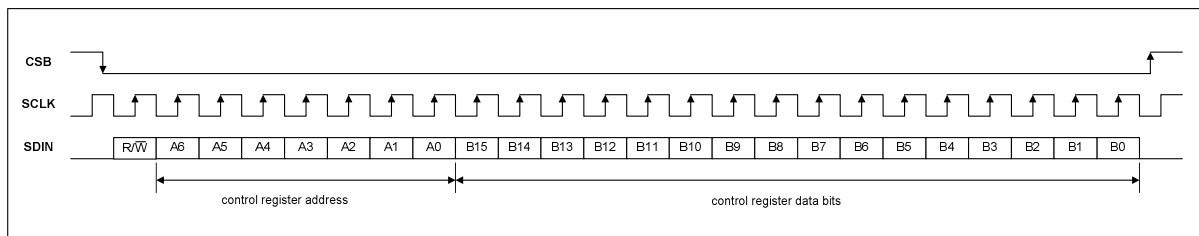
**Table 69 3-Wire / 4-Wire Control Interface Selection**

3-wire control mode is selected by setting RD\_3W\_ENA = 1. In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/ADDR latches in a complete control word consisting of the last 24 bits.

In Write operations (R/W=0), all SDIN bits are driven by the controlling device.

In Read operations (R/W=1), the SDIN pin is driven by the controlling device to clock in the register address, after which the WM8959 drives the SDIN pin to output the applicable data bits.

The 3-wire control mode timing is illustrated in Figure 83.



**Figure 83 3-Wire Serial Control Interface**

4-wire control mode is selected by setting RD\_3W\_ENA = 0.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), a GPIO pin must be selected to output SDOOUT by setting GPIO<sub>n</sub>\_SEL=0110b (n= 1, 3, 4 or 5). In this mode, the SDIN pin is ignored following receipt of the valid register address. SDOOUT is driven by the WM8959.

In 4-wire Push 0/1 mode, SDOOUT is driven low when not outputting register data bits. In Wired-OR mode, SDOOUT is undriven when not outputting register data bits.

The 4-wire control mode timing is illustrated in Figure 84 and Figure 85.

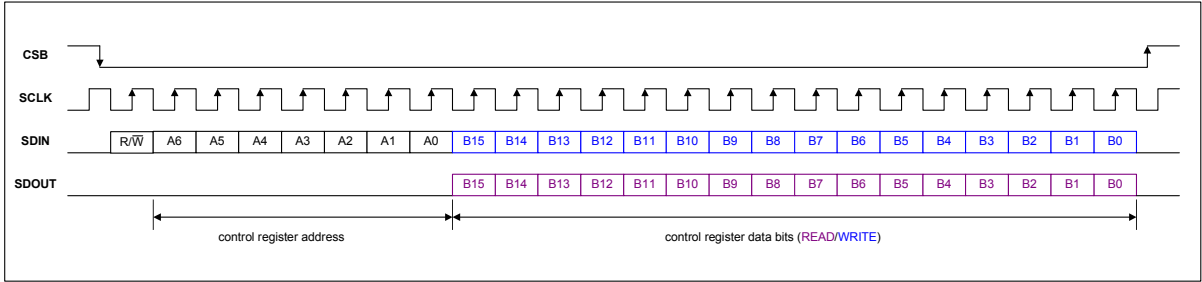


Figure 84 4-Wire Readback (Push 0/1)

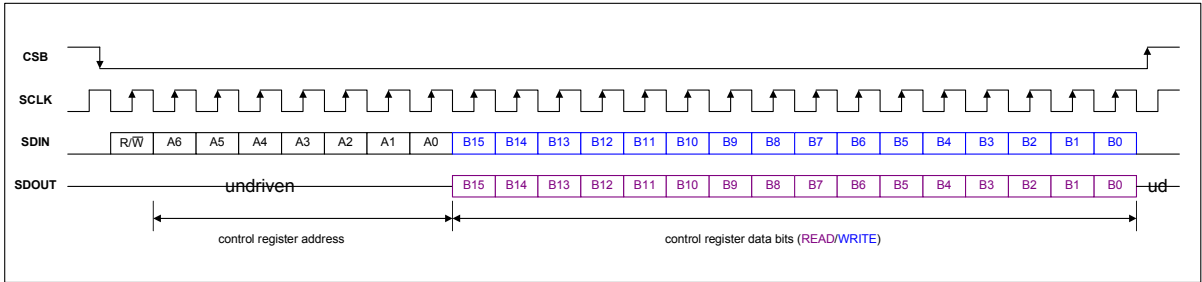


Figure 85 4-Wire Readback (wired-OR)

## POWER MANAGEMENT

## POWER MANAGEMENT REGISTERS

The WM8959 has three control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable functions in the correct order. See "Pop Suppression Control" for further details of recommended control sequences.

| REGISTER ADDRESS | BIT | LABEL                      | DEFAULT | DESCRIPTION   |
|------------------|-----|----------------------------|---------|---|
| R1 (1h)          | 12  | SPK_ENA<br>(rw)            | 0b      | SPKMIX Mixer, Speaker PGA and Speaker Output Enable<br>0 = disabled<br>1 = enabled  |
|                  | 11  | OUT3_ENA<br>(rw)           | 0b      | OUT3 and OUT3MIX Enable<br>0 = disabled<br>1 = enabled  |
|                  | 10  | OUT4_ENA<br>(rw)           | 0b      | OUT4 and OUT4MIX Enable<br>0 = disabled<br>1 = enabled  |
|                  | 9   | LOUT_ENA<br>(rw)           | 0b      | LOUT (Left Headphone Output) Enable<br>0 = disabled<br>1 = enabled  |
|                  | 8   | ROUT_ENA<br>(rw)           | 0b      | ROUT (Right Headphone Output) Enable<br>0 = disabled<br>1 = enabled   |
|                  | 4   | MICBIAS_ENA<br>(rw)        | 0b      | MICBIAS Enable<br>0 = OFF (high impedance output)<br>1 = ON   |
|                  | 2:1 | VMID_MODE<br>[1:0]<br>(rw) | 00b     | Vmid Divider Enable and Select<br>00 = Vmid disabled (for OFF mode)<br>01 = 2 x 50kΩ divider (Normal mode)<br>10 = 2 x 250kΩ divider (Standby mode)<br>11 = 2 x 5kΩ divider (for fast start-up) |
|                  | 0   | VREF_ENA<br>(rw)           | 0b      | VREF Enable (Bias for all analogue functions)<br>0 = VREF bias disabled<br>1 = VREF bias enabled  |
| R2 (02h)         | 15  | PLL_ENA<br>(rw)            | 0b      | PLL Enable<br>0 = disabled<br>1 = enabled   |
|                  | 14  | TSHUT_ENA<br>(rw)          | 0b      | Thermal Sensor Enable<br>0 = Thermal sensor disabled<br>1 = Thermal sensor enabled  |
|                  | 13  | TSHUT_OPDIS<br>(rw)        | 1b      | Thermal Shutdown Enable<br>(Requires thermal sensor to be enabled)<br>0 = Thermal shutdown disabled<br>1 = Thermal shutdown enabled   |
|                  | 11  | OPCLK_ENA<br>(rw)          | 0b      | GPIO Clock Output Enable<br>0 = disabled<br>1 = enabled   |
|                  | 9   | AINL_ENA<br>(rw)           | 0b      | Left Input Path Enable<br>(Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX)<br>0 = disabled<br>1 = enabled  |

| REGISTER ADDRESS | BIT | LABEL              | DEFAULT | DESCRIPTION   |
|------------------|-----|--------------------|---------|---|
|                  | 8   | AINR_ENA<br>(rw)   | 0b      | Right Input Path Enable (Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX)<br>0 = disabled<br>1 = enabled                  |
|                  | 7   | LIN34_ENA<br>(rw)  | 0b      | LIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                  | 6   | LIN12_ENA<br>(rw)  | 0b      | LIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                  | 5   | RIN34_ENA<br>(rw)  | 0b      | RIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                  | 4   | RIN12_ENA<br>(rw)  | 0b      | RIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
| R3 (03h)         | 13  | LON_ENA<br>(rw)    | 0b      | LON Line Out and LONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 12  | LOP_ENA<br>(rw)    | 0b      | LOP Line Out and LOPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 11  | RON_ENA<br>(rw)    | 0b      | RON Line Out and RONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 10  | ROP_ENA<br>(rw)    | 0b      | ROP Line Out and ROPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                  | 8   | SPKPGA_ENA<br>(rw) | 0b      | SPKMIX Mixer and Speaker PGA Enable<br>0 = disabled<br>1 = enabled<br>Note that SPKMIX and SPKPGA are also enabled when SPK_ENA is set. |
|                  | 7   | LOPGA_ENA<br>(rw)  | 0b      | LOPGA Left Volume Control Enable<br>0 = disabled<br>1 = enabled   |
|                  | 6   | ROPGA_ENA<br>(rw)  | 0b      | ROPGA Right Volume Control Enable<br>0 = disabled<br>1 = enabled  |
|                  | 5   | LOMIX_ENA<br>(rw)  | 0b      | LOMIX Left Output Mixer Enable<br>0 = disabled<br>1 = enabled   |
|                  | 4   | ROMIX_ENA<br>(rw)  | 0b      | ROMIX Right Output Mixer Enable<br>0 = disabled<br>1 = enabled  |
|                  | 1   | DACL_ENA<br>(rw)   | 0b      | Left DAC Enable<br>0 = disabled<br>1 = enabled  |
|                  | 0   | DACR_ENA<br>(rw)   | 0b      | Right DAC Enable<br>0 = disabled<br>1 = enabled   |

Table 70 Power Management

**CHIP RESET AND ID**

The device ID can be read back from register 0. Writing to this register will reset the device.

| REGISTER ADDRESS       | BIT  | LABEL                                  | DEFAULT | DESCRIPTION   |
|------------------------|------|--|---------|---|
| R0 (00h)<br>Reset / ID | 15:0 | SW_RESET_<br>CHIP_ID<br>[15:0]<br>(rr) | 8990h   | Writing to this register resets all registers to their default state.<br>Reading from this register will indicate device family ID 8990h. |

Table 71 Chip Reset and ID

**SAVING POWER AT HIGHER SUPPLY VOLTAGE**

The AVDD supply of the WM8959 can operate between 2.7V and 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 2.7V. At lower voltages, performance can be improved by increasing the bias current. If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown in Table 72.

| REGISTER ADDRESS | BIT | LABEL         | DEFAULT | DESCRIPTION   |
|------------------|-----|---------------|---------|---|
| R51 (33h)        | 8:7 | VSEL<br>[1:0] | 11      | Analogue Bias Optimisation<br>00 = Reserved<br>01 = Bias current optimized for AVDD=2.7V<br>1X = Bias current optimized for AVDD=3.3V |

Table 72 Bias Optimisation

## POP SUPPRESSION CONTROL

In normal operation, the analogue circuits in the WM8959 are referenced to VMID (AVDD/2). When this reference voltage is first enabled, it will ramp quickly from AGND to AVDD/2 and, if connected to an active output, will result in an audible pop being heard. Enabling or disabling the output stage after the internal reference has settled can also result in an audible pop as the output rises rapidly from AGND.

The WM8959 provides a number of features which enable these pops to be suppressed. The associated control bits are described in this section. Careful attention is required to the sequence and timing of these controls in order to get maximum benefit. An outline of some generic control sequences is provided in order to assist users in the definition of application-specific sequences.

## REFERENCE VOLTAGES

VMID is generated from AVDD via a programmable resistor chain as shown in the audio signal paths diagram on page 25. Together with the external decoupling capacitor on VMID, the programmable resistor chain results in a slow, normal or fast charging characteristic on VMID. The VMID reference is controlled by VMID\_MODE[1:0].

The analogue circuits in the WM8959 require a bias current. The default bias current is enabled by setting VREF\_ENA. Note that the default bias current source requires VMID to be enabled also.

| REGISTER ADDRESS | BIT | LABEL                      | DEFAULT | DESCRIPTION   |
|------------------|-----|----------------------------|---------|---|
| R1 (01h)         | 2:1 | VMID_MODE<br>[1:0]<br>(rw) | 00b     | VMID Divider Enable and Select<br>00 = VMID disabled (for OFF mode)<br>01 = 2 x 50kΩ divider (Normal mode)<br>10 = 2 x 250kΩ divider (Standby mode)<br>11 = 2 x 5kΩ divider (for fast start-up) |
|                  | 0   | VREF_ENA<br>(rw)           | 0b      | VREF Enable (Bias for all analogue functions)<br>0 = VREF bias disabled<br>1 = VREF bias enabled  |

Table 73 Reference Voltages

## SOFT START CONTROL

A pop-suppressed start-up requires VMID to be enabled smoothly, without the step change normally associated with the initial stage of the VMID capacitor charging. A pop-suppressed start-up also requires the analogue bias current to be enabled throughout the signal path prior to the VMID reference voltage being applied. The WM8959 incorporates pop-suppression circuits which address these requirements.

The WM8959 provides an alternative start-up bias circuit which can be used in place of the default bias current during start-up. The start-up bias current source is enabled by BUFDCOPEN. The start-up bias source is selected (in place of the default bias source) by POBCTRL. It is recommended that the start-up bias is used during start-up, before switching back to the higher quality, VREF-enabled bias.

A soft-start circuit is provided in order to control the switch-on of the VMID reference. The soft-start control circuit is enabled by setting SOFTST. When the soft-start circuit is enabled prior to enabling VMID\_MODE, the reference voltage rises smoothly, without the step change that would otherwise occur. It is recommended that the soft-start circuit and the output signal path be enabled before VMID is enabled by VMID\_MODE.

Soft shut-down of VMID is also provided by the soft-start control circuit and the start-up bias current generator. The soft shut-down of VMID is achieved by setting SOFTST = 1, BUFDCOPEN = 1 and POBCTRL = 1 prior to setting VMID\_MODE = 00.

The register fields associated with soft start control are described in Table 74.

| REGISTER ADDRESS          | BIT | LABEL     | DEFAULT | DESCRIPTION  |
|---------------------------|-----|-----------|---------|--|
| R57 (39h)<br>Anti-Pop (2) | 6   | SOFTST    | 0b      | Enables VMID soft start<br>0 = Disabled<br>1 = Enabled   |
|                           | 2   | BUFDCOPEN | 0b      | Enables the Start-Up bias current generator<br>0 = Disabled<br>1 = Enabled                                     |
|                           | 1   | POBCTRL   | 0b      | Selects the bias current source for output amplifiers and VMID buffer<br>0 = Default bias<br>1 = Start-Up bias |

**Table 74 Soft Start Control**

### DISABLED INPUT/OUTPUT CONTROL

After start-up, it may be desirable to disable an output stage, in order to reduce power consumption on an unused output. In order to avoid audible pops caused by a disabled output dropping to AGND, the WM8959 can maintain the output at VMID even when the output driver is disabled. This is achieved by connecting a buffered VMID reference to the output. The buffered VMID is enabled by setting BUFIOEN. When BUFIOEN is enabled, it will be connected to any disabled output driver. It is recommended that BUFIOEN is enabled prior to disabling the output driver.

The buffered VMID, enabled by BUFIOEN, also maintains the charge on the input capacitors connected to any disabled input amplifier. Buffered VMID is connected to each input through 1k $\Omega$  resistors. This suppresses the audible artefacts that would otherwise arise when an input amplifier is disabled or enabled. In some applications, a pop generated at an input stage can be entirely suppressed by correctly managing the output stages. However, it may be desirable to use the buffered VMID feature in order to eliminate the input PGA start-up delay (the input capacitor charging time) in addition to suppressing any mute/un-mute pops. In applications where frequent enabling and configuration of signal paths is used, it is recommended to enable BUFIOEN at all times.

| REGISTER ADDRESS          | BIT | LABEL   | DEFAULT | DESCRIPTION   |
|---------------------------|-----|---------|---------|---|
| R57 (39h)<br>Anti-Pop (2) | 3   | BUFIOEN | 0b      | Enables the Buffered VMID reference at disabled inputs/outputs<br>0 = Disabled<br>1 = Enabled |

**Table 75 Disabled Input/Output Control**

### OUTPUT DISCHARGE CONTROL

The output paths may also be actively discharged to AGND through internal resistors if desired. This is desirable at start-up in order to achieve a known output stage condition prior to enabling the soft-start VMID reference voltage. This is also desirable in shut-down in order to eliminate pops arising from memory effects in the output capacitors on completion of the controlled shut-down of the VMID reference. Note that, for any signal paths that do not use output capacitors (eg. capless headphone drive), the discharge control is not normally required.

It is recommended that the output paths should be actively discharged prior to commencing a start-up sequence. The active discharging should then be disabled prior to enabling the output drivers.

In shut-down, it is recommended that the output paths should be actively discharged after the VMID reference has settled to AGND and the output drivers have been disabled.

The line and headphone output pins are discharged by setting DIS\_LLINE, DIS\_RLINE, DIS\_OUT3, DIS\_OUT4, DIS\_LOUT and DIS\_ROUT, as described in Table 76. Note that the buffered VMID reference is not applied to an actively discharged output, regardless of BUFIOEN.



| REGISTER ADDRESS          | BIT | LABEL     | DEFAULT | DESCRIPTION   |
|---------------------------|-----|-----------|---------|---|
| R56 (38h)<br>Anti-Pop (1) | 5   | DIS_LLINE | 0b      | Discharges LOP and LON outputs via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging LOP and LON |
|                           | 4   | DIS_RLINE | 0b      | Discharges ROP and RON outputs via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging ROP and RON |
|                           | 3   | DIS_OUT3  | 0b      | Discharges OUT3 output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging OUT3                |
|                           | 2   | DIS_OUT4  | 0b      | Discharges OUT4 output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging OUT4                |
|                           | 1   | DIS_LOUT  | 0b      | Discharges LOUT output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging LOUT                |
|                           | 0   | DIS_ROUT  | 0b      | Discharges ROUT output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging ROUT                |

Table 76 Output Discharge Control

**VMID REFERENCE DISCHARGE CONTROL**

The VMID reference can be discharged to AGND through internal resistors. Discharging VMID ensures that a subsequent start-up procedure commences with a known voltage condition; this is necessary in order to ensure maximum suppression of audible pops associated with start-up. VMID is discharged by setting VMIDTOG, as described in Table 77.

| REGISTER ADDRESS          | BIT | LABEL   | DEFAULT | DESCRIPTION  |
|---------------------------|-----|---------|---------|--|
| R57 (39h)<br>Anti-Pop (2) | 0   | VMIDTOG | 0b      | Connects VMID to ground<br>0 = Disabled<br>1 = Enabled |

Table 77 VMID Reference Discharge Control

**EXAMPLE CONTROL SEQUENCES**

Pop-suppression control sequences are described below for typical WM8959 operations involving start-up, muting and disabling of signal paths. Note that these descriptions are intended for guidance only. Application software should be verified and tailored to ensure optimum performance.

**Start-up Sequence**

The following sequence describes the register settings required to enable the headphone outputs LOUT and ROUT. It assumes that VMID and VREF are initially disabled and actively discharged to AGND.

| STEP | DESCRIPTION   | REGISTER SETTING                            |
|------|---|---|
| 1    | Discharge output drivers.   | DIS_LOUT = 1<br>DIS_ROUT = 1                |
| 2    | Time delay for output capacitors to discharge.                            |   |
| 3    | Enable soft start control and start-up bias source. Select start-up bias. | SOFTST = 1<br>BUFCOPEN = 1<br>POBCTRL = 1   |
| 4    | Disable active discharging of VMID and Output drivers.                    | VMIDTOG = 0<br>DIS_LOUT = 0<br>DIS_ROUT = 0 |
| 5    | Enable Output drivers.  | LOUT_ENA = 1<br>ROUT_ENA = 1                |
| 6    | Enable VMID and VREF.   | VMID_MODE = 01<br>VREF_ENA = 1              |
| 7    | Time delay for soft-start to execute                                      |   |
| 8    | Select default bias source.   | POBCTRL = 0                                 |
| 9    | Disable soft start control and soft start voltage.                        | SOFTST = 0<br>BUFCOPEN = 0                  |

**Table 78 Example Start-Up Control Sequence****Output Mute Sequence**

The following sequence describes the register settings required to mute and disable the headphone outputs LOUT and ROUT. It assumes that the soft start bias voltage is initially disabled.

| STEP | DESCRIPTION  | REGISTER SETTING             |
|------|--|------------------------------|
| 1    | Enable buffered VMID at all input and output circuits. | BUFIOEN = 1                  |
| 2    | Disable output drivers                                 | LOUT_ENA = 0<br>ROUT_ENA = 0 |

**Table 79 Example Mute Control Sequence****Output Un-Mute Sequence**

The following sequence describes the register settings required to enable and un-mute the headphone outputs LOUT and ROUT.

| STEP | DESCRIPTION   | REGISTER SETTING             |
|------|---|------------------------------|
| 1    | Enable Output drivers.                                  | LOUT_ENA = 1<br>ROUT_ENA = 1 |
| 2    | Disable buffered VMID at all input and output circuits. | BUFIOEN = 0                  |

**Table 80 Example Un-Mute Control Sequence**

**Shut-down and Discharge Sequence**

The following sequence describes the register settings required to mute, disable and discharge the headphone outputs LOUT and ROUT. It assumes that the soft start control and voltage source is already disabled.

| <b>STEP</b> | <b>DESCRIPTION</b>  | <b>REGISTER SETTING</b>                   |
|-------------|---|---|
| 1           | Enable soft start control and start-up bias source. Select start-up bias. | SOFTST = 1<br>BUFCOPEN = 1<br>POBCTRL = 1 |
| 2           | Disable VMID  | VMID_MODE = 00                            |
| 3           | Time delay for soft-shutdown to execute                                   |   |
| 4           | Disable Output drivers.   | LOUT_ENA = 0<br>ROUT_ENA = 0              |
| 5           | Discharge output drivers.   | DIS_LOUT = 1<br>DIS_ROUT = 1              |
| 6           | Select default bias source.   | POBCTRL = 0                               |
| 7           | Disable soft start control and soft start voltage.                        | SOFTST = 0<br>BUFCOPEN = 0                |

**Table 81 Example Shut-down and Discharge Control Sequence**

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POWER DOMAINS

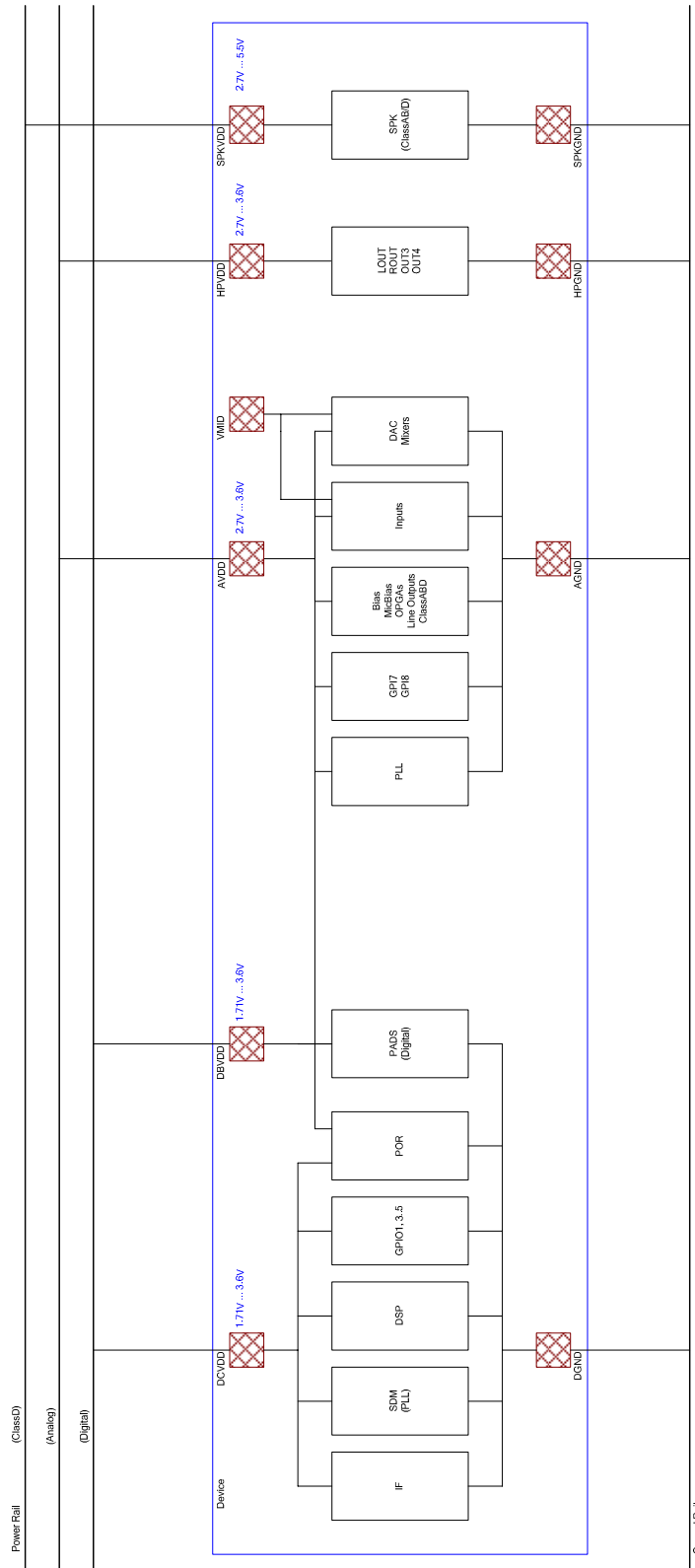


Figure 86 WM8959 Power Domains

REGISTER MAP

| Hex Addr | Hex Addr | Name                        | 15            | 14            | 13          | 12          | 11             | 10       | 9        | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bin Default         |
|----------|----------|-----------------------------|---------------|---------------|-------------|-------------|----------------|----------|----------|----------|---|---|---|---|---|---|---|---|---------------------|
| 0        | 0        | Reset                       |               |               |             |             |                |          |          |          |   |   |   |   |   |   |   |   | 1000_0001_1001_0000 |
| 1        | 1        | Power Management (1)        | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 2        | 2        | Power Management (2)        | PLL_ENA       | TSHUT_OPI2S   | TSHUT_OPI1S | LOUT_ENA    | OUT4_ENA       | OUT5_ENA | LOUT_ENA | ROUT_ENA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0110_0000_0000_0000 |
| 3        | 3        | Power Management (3)        | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 4        | 4        | Audio Interface (1)         | 0             | 1             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0100_0000_0101_0000 |
| 5        | 5        | Audio Interface (2)         | DACL_SRC      | DACR_SRC      | AIF_DAC_IDM | AIF_DAC_IDM | AIF_BOOST[1:0] | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0100_0000_0000_0000 |
| 6        | 6        | Clocking (1)                | TOCLK_RATE    | TOCLK_ENA     | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0001_1100_1000 |
| 7        | 7        | Clocking (2)                | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 8        | 8        | Audio Interface (3)         | AIF_MSTR1     | AIF_MSTR2     | AIF_SEL     | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 9        | 9        | Audio Interface (4)         | GPI01_ENA     | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0100_0000 |
| 10       | A        | DAC CTRL                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0100_0000 |
| 11       | B        | Left DAC Digital Volume     | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1100_0000 |
| 12       | C        | Right DAC Digital Volume    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1100_0000 |
| 13       | D        | Reserved                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 14       | E        | Reserved                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0001_0000_0000 |
| 15       | F        | Reserved                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1100_0000 |
| 16       | 10       | Reserved                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1100_0000 |
| 17       | 11       | Reserved                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 18       | 12       | GPI0 CTRL 1                 | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 19       | 13       | GPI01                       | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0001_0000_0000_0000 |
| 20       | 14       | GPI03 & GPI04               | GPI04_DEB_ENA | GPI04_IRQ_ENA | GPI04_PU    | GPI04_PD    | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0001_0000_0001_0000 |
| 21       | 15       | GPI05                       | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0001_0000_0001_0000 |
| 22       | 16       | GPI0 CTRL 2                 | RD_3W_ENA     | MODE_3W4      | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000_0000_0000_0000 |
| 23       | 17       | GPI0_POL                    | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_1000_0000_0000 |
| 24       | 18       | Left Line Input 1&2 Volume  | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1000_1011 |
| 25       | 19       | Left Line Input 3&4 Volume  | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1000_1011 |
| 26       | 1A       | Right Line Input 1&2 Volume | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1000_1011 |
| 27       | 1B       | Right Line Input 3&4 Volume | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_1000_1011 |
| 28       | 1C       | Left Output Volume          | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 29       | 1D       | Right Output Volume         | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0000_0000 |
| 30       | 1E       | Line Outputs Volume         | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0110_0110 |
| 31       | 1F       | Out5/4 Volume               | 0             | 0             | 0           | 0           | 0              | 0        | 0        | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000_0000_0010_0010 |

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| Dec Addr | Hex Addr | Name               | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8         | 7        | 6     | 5      | 4        | 3            | 2    | 1            | 0    | Bin Default         |                     |
|----------|----------|--------------------|----|----|----|----|----|----|---|-----------|----------|-------|--------|----------|--------------|------|--------------|------|---------------------|---------------------|
| 32       | 20       | Left OFGA Volume   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | OPVU[2]   | LOGGAZC  |       |        |          |              |      |              |      | 0000_0000_0111_1001 |                     |
| 33       | 21       | Right OFGA Volume  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | OPVU[3]   | ROPGAZC  |       |        |          |              |      |              |      | 0000_0000_0111_1001 |                     |
| 34       | 22       | Speaker Volume     | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0000_0000_0000_0011 |                     |
| 35       | 23       | ClassD1            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | CDMODE    | 0        | 0     | 0      | 0        | 0            | 0    | 1            | 0    | 0000_0000_0000_0011 |                     |
| 36       | 24       | ClassD2            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 1     | 0      | 1        | 0            | 1    | 0            | 0    | 0000_0000_0101_0101 |                     |
| 37       | 25       | ClassD3            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0000_0001_0000_0000 |                     |
| 38       | 26       | ClassD4            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | SPKZC    |       |        |          |              |      |              |      | 0000_0000_0111_1001 |                     |
| 39       | 27       | Input Mixer1       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | ANLMODE[1:0] |      | ANRMODE[1:0] |      | 0000_0000_0000_0000 |                     |
| 40       | 28       | Input Mixer2       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | LMP4      | LMP3     | LMP2  | LMP1   | LMN3     | LMN2         | LMN1 | RMP2         | RMP1 | 0000_0000_0000_0000 |                     |
| 41       | 29       | Input Mixer3       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | L34MNB    | L34MNBST | 0     | L12MNB | L12MNBST | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 42       | 2A       | Input Mixer4       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | R34MNB    | R34MNBST | 0     | R12MNB | R12MNBST | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 43       | 2B       | Input Mixer5       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 44       | 2C       | Input Mixer6       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 45       | 2D       | Output Mixer1      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 46       | 2E       | Output Mixer2      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 47       | 2F       | Output Mixer3      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 48       | 30       | Output Mixer4      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 49       | 31       | Output Mixer5      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 50       | 32       | Output Mixer6      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 51       | 33       | Out3/4 Mixer       | 0  | 0  | 0  | 0  | 0  | 0  | 0 | VSEL[1:0] | 0        | LI403 | LPGAO3 | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0001_1000_0000 |
| 52       | 34       | Line Mixer1        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 53       | 35       | Line Mixer2        | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 54       | 36       | Speaker Mixer      | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 55       | 37       | Additional Control | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 56       | 38       | AntiPOP1           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 57       | 39       | AntiPOP2           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 58       | 3A       | MICBIAS            | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 59       | 3B       | Reserved           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |
| 60       | 3C       | PLL1               | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_1000 |
| 61       | 3D       | PLL2               | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0011_0001 |
| 62       | 3E       | PLL3               | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0010_0110 |
| 63       | 3F       | Reserved           | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0         | 0        | 0     | 0      | 0        | 0            | 0    | 0            | 0    | 0                   | 0000_0000_0000_0000 |

Note:

A bin default value of 'p' indicates a register field where a default value is not applicable e.g. a volume update bit.

## REGISTER BITS BY ADDRESS

| REGISTER ADDRESS                     | BIT   | LABEL                              | DEFAULT | DESCRIPTION   |
|--------------------------------------|-------|------------------------------------|---------|---|
| R0 (00h)<br>Reset / ID               | 15:0  | SW_RESET_CHIP_ID<br>[15:0]<br>(rr) | 8990h   | Writing to this register resets all registers to their default state.<br>Reading from this register will indicate device family ID 8990h.   |
| R1 (01h)<br>Power Management<br>(1)  | 15:13 |                                    | 000b    | Reserved - Do Not Change  |
|                                      | 12    | SPK_ENA<br>(rw)                    | 0b      | SPKMIX Mixer, Speaker PGA and Speaker Output Enable<br>0 = disabled<br>1 = enabled  |
|                                      | 11    | OUT3_ENA<br>(rw)                   | 0b      | OUT3 and OUT3MIX Enable<br>0 = disabled<br>1 = enabled  |
|                                      | 10    | OUT4_ENA<br>(rw)                   | 0b      | OUT4 and OUT4MIX Enable<br>0 = disabled<br>1 = enabled  |
|                                      | 9     | LOUT_ENA<br>(rw)                   | 0b      | LOUT (Left Headphone Output) Enable<br>0 = disabled<br>1 = enabled  |
|                                      | 8     | ROUT_ENA<br>(rw)                   | 0b      | ROUT (Right Headphone Output) Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 7:5   |                                    | 000b    | Reserved - Do Not Change  |
|                                      | 4     | MICBIAS_ENA<br>(rw)                | 0b      | MICBIAS Enable<br>0 = OFF (high impedance output)<br>1 = ON   |
|                                      | 3     |                                    | 0b      | Reserved - Do Not Change  |
|                                      | 2:1   | VMID_MODE<br>[1:0]<br>(rw)         | 00b     | Vmid Divider Enable and Select<br>00 = Vmid disabled (for OFF mode)<br>01 = 2 x 50kΩ divider (Normal mode)<br>10 = 2 x 250kΩ divider (Standby mode)<br>11 = 2 x 5kΩ divider (for fast start-up) |
|                                      | 0     | VREF_ENA<br>(rw)                   | 0b      | VREF Enable (Bias for all analogue functions)<br>0 = VREF bias disabled<br>1 = VREF bias enabled  |
| R02 (02h)<br>Power Management<br>(2) | 15    | PLL_ENA<br>(rw)                    | 0b      | PLL Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 14    | TSHUT_ENA<br>(rw)                  | 1b      | Thermal Sensor Enable<br>0 = Thermal sensor disabled<br>1 = Thermal sensor enabled  |
|                                      | 13    | TSHUT_OPDIS<br>(rw)                | 1b      | Thermal Shutdown Enable<br>(Requires thermal sensor to be enabled)<br>0 = Thermal shutdown disabled<br>1 = Thermal shutdown enabled   |
|                                      | 12    |                                    | 0b      | Reserved - Do Not Change  |
|                                      | 11    | OPCLK_ENA<br>(rw)                  | 0b      | GPIO Clock Output Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 10    |                                    | 0b      | Reserved - Do Not Change  |

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| REGISTER ADDRESS                     | BIT               | LABEL              | DEFAULT  | DESCRIPTION   |
|--------------------------------------|-------------------|--------------------|--|---|
|                                      | 9                 | AINL_ENA<br>(rw)   | 0b   | Left Input Path Enable<br>(Enables AINLMUX, INMIXL, DIFFINL and RXVOICE input to AINLMUX)<br>0 = disabled<br>1 = enabled                |
|                                      | 8                 | AINR_ENA<br>(rw)   | 0b   | Right Input Path Enable<br>(Enables AINRMUX, INMIXR, DIFFINR and RXVOICE input to AINRMUX)<br>0 = disabled<br>1 = enabled               |
|                                      | 7                 | LIN34_ENA<br>(rw)  | 0b   | LIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 6                 | LIN12_ENA<br>(rw)  | 0b   | LIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 5                 | RIN34_ENA<br>(rw)  | 0b   | RIN34 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 4                 | RIN12_ENA<br>(rw)  | 0b   | RIN12 Input PGA Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 3:0               |                    | 0000b  | Reserved - Do Not Change  |
| R03 (03h)<br>Power Management<br>(3) | 15:14             |                    | 00b  | Reserved - Do Not Change  |
|                                      | 13                | LON_ENA<br>(rw)    | 0b   | LON Line Out and LONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 12                | LOP_ENA<br>(rw)    | 0b   | LOP Line Out and LOPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 11                | RON_ENA<br>(rw)    | 0b   | RON Line Out and RONMIX Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 10                | ROP_ENA<br>(rw)    | 0b   | ROP Line Out and ROPMIX Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 9                 |                    | 0b   | Reserved - Do Not Change  |
|                                      | 8                 | SPKPGA_ENA<br>(rw) | 0b   | SPKMIX Mixer and Speaker PGA Enable<br>0 = disabled<br>1 = enabled<br>Note that SPKMIX and SPKPGA are also enabled when SPK_ENA is set. |
|                                      | 7                 | LOPGA_ENA<br>(rw)  | 0b   | LOPGA Left Volume Control Enable<br>0 = disabled<br>1 = enabled   |
|                                      | 6                 | ROPGA_ENA<br>(rw)  | 0b   | ROPGA Right Volume Control Enable<br>0 = disabled<br>1 = enabled  |
|                                      | 5                 | LOMIX_ENA<br>(rw)  | 0b   | LOMIX Left Output Mixer Enable<br>0 = disabled<br>1 = enabled   |
| 4                                    | ROMIX_ENA<br>(rw) | 0b                 | ROMIX Right Output Mixer Enable<br>0 = disabled<br>1 = enabled |   |



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| REGISTER ADDRESS                 | BIT   | LABEL              | DEFAULT  | DESCRIPTION  |
|----------------------------------|-------|--------------------|----------|--|
|                                  | 3:2   |                    | 00b      | Reserved - Do Not Change   |
|                                  | 1     | DACL_ENA<br>(rw)   | 0b       | Left DAC Enable<br>0 = disabled<br>1 = enabled   |
|                                  | 0     | DACR_ENA<br>(rw)   | 0b       | Right DAC Enable<br>0 = disabled<br>1 = enabled  |
| R04 (04h)<br>Audio Interface (1) | 15:9  |                    | 0100000b | Reserved - Do Not Change   |
|                                  | 8     | AIF_BCLK_INV       | 0b       | BCLK Invert<br>0 = BCLK not inverted<br>1 = BCLK inverted  |
|                                  | 7     | AIF_LRCLK_INV      | 0b       | Right, left and I <sup>2</sup> S modes – DACLRC polarity<br>0 = normal DACLRC polarity<br>1 = invert DACLRC polarity<br>DSP Mode – mode A/B select<br>0 = MSB is available on 2nd BCLK rising edge after DACLRC rising edge (mode A)<br>1 = MSB is available on 1st BCLK rising edge after DACLRC rising edge (mode B) |
|                                  | 6:5   | AIF_WL<br>[1:0]    | 10b      | Digital Audio Interface Word Length<br>00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits<br>11 = 32 bits  |
|                                  | 4:3   | AIF_FMT<br>[1:0]   | 10b      | Digital Audio Interface Format<br>00 = Right justified<br>01 = Left justified<br>10 = I <sup>2</sup> S Format<br>11 = DSP Mode   |
|                                  | 2:0   |                    | 000b     | Reserved - Do Not Change   |
| R05 (05h)<br>Audio Interface (2) | 15    | DACL_SRC           | 0b       | Left DAC Data Source Select<br>0 = Left DAC outputs left channel data<br>1 = Left DAC outputs right channel data   |
|                                  | 14    | DACR_SRC           | 1b       | Right DAC Data Source Select<br>0 = Right DAC outputs left channel data<br>1 = Right DAC outputs right channel data  |
|                                  | 13    | AIFDAC_TDM         | 0b       | DAC TDM Enable<br>0 = Normal DACDAT operation<br>1 = TDM enabled on DACDAT   |
|                                  | 12    | AIFDAC_TDM_CHAN    | 0b       | DACDAT TDM Channel Select<br>0 = DACDAT data input on slot 0<br>1 = DACDAT data input on slot 1  |
|                                  | 11:10 | DAC_BOOST<br>[1:0] | 00b      | DAC Input Volume Boost<br>00 = 0dB<br>01 = +6dB (Input data must not exceed -6dBFS)<br>10 = +12dB (Input data must not exceed -12dBFS)<br>11 = +18dB (Input data must not exceed -18dBFS)  |
|                                  | 9:5   |                    | 00000b   | Reserved - Do Not Change   |
|                                  | 4     | DAC_COMP           | 0b       | DAC Companding Enable<br>0 = disabled<br>1 = enabled   |
|                                  | 3     | DAC_COMPMODE       | 0b       | DAC Companding Type<br>0 = $\mu$ -law<br>1 = A-law   |

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| REGISTER ADDRESS          | BIT  | LABEL             | DEFAULT | DESCRIPTION  |
|---------------------------|------|-------------------|---------|--|
|                           | 2:0  |                   | 000b    | Reserved - Do Not Change   |
| R06 (06h)<br>Clocking (1) | 15   | TOCLK_RATE        | 0b      | Timeout Clock Rate<br>(Selects clock to be used for volume update timeout and GPIO input de-bounce)<br>0 = SYSCLK / 2 <sup>21</sup> (Slower Response)<br>1 = SYSCLK / 2 <sup>19</sup> (Faster Response)  |
|                           | 14   | TOCLK_ENA         | 0b      | Timeout Clock Enable<br>(This clock is required for volume update timeout and GPIO input de-bounce)<br>0 = disabled<br>1 = enabled   |
|                           | 13   |                   | 0b      | Reserved - Do Not Change   |
|                           | 12:9 | OPCLKDIV<br>[3:0] | 0000b   | GPIO Output Clock Divider<br>0000 = SYSCLK<br>0001 = SYSCLK / 2<br>0010 = SYSCLK / 3<br>0011 = SYSCLK / 4<br>0100 = SYSCLK / 5.5<br>0101 = SYSCLK / 6<br>0110 = SYSCLK / 8<br>0111 = SYSCLK / 12<br>1000 = SYSCLK / 16<br>1001 to 1111 = Reserved  |
|                           | 8:6  | DCLKDIV<br>[2:0]  | 111b    | Class D Clock Divider<br>000 = SYSCLK<br>001 = SYSCLK / 2<br>010 = SYSCLK / 3<br>011 = SYSCLK / 4<br>100 = SYSCLK / 6<br>101 = SYSCLK / 8<br>110 = SYSCLK / 12<br>111 = SYSCLK / 16  |
|                           | 5    |                   | 0b      | Reserved - Do Not Change   |
|                           | 4:1  | BCLK_DIV<br>[3:0] | 0100b   | BCLK Frequency (Master Mode)<br>0000 = SYSCLK<br>0001 = SYSCLK / 1.5<br>0010 = SYSCLK / 2<br>0011 = SYSCLK / 3<br>0100 = SYSCLK / 4<br>0101 = SYSCLK / 5.5<br>0110 = SYSCLK / 6<br>0111 = SYSCLK / 8<br>1000 = SYSCLK / 11<br>1001 = SYSCLK / 12<br>1010 = SYSCLK / 16<br>1011 = SYSCLK / 22<br>1100 = SYSCLK / 24<br>1101 = SYSCLK / 32<br>1110 = SYSCLK / 44<br>1111 = SYSCLK / 48 |
|                           | 0    |                   | 0b      | Reserved - Do Not Change   |
| R07 (07h)                 | 15   |                   | 0b      | Reserved - Do Not Change   |

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| REGISTER ADDRESS                 | BIT   | LABEL            | DEFAULT | DESCRIPTION   |
|----------------------------------|-------|------------------|---------|---|
| Clocking (2)                     | 14    | SYSCLK_SRC       | 0b      | SYSCLK Source Select<br>0 = MCLK<br>1 = PLL output  |
|                                  | 13    | CLK_FORCE        | 0b      | Forces Clock Source Selection<br>0 = Existing SYSCLK source (MCLK or PLL output) must be active when changing to a new clock source.<br>1 = Allows existing MCLK source to be disabled before changing to a new clock source. |
|                                  | 12:11 | MCLK_DIV [1:0]   | 00b     | SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK.<br>00 = Divide SYSCLK by 1<br>01 = Reserved<br>10 = Divide SYSCLK by 2<br>11 = Reserved                               |
|                                  | 10    | MCLK_INV         | 0b      | MCLK Invert<br>0 = Master clock not inverted<br>1 = Master clock inverted   |
|                                  | 9:5   |                  | 00000b  | Reserved - Do Not Change  |
|                                  | 4:2   | DAC_CLKDIV [2:0] | 000b    | DAC Sample Rate Divider<br>000 = SYSCLK / 1.0<br>001 = SYSCLK / 1.5<br>010 = SYSCLK / 2.0<br>011 = SYSCLK / 3.0<br>100 = SYSCLK / 4.0<br>101 = SYSCLK / 5.5<br>110 = SYSCLK / 6.0<br>111 = Reserved                           |
|                                  | 1:0   |                  | 00b     | Reserved - Do Not Change  |
| R08 (08h)<br>Audio Interface (3) | 15    | AIF_MSTR1        | 0b      | Audio Interface 1 Master Mode Select<br>0 = Slave mode<br>1 = Master mode   |
|                                  | 14    | AIF_MSTR2        | 0b      | Audio Interface 2 Master Mode Select<br>0 = Slave mode<br>1 = Master mode   |
|                                  | 13    | AIF_SEL          | 0b      | Audio Interface Select<br>0 = Audio interface 1<br>1 = Audio interface 2 (GPIO3/BCLK2, GPIO4/DACLRC2, GPIO5/DACDAT2)  |
|                                  | 12:0  |                  | 0040h   | Reserved - Do Not Change  |
| R09 (09h)<br>Audio Interface (4) | 15    | GPIO1_ENA        | 0b      | GPIO1 Enable<br>0 = GPIO1 not enabled<br>1 = GPIO1 enabled  |
|                                  | 14    |                  | 0b      | Reserved - Do Not Change  |
|                                  | 13    | AIF_TRIS         | 0b      | Audio Interface and GPIO Tristate<br>0 = Audio interface and GPIO pins operate normally<br>1 = Tristate all audio interface and GPIO pins   |
|                                  | 12    |                  | 0b      | Reserved - Do Not Change  |
|                                  | 11    | DACLRC_DIR       | 0b      | DACLRC Direction<br>(Forces DACLRC clock to be output in slave mode)<br>0 = DACLRC normal operation<br>1 = DACLRC clock output enabled  |

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| REGISTER ADDRESS                        | BIT   | LABEL                 | DEFAULT                 | DESCRIPTION   |
|---|-------|-----------------------|-------------------------|---|
|   | 10:0  | DACLRC_RATE<br>[10:0] | 040h                    | DACLRC Rate<br>DACLRC clock output = BCLK / DACLRC_RATE<br><br>Integer (LSB = 1)<br>Valid from 8..2047  |
| R10 (0Ah)<br>DAC Control                | 15:13 |                       | 000b                    | Reserved - Do Not Change  |
|   | 12    | DAC_SDMCLK_RATE       | 0b                      | DAC clocking rate<br>0 = Normal operation (64fs)<br>1 = SYSCLK/4  |
|   | 11    |                       | 0b                      | Reserved - Do Not Change  |
|   | 10    | AIF_LRCLKRATE         | 0b                      | LRCLK Rate<br>0 = Normal mode (256 * fs)<br>1 = USB mode (272 * fs)   |
|   | 9     | DAC_MONO              | 0b                      | DAC Mono Mix<br>0 = Stereo<br>1 = Mono (Mono mix output on enabled DACs)  |
|   | 8     | DAC_SB_FILTER         | 0b                      | Selects DAC filter characteristics<br>0 = Normal mode<br>1 = Sloping stopband mode  |
|   | 7     | DAC_MUTERATE          | 0b                      | DAC Soft Mute Ramp Rate<br>0 = Fast ramp (fs/2, maximum ramp time is 10.7ms at fs=48k)<br>1 = Slow ramp (fs/32, maximum ramp time is 171ms at fs=48k)   |
|   | 6     | DAC_MUTEMODE          | 0b                      | DAC Soft Mute Mode<br>0 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to change immediately to DACL_VOL and DACR_VOL settings<br>1 = Disabling soft-mute (DAC_MUTE=0) will cause the DAC volume to ramp up gradually to the DACL_VOL and DACR_VOL settings |
|   | 5:4   | DEEMP[1:0]            | 00b                     | DAC De-Emphasis Control<br>00 = De-emphasis disabled<br>01 = De-emphasis enabled (Optimised for fs=32kHz)<br>10 = De-emphasis enabled (Optimised for fs=44.1kHz)<br>11 = De-emphasis enabled (Optimised for fs=48kHz)   |
|   | 3     |                       | 0b                      | Reserved - Do Not Change  |
|   | 2     | DAC_MUTE              | 1b                      | DAC Soft Mute Control<br>0 = DAC Un-mute<br>1 = DAC Mute  |
|   | 1     | DACL_DATINV           | 0b                      | Left DAC Invert<br>0 = Left DAC output not inverted<br>1 = Left DAC output inverted   |
|   | 0     | DACR_DATINV           | 0b                      | Right DAC Invert<br>0 = Right DAC output not inverted<br>1 = Right DAC output inverted  |
| R11 (0Bh)<br>Left DAC<br>Digital Volume | 15:9  |                       | 00h                     | Reserved - Do Not Change  |
|   | 8     | DAC_VU                | N/A                     | DAC Volume Update<br>Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously  |
|   | 7:0   | DACL_VOL<br>[7:0]     | 1100_000<br>0b<br>(0dB) | Left DAC Digital Volume<br>(See Table 18 for volume settings)   |
| R12 (0Ch)                               | 15:9  |                       | 00h                     | Reserved - Do Not Change  |

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| REGISTER ADDRESS         | BIT   | LABEL                  | DEFAULT          | DESCRIPTION   |
|--------------------------|-------|------------------------|------------------|---|
| Right DAC Digital Volume | 8     | DAC_VU                 | N/A              | DAC Volume Update<br>Writing a 1 to this bit will cause left and right DAC volume to be updated simultaneously  |
|                          | 7:0   | DACR_VOL [7:0]         | 1100_0000b (0dB) | Right DAC Digital Volume<br>(See Table 18 for volume settings)  |
| R13 (0Dh)                | 15:0  |                        | 0000h            | Reserved - Do Not Change  |
| R14 (0Eh)                | 15:0  |                        | 0100h            | Reserved - Do Not Change  |
| R15 (0Fh)                | 15:0  |                        | 0C00h            | Reserved - Do Not Change  |
| R16 (10h)                | 15:0  |                        | 0C00h            | Reserved - Do Not Change  |
| R17 (11h)                | 15:0  |                        | 0000h            | Reserved - Do Not Change  |
| R18 (12h)                | 15:13 |                        | 0dB              | Reserved - Do Not Change  |
| GPIO Control (1)         | 12    | IRQ (ro)               | Read Only        | IRQ Readback<br>(Allows polling of IRQ status)  |
|                          | 11    | TEMPOK (rr)            | Read or Reset    | Temperature OK status<br>Read-<br>0 = Device temperature NOT ok<br>1 = Device temperature ok<br>Write -<br>1 = Reset TEMPOK latch   |
|                          | 10    | MICSHRT (rr)           | Read or Reset    | MICBIAS short status<br>Read-<br>0 = MICBIAS ok<br>1 = MICBIAS shorted<br>Write-<br>1 = Reset MICSHRT latch   |
|                          | 9     | MICDET (rr)            | Read or Reset    | MICBIAS detect status<br>MICBIAS microphone detect Readback<br>Read-<br>0 = No Microphone detected<br>1 = Microphone detected<br>Write-<br>1 = Reset MICDET latch   |
|                          | 8     | PLL_LCK (rr)           | Read or Reset    | PLL Lock status<br>Read-<br>0 = PLL NOT locked<br>1 = PLL locked<br>Write-<br>1 = Reset PLL_LCK latch   |
|                          | 7:0   | GPIO_STATUS [7:0] (rr) | Read or Reset    | GPIO and GPI Input Pin Status<br>GPIO_STATUS[7] = GPI8 pin status<br>GPIO_STATUS[6] = GPI7 pin status<br>GPIO_STATUS[5] = Reserved<br>GPIO_STATUS[4] = GPIO5 pin status<br>GPIO_STATUS[3] = GPIO4 pin status<br>GPIO_STATUS[2] = GPIO3 pin status<br>GPIO_STATUS[1] = Reserved<br>GPIO_STATUS[0] = GPIO1 pin status |
| R19 (13h)                | 15:8  |                        | 10h              | Reserved - Do Not Change  |
| GPIO1                    | 7     | GPIO1_DEB_ENA          | 0b               | GPIO1 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)   |

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| REGISTER ADDRESS                | BIT  | LABEL              | DEFAULT | DESCRIPTION  |
|---------------------------------|------|--------------------|---------|--|
|                                 | 6    | GPIO1_IRQ_ENA      | 0b      | GPIO1 IRQ Enable<br>0 = disabled<br>1 = enabled (GPIO1 input will generate IRQ)  |
|                                 | 5    | GPIO1_PU           | 0b      | GPIO1 Pull-Up Resistor Enable<br>0 = Pull-up disabled<br>1 = Pull-up enabled (Approx 150kΩ)  |
|                                 | 4    | GPIO1_PD           | 0b      | GPIO1 Pull-Down Resistor Enable<br>0 = Pull-down disabled<br>1 = Pull-down enabled (Approx 150kΩ)  |
|                                 | 3:0  | GPIO1_SEL<br>[3:0] | 0000b   | GPIO1 Function Select<br>0000 = Input pin<br>0001 = Clock output (f=SYSCLK/OPCLKDIV)<br>0010 = Logic '0'<br>0011 = Logic '1'<br>0100 = PLL Lock output<br>0101 = Temperature OK output<br>0110 = SDOUT data output<br>0111 = IRQ output<br>1000 = MIC Detect<br>1001 = MIC Short Circuit Detect<br>1010 to 1111 = Reserved |
| R20 (14h)<br>GPIO3 and<br>GPIO4 | 15   | GPIO4_DEB_ENA      | 0b      | GPIO4 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)  |
|                                 | 14   | GPIO4_IRQ_ENA      | 0b      | GPIO4 IRQ Enable<br>0 = disabled<br>1 = enabled (GPIO4 input will generate IRQ)  |
|                                 | 13   | GPIO4_PU           | 0b      | GPIO4 Pull-Up Resistor Enable<br>0 = Pull-up disabled<br>1 = Pull-up enabled (Approx 150kΩ)  |
|                                 | 12   | GPIO4_PD           | 1b      | GPIO4 Pull-Down Resistor Enable<br>0 = Pull-down disabled<br>1 = Pull-down enabled (Approx 150kΩ)  |
|                                 | 11:8 | GPIO4_SEL<br>[3:0] | 0000b   | GPIO4 Function Select<br>0000 = Input pin<br>0001 = Clock output (f=SYSCLK/OPCLKDIV)<br>0010 = Logic '0'<br>0011 = Logic '1'<br>0100 = PLL Lock output<br>0101 = Temperature OK output<br>0110 = SDOUT data output<br>0111 = IRQ output<br>1000 = MIC Detect<br>1001 = MIC Short Circuit Detect<br>1010 to 1111 = Reserved |
|                                 | 7    | GPIO3_DEB_ENA      | 0b      | GPIO3 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)  |
|                                 | 6    | GPIO3_IRQ_ENA      | 0b      | GPIO3 IRQ Enable<br>0 = disabled<br>1 = enabled (GPIO3 input will generate IRQ)  |
|                                 | 5    | GPIO3_PU           | 0b      | GPIO3 Pull-Up Resistor Enable<br>0 = Pull-up disabled<br>1 = Pull-up enabled (Approx 150kΩ)  |

| REGISTER ADDRESS              | BIT   | LABEL              | DEFAULT | DESCRIPTION  |
|-------------------------------|-------|--------------------|---------|--|
|                               | 4     | GPIO3_PD           | 1b      | GPIO3 Pull-Down Resistor Enable<br>0 = Pull-down disabled<br>1 = Pull-down enabled (Approx 150kΩ)  |
|                               | 3:0   | GPIO3_SEL<br>[3:0] | 0000b   | GPIO3 Function Select<br>0000 = Input pin<br>0001 = Clock output (f=SYSCLK/OPCLKDIV)<br>0010 = Logic '0'<br>0011 = Logic '1'<br>0100 = PLL Lock output<br>0101 = Temperature OK output<br>0110 = SDOUT data output<br>0111 = IRQ output<br>1000 = MIC Detect<br>1001 = MIC Short Circuit Detect<br>1010 to 1111 = Reserved |
| R21 (15h)<br>GPIO5            | 15:8  |                    | 10h     | Reserved - Do Not Change   |
|                               | 7     | GPIO5_DEB_ENA      | 0b      | GPIO5 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)  |
|                               | 6     | GPIO5_IRQ_ENA      | 0b      | GPIO5 IRQ Enable<br>0 = disabled<br>1 = enabled (GPIO5 input will generate IRQ)  |
|                               | 5     | GPIO5_PU           | 0b      | GPIO5 Pull-Up Resistor Enable<br>0 = Pull-up disabled<br>1 = Pull-up enabled (Approx 150kΩ)  |
|                               | 4     | GPIO5_PD           | 1b      | GPIO5 Pull-Down Resistor Enable<br>0 = Pull-down disabled<br>1 = Pull-down enabled (Approx 150kΩ)  |
|                               | 3:0   | GPIO5_SEL<br>[3:0] | 0000b   | GPIO5 Function Select<br>0000 = Input pin<br>0001 = Clock output (f=SYSCLK/OPCLKDIV)<br>0010 = Logic '0'<br>0011 = Logic '1'<br>0100 = PLL Lock output<br>0101 = Temperature OK output<br>0110 = SDOUT data output<br>0111 = IRQ output<br>1000 = MIC Detect<br>1001 = MIC Short Circuit Detect<br>1010 to 1111 = Reserved |
| R22 (16h)<br>GPI7 and<br>GPI8 | 15    | RD_3W_ENA          | 1b      | 3- / 4-wire readback configuration<br>1 = 3-wire mode<br>0 = 4-wire mode, using GPIO pin   |
|                               | 14    | MODE_3W4W          | 0b      | 3-wire mode<br>0 = push 0/1<br>1 = open-drain<br>4-wire mode<br>0 = push 0/1<br>1 = wired-OR   |
|                               | 13:12 |                    | 00b     | Reserved - Do Not Change   |
|                               | 11    | TEMPOK_IRQ_ENA     | 0b      | Temperature Sensor IRQ Enable<br>0 = disabled<br>1 = enabled   |

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| REGISTER ADDRESS                 | BIT   | LABEL               | DEFAULT | DESCRIPTION  |
|----------------------------------|-------|---------------------|---------|--|
|                                  | 10    | MICSHRT_IRQ_ENA     | 0b      | MICBIAS short circuit detect IRQ Enable<br>0 = disabled<br>1 = enabled                                       |
|                                  | 9     | MICDET_IRQ_ENA      | 0b      | MICBIAS current detect IRQ Enable<br>0 = disabled<br>1 = enabled   |
|                                  | 8     | PLL_LCK_IRQ_ENA     | 0b      | PLL Lock IRQ Enable<br>0 = disabled<br>1 = enabled   |
|                                  | 7     | GPI8_DEB_ENA        | 0b      | GPI8 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)   |
|                                  | 6     | GPI8_IRQ_ENA        | 0b      | GPI8 IRQ Enable<br>0 = disabled<br>1 = enabled (GPI8 input will generate IRQ)                                |
|                                  | 5     |                     | 0b      | Reserved - Do Not Change   |
|                                  | 4     | GPI8_ENA            | 0b      | GPI8 Input Pin Enable<br>0 = RIN3/GPI8 pin disabled as GPI8 input<br>1 = RIN3/GPI8 pin enabled as GPI8 input |
|                                  | 3     | GPI7_DEB_ENA        | 0b      | GPI7 Input De-Bounce<br>0 = disabled (Not de-bounced)<br>1 = enabled (Requires MCLK input and TOCLK_ENA=1)   |
|                                  | 2     | GPI7_IRQ_ENA        | 0b      | GPI7 IRQ Enable<br>0 = disabled<br>1 = enabled (GPI7 input will generate IRQ)                                |
|                                  | 1     |                     | 0b      | Reserved - Do Not Change   |
|                                  | 0     | GPI7_ENA            | 0b      | GPI7 Input Pin Enable<br>0 = LIN3/GPI7 pin disabled as GPI7 input<br>1 = LIN3/GPI7 pin enabled as GPI7 input |
| R23 (17h)<br>GPIO Control<br>(2) | 15:13 |                     | 000b    | Reserved - Do Not Change   |
|                                  | 12    | IRQ_INV<br>(rw)     | 0b      | IRQ Invert<br>0 = IRQ output active high<br>1 = IRQ output active low  |
|                                  | 11    | TEMPOK_POL<br>(rw)  | 1b      | Temperature Sensor polarity<br>0 = Non-inverted<br>1 = Inverted  |
|                                  | 10    | MICSHRT_POL<br>(rw) | 0b      | MICBIAS short circuit detect polarity<br>0 = Non-inverted<br>1 = Inverted                                    |
|                                  | 9     | MICDET_POL<br>(rw)  | 0b      | MICBIAS current detect polarity<br>0 = Non-inverted<br>1 = Inverted  |
|                                  | 8     | PLL_LCK_POL<br>(rw) | 0b      | PLL Lock Polarity<br>0 = Non-inverted<br>1 = Inverted  |



| REGISTER ADDRESS                       | BIT  | LABEL                 | DEFAULT | DESCRIPTION   |
|--|------|-----------------------|---------|---|
|  | 7:0  | GPIO_POL[7:0]<br>(rw) | 00h     | GPIO Input Polarity<br>0 = Non-inverted<br>1 = Inverted<br>GPIO_POL[7]: GPI8 polarity<br>GPIO_POL[6]: GPI7 polarity<br>GPIO_POL[5]: Reserved<br>GPIO_POL[4]: GPIO5 polarity<br>GPIO_POL[3]: GPIO4 polarity<br>GPIO_POL[2]: GPIO3 polarity<br>GPIO_POL[1]: Reserved<br>GPIO_POL[0]: GPIO1 polarity |
| R24 (18h)<br>LIN12 Input<br>PGA Volume | 15:9 |                       | 00h     | Reserved - Do Not Change  |
|  | 8    | IPVU[0]               | N/A     | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)  |
|  | 7    | LI12MUTE              | 1b      | LIN12 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute   |
|  | 6    | LI12ZC                | 0b      | LIN12 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|  | 5    |                       | 0b      | Reserved - Do Not Change  |
|  | 4:0  | LIN12VOL<br>[4:0]     | 01011b  | LIN12 Volume<br>(See Table 6 for PGA volume range)  |
| R25 (19h)<br>LIN34 Input<br>PGA Volume | 15:9 |                       | 00h     | Reserved - Do Not Change  |
|  | 8    | IPVU[1]               | N/A     | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)  |
|  | 7    | LI34MUTE              | 1b      | LIN34 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute   |
|  | 6    | LI34ZC                | 0b      | LIN34 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|  | 5    |                       | 0b      | Reserved - Do Not Change  |
| R26 (1Ah)<br>RIN12 Input<br>PGA Volume | 4:0  | LIN34VOL<br>[4:0]     | 01011b  | LIN34 Volume<br>(See Table 6 for PGA volume range)  |
|  | 15:9 |                       | 00h     | Reserved - Do Not Change  |
|  | 8    | IPVU[2]               | N/A     | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)  |
|  | 7    | RI12MUTE              | 1b      | RIN12 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute   |
|  | 6    | RI12ZC                | 0b      | RIN12 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only  |
|  | 5    |                       | 0b      | Reserved - Do Not Change  |
| R27 (1Bh)<br>RIN34 Input<br>PGA Volume | 4:0  | RIN12VOL<br>[4:0]     | 01011b  | RIN12 Volume<br>(See Table 6 for PGA volume range)  |
|  | 15:9 |                       | 00h     | Reserved - Do Not Change  |
|  | 8    | IPVU[3]               | N/A     | Input PGA Volume Update<br>Writing a 1 to this bit will cause all input PGA volumes to be updated simultaneously (LIN12, LIN34, RIN12 and RIN34)  |

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| REGISTER ADDRESS                                    | BIT  | LABEL             | DEFAULT         | DESCRIPTION   |
|---|------|-------------------|-----------------|---|
|   | 7    | RI34MUTE          | 1b              | RIN34 PGA Mute<br>0 = Disable Mute<br>1 = Enable Mute   |
|   | 6    | RI34ZC            | 0b              | RIN34 PGA Zero Cross Detector<br>0 = Change gain immediately<br>1 = Change gain on zero cross only                          |
|   | 5    |                   | 0b              | Reserved - Do Not Change  |
|   | 4:0  | RIN34VOL<br>[4:0] | 01011b          | RIN34 Volume<br>(See Table 6 for PGA volume range)  |
| R28 (1Ch)<br>Left<br>Headphone<br>Output<br>Volume  | 15:9 |                   | 00h             | Reserved - Do Not Change  |
|   | 8    | OPVU[0]           | N/A             | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOUVOL<br>and ROUTVOL volumes simultaneously. |
|   | 7    | LOZC              | 0b              | Left Headphone Output Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled                                |
|   | 6:0  | LOUVOL<br>[6:0]   | 00h<br>(mute)   | Left Headphone Output Volume<br>(See Table 28 for output PGA volume control range)  |
| R29 (1Dh)<br>Right<br>Headphone<br>Output<br>Volume | 15:9 |                   | 00h             | Reserved - Do Not Change  |
|   | 8    | OPVU[1]           | N/A             | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOUVOL<br>and ROUTVOL volumes simultaneously. |
|   | 7    | ROZC              | 0b              | Right Headphone Output Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled                               |
|   | 6:0  | ROUTVOL<br>[6:0]  | 00h<br>(mute)   | Right Headphone Output Volume<br>(See Table 28 for output PGA volume control range)   |
| R30 (1Eh)<br>Line Output<br>Volume                  | 15:7 |                   | 000h            | Reserved - Do Not Change  |
|   | 6    | LONMUTE           | 1b              | LON Line Output Mute<br>0 = Un-mute<br>1 = Mute   |
|   | 5    | LOPMUTE           | 1b              | LOP Line Output Mute<br>0 = Un-mute<br>1 = Mute   |
|   | 4    | LOATTN            | 0b              | LOP Attenuation<br>0 = 0dB<br>1 = -6dB  |
|   | 3    |                   | 0b              | Reserved - Do Not Change  |
|   | 2    | RONMUTE           | 1b              | RON Line Output Mute<br>0 = Un-mute<br>1 = Mute   |
|   | 1    | ROPMUTE           | 1b              | ROP Line Output Mute<br>0 = Un-mute<br>1 = Mute   |
|   | 0    | ROATTN            | 0b              | ROP Attenuation<br>0 = 0dB<br>1 = -6dB  |
| R31 (1Fh)<br>OUT3 and<br>OUT4 Volume                | 15:6 |                   | 00000000<br>00b | Reserved - Do Not Change  |
|   | 5    | OUT3MUTE          | 1b              | OUT3 Mute<br>0 = Un-mute<br>1 = Mute  |

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| REGISTER ADDRESS               | BIT  | LABEL             | DEFAULT         | DESCRIPTION  |
|--------------------------------|------|-------------------|-----------------|--|
|                                | 4    | OUT3ATTN          | 0b              | OUT3 Attenuation<br>0 = 0dB<br>1 = -6dB  |
|                                | 3:2  |                   | 00b             | Reserved   |
|                                | 1    | OUT4MUTE          | 1b              | OUT4 Mute<br>0 = Un-mute<br>1 = Mute   |
|                                | 0    | OUT4ATTN          | 0b              | OUT4 Attenuation<br>0 = 0dB<br>1 = -6dB  |
| R32 (20h)<br>LOPGA<br>Volume   | 15:9 |                   | 00h             | Reserved - Do Not Change   |
|                                | 8    | OPVU[2]           | N/A             | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.  |
|                                | 7    | LOPGAZC           | 0b              | LOPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled   |
|                                | 6:0  | LOPGAVOL<br>[6:0] | 79h<br>(0dB)    | LOPGA Volume<br>(See Table 28 for output PGA volume control range)   |
| R33 (21h)<br>ROPGA<br>Volume   | 15:9 |                   | 00h             | Reserved - Do Not Change   |
|                                | 8    | OPVU[3]           | N/A             | Output PGA Volume Update<br>Writing a 1 to this bit will update LOPGA, ROPGA, LOUTVOL and ROUTVOL volumes simultaneously.  |
|                                | 7    | ROPGAZC           | 0b              | ROPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled   |
|                                | 6:0  | ROPGAVOL<br>[6:0] | 79h<br>(0dB)    | ROPGA Volume<br>(See Table 28 for output PGA volume control range)   |
| R34 (22h)<br>Speaker<br>Volume | 15:2 |                   | 0000h           | Reserved - Do Not Change   |
|                                | 1:0  | SPKATTN<br>[1:0]  | 11b             | Speaker Output Attenuation (SPKN and SPKP)<br>00 = 0dB<br>01 = -6dB<br>10 = -12dB<br>11 = mute   |
| R35 (23h)<br>Class D (1)       | 15:9 |                   | 00h             | Reserved - Do Not Change   |
|                                | 8    | CDMODE            | 0b              | Speaker Class D Mode Enable<br>0 = Class D mode<br>1 = Class AB mode   |
|                                | 7:0  |                   | 00000011<br>b   | Reserved - Do Not Change   |
| R36 (24h)<br>Class D (2)       | 15:0 |                   | 0055h           | Reserved - Do Not Change   |
| R37 (25h)<br>Class D (3)       | 15:6 |                   | 00000001<br>00b | Reserved - Do Not Change   |
|                                | 5:3  | DCGAIN<br>[2:0]   | 000b            | DC Speaker Boost<br>000 = 1.00x boost (+0dB)<br>001 = 1.27x boost (+2.1dB)<br>010 = 1.40x boost (+2.9dB)<br>011 = 1.52x boost (+3.6dB)<br>100 = 1.67x boost (+4.5dB)<br>101 = 1.8x boost (+5.1dB)<br>110 to 111 = Reserved |

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| REGISTER ADDRESS                 | BIT  | LABEL             | DEFAULT      | DESCRIPTION  |
|----------------------------------|------|-------------------|--------------|--|
|                                  | 2:0  | ACGAIN<br>[2:0]   | 000b         | AC Speaker Boost<br>000 = 1.00x boost (+0dB)<br>001 = 1.27x boost (+2.1dB)<br>010 = 1.40x boost (+2.9dB)<br>011 = 1.52x boost (+3.6dB)<br>100 = 1.67x boost (+4.5dB)<br>101 = 1.8x boost (+5.1dB)<br>110 to 111 = Reserved |
| R38 (26h)<br>Class D (4)         | 15:8 |                   | 00h          | Reserved - Do Not Change   |
|                                  | 7    | SPKZC             | 0b           | SPKPGA Zero Cross Enable<br>0 = Zero cross disabled<br>1 = Zero cross enabled  |
|                                  | 6:0  | SPKVOL<br>[6:0]   | 79h<br>(0dB) | SPKPGA Volume<br>(see Table 28 for SPKPGA volume control range)  |
| R39 (27h)<br>Input Mixers<br>(1) | 15:4 |                   | 000h         | Reserved - Do Not Change   |
|                                  | 3:2  | AINLMODE<br>[1:0] | 00b          | AINLMUX Input Source<br>00 = INMIXL (Left Input Mixer)<br>01 = RXVOICE (RXP - RXN)<br>10 = DIFFINL (LIN12 PGA - LIN34 PGA)<br>11 = (Reserved)  |
|                                  | 1:0  | AINRMODE<br>[1:0] | 00b          | AINRMUX Input Source<br>00 = INMIXR (Right Input Mixer)<br>01 = RXVOICE (RXP - RXN)<br>10 = DIFFINR (RIN12 PGA - RIN34 PGA)<br>11 = (Reserved)   |
| R40 (28h)<br>Input Mixers<br>(2) | 15:8 |                   | 00h          | Reserved - Do Not Change   |
|                                  | 7    | LMP4              | 0b           | LIN34 PGA Non-Inverting Input Select<br>0 = LIN4 not connected to PGA<br>1 = LIN4 connected to PGA   |
|                                  | 6    | LMN3              | 0b           | LIN34 PGA Inverting Input Select<br>0 = LIN3 not connected to PGA<br>1 = LIN3 connected to PGA   |
|                                  | 5    | LMP2              | 0b           | LIN12 PGA Non-Inverting Input Select<br>0 = LIN2 not connected to PGA<br>1 = LIN2 connected to PGA   |
|                                  | 4    | LMN1              | 0b           | LIN12 PGA Inverting Input Select<br>0 = LIN1 not connected to PGA<br>1 = LIN1 connected to PGA   |
|                                  | 3    | RMP4              | 0b           | RIN34 PGA Non-Inverting Input Select<br>0 = RIN4 not connected to PGA<br>1 = RIN4 connected to PGA   |
|                                  | 2    | RMN3              | 0b           | RIN34 PGA Inverting Input Select<br>0 = RIN3 not connected to PGA<br>1 = RIN3 connected to PGA   |
|                                  | 1    | RMP2              | 0b           | RIN12 PGA Non-Inverting Input Select<br>0 = RIN2 not connected to PGA<br>1 = RIN2 connected to PGA   |
|                                  | 0    | RMN1              | 0b           | RIN12 PGA Inverting Input Select<br>0 = RIN1 not connected to PGA<br>1 = RIN1 connected to PGA   |
| R41 (29h)<br>Input Mixers<br>(3) | 15:9 |                   | 00h          | Reserved - Do Not Change   |
|                                  | 8    | L34MNB            | 0b           | LIN34 PGA Output to INMIXL Mute<br>0 = Mute<br>1 = Un-Mute   |

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| REGISTER ADDRESS                 | BIT  | LABEL            | DEFAULT | DESCRIPTION  |
|----------------------------------|------|------------------|---------|--|
|                                  | 7    | L34MNBST         | 0b      | LIN34 PGA Output to INMIXL Gain<br>0 = 0dB<br>1 = +30dB  |
|                                  | 6    |                  | 0b      | Reserved - Do Not Change   |
|                                  | 5    | L12MNB           | 0b      | LIN12 PGA Output to INMIXL Mute<br>0 = Mute<br>1 = Un-Mute   |
|                                  | 4    | L12MNBST         | 0b      | LIN12 PGA Output to INMIXL Gain<br>0 = 0dB<br>1 = +30dB  |
|                                  | 3:0  |                  | 0000b   | Reserved - Do Not Change   |
| R42 (2Ah)<br>Input Mixers<br>(4) | 15:9 |                  | 00h     | Reserved - Do Not Change   |
|                                  | 8    | R34MNB           | 0b      | RIN34 PGA Output to INMIXR Mute<br>0 = Mute<br>1 = Un-Mute   |
|                                  | 7    | R34MNBST         | 0b      | RIN34 PGA Output to INMIXR Gain<br>0 = 0dB<br>1 = +30dB  |
|                                  | 6    |                  | 0b      | Reserved - Do Not Change   |
|                                  | 5    | R12MNB           | 0b      | RIN12 PGA Output to INMIXR Mute<br>0 = Mute<br>1 = Un-Mute   |
|                                  | 4    | R12MNBST         | 0b      | RIN12 PGA Output to INMIXR Gain<br>0 = 0dB<br>1 = +30dB  |
|                                  | 3:0  |                  | 0000b   | Reserved - Do Not Change   |
| R43 (2Bh)<br>Input Mixers<br>(5) | 15:9 |                  | 00h     | Reserved - Do Not Change   |
|                                  | 8:6  | LI2BVOL<br>[2:0] | 000b    | LIN2 Pin to INMIXL Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB |
|                                  | 5:3  | LR4BVOL<br>[2:0] | 000b    | RXVOICE to AINLMUX Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB |

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| REGISTER ADDRESS                  | BIT  | LABEL            | DEFAULT | DESCRIPTION  |
|-----------------------------------|------|------------------|---------|--|
|                                   | 2:0  | LL4BVOL<br>[2:0] | 000b    | LIN4/RXN Pin to INMIXL Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB |
| R44 (2Ch)<br>Input Mixers<br>(6)  | 15:9 |                  | 00h     | Reserved - Do Not Change   |
|                                   | 8:6  | RI2BVOL<br>[2:0] | 000b    | RIN2 Pin to INMIXR Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB     |
|                                   | 5:3  | RL4BVOL<br>[2:0] | 000b    | RXVOICE to AINRMUX Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB     |
|                                   | 2:0  | RR4BVOL<br>[2:0] | 000b    | RIN4/RXP Pin to INMIXR Gain and Mute<br>000 = Mute<br>001 = -12dB<br>010 = -9dB<br>011 = -6dB<br>100 = -3dB<br>101 = 0dB<br>110 = +3dB<br>111 = +6dB |
| R45 (2Dh)<br>Output Mixers<br>(1) | 15:8 |                  | 00h     | Reserved - Do Not Change   |
|                                   | 7    | LRBLO            | 0b      | AINRMUX Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
|                                   | 6    | LLBLO            | 0b      | AINLMUX Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
|                                   | 5    | LRI3LO           | 0b      | RIN3 to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
|                                   | 4    | LLI3LO           | 0b      | LIN3 to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |
|                                   | 3    | LR12LO           | 0b      | RIN12 PGA Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute  |

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| REGISTER ADDRESS                  | BIT                | LABEL              | DEFAULT   | DESCRIPTION   |
|-----------------------------------|--------------------|--------------------|---|---|
|                                   | 2                  | LL12LO             | 0b  | LIN12 PGA Output to LOMIX Mute<br>0 = Mute<br>1 = Un-mute                                   |
|                                   | 1                  |                    | 0b  | Reserved - Do Not Change  |
|                                   | 0                  | LDLO               | 0b  | Left DAC to LOMIX Mute<br>0 = Mute<br>1 = Un-mute<br>Note: LDLO must be muted when LDSPK=1  |
| R46 (2Eh)<br>Output Mixers<br>(2) | 15:8               |                    | 00h   | Reserved - Do Not Change  |
|                                   | 7                  | RLBRO              | 0b  | AINLMUX Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute                                     |
|                                   | 6                  | RRBRO              | 0b  | AINRMUX Output to ROMIX<br>0 = Mute<br>1 = Un-mute  |
|                                   | 5                  | RLI3RO             | 0b  | LIN3 to ROMIX Mute<br>0 = Mute<br>1 = Un-mute   |
|                                   | 4                  | RRI3RO             | 0b  | RIN3 to ROMIX Mute<br>0 = Mute<br>1 = Un-mute   |
|                                   | 3                  | RL12RO             | 0b  | LIN12 PGA Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute                                   |
|                                   | 2                  | RR12RO             | 0b  | RIN12 PGA Output to ROMIX Mute<br>0 = Mute<br>1 = Un-mute                                   |
|                                   | 1                  |                    | 0b  | Reserved - Do Not Change  |
|                                   | 0                  | RDRO               | 0b  | Right DAC to ROMIX Mute<br>0 = Mute<br>1 = Un-mute<br>Note: RDRO must be muted when RDSPK=1 |
| R47 (2Fh)<br>Output Mixers<br>(3) | 15:9               |                    | 00h   | Reserved - Do Not Change  |
|                                   | 8:6                | LLI3LOVOL<br>[2:0] | 000b  | LIN3 Pin to LOMIX Volume<br>(See Table 26 for Volume Range)                                 |
|                                   | 5:3                | LR12LOVOL<br>[2:0] | 000b  | RIN12 PGA Output to LOMIX Volume<br>(See Table 26 for Volume Range)                         |
| 2:0                               | LL12LOVOL<br>[2:0] | 000b               | LIN12 PGA Output to LOMIX Volume<br>(See Table 26 for Volume Range) |   |
| R48 (30h)<br>Output Mixers<br>(4) | 15:9               |                    | 00h   | Reserved - Do Not Change  |
|                                   | 8:6                | RRI3ROVOL<br>[2:0] | 000b  | RIN3 to ROMIX Volume<br>(See Table 26 for Volume Range)                                     |
|                                   | 5:3                | RL12ROVOL<br>[2:0] | 000b  | LIN12 PGA Output to ROMIX Volume<br>(See Table 26 for Volume Range)                         |
| 2:0                               | RR12ROVOL<br>[2:0] | 000b               | RIN12 PGA Output to ROMIX Volume<br>(See Table 26 for Volume Range) |   |
| R49 (31h)<br>Output Mixers<br>(5) | 15:9               |                    | 000h  | Reserved - Do Not Change  |
|                                   | 8:6                | LRI3LOVOL<br>[2:0] | 000b  | RIN3 to LOMIX Volume<br>(See Table 26 for Volume Range)                                     |
|                                   | 5:3                | LRBLOVOL<br>[2:0]  | 000b  | AINRMUX Output to LOMIX Volume<br>(See Table 26 for Volume Range)                           |
| 2:0                               | LLBLOVOL<br>[2:0]  | 000b               | AINLMUX Output to LOMIX Volume<br>(See Table 26 for Volume Range)   |   |

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| REGISTER ADDRESS                       | BIT  | LABEL              | DEFAULT | DESCRIPTION   |
|--|------|--------------------|---------|---|
| R50 (32h)<br>Output Mixers<br>(6)      | 15:9 |                    | 00h     | Reserved - Do Not Change  |
|  | 8:6  | RLI3ROVOL<br>[2:0] | 000b    | LIN3 to ROMIX Volume<br>(See Table 26 for Volume Range)   |
|  | 5:3  | RLBROVOL<br>[2:0]  | 000b    | AINLMUX Output to ROMIX Volume<br>(See Table 26 for Volume Range)   |
|  | 2:0  | RRBROVOL<br>[2:0]  | 000b    | AINRMUX Output to ROMIX Volume<br>(See Table 26 for Volume Range)   |
| R51 (33h)<br>OUT3 and<br>OUT4 Mixers   | 15:9 |                    | 00h     | Reserved - Do Not Change  |
|  | 8:7  | VSEL<br>[1:0]      | 11b     | Analogue Bias Optimisation<br>00 = Reserved<br>01 = Bias current optimized for AVDD=2.7V<br>1X = Lowest bias current, optimized for AVDD=3.3V |
|  | 6    |                    | 0b      | Reserved - Do Not Change  |
|  | 5    | LI4O3              | 0b      | LIN4/RXN Pin to OUT3MIX<br>0 = Mute<br>1 = Un-mute  |
|  | 4    | LPGA03             | 0b      | LOPGA to OUT3MIX<br>0 = Mute<br>1 = Un-mute   |
|  | 3:2  |                    | 00b     | Reserved - Do Not Change  |
|  | 1    | RI4O4              | 0b      | RIN4/RXP Pin to OUT4MIX<br>0 = Mute<br>1 = Un-mute  |
|  | 0    | RPGA04             | 0b      | ROPGA to OUT4MIX<br>0 = Mute<br>1 = Un-mute   |
| R52 (34h)<br>Line Output<br>Mixers (1) | 15:7 |                    | 000h    | Reserved - Do Not Change  |
|  | 6    | LLOPGALON          | 0b      | LOPGA to LONMIX<br>0 = Mute<br>1 = Un-mute  |
|  | 5    | LROPGALON          | 0b      | ROPGA to LONMIX<br>0 = Mute<br>1 = Un-mute  |
|  | 4    | LOPLON             | 0b      | Inverted LOP Output to LONMIX<br>0 = Mute<br>1 = Un-mute  |
|  | 3    |                    | 0b      | Reserved - Do Not Change  |
|  | 2    | LR12LOP            | 0b      | RIN12 PGA Output to LOPMIX<br>0 = Mute<br>1 = Un-mute   |
|  | 1    | LL12LOP            | 0b      | LIN12 PGA Output to LOPMIX<br>0 = Mute<br>1 = Un-mute   |
|  | 0    | LLOPGALOP          | 0b      | LOPGA to LOPMIX<br>0 = Mute<br>1 = Un-mute  |
| R53 (35h)<br>Line Output<br>Mixers (2) | 15:7 |                    | 000h    | Reserved - Do Not Change  |
|  | 6    | RROPGARON          | 0b      | ROPGA to RONMIX<br>0 = Mute<br>1 = Un-mute  |
|  | 5    | RLOPGARON          | 0b      | LOPGA to RONMIX<br>0 = Mute<br>1 = Un-mute  |



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| REGISTER ADDRESS                     | BIT  | LABEL     | DEFAULT | DESCRIPTION  |
|--------------------------------------|------|-----------|---------|--|
|                                      | 4    | ROPRON    | 0b      | Inverted ROP Output to RONMIX<br>0 = Mute<br>1 = Un-mute   |
|                                      | 3    |           | 0b      | Reserved - Do Not Change   |
|                                      | 2    | RL12ROP   | 0b      | LIN12 PGA Output to ROPMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 1    | RR12ROP   | 0b      | RIN12 PGA Output to ROPMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 0    | RROPGAROP | 0b      | ROPGA to ROPMIX<br>0 = Mute<br>1 = Un-mute   |
| R54 (36h)<br>Speaker<br>Output Mixer | 15:8 |           | 000h    | Reserved - Do Not Change   |
|                                      | 7    | LB2SPK    | 0b      | AINLMUX Output to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 6    | RB2SPK    | 0b      | AINRMUX Output to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 5    | LI2SPK    | 0b      | LIN2 to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 4    | RI2SPK    | 0b      | RIN2 to SPKMIX<br>0 = Mute<br>1 = Un-mute  |
|                                      | 3    | LOPGASPK  | 0b      | LOPGA to SPKMIX<br>0 = Mute<br>1 = Un-mute   |
|                                      | 2    | ROPGASPK  | 0b      | ROPGA to SPKMIX<br>0 = Mute<br>1 = Un-mute   |
|                                      | 1    | LDSPK     | 0b      | Left DAC to SPKMIX<br>0 = Mute<br>1 = Un-mute<br>Note: LDSPK must be muted when LDLO=1   |
|                                      | 0    | RDSPK     | 0b      | Right DAC to SPKMIX<br>0 = Mute<br>1 = Un-mute<br>Note: RDSPK must be muted when RDRO=1  |
| R55 (37h)<br>Additional<br>Control   | 15:1 |           | 0000h   | Reserved - Do Not Change   |
|                                      | 0    | VROI      | 0b      | VREF to Analogue Output Resistance (Disabled Outputs)<br>0 = 20k $\Omega$ (Headphone) or 10k $\Omega$ (Line Out) from buffered VMID to output<br>1 = 500 $\Omega$ from buffered VMID to output |
| R56 (38h)<br>Anti-Pop (1)            | 15:6 |           | 000h    | Reserved - Do Not Change   |
|                                      | 5    | DIS_LLINE | 0b      | Discharges LOP and LON outputs via approx 500 $\Omega$ resistor<br>0 = Not active<br>1 = Actively discharging LOP and LON  |
|                                      | 4    | DIS_RLINE | 0b      | Discharges ROP and RON outputs via approx 500 $\Omega$ resistor<br>0 = Not active<br>1 = Actively discharging ROP and RON  |

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| REGISTER ADDRESS             | BIT  | LABEL           | DEFAULT          | DESCRIPTION  |
|------------------------------|------|-----------------|------------------|--|
|                              | 3    | DIS_OUT3        | 0b               | Discharges OUT3 output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging OUT3   |
|                              | 2    | DIS_OUT4        | 0b               | Discharges OUT4 output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging OUT4   |
|                              | 1    | DIS_LOUT        | 0b               | Discharges LOUT output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging LOUT   |
|                              | 0    | DIS_ROUT        | 0b               | Discharges ROUT output via approx 500Ω resistor<br>0 = Not active<br>1 = Actively discharging ROUT   |
| R57 (39h)<br>Anti-Pop (2)    | 15:7 |                 | 0000_000<br>0_0b | Reserved - Do Not Change   |
|                              | 6    | SOFTST          | 0b               | Enables VMID soft start<br>0 = Disabled<br>1 = Enabled   |
|                              | 5:4  |                 | 00b              | Reserved - Do Not Change   |
|                              | 3    | BUFIOEN         | 0b               | Enables the VGS / R current generator and the analogue input and output bias<br>0 = Disabled<br>1 = Enabled  |
|                              | 2    | BUFDOPEN        | 0b               | Enables the VGS / R current generator<br>0 = Disabled<br>1 = Enabled   |
|                              | 1    | POBCTRL         | 0b               | Selects the bias current source for output amplifiers and VMID buffer<br>0 = VMID / R bias<br>1 = VGS / R bias   |
|                              | 0    | VMIDTOG         | 0b               | Connects VMID to ground<br>0 = Disabled<br>1 = Enabled   |
| R58 (3Ah)<br>Microphone Bias | 15:8 |                 | 00h              | Reserved - Do Not Change   |
|                              | 7:6  | MCDSTH<br>[1:0] | 00b              | MICBIAS Short Circuit Current Detect Threshold<br>00 = 600uA<br>01 = 120uA<br>10 = 1800uA<br>11 = 2400uA<br>These values are for AVDD=3.3V and scale proportionally with AVDD.   |
|                              | 5:3  | MDCTHR<br>[2:0] | 000b             | MICBIAS Current Detect Threshold<br>000 = 200uA<br>001 = 350uA<br>010 = 500uA<br>011 = 650uA<br>100 = 800uA<br>101 = 950uA<br>110 = 1100uA<br>111 = 1200uA<br>These values are for AVDD=3.3V and scale proportionally with AVDD. |
|                              | 2    | MCD             | 0b               | MICBIAS Current and Short Circuit Detect Enable<br>0 = disabled<br>1 = enabled   |
|                              | 1    |                 | 0b               | Reserved - Do Not Change   |

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| REGISTER ADDRESS           | BIT      | LABEL          | DEFAULT | DESCRIPTION   |
|----------------------------|----------|----------------|---------|---|
|                            | 0        | MBSEL          | 0b      | Microphone Bias Voltage Control<br>0 = 0.9 * AVDD<br>1 = 0.65 * AVDD                    |
| R59 (3Bh)                  | 15:0     |                | 0000h   | Reserved - Do Not Change  |
| R60 (3Ch)                  | 15:8     |                | 00h     | Reserved - Do Not Change  |
| PLL (1)                    | 7        | SDM            | 0b      | Enable PLL Integer Mode<br>0 = Integer mode<br>1 = Fractional mode                      |
|                            | 6        | PRESCALE       | 0b      | Divide MCLK by 2 at PLL input<br>0 = Divide by 1<br>1 = Divide by 2                     |
|                            | 5:4      |                | 00b     | Reserved - Do Not Change  |
|                            | 3:0      | PLLN<br>[3:0]  | 8h      | Integer (N) part of PLL frequency ratio.<br>Use values greater than 5 and less than 13. |
|                            |          |                |         |   |
| R61 (3Dh)                  | 15:8     |                | 00h     | Reserved - Do Not Change  |
|                            | 7:0      | PLLK<br>[15:8] | 31h     | Fractional (K) part of PLL frequency ratio<br>(Most significant bits)                   |
| R62 (3Eh)                  | 15:8     |                | 00h     | Reserved - Do Not Change  |
|                            | 7:0      | PLLK<br>[7:0]  | 26h     | Fractional (K) part of PLL frequency ratio<br>(Least significant bits)                  |
| R63 (3Fh) to<br>R127 (7Fh) | Reserved |                |         |   |

**DIGITAL FILTER CHARACTERISTICS**

| PARAMETER                          | TEST CONDITIONS | MIN      | TYP    | MAX      | UNIT |
|------------------------------------|-----------------|----------|--------|----------|------|
| <b>DAC Normal Filter</b>           |                 |          |        |          |      |
| Passband                           | +/- 0.03dB      | 0        |        | 0.454 fs |      |
|                                    | -6dB            |          | 0.5 fs |          |      |
| Passband Ripple                    | 0.454 fs        |          |        | +/- 0.03 | dB   |
| Stopband                           |                 | 0.546 fs |        |          |      |
| Stopband Attenuation               | F > 0.546 fs    | -50      |        |          | dB   |
| <b>DAC Sloping Stopband Filter</b> |                 |          |        |          |      |
| Passband                           | +/- 0.03dB      | 0        |        | 0.25 fs  |      |
|                                    | +/- 1dB         | 0.25 fs  |        | 0.454 fs |      |
|                                    | -6dB            |          | 0.5 fs |          |      |
| Passband Ripple                    | 0.25 fs         |          |        | +/- 0.03 | dB   |
| Stopband 1                         |                 | 0.546 fs |        | 0.7 fs   |      |
| Stopband 1 Attenuation             | f > 0.546 fs    | -60      |        |          | dB   |
| Stopband 2                         |                 | 0.7 fs   |        | 1.4 fs   |      |
| Stopband 2 Attenuation             | f > 0.7 fs      | -85      |        |          | dB   |
| Stopband 3                         |                 | 1.4 fs   |        |          |      |
| Stopband 3 Attenuation             | F > 1.4 fs      | -55      |        |          | dB   |

| DAC FILTERS      |             |
|------------------|-------------|
| MODE             | GROUP DELAY |
| Normal           | 18 / fs     |
| Sloping Stopband | 18 / fs     |

## DAC FILTER RESPONSES

### DAC STOPBAND ATTENUATION

The DAC digital filter type is selected by the DAC\_SB\_FILT register bit as shown in Table 82.

| REGISTER ADDRESS | BIT | LABEL       | DEFAULT | DESCRIPTION  |
|------------------|-----|-------------|---------|--|
| R10 (0Ah)        | 8   | DAC_SB_FILT | 0b      | Selects DAC filter characteristics<br>0 = Normal mode<br>1 = Sloping stopband mode |

Table 82 DAC Filter Selection

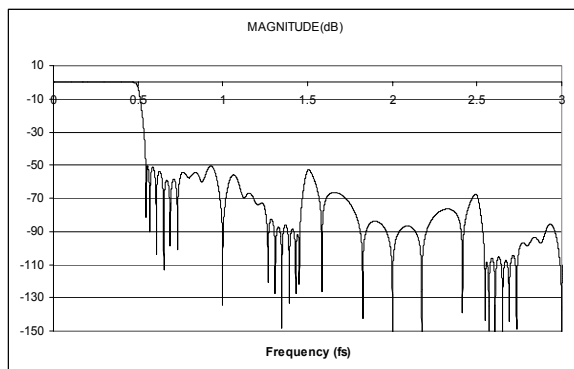


Figure 87 DAC Digital Filter Frequency Response (Normal Mode)

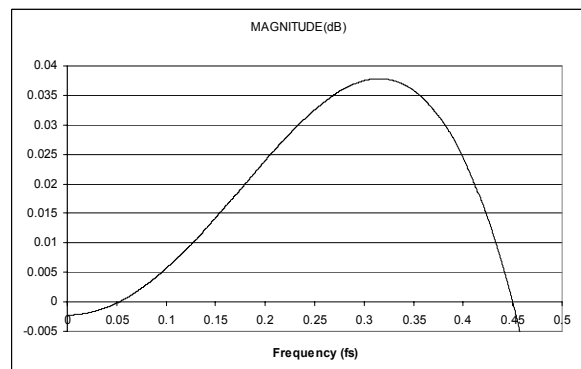


Figure 88 DAC Digital Filter Ripple (Normal Mode)

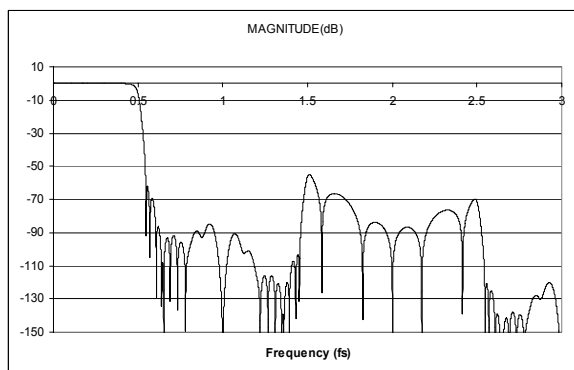


Figure 89 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

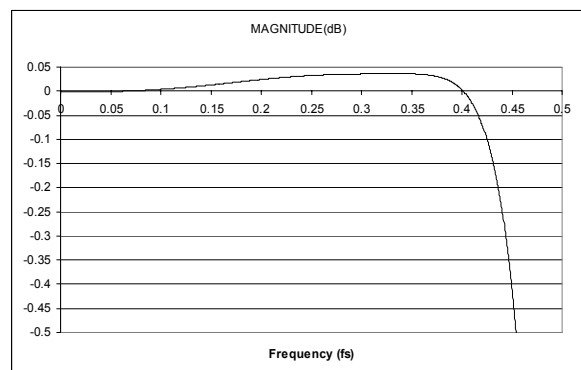
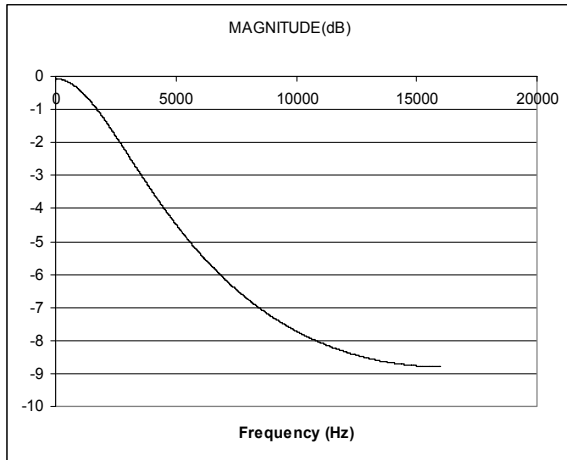


Figure 90 DAC Digital Filter Ripple (Sloping Stopband Mode)

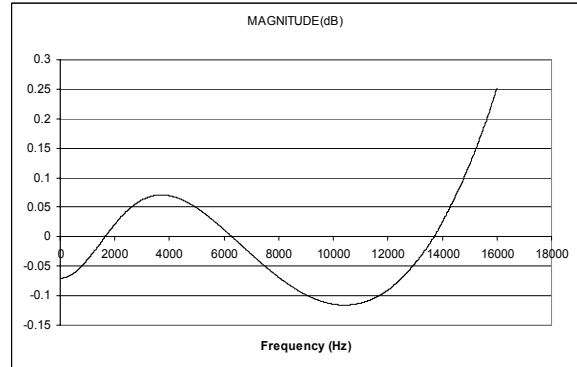
**WM8959**

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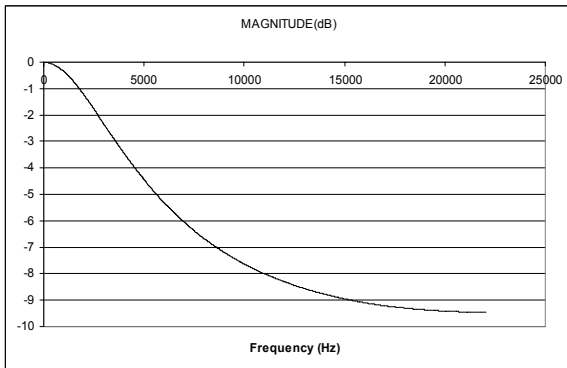
**DE-EMPHASIS FILTER RESPONSES**



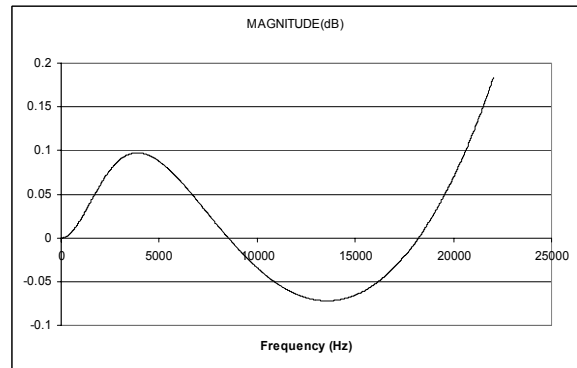
**Figure 91 De-Emphasis Digital Filter Response (32kHz)**



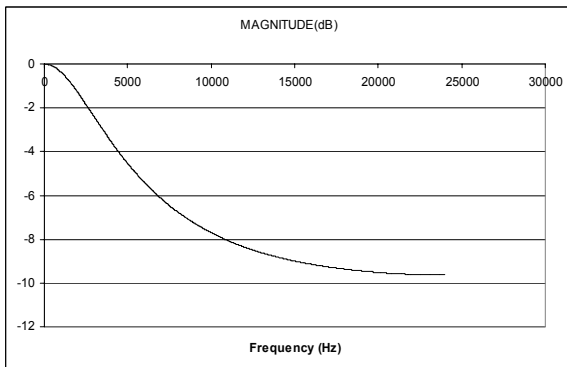
**Figure 92 De-Emphasis Error (32kHz)**



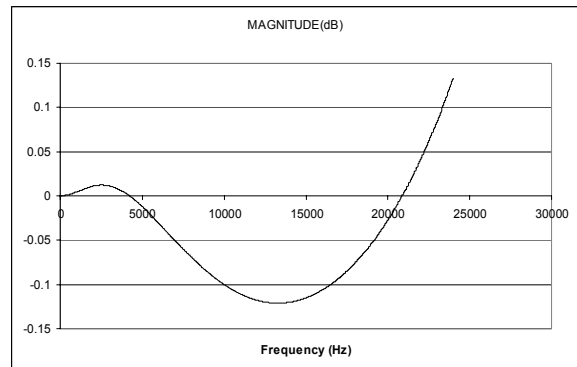
**Figure 93 De-Emphasis Digital Filter Response (44.1kHz)**



**Figure 94 De-Emphasis Error (44.1kHz)**



**Figure 95 De-Emphasis Digital Filter Response (48kHz)**



**Figure 96 De-Emphasis Error (48kHz)**

## APPLICATIONS INFORMATION

### SPEAKER SELECTION

For filterless operation, it is important to select a speaker with appropriate internal inductance. The internal inductance and the speaker's load resistance create a low-pass filter with a cut-off frequency of:

$$f_c = R_L / 2\pi L$$

e.g. for an 8Ω speaker and required cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20\text{kHz} = 64\mu\text{H}$$

8Ω speakers typically have an inductance in the range 20μH to 100μH. Care should be taken to ensure that the cut-off frequency of the speaker's internal filtering is low enough to prevent speaker damage. The class D outputs of the WM8959 operate at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter should be low enough to protect the speaker.

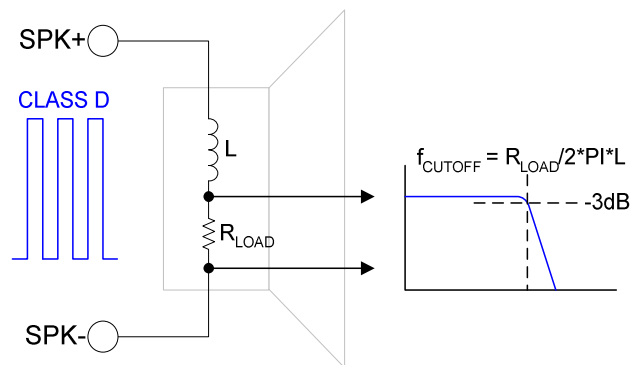
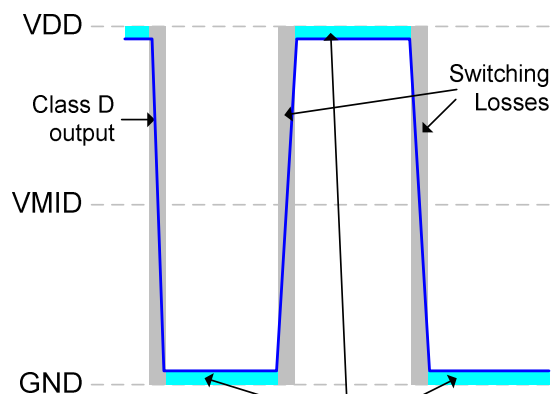


Figure 97 Speaker Equivalent Circuit

### PCB LAYOUT CONSIDERATIONS

The efficiency of the speaker drivers is affected by the series resistance between the WM8959 and the speaker (e.g. inductor ESR) as shown in Figure 98. This resistance should be as low as possible to maximise efficiency.



Losses due to resistance between WM8959 and speaker (e.g. inductor ESR)  
This resistance must be minimised in order to maximise efficiency.

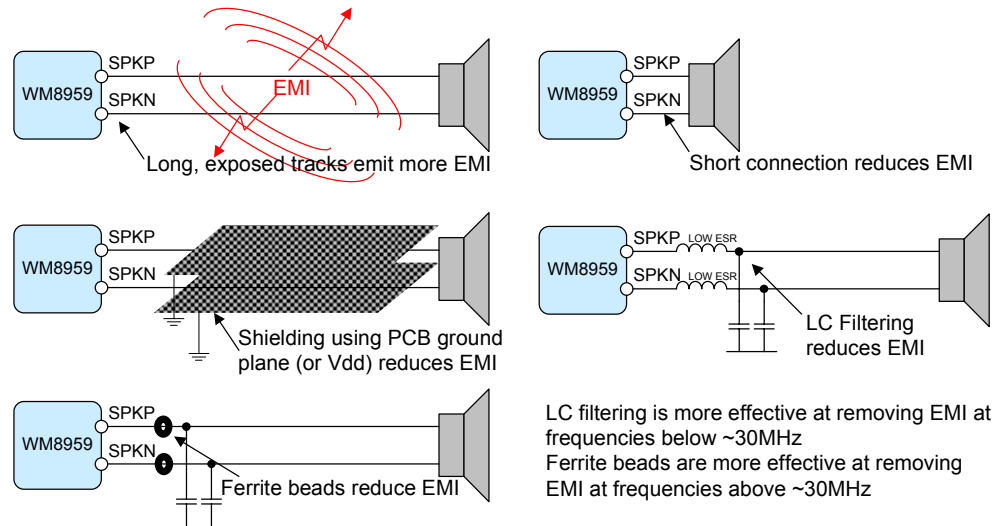
Figure 98 Speaker Connection Losses

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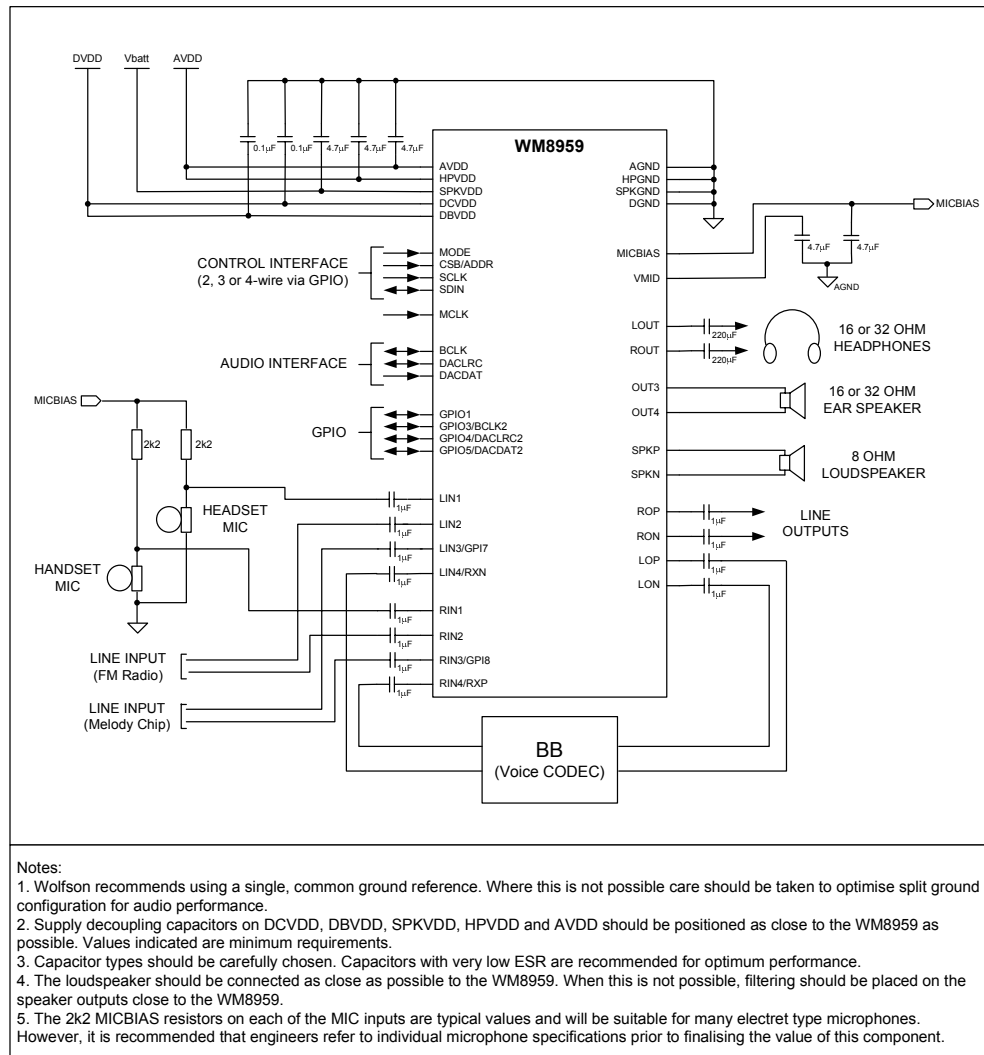
The distance between the WM8959 and the speakers should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 99. When additional passive filtering is used, low ESR components should be chosen to minimise series resistance between the WM8959 and the speaker, maximising efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.

**Figure 99 EMI Reduction Techniques**



## RECOMMENDED EXTERNAL COMPONENTS



## Notes:

1. Wolfson recommends using a single, common ground reference. Where this is not possible care should be taken to optimise split ground configuration for audio performance.
2. Supply decoupling capacitors on DCVDD, DBVDD, SPKVDD, HPVDD and AVDD should be positioned as close to the WM8959 as possible. Values indicated are minimum requirements.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.
4. The loudspeaker should be connected as close as possible to the WM8959. When this is not possible, filtering should be placed on the speaker outputs close to the WM8959.
5. The 2k2 MICBIAS resistors on each of the MIC inputs are typical values and will be suitable for many electret type microphones. However, it is recommended that engineers refer to individual microphone specifications prior to finalising the value of this component.

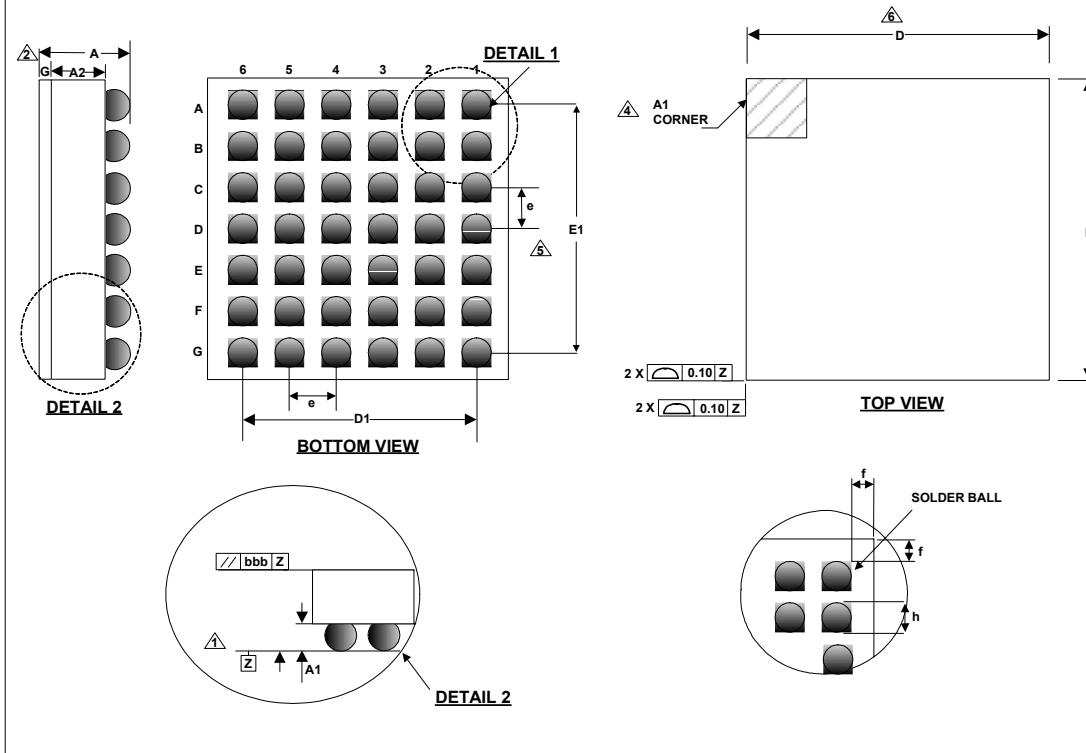
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## PACKAGE DIMENSIONS

B: 42 BALL W-CSP PACKAGE 3.226 x 3.440 x 0.7mm BODY, 0.50 mm BALL PITCH

DM049.C



| Symbols | Dimensions (mm) |           |       | NOTE |
|---------|-----------------|-----------|-------|------|
|         | MIN             | NOM       | MAX   |      |
| A       | 0.615           | 0.7       | 0.785 |      |
| A1      | 0.225           | 0.250     | 0.275 |      |
| A2      | 0.355           | 0.380     | 0.405 |      |
| D       |                 | 3.226 BSC |       |      |
| D1      |                 | 2.500 BSC |       |      |
| E       |                 | 3.440 BSC |       |      |
| E1      |                 | 3.00 BSC  |       |      |
| e       |                 | 0.50 BSC  |       | 5    |
| f       | 0.060 BSC       |           |       |      |
| g       | 0.035           | 0.070     | 0.105 |      |
| h       |                 | 0.315 BSC |       |      |

## NOTES:

1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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