



**DESCRIPTION**

WM9703 is a high-quality stereo audio codec compliant with the AC'97 Revision 2.1 specification. It performs full duplex 18-bit codec functions and supports variable sample rates from 8 to 48k samples/s and offers excellent quality with high SNR. Additional features include 3D sound and line-level outputs. In addition, support is provided for variable sample rates and accommodation is made for master/slave mode operation.

WM9703 is interchangeable with AC'97 codecs from Wolfson and other suppliers. The WM9703 is fully operable on 3.3V or 5V or mixed 3.3/5V supplies, and is packaged in the industry standard 48-pin TQFP package with 7mm-body size.

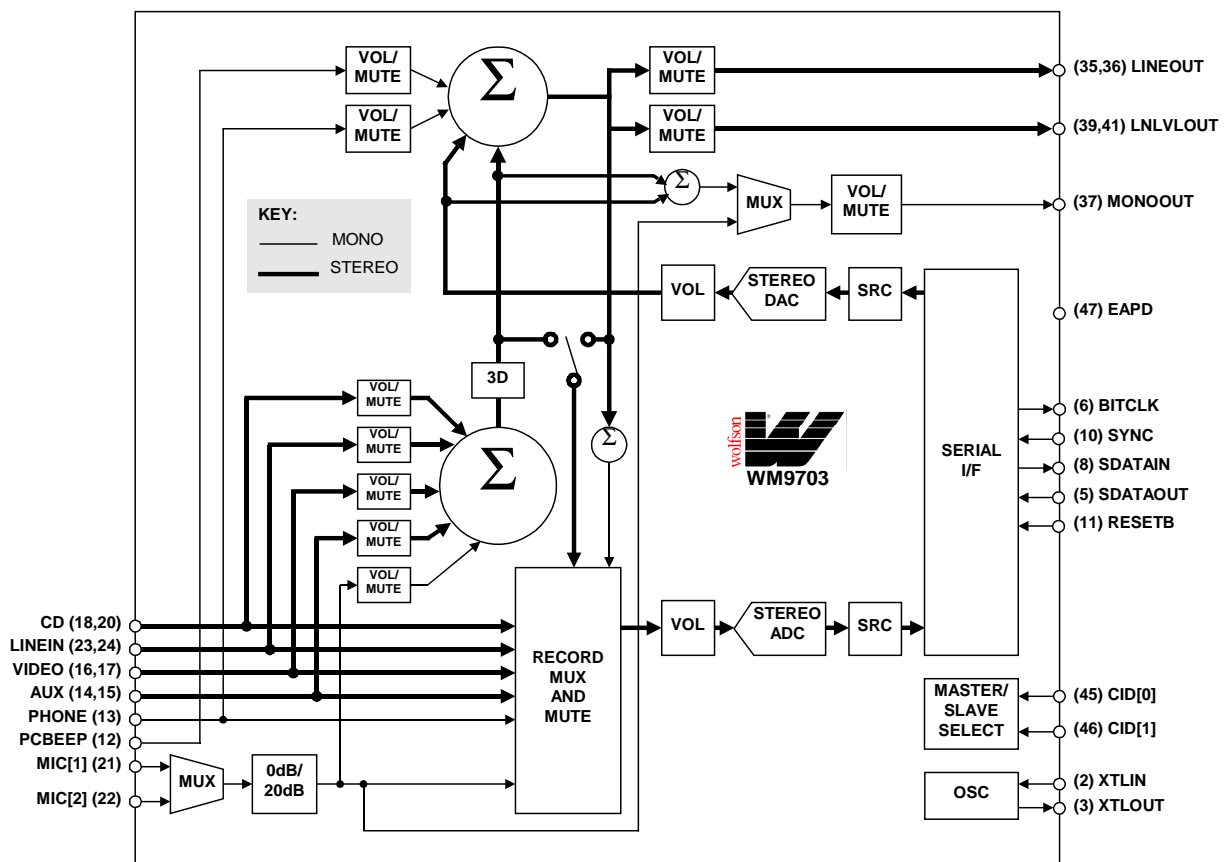
**AC'97 FEATURES**

- 3.3V or 5V operation
- 18-bit stereo codec
- S/N ratio > 95dB
- Multiple stereo input mixer
- Mono and stereo volume control
- 48-pin TQFP package
- Power management features
- Low power implementation
- Very low standby power

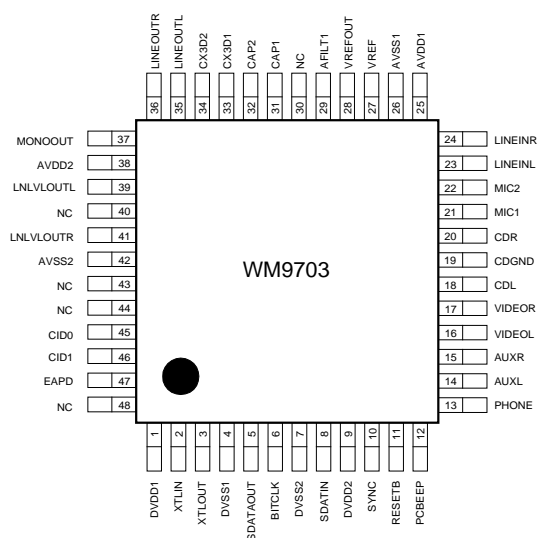
**AC'97 REVISION 2.1 FEATURES**

- Variable rate audio (VRA) support
- Analogue 3D stereo enhancement
- Line level outputs
- Supports Revision. 2.1 specified modem sample rates and filtering
- Master/slave ID selection
- PC-beep connection when device held reset

**BLOCK DIAGRAM**



## PIN CONFIGURATION



## ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM9703CFT/V	0 to 70°C	48-pin TQFP

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per specifications IPC/JEDEC J-STD-020A and JEDEC A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVDD -0.3V	AVDD +0.3V
Operating temperature range, T <sub>A</sub>	0°C	+70°C
Storage temperature	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

**Note:**

- The digital supply voltage (DVDD) must always be less than or equal to the analogue supply voltage (AVDD).

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD1, DVDD2		-10%	3.3 to 5.0	+10%	V
Analogue supply range	AVDD1, AVDD2		-10%	3.3 to 5.0	+10%	V
Digital ground	DVSS1, DVSS2			0		V
Analogue ground	AVSS1, AVSS2			0		V
Difference DVSS to AVSS			-0.3	0	+0.3	V
Analogue supply current		DVDD, AVDD = 5V		35		mA
Digital supply current		DVDD, AVDD = 5V		25		mA
Standby supply current (all PRs set)		DVDD, AVDD = 5V		10		µA
Analogue supply current		DVDD, AVDD = 3.3V		22		mA
Digital supply current		DVDD, AVDD = 3.3V		15		mA
Standby supply current (all PRs set)		DVDD, AVDD = 3.3V		6		µA

**ELECTRICAL CHARACTERISTICS****Test Characteristics:**AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Digital Logic Levels (DVDD = 3.3 or 5.0V)</b>						
Input LOW level	V <sub>IL</sub>		AVSS -0.3		0.8	V
Input HIGH level	V <sub>IH</sub>		2.2		AVDD +0.3	V
Output LOW	V <sub>OL</sub>				0.1 x DVDD	V
Output HIGH	V <sub>OH</sub>		0.9 x DVDD			V
<b>Analogue I/O Levels (Input Signals on any inputs, Outputs on LINEOUT L, R and MONOOUT)</b>						
Input level		Minimum input impedance = 10k	AVSS -100mV		AVDD +100mV	V
Output level		Into 10kohm load	AVSS +100mV	Near rail to rail	AVDD -100mV	V
<b>Reference Levels</b>						
Reference input/output	CAP2		2/5 AVDD	AVDD/2	3/5 AVDD	V
CAP2 impedance				75		kohms
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
ADC reference	CAP1			Buffered CAP2		V
DAC reference	AFILT1			Buffered CAP2		V
MIDBUFF current sink (pins CAP1, AFILT2, VREF and VREFOUT)		AVDD = 5V	-5	-15		mA
MIDBUFF current source (pins CAP1, AFILT1, VREF and VREFOUT)		AVDD = 5V	5	15		mA
MIDBUFF current source (pins CAP1, AFILT1, VREF and VREFOUT)		AVDD = 3.3V		5		mA

**Test Characteristics:**AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DAC Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR A-weighted (Note 1)			85	96		dB
Full scale output voltage		VREF = 2.5V		1.0		Vrms
THD		-3dBfs input	74	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB
<b>ADC Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR A-weighted (Note 1)			75	85		dB
ADC input for full scale output		VREF = 2.5V		1.0		Vrms
THD		-6dBV input	74	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
<b>Mixer Circuit Specifications (AVDD = 5V) 48kHz sampling</b>						
SNR CD path A-weighted (Note 1)			90	100		dB
SNR Other paths A-weighted (Note 1)			85	95		dB
Maximum input voltage			AVSS	1.0	AVDD	Vrms
Maximum output voltage on LINEOUT			1.0	1.8		Vrms
THD		0dBV input	74	90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain	10	15		kohm
Input impedance (other mixer inputs)		At max gain	10	20		kohm
		At 0db gain		100		kohm
Input impedance Mic inputs		At max gain		80		kohm
		At 0db gain	10	15		kohm
PSRR		20 to 20kHz		40		dB
<b>DAC Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR A-weighted (Note 1)				96		dB
Full scale output voltage		VREF = 1.65V		0.7		Vrms
THD		3dBfs input		90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB

**Test Characteristics:**AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR A-weighted (Note 1)				82		dB
ADC input for full scale output		VREF = 1.65V		0.7		Vrms
THD		-9dBV input		80		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
<b>Mixer Circuit Specifications (AVDD = 3.3V) 48kHz sampling</b>						
SNR CD path A-weighted (Note 1)				97		dB
SNR Other paths A-weighted (Note 1)				92		dB
Maximum input voltage				0.7		Vrms
Maximum output voltage on LINEOUT				0.7		Vrms
THD		-3dBV input		90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kohm
Input impedance (other Mixer inputs)		At max gain		20		kohm
		At 0db gain		100		kohm
Input impedance MIC inputs		At max gain		80		kohm
		At 0db gain		15		kohm
PSRR		20 to 20kHz		40		dB
<b>Clock Frequency Range</b>						
Crystal clock				24.576		MHz
BIT_CLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

**Note:**

1. SNR is the ratio of 0dB signal output level to the output level with no signal, measured A-weighted over a 20Hz to 20kHz bandwidth.

## PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital positive supply
2	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
3	XTLOUT	Digital output	Clock crystal connection
4	DVSS1	Supply	Digital ground supply
5	SDATAOUT	Digital input	Serial data input
6	BITCLK	Digital output (master) Digital input (slave)	Serial interface clock output to AC'97 controller or input from AC'97 master codec
7	DVSS2	Supply	Digital ground supply
8	SDATAIN	Digital output	Serial data output to AC'97 controller
9	DVDD2	Supply	Digital positive supply
10	SYNC	Digital input	Serial interface sync pulse from AC'97 controller
11	RESETB	Digital input	NOT reset input (active low, resets registers)
12	PCBEEP	Analogue input	Mixer input, typically for PCBEEP signal
13	PHONE	Analogue input	Mixer input, typically for PHONE signal
14	AUXL	Analogue input	Mixer input, typically for AUX signal
15	AUXR	Analogue input	Mixer input, typically for AUX signal
16	VIDEOL	Analogue input	Mixer input, typically for VIDEO signal
17	VIDEOR	Analogue input	Mixer input, typically for VIDEO signal
18	CDL	Analogue input	Mixer input, typically for CD signal
19	CDGND	Analogue input	CD input common mode reference (ground)
20	CDR	Analogue input	Mixer input, typically for CD signal
21	MIC1	Analogue input	Mixer input with extra gain if required
22	MIC2	Analogue input	Mixer input with extra gain if required
23	LINEINL	Analogue input	Mixer input, typically for LINE signal
24	LINEINR	Analogue input	Mixer input, typically for LINE signal
25	AVDD1	Supply	Analogue positive supply
26	AVSS1	Supply	Analogue ground supply, chip substrate
27	VREF( note1)	Analogue output	Buffered CAP2
28	VREFOUT	Analogue output	Reference for microphones; buffered CAP2
29	AFILT1( note1)	Analogue output	Buffered CAP2
30	NC		No internal connection
31	CAP1(note 1)	Analogue output	Buffered CAP2
32	CAP2	Analogue input	Reference input/output; pulls to midrail if not driven
33	CX3D1	Analogue output	Output pin for 3D difference signal
34	CX3D2	Analogue input	Input pin for 3D difference signal
35	LINEOUTL	Analogue output	Main analogue output for left channel
36	LINEOUTR	Analogue output	Main analogue output for right channel
37	MONOOUT	Analogue output	Main mono output
38	AVDD2	Supply	Analogue positive supply
39	LNLVLOUTL	Analogue output	Left channel line level output
40	NC		No internal connection
41	LNLVLOUTR	Analogue output	Right channel line level output
42	AVSS2	Supply	Analogue ground supply, chip substrate
43	NC		No internal connection
44	NC		No internal connection
45	CID0	Digital input	Master/slave ID select (internal pull-up)
46	CID1	Digital input	Master/slave ID select (internal pull-up)
47	EAPD	Digital output	External amplifier powerdown/GPO
48	NC		No internal connection

**Note:**

1 Pins 27, 29 and 31 have an internal connection.

## DETAILED TIMING DIAGRAMS

**Test Characteristics:**

AVDD = 5V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated.

DVDD = 3.3V, GND = 0V .....T<sub>A</sub> = 0°C to +70°C, unless otherwise stated.

All measurements are taken at 10% to 90% VDD, unless otherwise stated.

### AC-LINK LOW POWER MODE

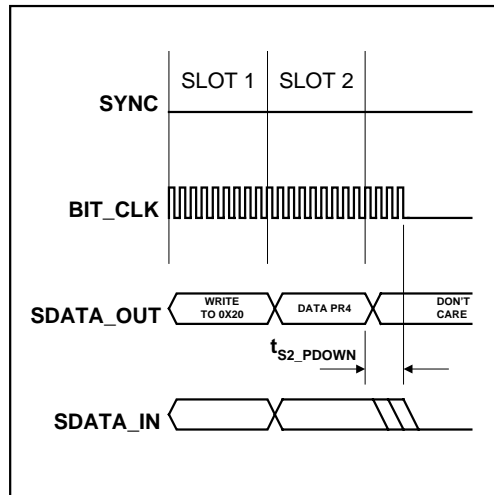


Figure 1 AC-Link Powerdown Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BITCLK SDATIN low	t <sub>s2_PDOWN</sub>			1.0	μs

### COLD RESET

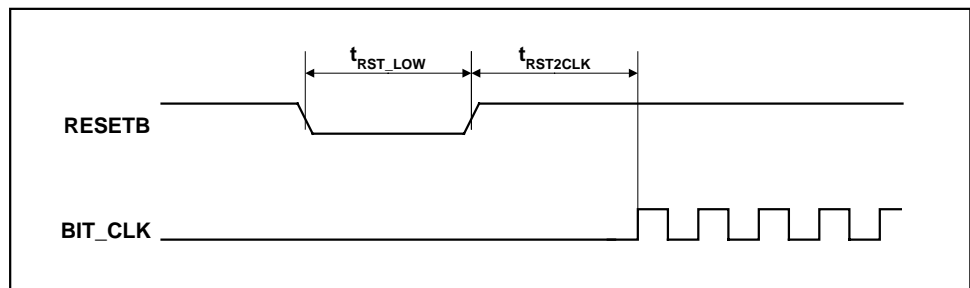
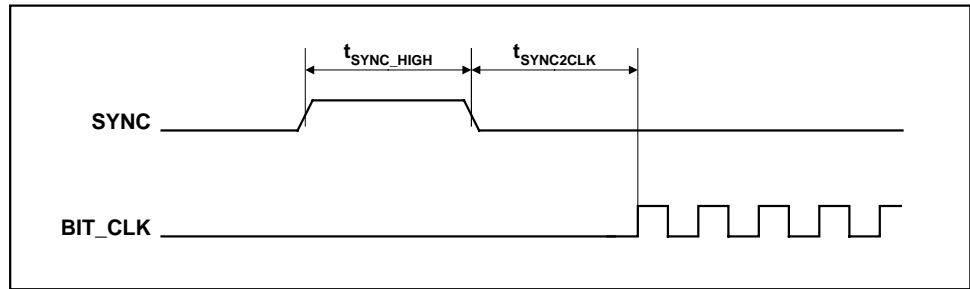


Figure 2 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t <sub>RST_LOW</sub>	1.0			μs
RESETB inactive to BIT_CLK start-up delay	t <sub>RST2_CLK</sub>	162.8			ns

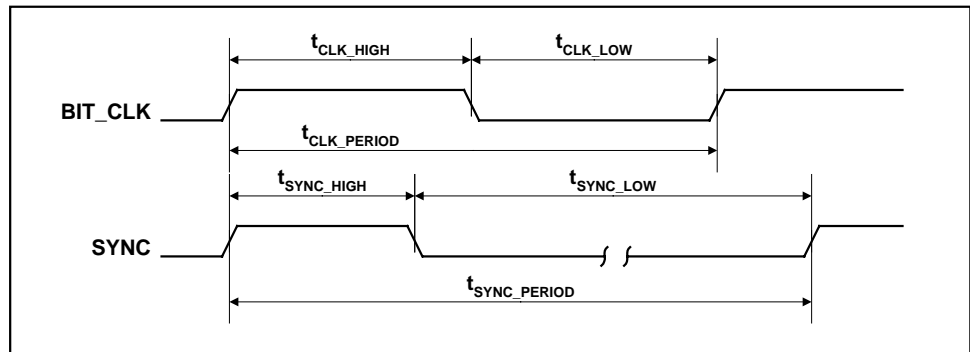
**WARM RESET**



**Figure 3 Warm Reset Timing**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	$t_{\text{SYNC\_HIGH}}$		1.3		$\mu\text{s}$
SYNC inactive to BIT_CLK start-up delay	$t_{\text{SYNC2\_CLK}}$	162.4			ns

**CLOCK SPECIFICATIONS**



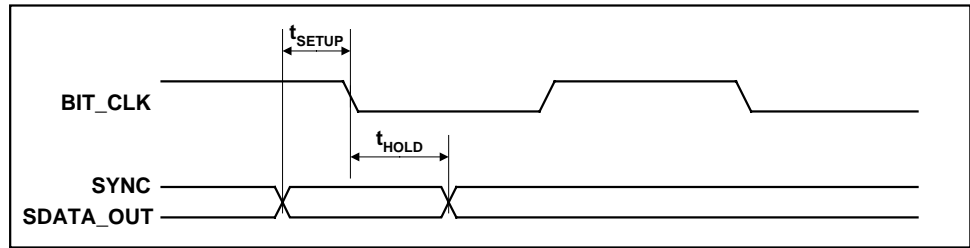
**Figure 4 Clock Specifications (50pF External Load)**

Note: Worst case duty cycle restricted to 40/60.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK frequency			12.288		MHz
BIT_CLK period	$t_{\text{CLK\_PERIOD}}$		81.4		ns
BIT_CLK output jitter				750	ps
BIT_CLK high pulse width (Note 1)	$t_{\text{CLK\_HIGH}}$	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 1)	$t_{\text{CLK\_LOW}}$	32.56	40.7	48.84	ns
SYNC frequency			48.0		kHz
SYNC period	$t_{\text{SYNC\_PERIOD}}$		20.8		$\mu\text{s}$
SYNC high pulse width	$t_{\text{SYNC\_HIGH}}$		1.3		$\mu\text{s}$
SYNC low pulse width	$t_{\text{SYNC\_LOW}}$		19.5		$\mu\text{s}$



**DATA SETUP AND HOLD (50PF EXTERNAL LOAD)**

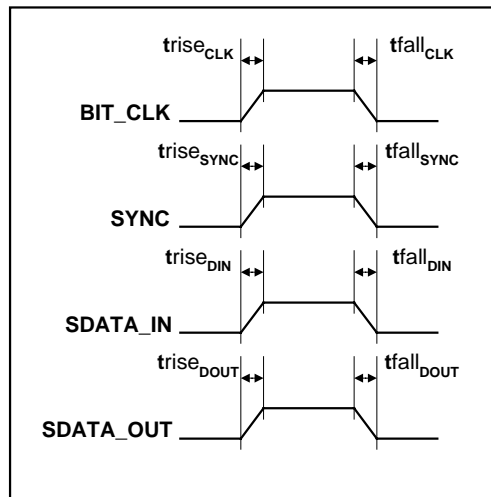


**Figure 5 Data Setup and Hold (50pF External Load)**

Note: Setup and hold time parameters for SDATA\_IN are with respect to AC'97 Controller.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BIT_CLK	$t_{SETUP}$	15.0			ns
Hold from falling edge of BIT_CLK	$t_{HOLD}$	5.0			ns

**SIGNAL RISE AND FALL TIMES**



**Figure 6 Signal Rise and Fall Times (50pF External Load)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK rise time	$trise_{CLK}$	2		6	ns
BIT_CLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATA_IN rise time	$trise_{DIN}$	2		6	ns
SDATA_IN fall time	$trise_{DIN}$	2		6	ns
SDATA_OUT rise time	$trise_{DOUT}$	2		6	ns
SDATA_OUT fall time	$tfall_{DOUT}$	2		6	ns

SYSTEM INFORMATION

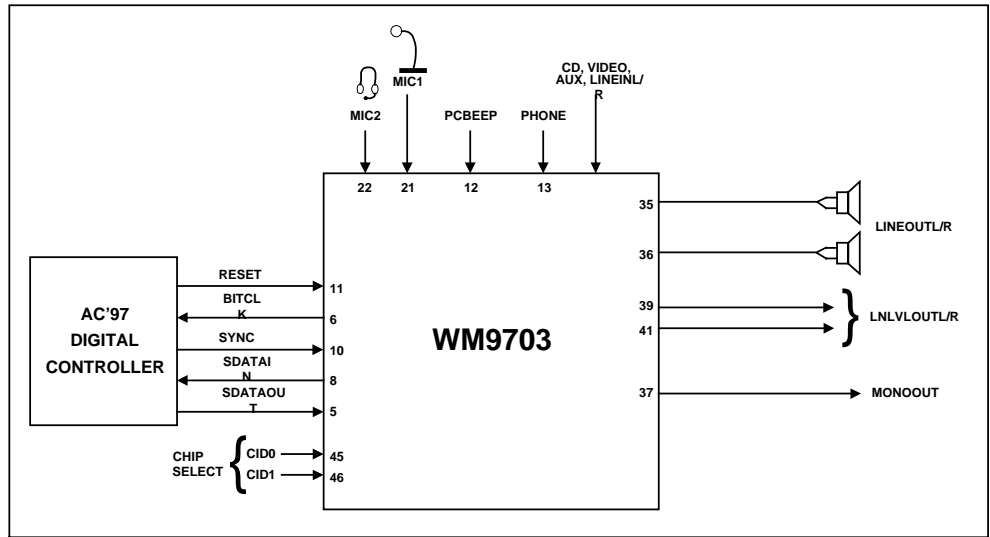


Figure 8 Revision 2.1 Compliant 2-Channel Codec

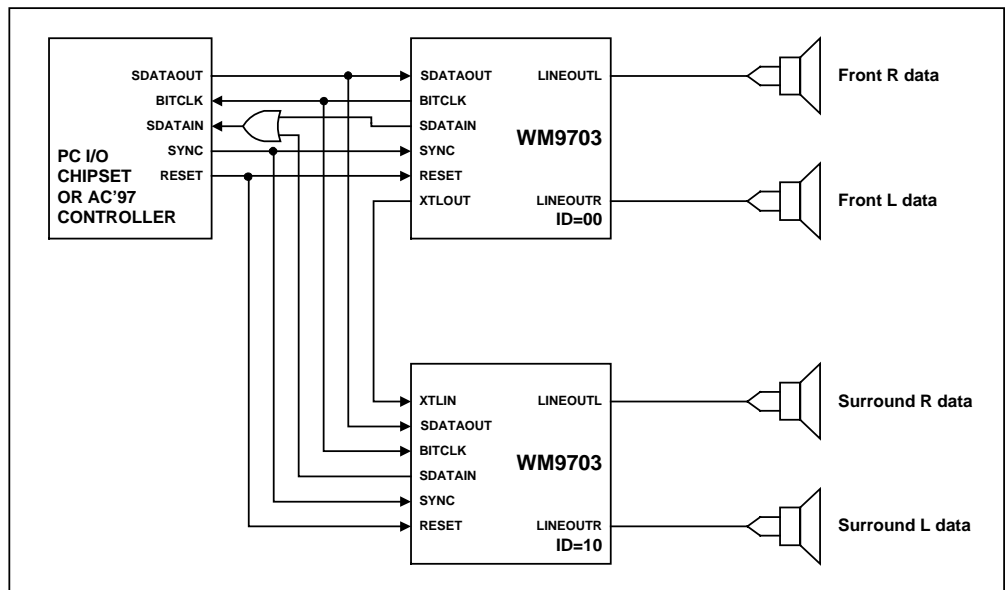


Figure 9 WM9703 in a 4 Channel System

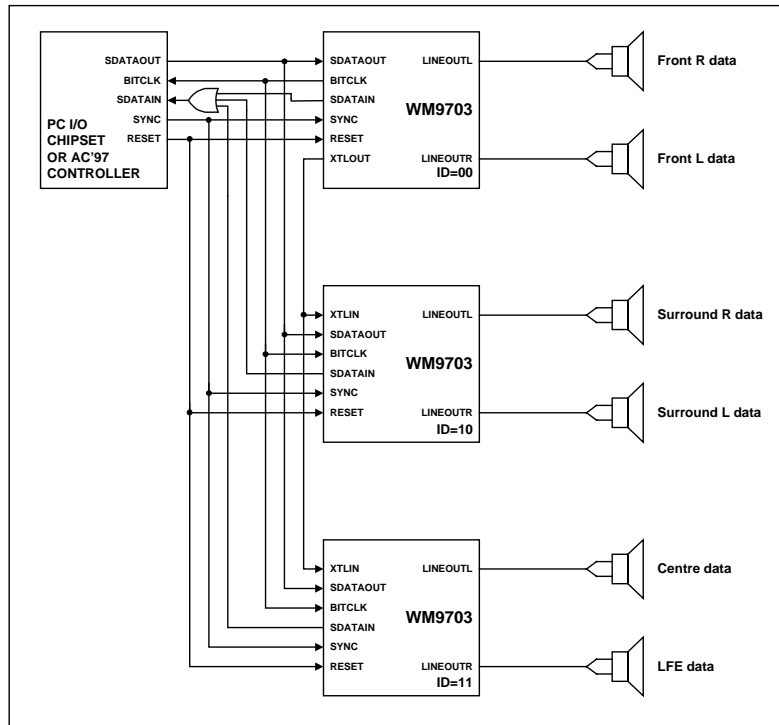


Figure 10 WM9703 in a 6 Channel System

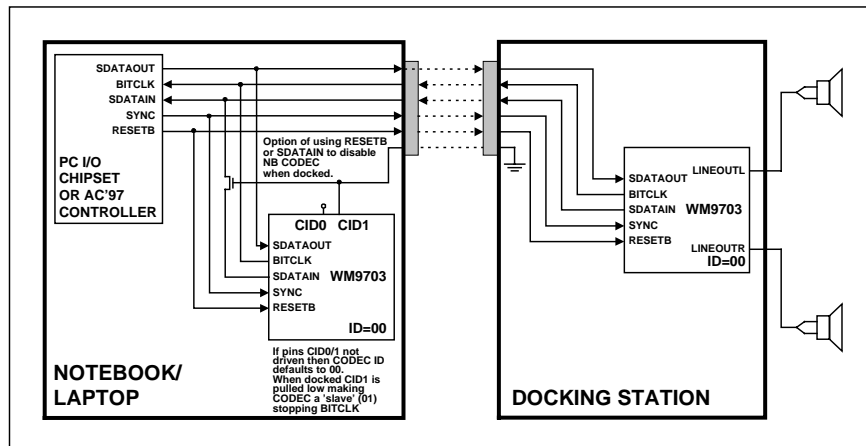


Figure 11 WM9703 in a Docking Station System

## DEVICE DESCRIPTION

### INTRODUCTION

The WM9703 is fully compliant with Revision 2.1 of the AC'97 specification.

The WM9703 comprises a stereo 18-bit Codec, (that is, 2 ADCs and 2 DACs) plus a comprehensive analogue mixer with 4 sets of stereo inputs, plus phone, 2 microphone, and PC-beep inputs. Additionally, on-chip reference generation circuits generate the necessary bias voltages for the device, and a bidirectional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller. The WM9703 supports 18-bit resolution within the DAC and ADC functions, but the AC'97 serial interface specification allows any word length up to 20-bits to be written to, or read from, the AC'97 Codec. These words are MSB justified, and any LSBs not used will simply default to 0. Normally it is anticipated that 16-bit words will be used in most PC type systems. Therefore, for the DAC, 16-bit words will be downloaded into the Codec from the controller, along with padding of 0s to make the 16-bit word up to 20-bit length. In this case, the WM9703 will process the 16-bit word along with 0 padding bits in the 2 LSB locations (to make 18-bit). At the ADC output, WM9703 will provide an 18-bit word, again with 0s in the two LSB locations (20-bit). The AC'97 controller will then ignore the 4 LSBs of the 20-bit word. When the WM9703 is interrogated, it responds indicating it is an 18-bit device.

The WM9703 has the ADC and DAC functions implemented using oversampled, or sigma-delta converters, and uses on-chip digital filters to convert these 1-bit signals to and from the 48ks/s 16/18-bit PCM words that the AC'97 controller requires. The digital parts of the device are powered separately from the analogue to optimise performance and 3.3V digital and 5V analogue supplies may be used on the same device to further optimise performance. Digital IOs are 5V tolerant when the analogue supplies are 5V, so the WM9703 may be connected to a controller running on 5V supplies, but use 3.3V for the digital section of WM9703. WM9703 is also capable of operating with a 3.3V supply only (digital and analogue).

An internally generated midrail reference is provided at pin CAP2 which is used as the chip reference. This pin should be heavily decoupled.

The WM9703 is not limited to PC-only applications. The ability to powerdown sections of the device selectively, and the option to choose alternative master clock, and hence sample rates, means that many alternative applications in areas such as telecomms, may be anticipated.

Additional features added to the Intel AC'97 specification, such as the EAPD (External Amplifier Power Down) bit, internal connection of PC-beep to the outputs in the case where the device is reset, are supported, along with optional features such as variable sample rate support.

### 3D STEREO ENHANCEMENT

This device contains a stereo enhancement circuit, designed to optimise the listening experience when the device is used in a typical PC operating environment. That is, with a pair of speakers placed either side of the monitor with little spatial separation. This circuit creates a difference signal by differencing left and right channel playback data, then filters this difference signal using lowpass and highpass filters whose time constants are set using external capacitors connected to the CX3D pins 33 and 34. Typically the values of 100nF and 47nF set highpass and lowpass poles at about 100Hz and 1kHz respectively. This frequency band corresponds to the range over which the ear is most sensitive to directional effects.

The filtered difference signal is gain adjusted by an amount set using the 4-bit value written to register 22h bits 3 to 0. Value 0h is disable, value Fh is maximum effect. Typically a value of 8h is optimum. The user interface would most typically use a slider type of control to allow the user to adjust the level of enhancement to suit the program material. Bit D13 3D in register 20h is the overall 3D enable bit. The capability register 00h reads back the value 11000 in bits D14 to D10. This corresponds to decimal 24, which is registered with Intel as Wolfson Stereo Enhancement.

Note that the external capacitors setting the filtering poles applied to the difference signal may be adjusted in value, or even replaced with a direct connection between the pins. If such adjustments are made, then the amount of difference signal fed back into the main signal paths may be significant, and can cause large signals which may limit, distort, or overdrive signal paths or speakers. Adjust these values with care, to select the preferred acoustic effect.

There is no provision for pseudo-stereo effects. Mono signals will have no enhancement applied (if the signals are in phase and of the same amplitude).

Signals from the PCM DAC channels do not have stereo enhancement applied. It is assumed that these signals will already have been processed digitally with any required 3D enhancement effect. Applying the analogue 3D enhancement will corrupt this digital effect. This is equivalent to setting the POP bit in register 20h. As a result, the readback value of this bit is fixed as 1, and attempts to change it will be ignored. POP bit is set to one and cannot be re-set.

## VARIABLE SAMPLE RATE SUPPORT

The DACs and ADCs on this device support all the recommended sample rates specified in the Intel Revision 2.1 specification for both audio and modem rates. Default rates are 48ks/s. If alternative rates are selected, the AC'97 interface continues to run at 48k words per second, but data is transferred across the link in bursts such that the net sample rate selected is achieved. It is up to the AC'97 Revision 2.1 compliant controller to ensure that data is supplied to the AC link, and received from the AC link, at the appropriate rate.

The device supports on demand sampling. That is, when the DAC signal processing circuits need another sample, a sample request is sent to the controller which must respond with a data sample in the next frame it sends. For example, if a rate of 24ks/s is selected, on average the device will request a sample from the controller every other frame, for each of the stereo DACs. Note that if an unsupported rate is written to one of the rate registers, the rate will default to the nearest rate supported. The register will then respond when interrogated with the supported rate the device has defaulted to.

ADCs are controlled similarly but with one difference: Normally the left and right channel ADCs sample at the same rate.

AUDIO SAMPLE RATE	CONTROL VALUE D15-D0	MODEM SAMPLE RATE	CONTROL VALUE D15-D0
8000	1F40	7200	1C20
11025	2B11	8228.57 (57600/7)	2024
16000	3E80	8400	20D0
22050	5622	9000	2328
44100	AC44	9600	2580
48000	BB80	10285.71 (72000/7)	282D
		12000	2EE0
		13714.28 (96000/7)	3592
		19200	4B00
		24000	5DC0

**Table 3 Variable Sample Rates Supported**

The following table shows which registers control which DAC rates, versus Mode and ID selected

CODEC ID	FRONT DAC RATE REGISTER	ADC RATE REG
00 and 01	2Ch	32h
10	2Eh	
11	2Ch (centre) and 30h (LFE)	

**Table 4 Variable Rate Register Location Versus ID**

**GAIN CONTROL REGISTER LOCATION VERSUS ID**

PGA	CODEC ID	CONTROL REG	MUTE DEFAULT
DAC	0x	18h	Muted (bit-15)
	10		AND with 38h, 7, 15
	11		AND with 36h, 7, 15
Mixer	0x	72h	Not-muted (bit-15)
	10		
	11		
Volume	0x	02h	Muted (15)
	10	38h	Muted (7 and 15)
	11	36h	Muted (7 and 15)

**Table 5 Gain Control Register Location Versus ID****MASTER/SLAVE ID0/1 SUPPORT**

WM9703 supports operation as either a master or a slave codec. Configuration of the device as either a master or as a slave, is selected by tying the CID pins CID0 and CID1, pins 45 and 46 on the package.

Fundamentally, a device identified as a master (ID = 00) produces BITCLK as an output, whereas a slave (any other ID) must be provided with BITCLK as an input. This has the obvious implication that if the master device on an AC link is disabled, the slave devices cannot function.

The AC'97 Revision 2.1 specification defines that the CID pins have inverting sense, and are provided with internal weak pull ups. Therefore, if no connections are made to the CID0/1 pins, then the pins pull hi and an ID = 00 is selected, i.e. master. External connects to ground will select other IDs.

PIN46 CID1	PIN45 CID0	ID SELECTED	MASTER OR SLAVE	BITCLK
NC	NC	00	Master	Output
NC	Ground	01	Slave	Input
Ground	NC	10	Slave	Input
Ground	Ground	11	Slave	Input

**Table 6 ID Selection**

WM9703 supports the AMAP function whereby selection of an ID will automatically map the data from the interface onto the PCM DACs. This allows a 6-channel audio system to be built using 3 WM9703 devices, with one device configured as a master (ID 00) and the other two as slaves (ID 10 and 11). (See figure 10). In this case, the main channel DACs will have mapped onto them the data from the normal, surround, and LFE and centre slots respectively, without any user selection.

CODEC ID	AC-LINK FRAME DATA USED FOR DACS		COMMENTS
	PCM left DAC uses data from slot No.	PCM right DAC uses data from slot No.	
00	3	4	Original definition (master)
01	3	4	Original definition (docking)
10	7	8	Left/right surround channels
11	6	9	Centre/LFE channels

The codec ID is available to the controller via register 28h, bits D15 and D14

**Table 7 Default Slot to DAC Mappings Based on Codec ID**

CODEC ID	SLOTS MAPPED TO DACS
00 or 01	3 and 4
10	7 and 8
11	6 and 9

**Table 8 Slot to DAC and Mapping Based on Codec ID**

### CONTROL INTERFACE

A digital interface has been provided to control the WM9703 and transfer data to and from it. This serial interface is compatible with the Intel AC'97.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller
- Selection of powerdown modes

### AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

The WM9703 incorporates a 5-pin digital serial interface that links it to the AC'97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The WM9703 provides support for 18-bit operation.

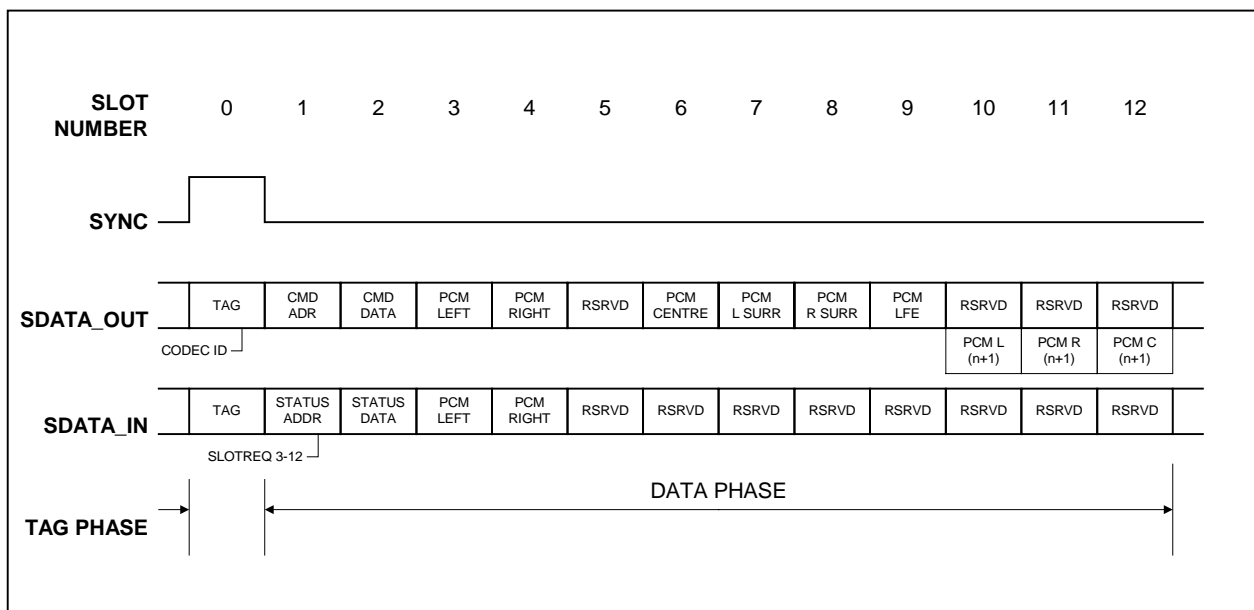


Figure 12 AC'97 Standard Bi-directional Audio Frame

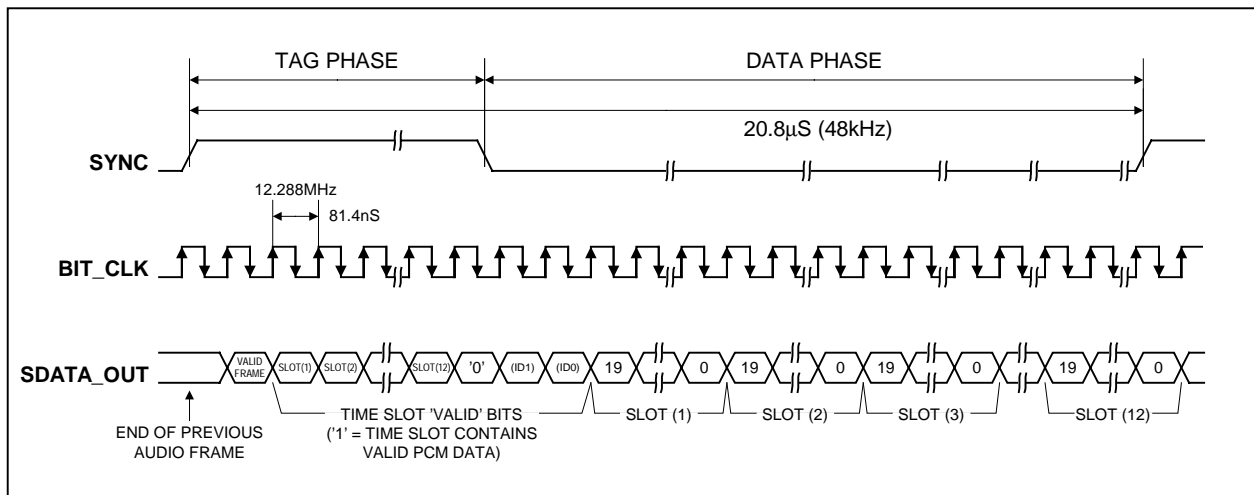


Figure 13 AC-link Audio Output Frame

The datastreams currently defined by the AC'97 specification include:

<b>PCM playback - 2 output slots</b>	2-channel composite PCM output stream
<b>PCM record data - 2 input slots</b>	2-channel composite PCM input stream
<b>Control - 2 output slots</b>	Control register write port
<b>Status - 2 input slots</b>	Control register read port
<b>Optional modem line codec output - 1 output slot</b>	Modem line codec DAC input stream
<b>Optional modem line codec input - 1 input slot</b>	Modem line codec ADC output stream
<b>Optional dedicated microphone input - 1 input slot</b>	Dedicated microphone input stream in support of stereo AEC and/or other voice applications.

Synchronisation of all AC-link data transactions is signalled by the WM9703 controller. The WM9703 drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial clock (BIT\_CLK). BIT\_CLK, fixed at 12.288MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT\_CLK. The receiver of AC-link data, (WM9703 for outgoing data and AC'97 controller for incoming data), samples each serial bit on the falling edges of BIT\_CLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (the WM9703 for the input stream, AC'97 controller for the output stream); to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT\_CLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the Data Phase. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that the WM9703 be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

## AC-LINK AUDIO OUTPUT FRAME (SDATA\_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the WM9703's DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

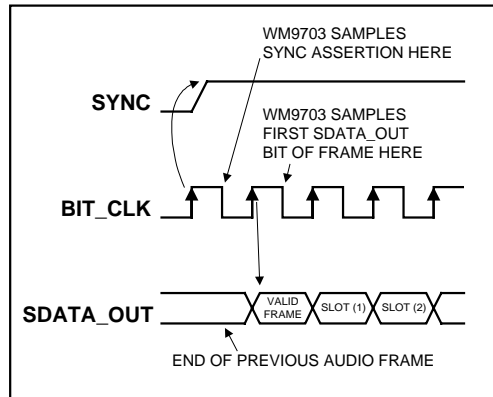
### OUTPUT TAG SLOT (16-BITS)

Bit (15)	Frame Valid	
Bit (14)	Slot 1 Valid Command Address bit	(Primary Codec only)
Bit (13)	Slot 2 Valid Command Data bit	(Primary Codec only)
Bit (12:3)	Slot 3-12 Valid bits as defined by AC'97	
Bit 2	Reserved	(Set to 0)
Bit (1:0)	2-bit Codec ID field	(00 reserved for Primary; 01, 10, 11 indicate Secondary)
New definitions for Secondary Codec Register Access		

Within slot 0 the first bit is a global bit (SDATA\_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the Valid Frame bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by the WM9703 indicate which of the corresponding 12 time slots contain valid data.

In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. Figure 13 illustrates the time slot based AC-link protocol.





**Figure 14 Start of an Audio Output Frame**

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 14. SYNC is synchronous to the rising edge of BIT\_CLK. On the immediately following falling edge of BIT\_CLK, the WM9703 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT\_CLK, AC'97 transitions SDATA\_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT\_CLK, and subsequently sampled by the WM9703 on the following falling edge of BIT\_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC'97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48ks/s on the AC'97 controller.

This requirement is necessary to ensure that interoperability between the AC'97 controller and the WM9703, among other things, can be guaranteed by definition for baseline specified AC'97 features.

SDATA\_OUT's composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC'97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC'97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

As an example, consider an 8-bit sample stream that is being played out to one of the WM9703's DACs. The first 8 bit positions are presented to the DAC (MSB justified) followed by the next 12 bit positions, which are stuffed with 0s by the AC'97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

**SLOT 1: COMMAND ADDRESS PORT**

The command port is used to control features, and monitor status for the WM9703 functions including, but not limited to, mixer settings, and power management (refer to the register section). The control interface architecture supports up to 64, 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid, odd register (01h, 03h, etc.) accesses are discouraged (if supported they should default to the preceding even byte boundary - i.e. a read to 01h will return the 16-bit contents of 00h). The WM9703's control register file is nonetheless readable as well as writable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and read/write command information to the WM9703.

**COMMAND ADDRESS PORT BIT ASSIGNMENTS**

Bit (19)	Read/write command (1 = read, 0 = write)
Bit (18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by the WM9703 indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC'97 controller.

**SLOT 2: COMMAND DATA PORT**

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (As indicated by slot 1, bit 19).

Bit (19:4)	Control register write data (stuffed with 0s if current operation is a read)
Bit (3:0)	Reserved (stuffed with 0s)

If the current command port operation is a read then the entire time slot must be stuffed with 0s by the AC'97 controller.

**SLOT 3: PCM PLAYBACK LEFT CHANNEL**

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

**SLOT 4: PCM PLAYBACK RIGHT CHANNEL**

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples.

If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

**SLOT 5: OPTIONAL MODEM LINE CODEC**

Audio output frame slot 5 contains the MSB justified modem DAC input data. This optional AC'97 feature is not supported in the WM9703, and if data is written to this location it is ignored. This may be determined by the AC'97 controller interrogating the WM9703 Vendor ID registers.

**SLOTS 6 TO 9: SURROUND SOUND DATA**

Audio output frame slots 6 to 9 are used to send surround sound data. This data is mapped onto the internal DACs depending on Codec ID, see Table 8.

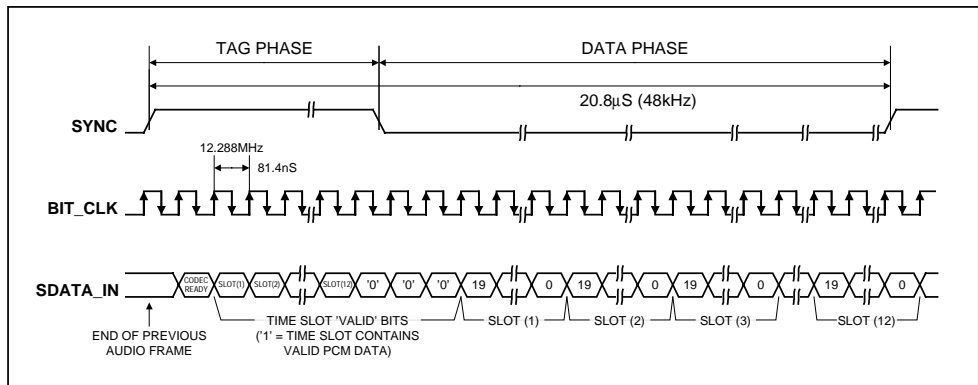
**SLOTS 10 AND 11: LINE2 AND HANDSET DAC**

These data slots are not supported.

**SLOT 12: GPIO CONTROL**

These data slots are not supported.

**AC-LINK AUDIO INPUT FRAME (SDATA\_IN)**



**Figure 15 AC-link Audio Input Frame**

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots.

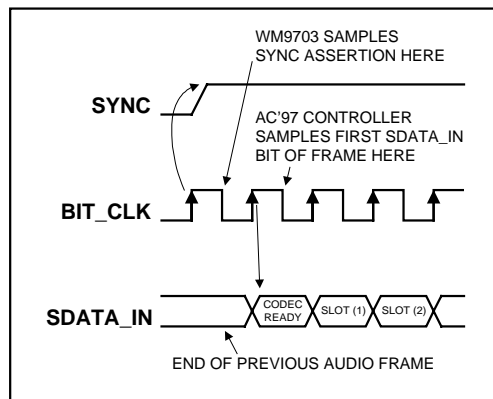
Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA\_IN slot 0, bit 15) which flags whether the WM9703 is in the Codec Ready state or not. If the Codec Ready bit is a 0, this indicates that the WM9703 is not ready for normal operation. This condition is normal following the desertion of power on reset for example, while the WM9703's voltage references settle. When the AC-link Codec Ready indicator bit is a 1, it indicates that the AC-link and the WM9703 control and status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting the WM9703 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA\_IN slot 0, bit 15) for an indication that the WM9703 has gone Codec Ready.

Once the WM9703 is sampled Codec Ready then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 15 illustrates the time slot based AC-link protocol.

There are several subsections within the WM9703 that can independently go busy/ready. It is the responsibility of the WM9703 controller to probe more deeply into the WM9703 register file to determine which the WM9703 subsections are actually ready.



**Figure 16 Start of an Audio Input Frame**

A new audio input frame begins with a low to high transition of SYNC as shown in Figure 16. SYNC is synchronous to the rising edge of BIT\_CLK. On the immediately following falling edge of BIT\_CLK, AC'97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT\_CLK, AC'97 transitions SDATA\_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT\_CLK, and subsequently sampled by the AC'97 Controller on the following falling edge of BIT\_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA\_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the WM9703. SDATA\_IN should be sampled on the falling edges of BIT\_CLK.

**SLOT 1: STATUS ADDRESS PORT**

The status port is used to monitor status for the WM9703 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1 echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged valid by the WM9703 during slot 0).

**STATUS ADDRESS PORT BIT ASSIGNMENTS:**

Bit (19)	RESERVED (stuffed with 0s)
Bit (18:12)	Control register index (echo of register index for which data is being returned)
Bit (11:2)	Variable sample rate SLOTREQ bits.
Bit (1:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by the WM9703 is always stuffed with an 0. The following 7 bit positions communicate the associated control register address. The next 10 bits support the AC'97 Rev 2.1 variable sample rate signalling protocol, and the trailing 2 bit positions are stuffed with 0s by AC'97.

**SLOT 2: STATUS DATA PORT**

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control register read data (stuffed with 0s if tagged invalid by WM9701)
Bit (3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged invalid by the WM9703, then the entire slot will be stuffed with 0s by the WM9703.

**SLOT 3: PCM RECORD LEFT CHANNEL**

Audio input frame slot 3 is the left channel output of the WM9703's input Mux, post-ADC.

The WM9703 sends out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

**SLOT 4: PCM RECORD RIGHT CHANNEL**

Audio input frame slot 4 is the right channel output of the WM9703's input Mux, post-ADC.

The WM9703's ADCs can be implemented to support 16, 18, or 20-bit resolution.

The WM9703 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

**SLOT 5: OPTIONAL MODEM LINE CODEC**

Audio input frame slot 5 contains MSB justified modem ADC output data. This optional feature is not supported by WM9703. This may be determined by the AC'97 controller interrogating the WM9703 Vendor ID register.

**SLOT 6: OPTIONAL DEDICATED MICROPHONE RECORD DATA**

Audio input frame slot 6 is an optional (post-ADC) third PCM system, input channel available for dedicated use by a desktop microphone. This optional AC'97 feature is not supported by the WM9703. This may be determined by the AC'97 controller interrogating the WM9703 Vendor ID register.

**SLOTS 7 TO 12: RESERVED**

Audio input frame slots 7 to 12 are reserved for future use and are always stuffed with 0s by the WM9703.

**AC-LINK LOW POWER MODE**

The AC-link signals can be placed in a low power mode. When the WM9703's Powerdown Register 26h, is programmed to the appropriate value, both BIT\_CLK and SDATA\_IN will be brought to, and held at a logic low voltage level.

BIT\_CLK and SDATA\_IN are transitioned low immediately following the decode of the write to the Powerdown Register 26h with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralised.

The AC'97 controller should also drive SYNC and SDATA\_OUT low after programming the WM9703 to this low power, halted mode.

Once the WM9703 has been instructed to halt BIT\_CLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT\_CLK.

**WAKING UP THE AC-LINK**

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 controller that performs the wake up task.

AC-link protocol provides for a Cold WM9703 Reset, and a Warm WM9703 Reset.

The current powerdown state would ultimately dictate which form of WM9703 reset is appropriate. Unless a cold or register reset (a write to the reset register) is performed, wherein the WM9703 registers are initialised to their default values, registers are required to keep state during all powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the powerdown was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

#### COLD WM9703 RESET

A cold reset is achieved by asserting RESETB for the minimum specified time. By driving RESETB low, BIT\_CLK, and SDATA\_OUT will be activated, or re-activated as the case may be, and all the WM9703 control registers will be initialised to their default power on reset values.

RESETB is an asynchronous WM9703 input.

#### WARM WM9703 RESET

A warm WM9703 reset will re-activate the AC-link without altering the current WM9703 register values. A warm reset is signalled by driving SYNC high for a minimum of 1 $\mu$ S in the absence of BIT\_CLK.

Within normal audio frames SYNC is a synchronous input. In the absence of BIT\_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the WM9703. The WM9703 will not respond with the activation of BIT\_CLK until SYNC has been sampled low again by the WM9703. This will preclude the false detection of a new audio frame.

## SERIAL INTERFACE REGISTER MAP DESCRIPTION

(See Table 21)

The serial interface bits perform control functions described as follows: The register map is fully specified by the AC'97 specification, and this description is simply repeated below, with optional unsupported features omitted.

#### RESET REGISTER (INDEX 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part, indication of modem support (not supported by the WM9703) and a code for the type of 3D stereo enhancement.

The ID decodes the capabilities of the WM9703 based on the following:

BIT	FUNCTION	VALUE ON WM9703
ID0	Dedicated Mic PCM in channel	0
ID1	Modem line codec support	0
ID2	Bass and treble control	0
ID3	Simulated stereo (mono to stereo)	0
ID4	Headphone out support	1
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	1
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	1
ID9	20-bit ADC resolution	0
SE4...SE0	Wolfson Microelectronics 3D enhancement	11000

**Table 9 Reset Register Function**

Note that the WM9703 defaults to indicate 18-bit compatibility. However, a control bit may be set in the vendor-specific registers that changes bits ID6 and ID8 to be 0, indicating a 16-bit device. It is unlikely that this function will be required, however, as the MSB justification of the ADC and DAC data means that a nominally 18-bit device should be fully compatible with controllers that only provide 16-bit support. Most PC type applications will only require 16-bit operation.

#### PLAY MASTER VOLUME REGISTERS (INDEX 02h, 04h AND 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), Register 04h controls the optional stereo headphone out, and Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

ML5 to ML0 is for left channel level, MR5 to MR0 is for the right channel and MM5 to MM0 is for the mono out channel.

Support for the MSB of the volume level is not provided by the WM9703. If the MSB is written to, then the WM9703 detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxx the WM9703 interprets that as x11111. It will also respond when read with x11111 rather than 1xxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	$\infty$ dB attenuation

**Table 10 Volume Register Function**

### MASTER TONE CONTROL REGISTERS (INDEX 08h)

Optional register for support of tone controls (bass and treble). The WM9703 does not support bass and treble and writing to this register will have no effect. Reading will result in all don't care values.

### PC BEEP REGISTER (INDEX 0Ah)

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

WM9703 defaults to the PC-beep path being muted, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	$\infty$ dB attenuation

**Table 11 PC-beep Register Function**

### ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0Ch - 18h)

This controls the gain/attenuation for each of the analogue inputs. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at  $-\infty$ dB.

### REGISTER 0Eh (MIC VOLUME REGISTER)

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008, which corresponds to 0dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	XXXXX	$-\infty$ dB gain

**Table 12 Mixer Gain Control Register Function**

**RECORD SELECT CONTROL REGISTER (INDEX 1Ah)**

Used to select the record source independently for right and left (see Table 13). The default value is 0000h, which corresponds to Mic in.

SR2 TO SR0	RIGHT RECORD SOURCE	SL2 TO SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
2	Video in (R)	2	Video in (L)
3	Aux in (R)	3	Aux in (L)
4	Line in (R)	4	Line in (L)
5	Stereo mix (R)	5	Stereo mix (L)
6	Mono mix	6	Mono mix
7	Phone	7	Phone

**Table 13 Record Select Register Function**

**RECORD GAIN REGISTERS (INDEX 1Ch AND 1Eh)**

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio Mic channel. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at  $-\infty$ dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	$-\infty$ dB gain

**Table 14 Record Gain Register Function**

**GENERAL PURPOSE REGISTER (INDEX 20h)**

This register is used to control several miscellaneous functions of the WM9703.

Below is a summary of each bit and its function. Only the 3D, MIX, MS and LPBK bits are supported by the WM9703. The MS bit controls the Mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 8000h which is all off.

BIT	FUNCTION	WM9703 SUPPORT
POP	PCM out path and mute, 0 = pre-3D, 1 = post-3D	Yes, but fixed at 1
ST	Simulated stereo enhancement, on/off 1 = on	No
3D	3D stereo enhancement on/off, 1 = on	Yes
LD	Loudness (bass boost) on/off, 1 = on	No
LLBK	Local loop back - for modem, line codec	No
RLBK	Remote loop back - for modem, line codec	No
MIX	Mono output select 0 = Mix, 1 = Mic	Yes
MS	Mic select 0 = Mic1, 1 = Mic2	Yes
LPBK	ADC/DAC/ loopback mode	Yes

**Table 15 General Purpose Register Function**

**3D CONTROL REGISTER (INDEX 22h)**

This register is used to control the centre and/or depth of the 3D stereo enhancement function built into of the AC'97 component. Only the depth bits, DP0 to 3 have effect in the WM9703.

DP3...DP0	DEPTH
0	0%
1	
-	
8	Typical value
-	
15	100%

**RESERVED REGISTER (INDEX 24h)**

This register was originally specified to control what sample rate AC'97 is sending or receiving samples for the optional modem in and out. Not supported by the WM9703.

**POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)**

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is *ready*. *Ready* is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0 to 7.

When the AC-link Codec Ready indicator bit (SDATA\_IN slot 0, bit 15) is a 1 it indicates that the AC-link and the WM9703 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

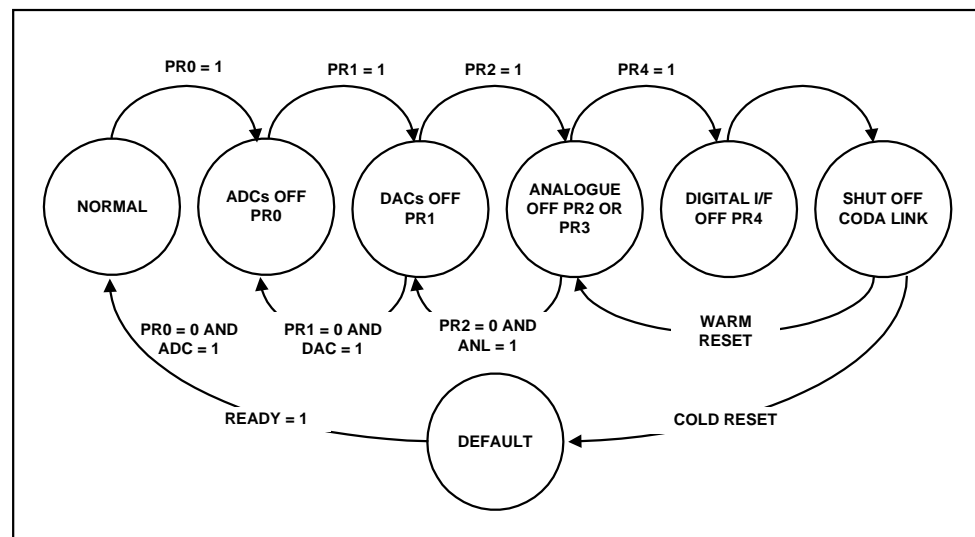
READ BIT	FUNCTION
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

**Table 16 Powerdown Status Register Function**

The powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR6 is not supported by the WM9703.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux powerdown
PR1	PCM out DACs powerdown
PR2	Analogue mixer powerdown (VREF still on)
PR3	Analogue mixer powerdown (VREF off)
PR4	Digital interface (AC-link) powerdown (external clock off)
PR5	Internal clock disable
PR6	HP amp powerdown – not supported
EAPD	External amplifier powerdown

**Table 17 Powerdown Control Register Function**



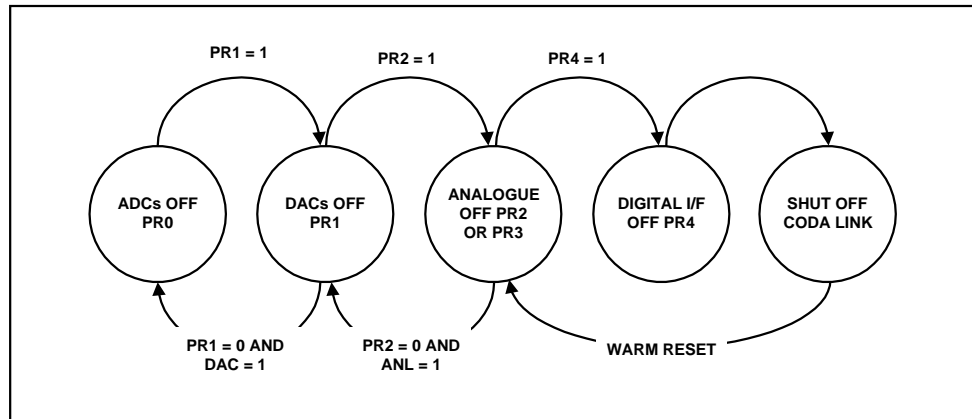
**Figure 17 An Example of the WM9703 Powerdown/Powerup Flow**



Figure 17 illustrates one example of a procedure to do a complete powerdown of the WM9703. From normal operation sequential writes to the Powerdown Register are performed to powerdown the WM9703 a piece at a time. After everything has been shut off (PR0 to PR3 set), a final write (of PR4) can be executed to shut down the WM9703's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up the WM9703, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart the WM9703's digital interface (resetting PR4 to 0). The WM9703 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the Powerdown Control/Status Register index 26h should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

Alternatively if RESETB is held low, all PR bits are held set so the device is held powered off until RESETB is taken high again.



**Figure 18 The WM9703 Powerdown/Flow with Analogue Still Alive**

Figure 18 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user is playing a CD (or external LINEIN source) through WM9703 to the speakers but has most of the system in low power mode. The procedure for this follows the previous except that the analogue mixer is never shut down.

**POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)**

Note that in order to go into ultimate low power mode, PR5 is required to be set which turns off the oscillator circuit. Asserting SYNC resets the PR5 bit and re-starts the oscillator in the same way as the AC link is restarted.

Also when RESETB pin is asserted low, all PR bits are over-ridden and the entire device is powered off to ultra low power state for as long as RESETB = low. On releasing RESETB, the device is reset (all active) and powered up.

**REVISION 2.1 REGISTERS (INDEX 28h TO 58h)**

These registers are specified as to use in Revision 2.1 of the AC'97 specification and have the following functions on the WM9703:

**REGISTER 28h – EXTENDED AUDIO ID**

The Extended Audio ID register is a read only register that identifies which extended audio features are supported (in addition to the original AC'97 features identified by reading the reset register at index 00h). A non zero value indicates the feature is supported.

DATA BIT	FUNCTION	ANY MODE
VRA	Variable rate audio support	1
DRA	Double rate audio support	0
VRM	Variable rate Mic ADC support	0
CDAC	Centre DAC support	0
SDAC	Surround DAC support	0
LDAC	LFE DAC support	0
AMAP	Slot to front DAC mapping support	1
ID1	Codec configuration – pin 45 value	Inverse of level at pin 45
ID0	Codec configuration – pin 46 value	Inverse of level at pin 46

**Table 18 Extended Audio Capability Register**

### REGISTER 2Ah – EXTENDED AUDIO STATUS AND CONTROL REGISTER

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

DATA BIT	FUNCTION	READ/WRITE	WM9703 SUPPORT
VRA	Enables variable rate audio mode	Read/write	Yes
DRA	Enable double rate audio mode	Read/write	No
VRM	Enables variable rate Mic ADC	Read/write	No
CDAC	Indicates centre DAC ready	Read	Yes
SDAC	Indicates surround DAC ready	Read	Yes
LDAC	Indicates LFE DAC ready	Read	Yes
MADC	Indicates Mic ADC ready	Read	No
PRI	Set to turn off centre DAC	Read/write	Enable only
PRJ	Set to turn off surround DACs	Read/write	Enable only
PRK	Set to turn off LFE DACs	Read/write	Enable only
PRL	Set to turn off Mic ADC	Read/write	No

**Table 19 Extended Audio Status and Control Register**

### REGISTER 2Ch TO 32h – AUDIO SAMPLE RATE CONTROL REGISTERS

These registers are read/write registers that are written to, to select alternative sample rates for the audio PCM converters. Default is the 48ks/s rate. Note that only Revision 2.1 recommended rates are supported by the WM9703, selection of any other unsupported rates will cause the rate to default to the nearest supported rate, and the supported rate value to be latched and so read back.

Register 2Ch is the front DAC rate register, but is also used for centre channel data rate.

### REGISTERS 36h AND 38h – 6 CHANNEL VOLUME CONTROL

These read/write registers control the output volume of the optional four PCM channels. (not supported by the WM9703)

## VENDOR RESERVED REGISTERS (INDEX 5Ah AND 7Ah)

These registers are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC '97 component.

### VENDOR SPECIFIC GAIN CONTROL REGISTERS – (INDEX 70h TO 74h)

Not used in the WM9703.

### VENDOR ID REGISTERS (INDEX 7Ch TO 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0, and the third T7 to T0. These three characters are ASCII encoded. The REVISION7 to REVISION0 field is for the Vendor Revision number. In the WM9703 the vendor ID is set to WML3.

Wolfson is a registered Microsoft Plug and Play vendor.

## SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	efault
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master volume mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	8000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Rec select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Rec gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General purpose	POP	ST	3D	ID	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0000h
26h	Power/down control status	APD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Ext'd audio ID	ID1	ID0	X	X	X	X	Amap	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0201h
2Ah	Ext'd audio stat/ctrl	X	PRL	PRK	PRJ	PRI	X	Madc	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0000h
2Ch	Front DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
72h	Front mixer volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	0808h
74h	Surround sound	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
7Ah	Vendor reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0	4C03h

**Table 21 Serial Interface Register Map Description**

RECOMMENDED EXTERNAL COMPONENTS

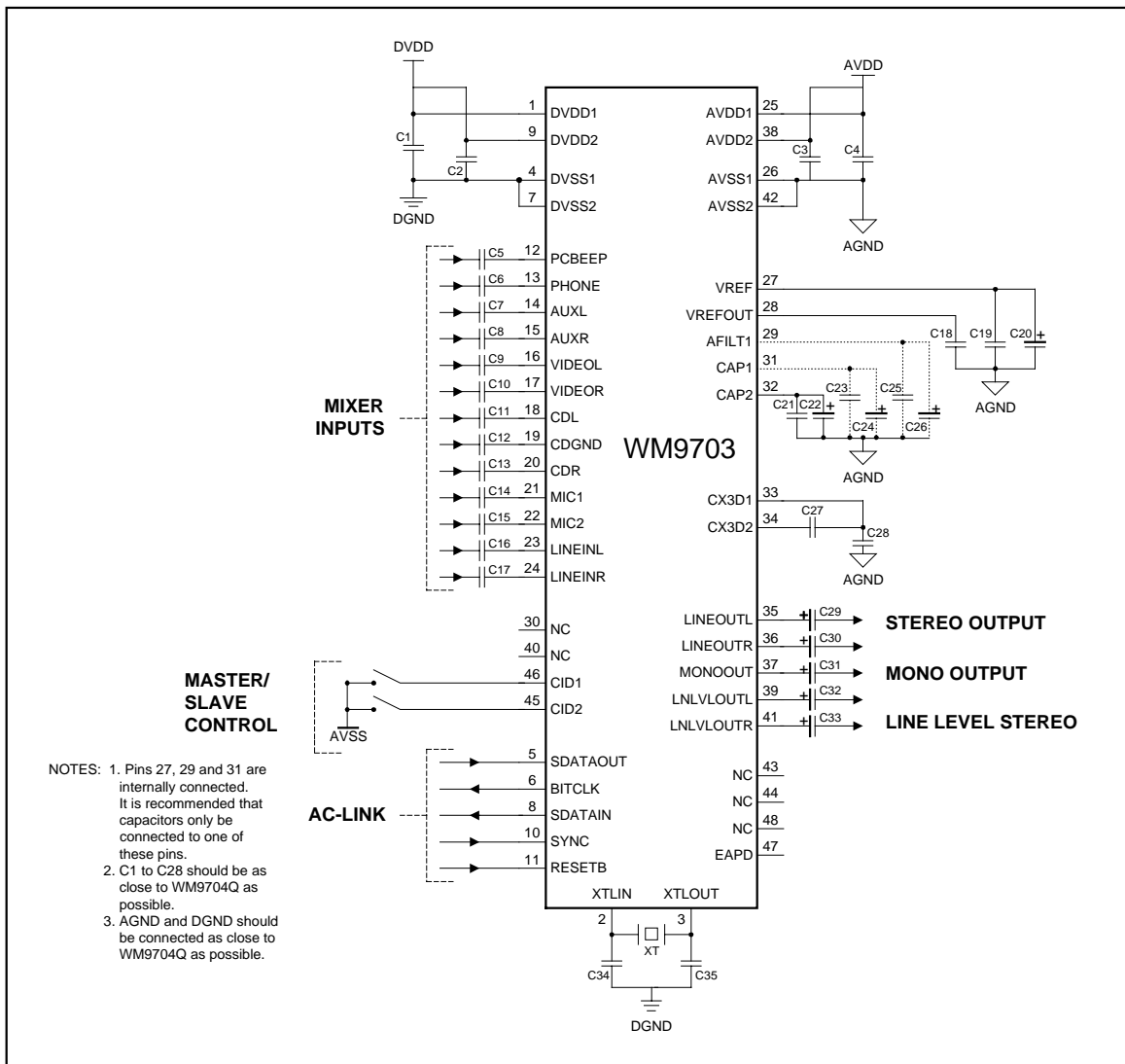


Figure 19 External Components Diagram

**RECOMMENDED EXTERNAL COMPONENTS VALUES**

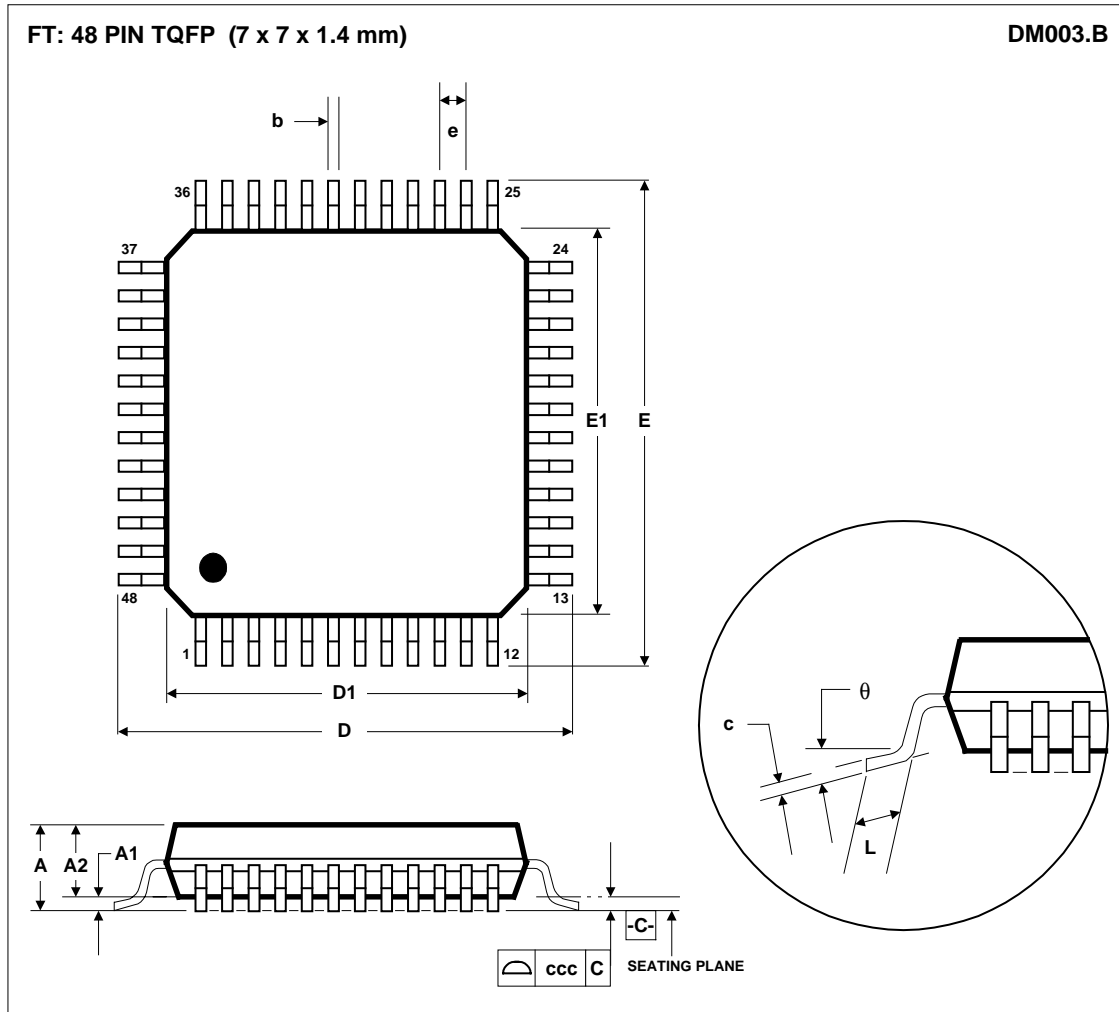
COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	10nF	De-coupling for DVDD and AVDD
C5 to C17	470nF	AC coupling capacitors for setting DC level of analogue inputs to VCAP1. Value chosen to give corner frequency below 20Hz for min 10K input impedance.
C18	1 $\mu$ F	Reference de-coupling capacitors for ADC, DAC, Mixer and CAP2 references. Ceramic type or similar.
C19	0.1 $\mu$ F	
C20	10 $\mu$ F	
C21	0.1 $\mu$ F	
C22	10 $\mu$ F	
C23	0.1 $\mu$ F	
C24	10 $\mu$ F	
C25	0.1 $\mu$ F	
C26	10 $\mu$ F	
C27	100nF	
C28	47nF	3D high pass filter. This value sets nominal 1kHz.
C29 to C33	10 $\mu$ F	Output AC coupling caps to remove VREF DC level from outputs.
C34 and C35	22pF	Optional capacitors for better crystal frequency stability.
XT	24.576 MHz	AC'97 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1M $\Omega$ ).

**Table 24 External Component Values****RECOMMENDATIONS FOR 3.3V OPERATION**

The device's performance with AVDD = 3.3V is shown in Electrical Characteristics.

In 3.3V analogue operation, mid-rail reference scales to 1.5V. All ADC and DAC references are 3/5<sup>th</sup>s of their nominal 5V value. Input and output signals that are 1V<sub>rms</sub> in 5V applications, scale to 660mV<sub>rms</sub> in 3.3V applications. If 1V<sub>rms</sub> output is required, the mixer gain adjust PGAs need to be increased by 3 times 1.5dB steps.

PACKAGE DIMENSIONS



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.60
A <sub>1</sub>	0.05	-----	0.15
A <sub>2</sub>	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D <sub>1</sub>	7.00 BSC		
E	9.00 BSC		
E <sub>1</sub>	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
$\theta$	0°	3.5°	7°
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

- NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.  
 D. MEETS JEDEC.95 MS-026, VARIATION = BBC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.