512Kx8 MONOLITHIC FLASH, SMD 5962-96692

FEATURES

- Access Times of 60, 70, 90, 120, 150ns
- Packaging
  - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
  - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
  - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
  - 32 lead Flatpack (Package 220)
- 1,000,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

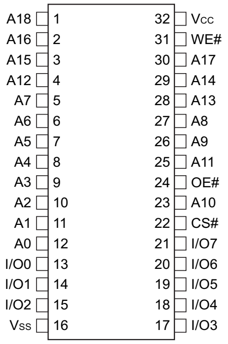
Note: For programming information refer to Flash Programming 4M5 Application Note.

This product is subject to change without notice.

Pin Configuration For WMF512K8-XXX5

32 DIP
32 CSOJ
32 Flatpack

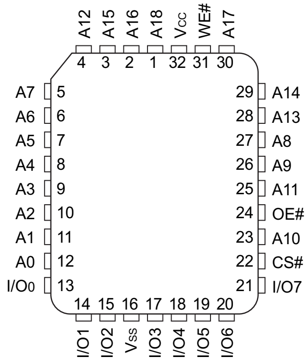
Top View



Pin Configuration For WMF512K8-XCLX5

32 CLCC

Top View



Pin Description

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (V_{CC}) (1)	-2.0 to +7.0	V
Signal Voltage Range(any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	20	years
Endurance - erase/program cycles (Mil Temp)	100,000 min	cycles
A9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	CAD	VI/O = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	COE	VIN = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	CWE	VIN = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	CCS	VIN = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	CI/O	VI/O = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS — CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	μA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	μA
V_{CC} Active Current for Read (1)	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz		50	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	CS# = V_{IL}, OE# = V_{IH}		60	mA
V_{CC} Standby Current	I_{CC4}	V_{CC} = 5.5, CS# = V_{IH}, f = 5MHz		1.6	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

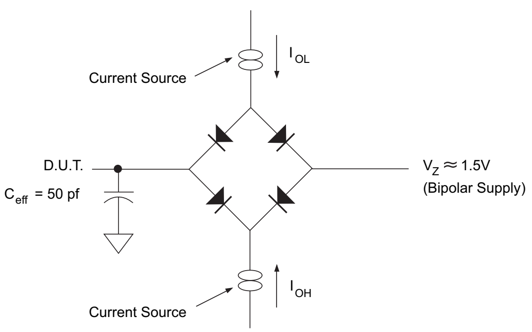
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	40		45		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	40		45		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	40		45		45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		0		0		ns
Chip Programming Time				11		11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase time is 8sec.

AC TEST CIRCUIT



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	VIL = 0, VIH = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE# CONTROLLED

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	60		70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	40		45		45		50		50		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	40		45		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		ns
Address Hold Time	t_{WHAX}	t_{AH}	40		45		45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		0		0		ms
VCC Set-up Time		t_{VCS}	50		50		50		50		50		µs
Chip Programming Time				11		11		11		11		11	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		ns
Output Enable Hold Time (4)		t_{OEH}	10		10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase time is 8sec.
4. For Toggle and Data# Polling.

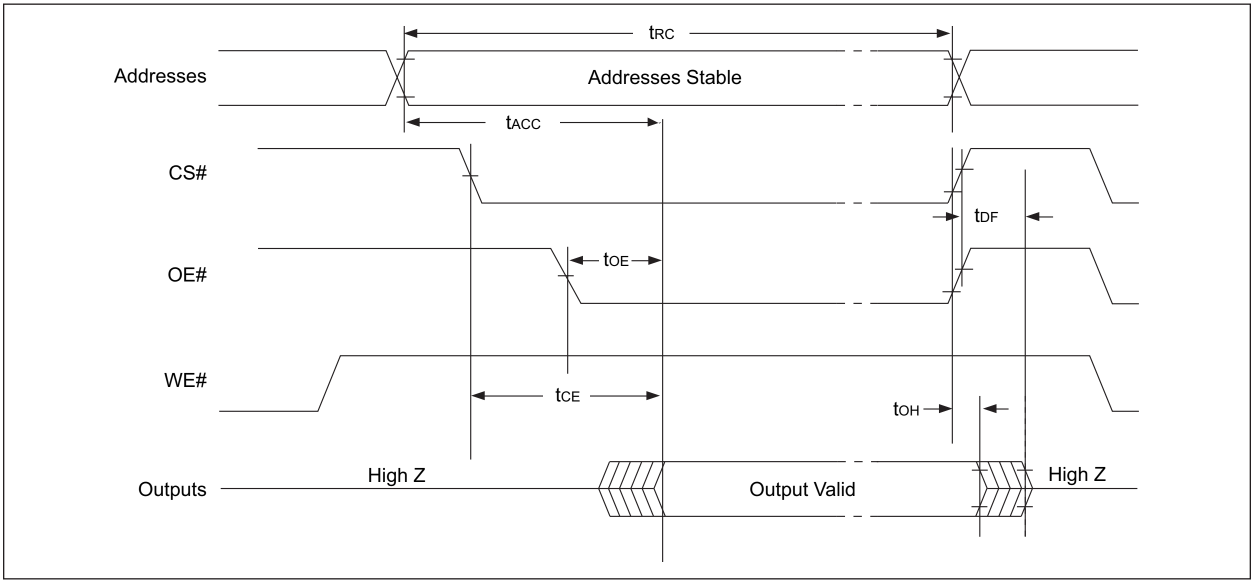
AC CHARACTERISTICS – READ ONLY OPERATIONS

V_{CC} = 5.0V, -55°C ≤ T_A ≤ +125°C

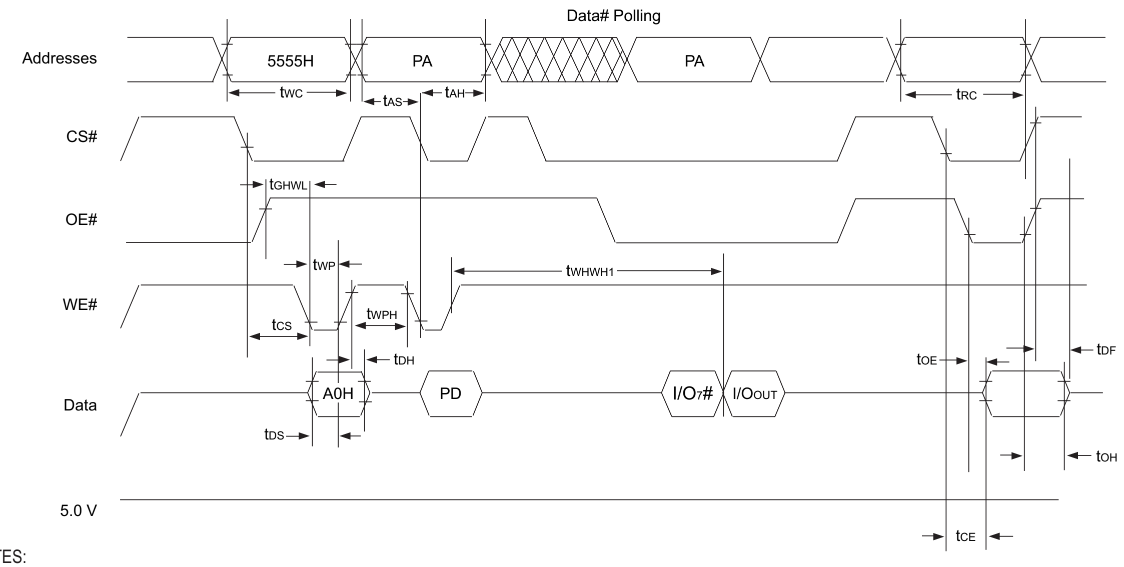
Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		60		70		90		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		35		35		35		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20		30		35	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		20		30		35	ns
Output Hold from Address, CS# or OE# Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		0		0		ns

NOTES:
1. Guaranteed by design, but not tested

AC WAVEFORMS FOR READ OPERATIONS

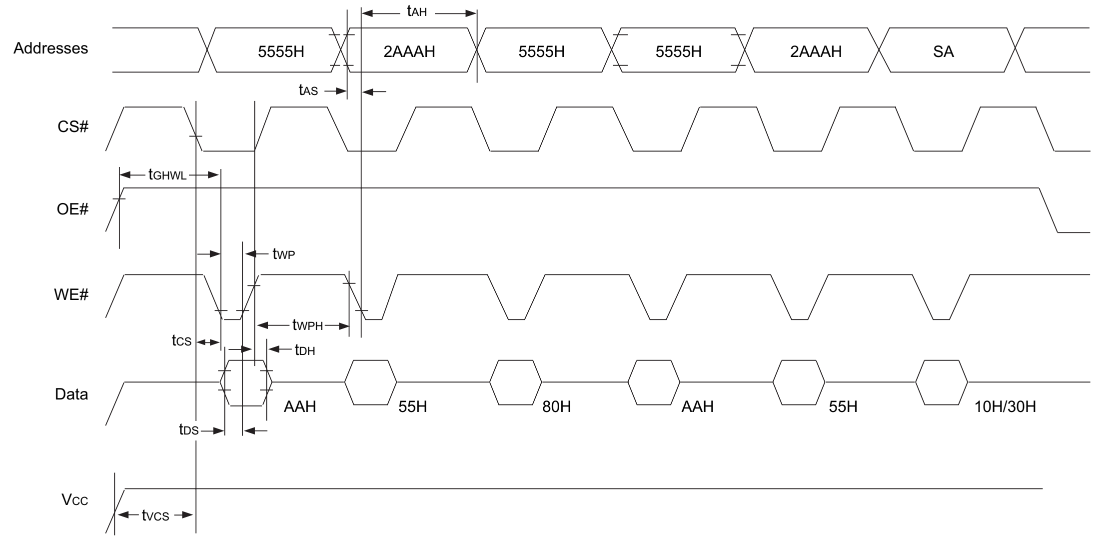


WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



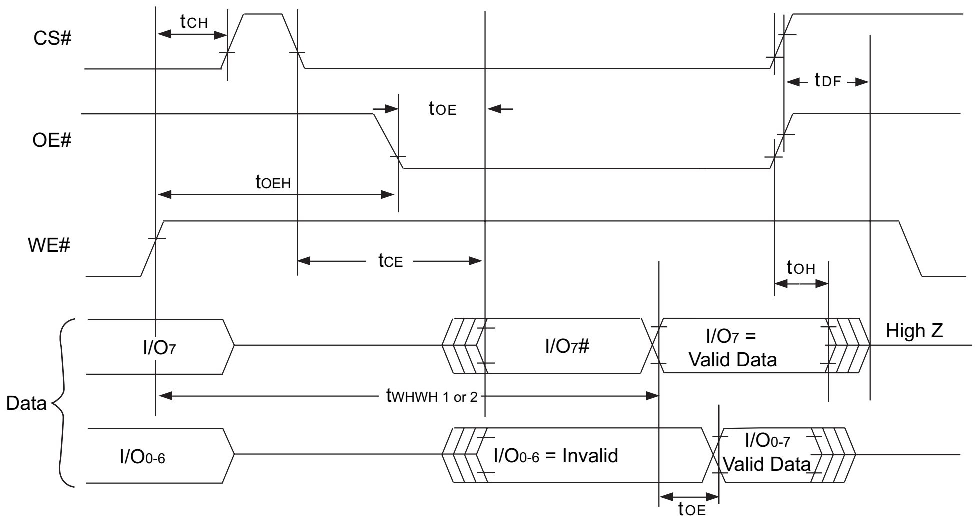
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. I/O7# is the output of the complement of the data written to the device.
4. I/OOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

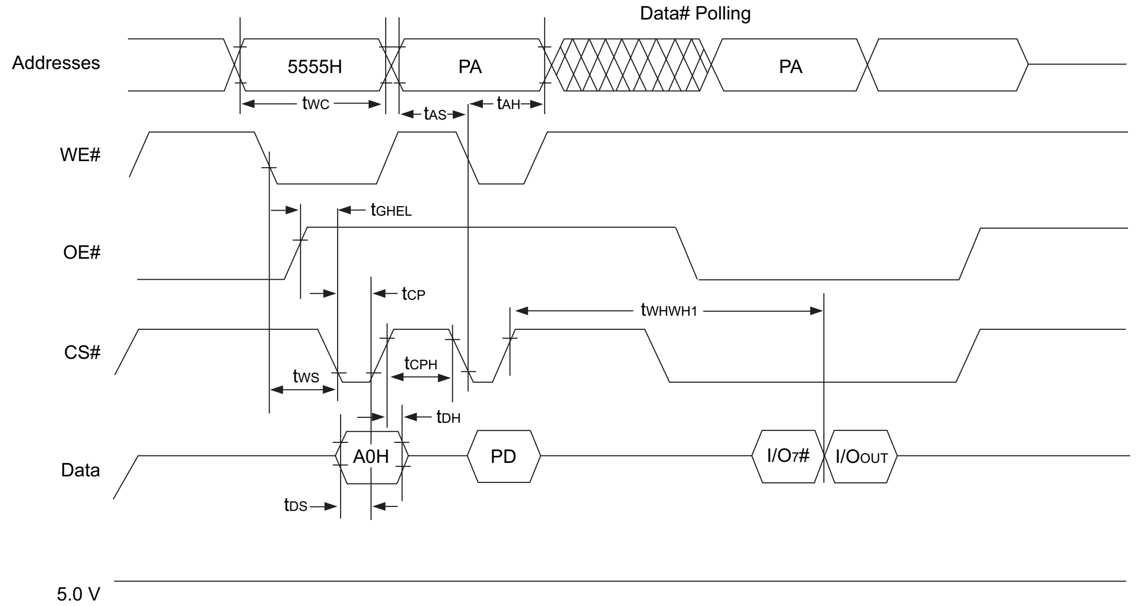


NOTES:
1. SA is the Sector Address for Sector Erase.

AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

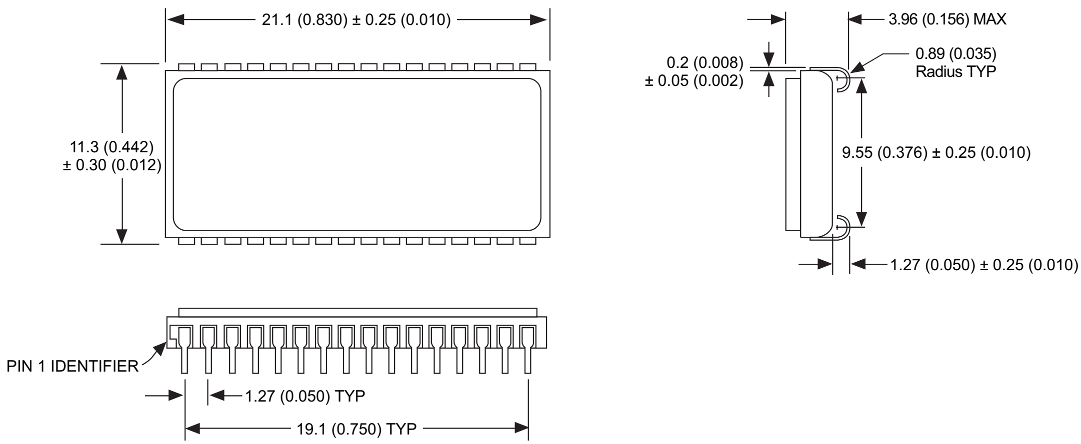


ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS



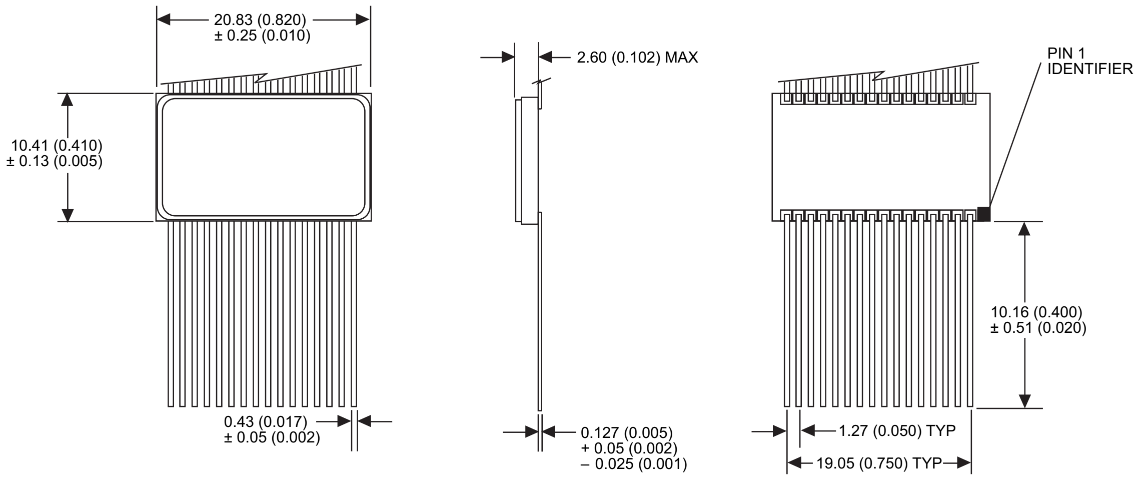
Notes:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. I/O7# is the output of the complement of the data written to the device.
4. I/OOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 101: 32 LEAD, CERAMIC SOJ



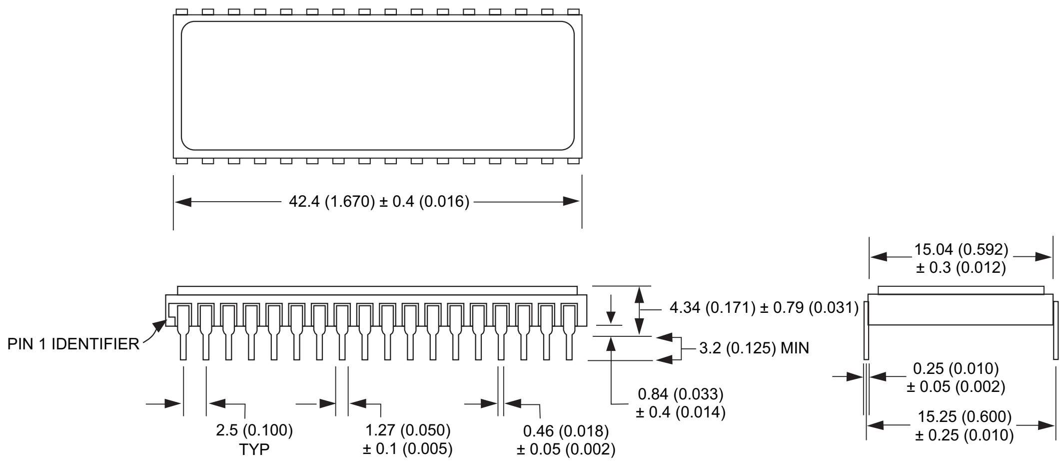
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 220: 32 LEAD, CERAMIC FLATPACK



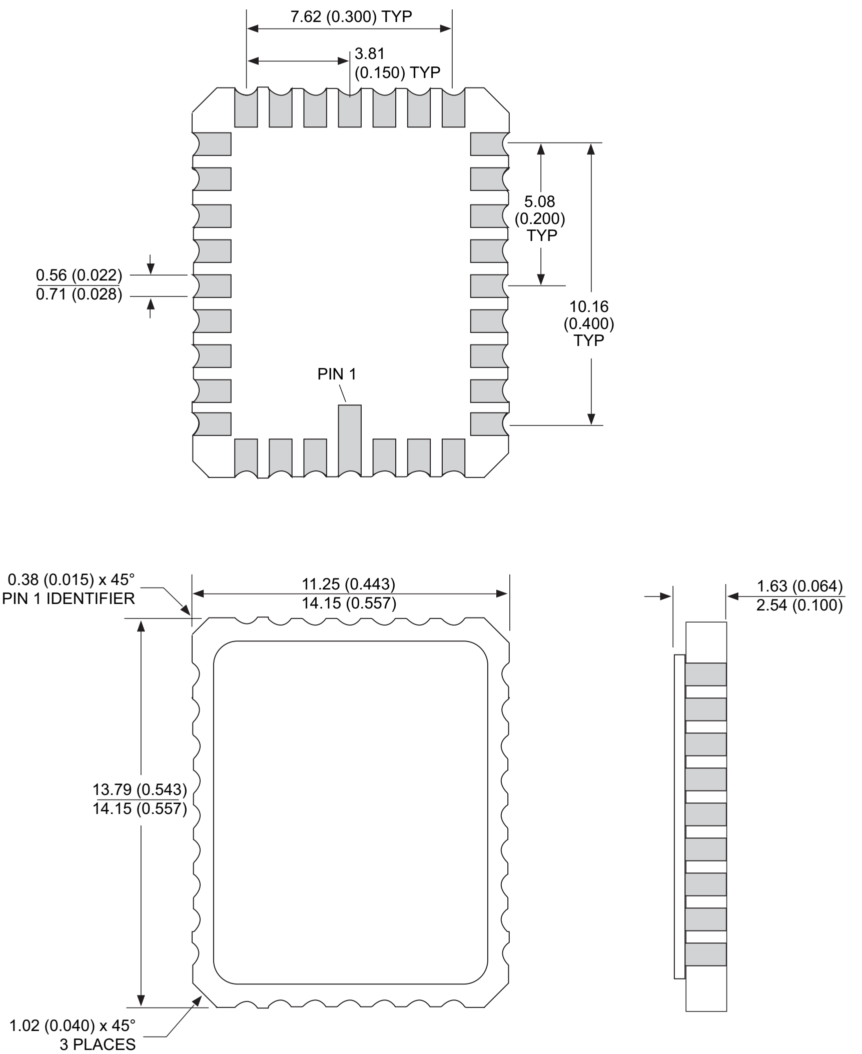
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M F 512K 8 - XXX X X 5 X

WHITE ELECTRONIC DESIGNS CORP.

MONOLITHIC

Flash

ORGANIZATION, 512K x 8

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 Pin Ceramic DIP (Package 300)

CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)

DE = 32 Lead Ceramic SOJ (Package 101)

FE = 32 Lead Flatpack (Package 220)

DEVICE GRADE:

M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

V_{PP} PROGRAMMING VOLTAGE

5 = 5V

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
512K x 8 Flash Monolithic	64KByte	150ns	32 pin DIP (C)	5962-96692 01HXX
512K x 8 Flash Monolithic	64KByte	120ns	32 pin DIP (C)	5962-96692 02HXX
512K x 8 Flash Monolithic	64KByte	90ns	32 pin DIP (C)	5962-96692 03HXX
512K x 8 Flash Monolithic	64KByte	70ns	32 pin DIP (C)	5962-96692 04HXX
512K x 8 Flash Monolithic	64KByte	150ns	32 lead SOJ (DE)	5962-96692 01HYX
512K x 8 Flash Monolithic	64KByte	120ns	32 lead SOJ (DE)	5962-96692 02HYX
512K x 8 Flash Monolithic	64KByte	90ns	32 lead SOJ (DE)	5962-96692 03HYX
512K x 8 Flash Monolithic	64KByte	70ns	32 lead SOJ (DE)	5962-96692 04HYX
512K x 8 Flash Monolithic	64KByte	150ns	32 lead Flatpack (FE)	5962-96692 01HUX
512K x 8 Flash Monolithic	64KByte	120ns	32 lead Flatpack (FE)	5962-96692 02HUX
512K x 8 Flash Monolithic	64KByte	90ns	32 lead Flatpack (FE)	5962-96692 03HUX
512K x 8 Flash Monolithic	64KByte	70ns	32 lead Flatpack (FE)	5962-96692 04HUX
512K x 8 Flash Monolithic	64KByte	150ns	32 lead Flatpack (FF)	5962-96692 01HTX
512K x 8 Flash Monolithic	64KByte	120ns	32 lead Flatpack (FF)	5962-96692 02HTX
512K x 8 Flash Monolithic	64KByte	90ns	32 lead Flatpack (FF)	5962-96692 03HTX
512K x 8 Flash Monolithic	64KByte	70ns	32 lead Flatpack (FF)	5962-96692 04HTX

Document Title

512K x 8 Flash Monolithic

Revision History

Rev #	History	Release Date	Status
Rev 1	Initial Release	September 1996	Preliminary
	Changes (Pg. 1) 1.1 Change status to Final	May 1997	Final
	Changes (Pg. 1) 1.1 Correct typo of Ceramic	February 1998	Final
	Changes (Pg. 10) 1.1 Remove pedestal from Flatpack package drawing	April 1998	Final
	Changes (Pg. 1) 1.1 Change name from 'FP' to Flatpack	February 1999	Final
Rev 2	Changes (Pg. 1, 2, 3, 4, 13) 2.1 Change number of max program/erases to 1,000,000 2.2 Change temperature of max program/erases to 25C 2.3 Absolute Maximum Ratings Table: 2.3.1 Change Data Retention to 20years 2.3.2 Change Endurance to 100,000 cycles minimum 2.4 Write/Erase/Program Operations Tables: 2.4.1 Change t_{WHWH1} to 300µs 2.4.2 Add Note (1) Typical t_{WHWH1} = 7µs 2.4.3 Change t_{WHWH2} to 15sec 2.4.4 Add Note (2) Typical t_{WHWH2} = 1 sec 2.4.5 Change Chip Programming Time to 11 sec 2.4.6 Change Chip Erase Time too 64 sec 2.4.7 Add Note (3) Chip Erase Time = 8 sec 2.5 Ordering Information 2.5.1 Change Company Name to White EDC 2.6 Change Title Style to new WEDC look	May 1999	Final
Rev 3	Changes (Pg. 1, 2, 10, 12, 13) 3.1 Change package 206 to package 220 3.2 Remove temperature range notice for Endurance 3.3 Change width spec to 0.457" minimum for package 601	May 1999	Final
Rev 4	Changes (Pg. 1, 3, 4) 4.1 Add 60ns speed grade option	January 2003	Final
Rev 5	Changes (Pg. 1, 11, 13) 5.1 Add 'T' case outline for 'FF' package	April 2005	Final
Rev 6	Changes (Pg. 1, 13) 6.1 Change revision history Rev 2.4.1 to 300 µs 6.2 Change revision history Rev 2.4.2 to 7µs	November 2005	Final