

**PRELIMINARY**



# **WMS7140/1**

**NONVOLATILE DIGITAL POTENTIOMETERS**

**WITH UP/DOWN (3-WIRE) INTERFACE,**

**10KOHM, 50KOHM, 100KOHM RESISTANCE**

**16 TAPS**

**WITH OPTIONAL OUTPUT BUFFER**

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## 1. GENERAL DESCRIPTION

The WMS714x is a 16 non-volatile linear digital potentiometers available in 10K $\Omega$ , 50K $\Omega$  and 100K $\Omega$  resistance values. The WMS7140/1 can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications.

The output of each potentiometer is determined by the wiper position, which varies in linearly between  $V_A$  and  $V_B$  terminal according to the content stored in the volatile Tap Register (TR) which is programmed through Up/Down (Increment/Decrement) interface. The channel has one non-volatile memory location (NVMEM0) that can be directly written to by users through the Up/Down interface. Power-on recall is also built in so the content of the NVMEM0 to Tap Register is automatically loaded.

The WMS7140/1 devices pin out the resistor wiper directly. The WMS7141 devices feature an output buffer with 3mA minimum drive capability.

All the WMS7140/1 devices are single channel devices offered in 8-pin PDIP, SOIC and MSOP packages. The WMS7140/1 devices operate over a wide operating voltage ranging from 2.7V to 5.5V.

## 2. FEATURES

- Drop-in replacements for many popular parts
- Available output buffer for WMS7141 devices
- Single linear-taper channel
- 16 taps
- 10K, 50K and 100K end-to end resistance
- $V_{SS}$  to  $V_{DD}$  terminal voltages
- Non-volatile storage of wiper positions with power-on recall
- Data storage and potentiometer control through Up/Down (3-wire) interface
- Endurance 100,000 write cycles
- Data retention 100 years
- Package options:
  - 8-pin PDIP, SOIC or MSOP
- Industrial temperature range: -40° ~ 85°C
- Single supply operation 2.7V to 5.5V



3. BLOCK DIAGRAM

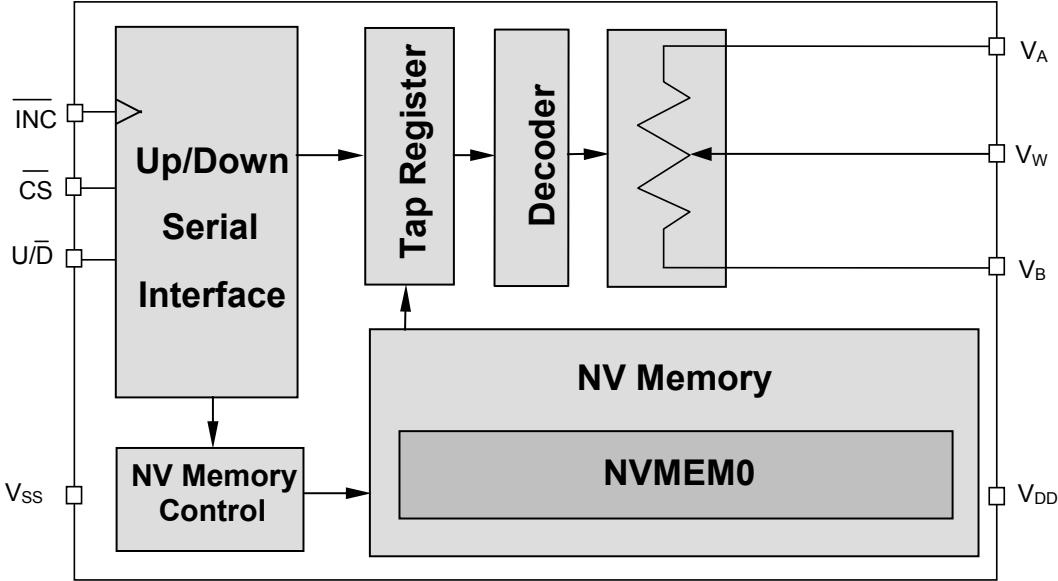


FIGURE 1 – WMS7140 BLOCK DIAGRAM (Rheostat Mode)

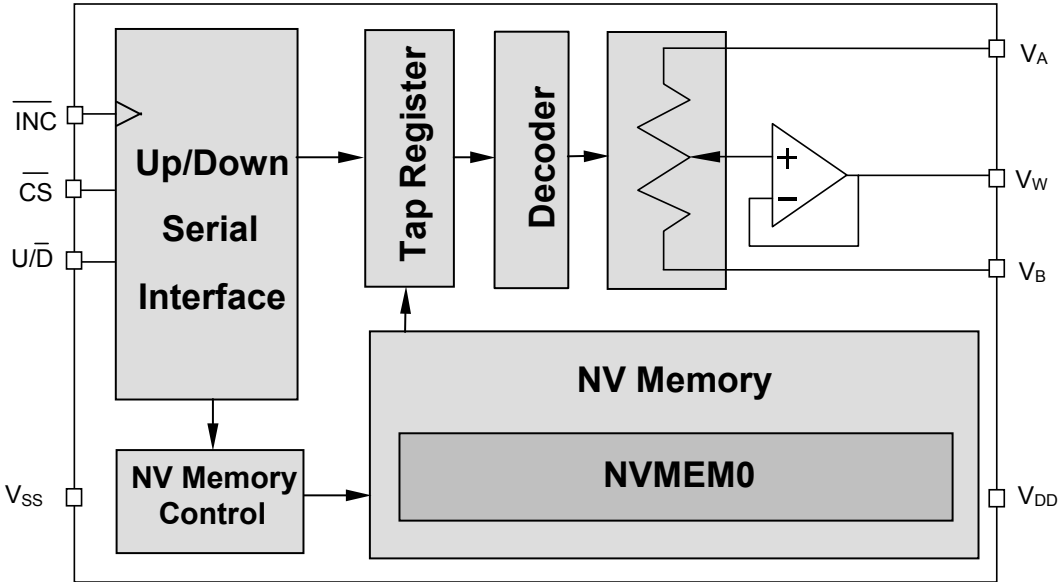


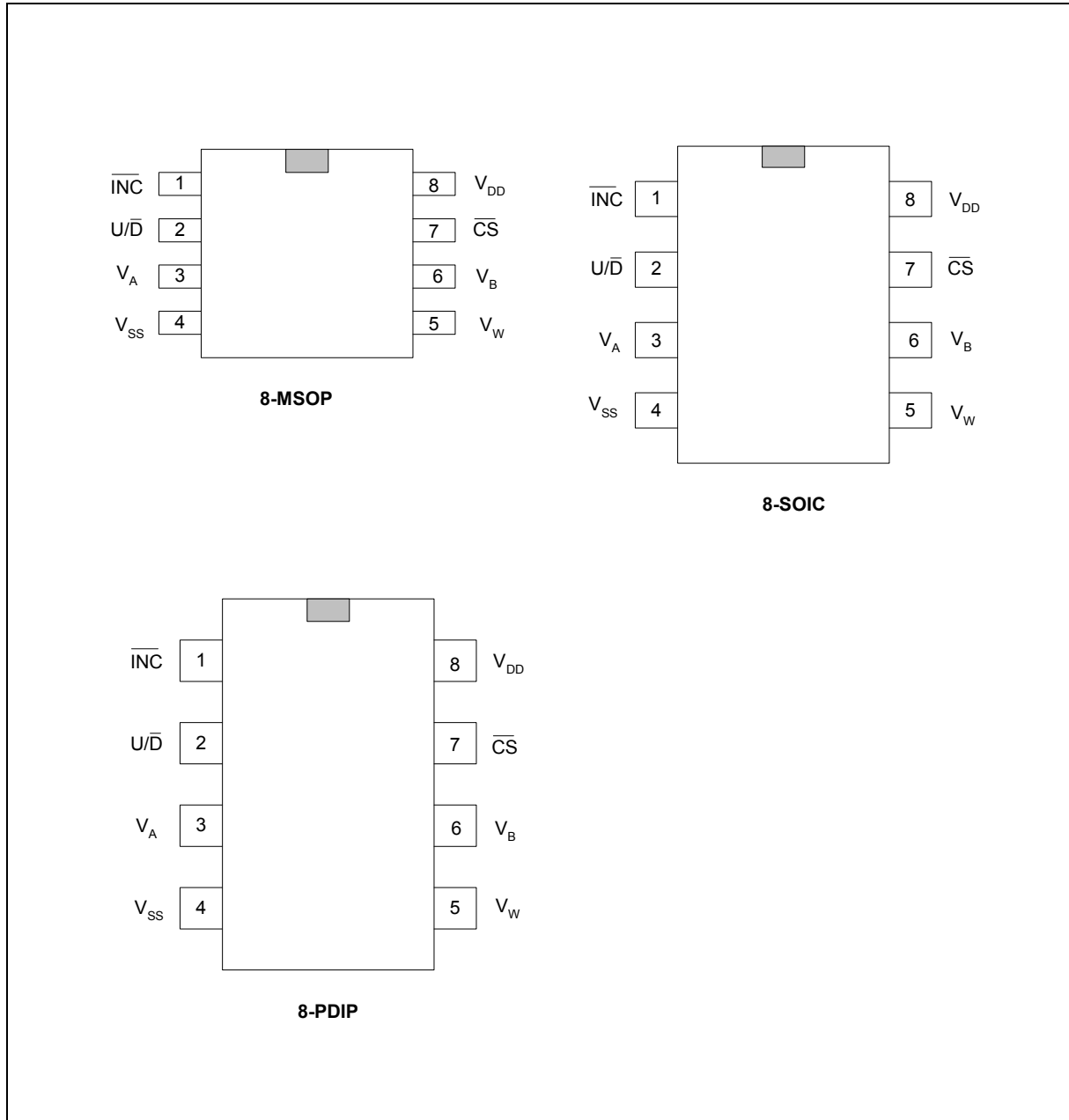
FIGURE 2 – WMS7141 BLOCK DIAGRAM (Divider Mode)



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## 5. PIN CONFIGURATION



## 6. PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Pin Name	I/O	Description
$\overline{\text{INC}}$	I	Increment Control. A High-Low transition of $\overline{\text{INC}}$ when $\overline{\text{CS}}$ is low will move the wiper up or down for one increment based on the $\overline{\text{U/D}}$ input
$\overline{\text{U/D}}$	I	Up/Down control Input. High state will cause the wiper to move to the $V_B$ terminal, Low state to the $V_A$ terminal
$V_A$	-	High terminal of WinPot
$V_{SS}$	-	Ground pin, logic ground reference
$V_{DD}$	-	Power Supply
$\overline{\text{CS}}$	I	Chip Select. When $\overline{\text{CS}}$ is HIGH, the part is deselected and the device will be in the standby mode. $\overline{\text{CS}}$ LOW enables the part, placing it in the active power mode
$V_B$	-	Low terminal of WinPot
$V_W$	O	Wiper terminal of WinPot (can be buffered), its position on the resistor array is controlled by the inputs on $\overline{\text{INC}}$ , $\overline{\text{U/D}}$ , and $\overline{\text{CS}}$



## 7. FUNCTIONAL DESCRIPTION

The WMS7140/1, a nonvolatile digitally programmable potentiometers with 16 taps, with or without output buffer, is designed to operate as both a potentiometer or a variable resistor depending upon the output configuration selected.

The chip can store up to one 8-bit word in a nonvolatile memory (NVMEM0) in order to set the tap register value when the device is powered up.

The WMS7140/1 is controlled by a serial Up-Down (3-wire) interface that allows setting the tap register value as well as storing data in the nonvolatile memory.

### 7.1. POTENTIOMETER AND RHEOSTAT MODES

The WMS7140/1 can operate as either a rheostat or as a potentiometer (voltage divider). When in the potentiometer configuration there are two possible modes. One is done using WMS7140 Winpot device without the output buffer and the other mode is done with WMS7141 WinPot device with the output buffer.

#### 7.1.1. Rheostat Configuration

The WMS7140/1 acts as a two terminal resistive element in the rheostat configuration where one terminal can be connected to either the end point pins of the resistor ( $V_A$  and  $V_B$ ) and the other terminal is the wiper ( $V_W$ ) pin. This configuration controls the resistance between the two terminals and the resistance can be adjusted by sending the corresponding tap register setting to the WMS7140/1 or can also be set by loading a pre-set tap register value from nonvolatile memory NVMEM0 upon power up.

#### 7.1.2. Potentiometer Configuration

In potentiometer configuration an input voltage is applied to either one of the end point pins ( $V_A$  or  $V_B$ ). The voltage on the wiper pin will be proportional to the voltage difference between  $V_A$  and  $V_B$  and the wiper setting. The resistance cannot be directly measured in this configuration.

### 7.2. NON-VOLATILE MEMORY (NVMEM)

The WMS7140/1 has one NVMEM position available for storing the potentiometer setting. The NVMEM position can be directly written via the Up/Down interface. The potentiometer is loaded with the value stored in the NVMEM0 on power up.



### 7.3. SERIAL DATA INTERFACE

The Up/Down family has a 3-wire Serial Data Interface consisting of  $\overline{CS}$ ,  $\overline{INC}$ ,  $U/\overline{D}$  pins. Only UP/DOWN operations can be performed. The key features of this interface include:

- Increment/Decrement operations on the tap register (TR)
- Direct refresh of tap register (TR) from internal NVMEM
- Nonvolatile storage of the present tap register value into the NVMEM and automatic recall at power up
- For WMS7141 devices, output buffer amplifier

### 7.4. OPERATION OVERVIEW

The wiper position or the Tap Register(TR) setting can only be changed by the UP/DOWN operation with the combination of  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$  signals. When  $\overline{CS}$  is low, the part will be activated and the TR setting can be changed by toggling  $\overline{INC}$ , and TR will move up when  $U/\overline{D}$  is High and move down when  $U/\overline{D}$  is Low. The TR setting will be stored into the user NVMEM automatically each time  $\overline{CS}$  goes high while  $\overline{INC}$  holds high. Otherwise, if  $\overline{INC}$  is low when  $\overline{CS}$  goes high, the TR setting will not be stored. The NVMEM content will be automatically loaded into TR at Power On. The user NVMEM can be tested through the voltage measurement on the wiper pin after saving TR setting into the NVMEM and reloading into the TR. When the TR setting is already at LOW, further DOWN operations won't change the setting. Similarly, when TR setting is at HIGH, further UP operations won't change the setting.

When  $\overline{CS}$  is held HIGH, the part will be in Standby mode and the TR setting will not be changed.

The operating modes of Up/Down are summarized below.

$\overline{CS}$	$U/\overline{D}$	$\overline{INC}$	Operation
Low	High	High to Low	Wiper toward $V_A$
Low	Low	High to Low	Wiper toward $V_B$
Low to High	x	High	Store Wiper Position
Low to High	x	Low	No Store, Return to Standby
High	x	x	Standby

Note: x means don't care



### 8. TIMING DIAGRAMS

Conditions:  $V_{DD} = +2.7V$  to  $5.5V$ ,  $V_A = V_{DD}$ ,  $V_B = 0V$ ,  $T = 25^\circ C$

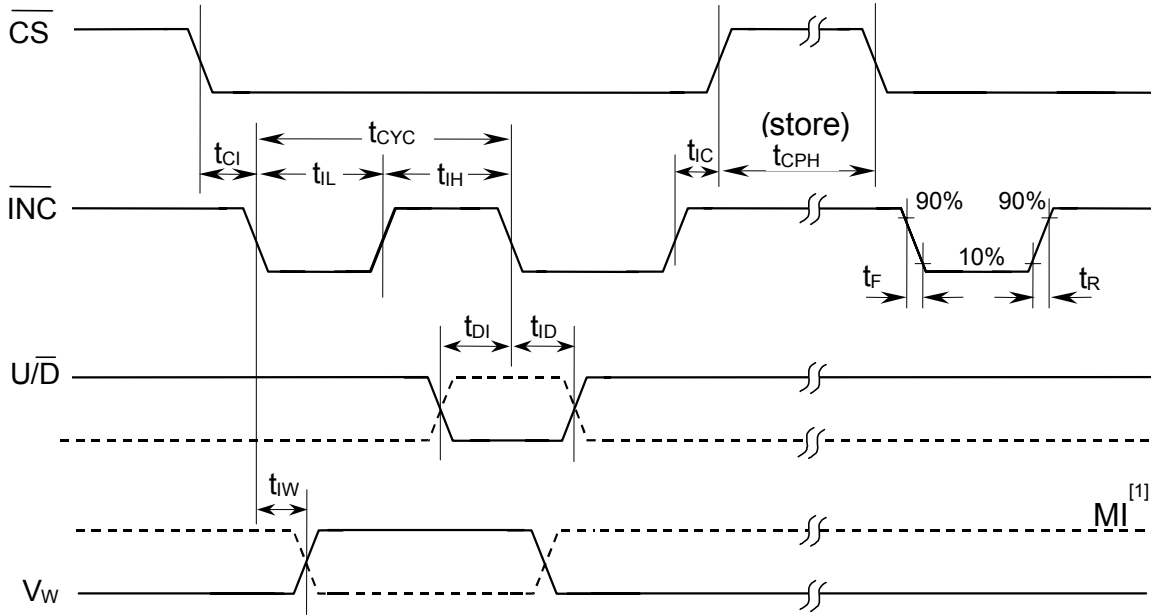


FIGURE 3 –WMS7140/1 TIMING DIAGRAM

Note:

[1] MI in the AC Timing diagram (Figure 3) refers to the minimum incremental change in the wiper output due to a change in the wiper position.

TABLE 10 – TIMING PARAMETERS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
$\overline{\text{CS}}$ to $\overline{\text{INC}}$ Setup	$t_{\text{CI}}$	100		ns
U/D to $\overline{\text{INC}}$ Setup	$t_{\text{DI}}$	50		ns
U/D to $\overline{\text{INC}}$ Hold	$t_{\text{ID}}$	100		ns
$\overline{\text{INC}}$ LOW Period	$t_{\text{IL}}$	250		ns
$\overline{\text{INC}}$ HIGH Period	$t_{\text{IH}}$	250		ns
$\overline{\text{INC}}$ Inactive to $\overline{\text{CS}}$ Inactive	$t_{\text{IC}}$	1		$\mu\text{s}$
$\overline{\text{CS}}$ Deselect Time (NO STORE)	$t_{\text{CPH}}$	100		ns
$\overline{\text{CS}}$ Deselect Time (STORE)	$t_{\text{CPH}}$	15 (2.7V)		ms
$\overline{\text{INC}}$ to $V_{\text{W}}$ Change	$t_{\text{IW}}$		5	$\mu\text{s}$
$\overline{\text{INC}}$ Cycle Time	$t_{\text{CYC}}$	1		$\mu\text{s}$
$\overline{\text{INC}}$ Input Rise and Fall Time	$t_{\text{R}}, t_{\text{F}}$		500	$\mu\text{s}$
Power-Up to Wiper Stable	$t_{\text{PU}}$		1	ms
$V_{\text{CC}}$ Power-Up rate	$t_{\text{R}} V_{\text{CC}}$	0.2 (13ms 0-2.7V)	50 (54 $\mu\text{s}$ 0-2.7V)	V/ms



## 9. ABSOLUTE MAXIMUM RATINGS

**TABLE 11 – ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)<sup>[1]</sup>**

Conditions	Values
Junction temperature	150°C
Storage temperature	-65° to +150°C
Voltage applied to any pad	(V <sub>SS</sub> – 0.3V) to (V <sub>DD</sub> + 0.3V)
V <sub>DD</sub> – V <sub>SS</sub>	-0.3 to 7.0V

**TABLE 12 – OPERATING CONDITIONS (PACKAGED PARTS)**

Conditions	Values
Commercial operating temperature range	0°C to +70°C
Extended operating temperature	-20°C to +70°C
Industrial operating temperature	-40°C to +85°C
Supply voltage (V <sub>DD</sub> )	+2.7V to +5.5V
Ground voltage (V <sub>SS</sub> )	0V

<sup>[1]</sup> Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions

**10. ELECTRICAL CHARACTERISTICS**
**TABLE 12 – ELECTRICAL CHARACTERISTICS (Packaged parts)**

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>Rheostat Mode</b>						
Nominal Resistance	R	-20		+20	%	T=25°C, V <sub>W</sub> open
Different Non Linearity <sup>[2]</sup>	DNL	-1		+1	LSB	
Integral Non Linearity <sup>[2]</sup>	INL	-1		+1	LSB	
Tempo <sup>1</sup>	$\Delta R_{AB}/\Delta T$		300		ppm/°C	
Wiper Resistance <sup>[2]</sup>	R <sub>W</sub>		50		Ω	V <sub>DD</sub> =5V, I=V <sub>DD</sub> /R <sub>Total</sub>
			80		Ω	V <sub>DD</sub> =2.7V, I=V <sub>DD</sub> /R <sub>Total</sub>
Wiper Current	I <sub>W</sub>	-1		1	mA	
<b>Divider Mode</b>						
Resolution	N	8			Bits	
Different Non Linearity <sup>[2]</sup>	DNL	-1	±0.2	+1	LSB	
Integral Non Linearity <sup>[2]</sup>	INL	-1	±0.2	+1	LSB	
Temperature Coefficient <sup>[1]</sup>	$\Delta V_w/\Delta T$		+20		ppm/°C	Code = 80h
Full Scale Error	V <sub>FSE</sub>	-1		0	LSB	Code = Full Scale
Zero Scale Error	V <sub>ZSE</sub>	0		1	LSB	Code = Zero Scale
<b>Resistor Terminal</b>						
Voltage Range	V <sub>A</sub> , V <sub>B</sub> , V <sub>W</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V	
Terminal Capacitance <sup>[1]</sup>	C <sub>A</sub> , C <sub>B</sub>		30		pF	
Wiper Capacitance <sup>[1]</sup>			30		pF	
<b>Dynamic Characteristics <sup>[1]</sup></b>						
Bandwidth –3dB	BW <sub>10K</sub>		1.5		MHz	V <sub>DD</sub> =5V, V <sub>B</sub> =V <sub>SS</sub>
	BW <sub>50K</sub>		300		KHz	Code = 80h
	BW <sub>100K</sub>		200		KHz	
Settling Time to 1 LSB	T <sub>S</sub>		80	100	uS	
<b>Analog Output (Buffer enables)</b>						
Amp Output Current	I <sub>OUT</sub>	3			mA	V <sub>O</sub> =1/2 scale
Amp Output Resistance	R <sub>out</sub>		1	10	Ω	I <sub>L</sub> = 100uA
Total Harmonic Distortion <sup>[1]</sup>	THD			0.08	%	V <sub>A</sub> =2.5V, V <sub>DD</sub> =5V, f=1kHz, V <sub>IN</sub> =1V <sub>RMS</sub>
<b>Digital Inputs/Outputs</b>						
Input High Voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>			V	
Input Low Voltage	V <sub>IL</sub>			0.3V <sub>DD</sub>	V	

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Low Voltage	$V_{OL}$			0.4	V	$I_{OL}=2mA$
Input Leakage Current	$I_{LI}$	-1		+1	$\mu A$	$\overline{CS}=V_{DD}, Vin=V_{SS} \sim V_{DD}$
Output Leakage Current	$I_{Lo}$	-1		+1	$\mu A$	$\overline{CS}=V_{DD}, Vin=V_{SS} \sim V_{DD}$
Input Capacitance <sup>[1]</sup>	$C_{IN}$		25		pF	$V_{DD}=5V, fc = 1Mhz$
Output Capacitance <sup>[1]</sup>	$C_{OUT}$		25		pF	$V_{DD}=5V, fc = 1Mhz$
<b>Power Requirements</b>						
Operating Voltage	$V_{DD}$	2.7		5.5	V	
Operating Current	$I_{DDR}$		0.5	1	mA	All ops except NVMEM program
Operating Current	$I_{DDW}$		1	2	mA	During Non-volatile memory program
Standby Current	$I_{SA}$ <sup>[3]</sup>		0.5	1	mA	Buffer is active, NOP, no load
	$I_{SB}$ <sup>[4]</sup>		0.1	1	$\mu A$	Buffer is inactive, Power Down, No load
Power Supply Rejection Ratio	PSRR			1	LSB/V	$V_{DD}=5V \pm 10\%, Code=80H$

Notes:

[1] Not subject to production test.

[2]  $LSB = (V_A - V_B) / (T - 1)$ ;  $DNL = (V_{i+1} - V_i) / LSB$ ;  $INL = (V_i - i*LSB) / LSB$ ;  
where  $i = [0, (T - 1)]$  and  $T = \#$  of taps of the device.

[3] WMS71x1 only.

[4] WMS71x0 only.

## 10.1 TEST CIRCUITS

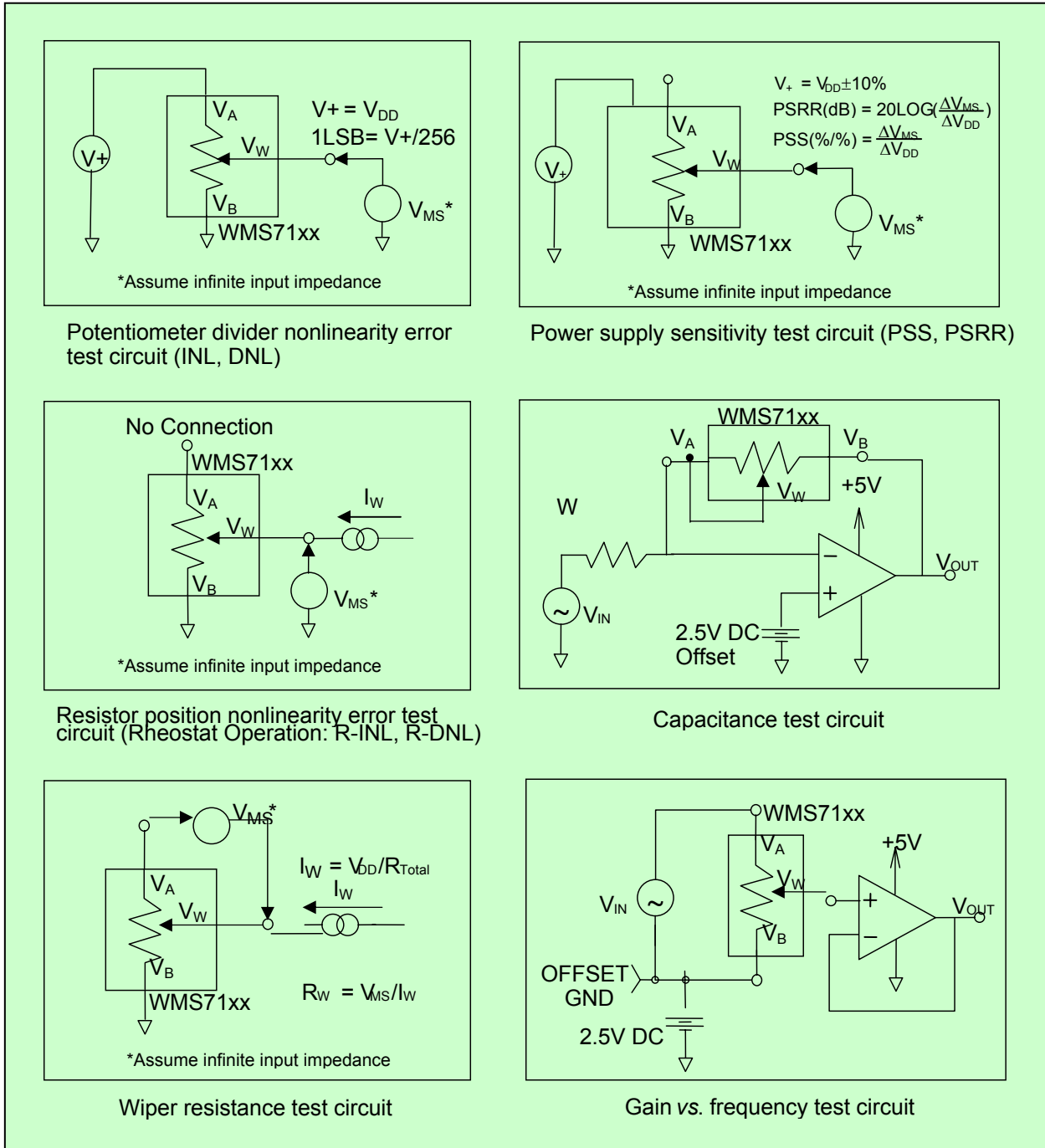


FIGURE 4 – TEST CIRCUITS

11. TYPICAL APPLICATION CIRCUITS

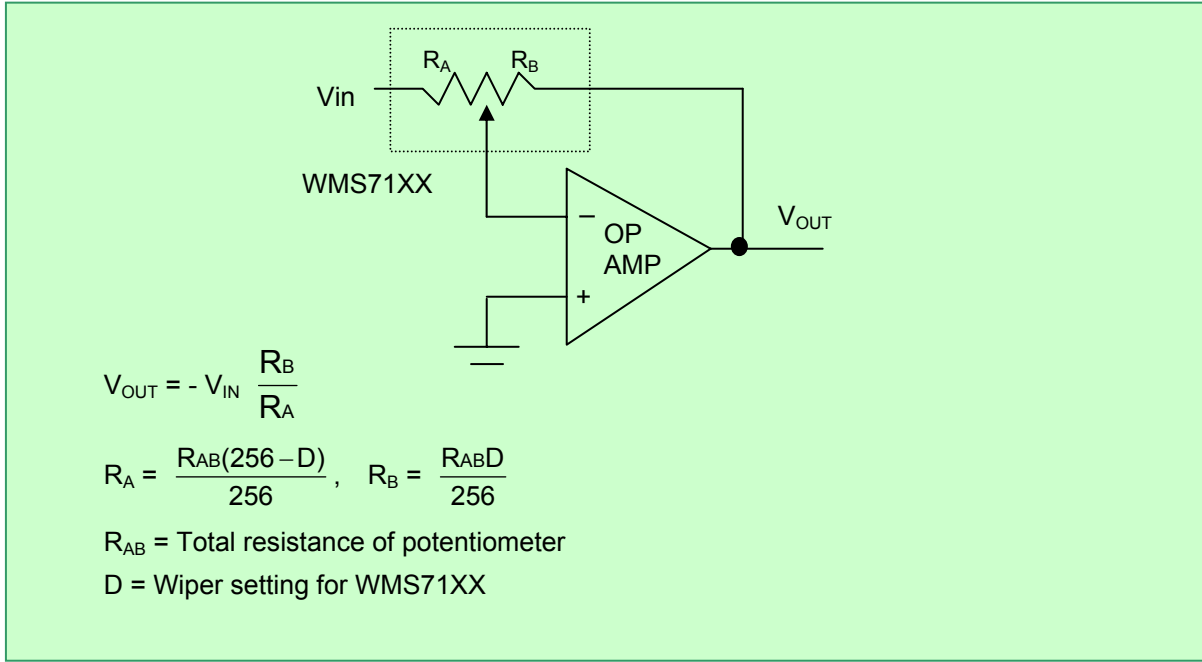


FIGURE 5 – PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE WMS7140/1

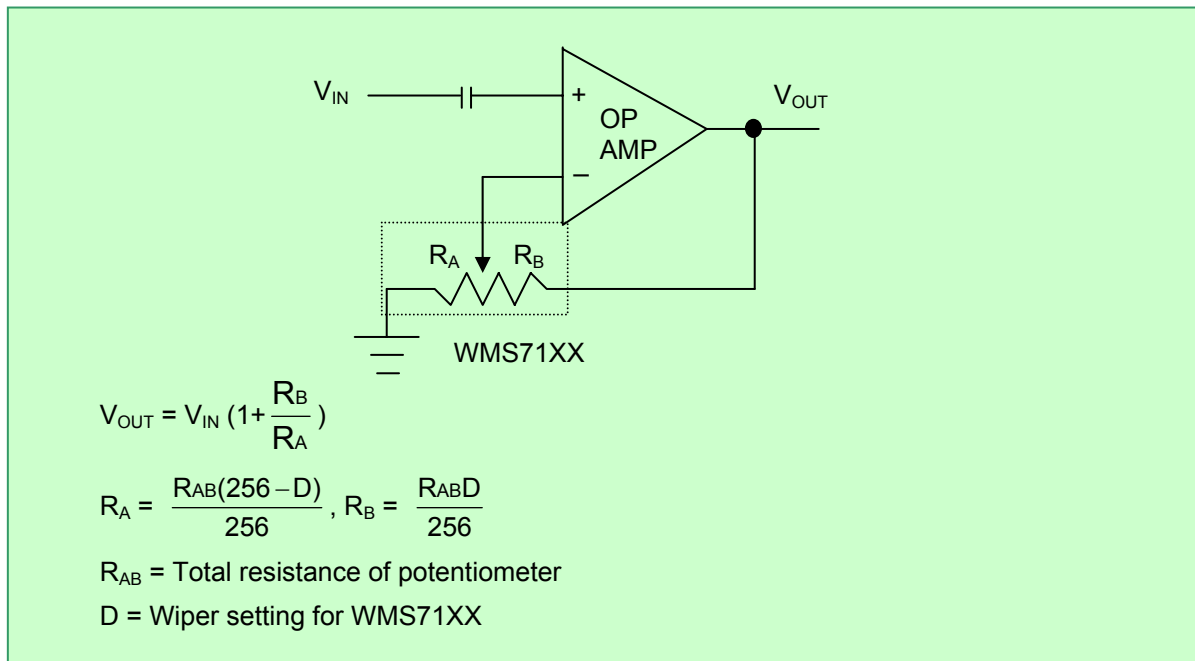
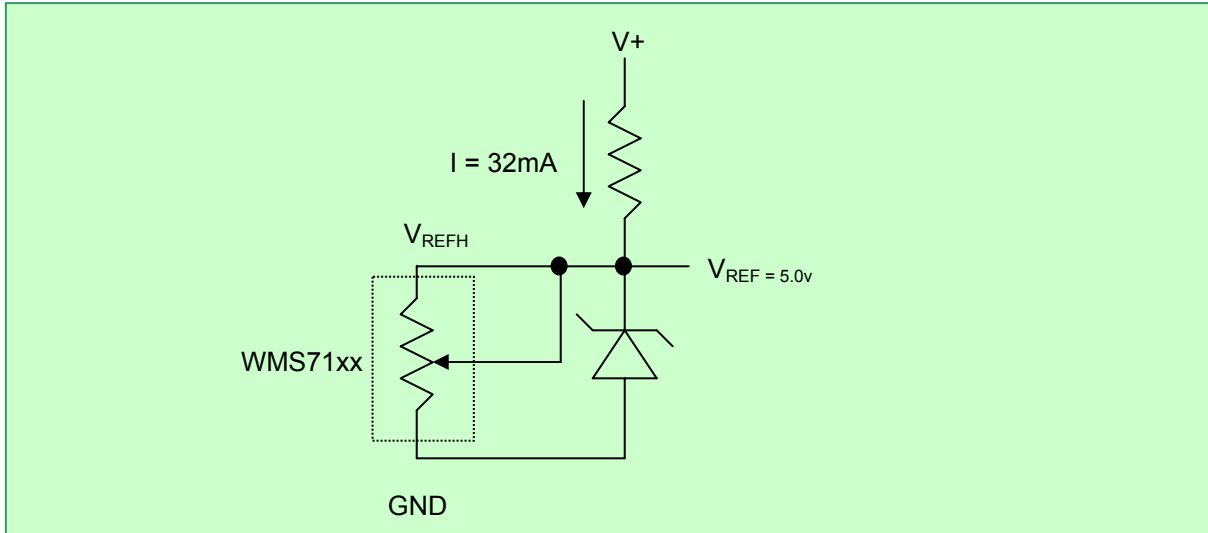
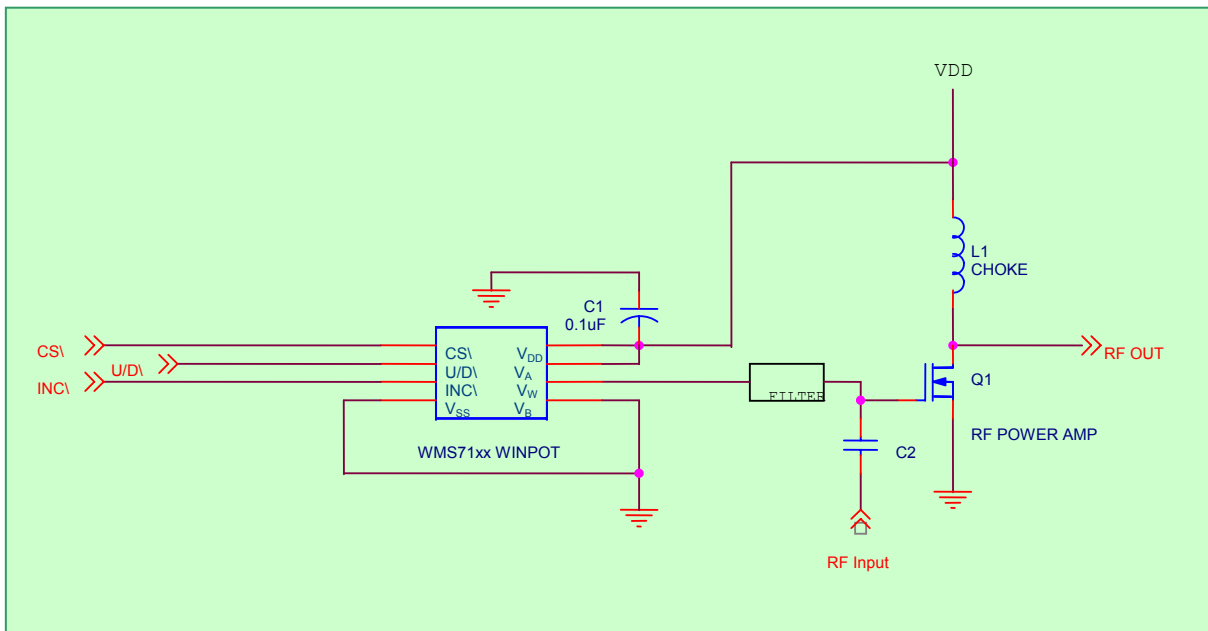


FIGURE 6 – PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE WMS7140/1



**FIGURE 7 – WMS7140/1 TRIMMING VOLTAGE REFERENCE**



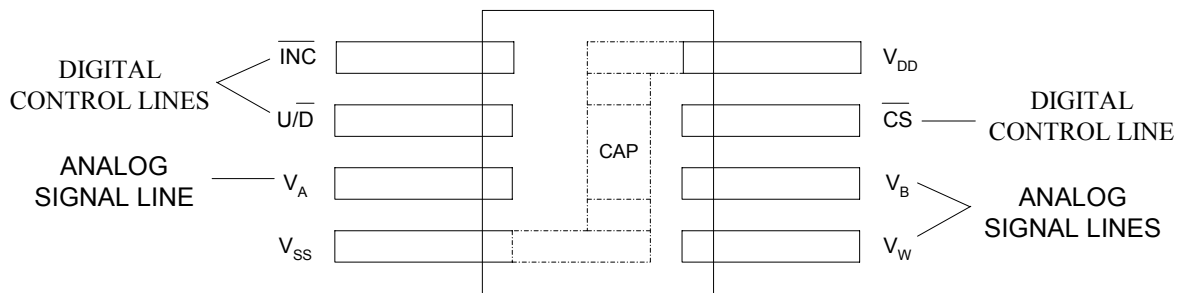
**FIGURE 8 – WMS7140/1 RF AMP CONTROL**



## 11.1. LAYOUT CONSIDERATIONS

Use a 0.1 $\mu$ F bypass capacitor as close as possible to the  $V_{DD}$  pin. This is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the  $V_{DD}$  and  $V_{SS}$  pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.



**FIGURE 9 – WMS7140/1 LAYOUT**

12. PACKAGE DRAWINGS AND DIMENSIONS

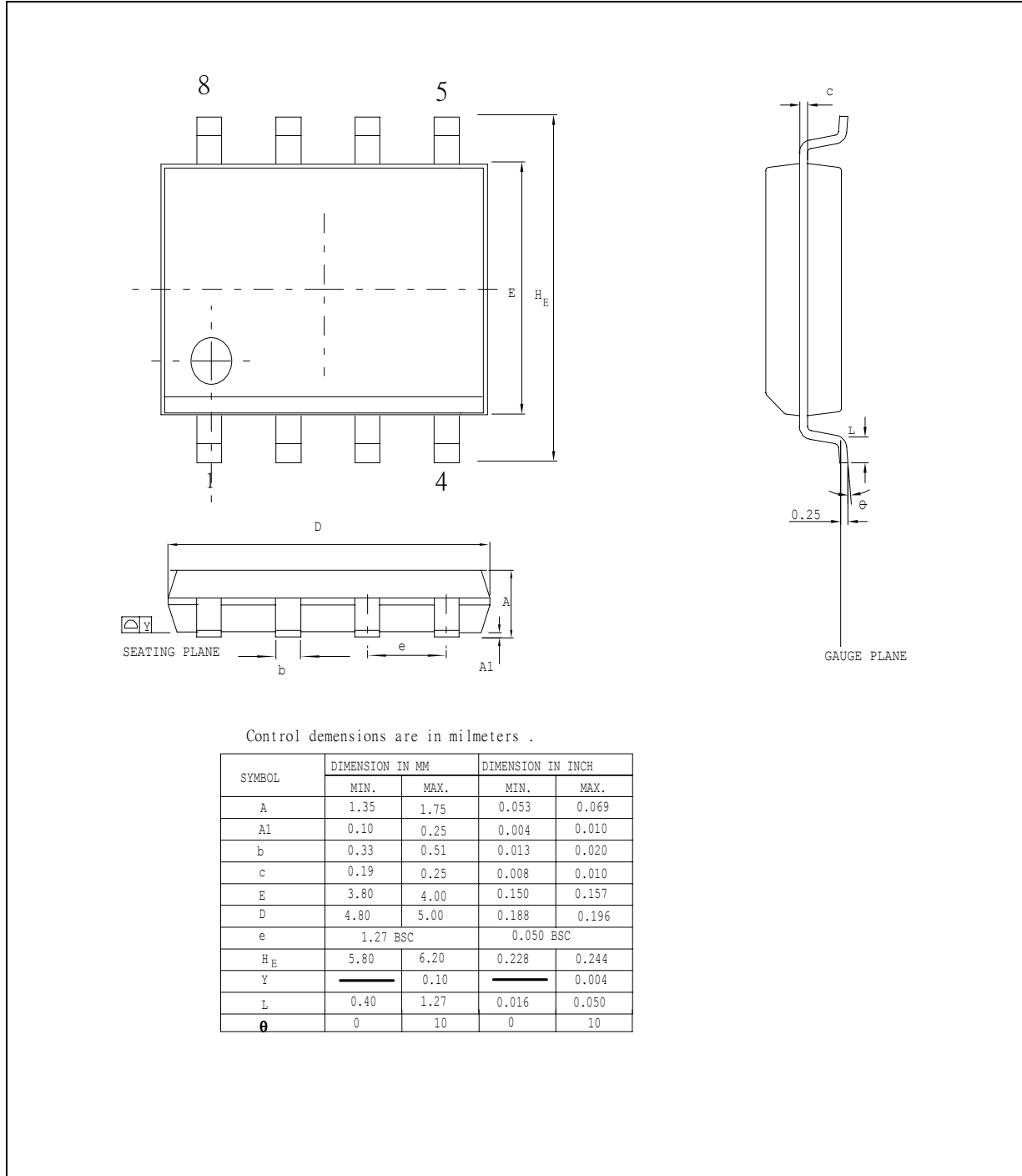


FIGURE 10: 8L 150MIL SOIC

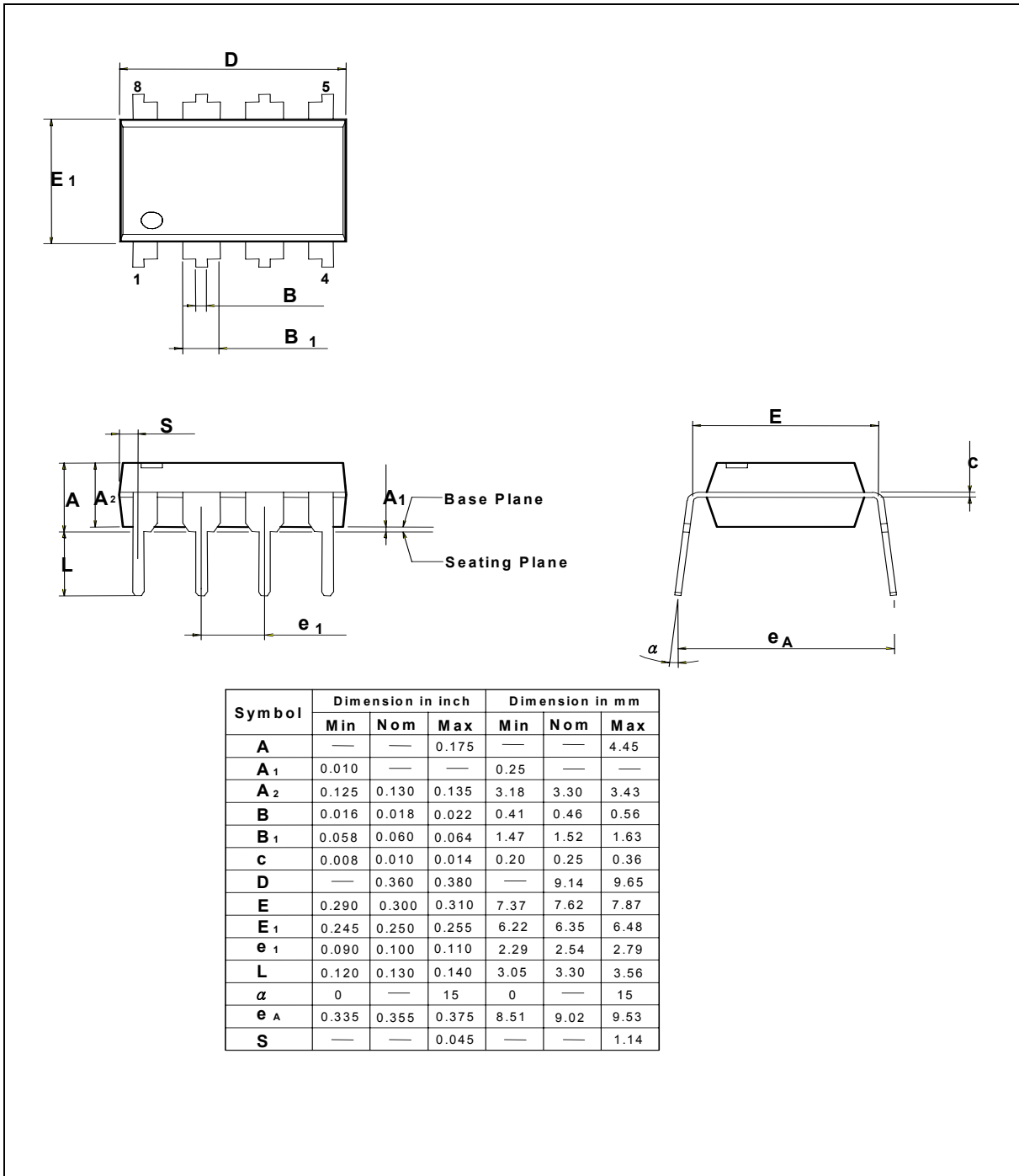


FIGURE 11: 8L 300MIL PDIP

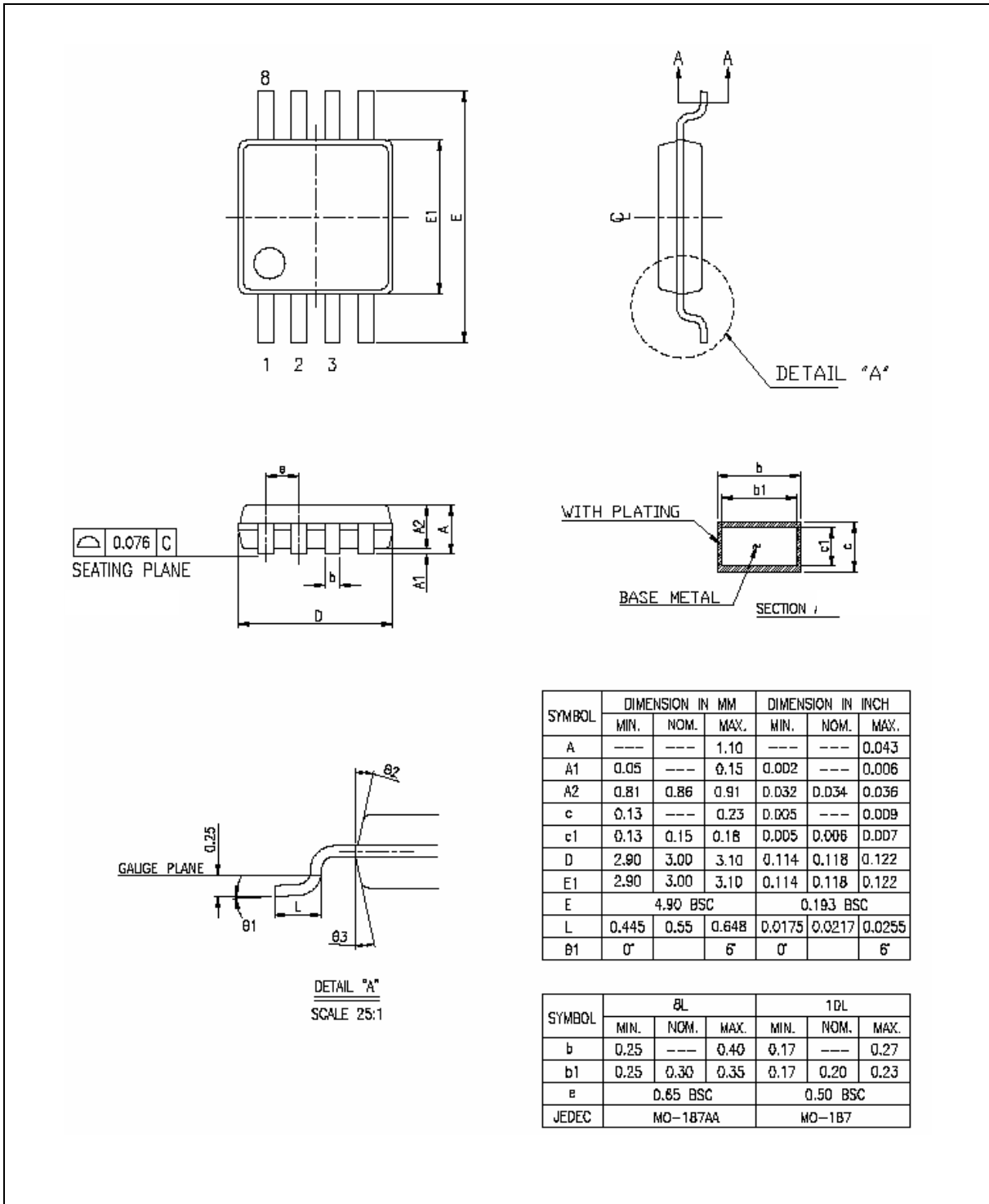
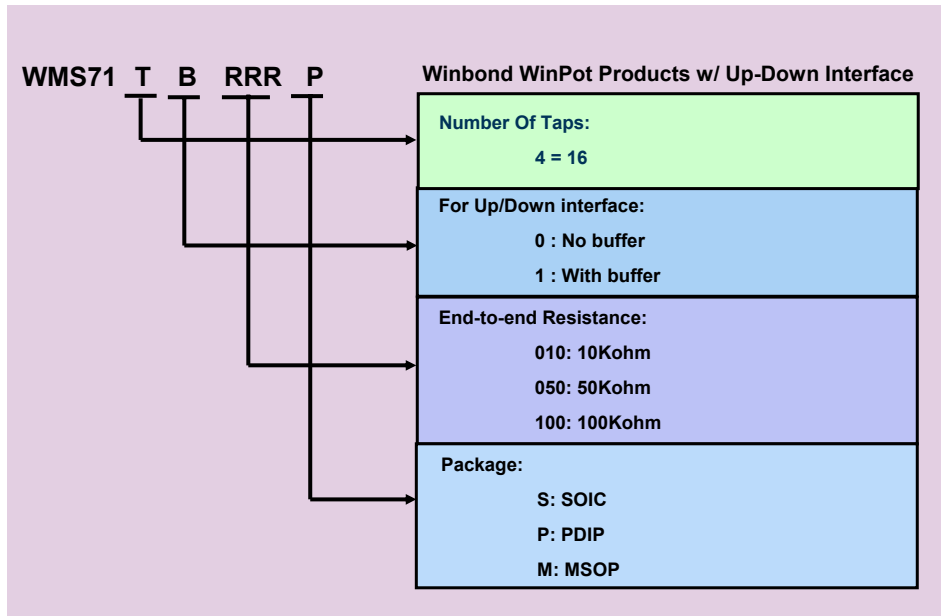


FIGURE 12: 8L 3MM MSOP



## 13. ORDERING INFORMATION

Winbond's WinPot Part Number Description:



Output Buffer	End-to-End Resistance	SOIC	PDIP	MSOP
NO	10K	WMS7140010S	WMS7140010P	WMS7140010M
	50K	WMS7140050S	WMS7140050P	WMS7140050M
	100K	WMS7140100S	WMS7140100P	WMS7140100M
YES	10K	WMS7141010S	WMS7141010P	WMS7141010M
	50K	WMS7141050S	WMS7141050P	WMS7141050M
	100K	WMS7141100S	WMS7141100P	WMS7141100M

Notes:

Part number with white background: Available for sampling and mass production.

Part numbers with shaded background: Call factory for availability.

For the latest product information, access Winbond's worldwide website at <http://www.winbond-usa.com>



**14. VERSION HISTORY**

VERSION	DATE	DESCRIPTION
1.0	June 2003	Initial issue
1.1	April 2005	Revise disclaim section



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#### Headquarters

No. 4, Creation Rd. III  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5665577  
<http://www.winbond.com.tw/>

#### Winbond Electronics Corporation America

2727 North First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 1-408-9436666  
FAX: 1-408-5441797  
<http://www.winbond-usa.com/>

#### Winbond Electronics (Shanghai) Ltd.

27F, 299 Yan An W. Rd. Shanghai,  
200336 China  
TEL: 86-21-62365999  
FAX: 86-21-62356998

#### Taipei Office

9F, No. 480, Pueiguang Rd.  
Neihu District  
Taipei, 114 Taiwan  
TEL: 886-2-81777168  
FAX: 886-2-87153579

#### Winbond Electronics Corporation Japan

7F Daini-ueno BLDG. 3-7-18  
Shinyokohama Kohokoku,  
Yokohama, 222-0033  
TEL: 81-45-4781881  
FAX: 81-45-4781800

#### Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,  
No. 378 Kwun Tong Rd.,  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

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