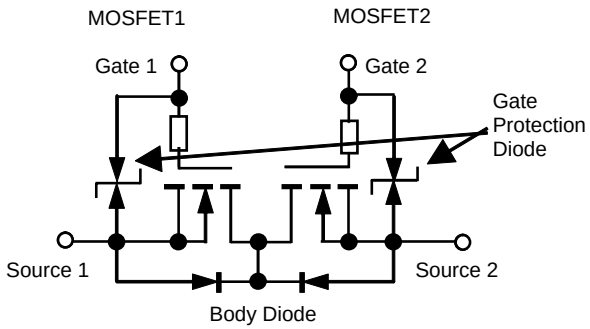
WNMD2171

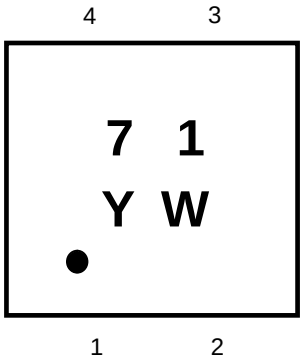
Dual N-Channel, 20V, 6A, Power MOSFET

www.sh-willsemi.com

V_{sss} (V)	Typ $R_{ss(on)}$ (mΩ)
20	36@ V_{GS}=4.5V
	38@ V_{GS}=4.0V
	41@ V_{GS}=3.1V
	43@ V_{GS}=2.5V
ESD Rating:2000V HBM	



CSP 4L



1: Source 1 71 = Device Code

2: Gate 1 Y = Year

3: Gate 2 W = Week（A~z）

4: Source 2

Pin configuration (TOP view) & Marking

Descriptions

The WNMD2171 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent $R_{SS(ON)}$ with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2171 is available in CSP-4L package. Standard Product WNMD2171 is Pb-free and Halogen-free.

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Small package CSP 4L

Applications

- Lithium-Ion battery protection circuit

Order information

Device	Package	Shipping
WNMD2171-4/TR	CSP 4L	3000/Reel&Tape

Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V_{SSS}	V_{GS} = 0 V, I_S = 250uA	20			V
Zero Gate Voltage Drain Current	I_{SSS}	V_{SS} =16 V, V_{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±12V TEST CIRCUIT 2			±10	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{GS} = V_{SS}, I_S = 250uA TEST CIRCUIT 3	0.4	0.74	1.0	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 3.0A TEST CIRCUIT 5	17	36	45	mΩ
		V_{GS} = 4.0V, I_S = 3.0A TEST CIRCUIT 5	18	38	47	
		V_{GS} = 3.1V, I_S = 3.0A TEST CIRCUIT 5	19	41	54	
		V_{GS} = 2.5V, I_S = 3.0A TEST CIRCUIT 5	21	43	65	
Forward Transfer Admittance	| yfs |	V_{SS} = 10 V, I_S = 1.8A TEST CIRCUIT 4		11		S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1kHz, V_{SS} = 10 V TEST CIRCUIT 7		1210		pF
Output Capacitance	C_{OSS}			149		
Reverse Transfer Capacitance	C_{RSS}			135		
Total Gate Charge	$Q_{G(TOT)}$	V_{G1S1} = 4.5 V, V_{SS} = 10V, I_S =6A TEST CIRCUIT 9		15.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.15		
Gate-to-Source Charge	Q_{GS}			2.8		
Gate-to-Drain Charge	Q_{GD}			3.8		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 4.5 V, V_{SS} =10V, I_S=5.0A, R_G=6Ω TEST CIRCUIT 8		410		ns
Rise Time	tr			1200		
Turn-Off Delay Time	td(OFF)			6100		
Fall Time	tf			3500		
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	$V_{F(S-S)}$	V_{GS} = 0 V, I_F = 1.0A TEST CIRCUIT 6			1.5	V

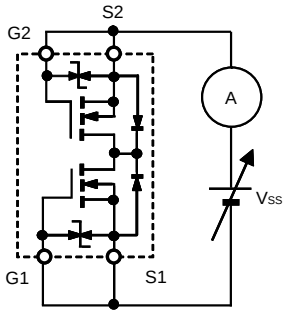
Absolute Maximum ratings

Parameter	Symbol	10 s	Steady State	Unit
Source to Source Voltage (V_{GS} = 0 V)	V_{SSS}	20		V
Gate to Source Voltage (V_{SS} = 0 V)	V_{GSS}	±12		
Source Current (pulse)[Note.c]	$I_{S(pulse)}$	60		A
Source Current (DC)	I_S	6		A
Channel Temperature	T_{ch}	150		°C
Storage Temperature Range	T_{stg}	-55 to 150		°C

Note.c PW≤10μs, duty cycle≤1%;

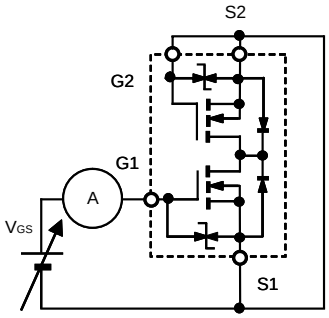
Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

TEST CIRCUIT 1 I_{SSS}



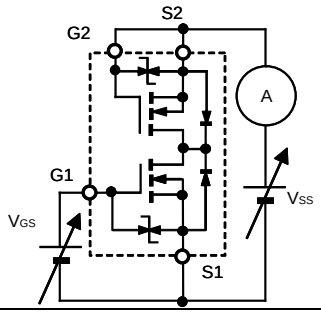
TEST CIRCUIT 2 I_{GSS}

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



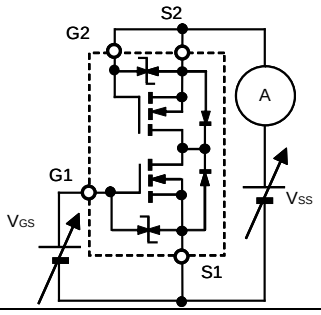
TEST CIRCUIT 3 $V_{GS(off)}$

When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



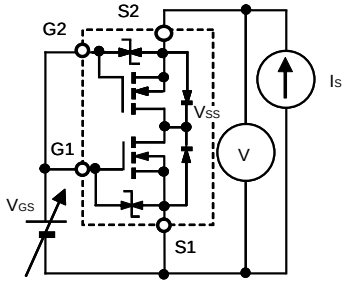
TEST CIRCUIT 4 $|y_{fs}|$

ΔIs/ΔVGS



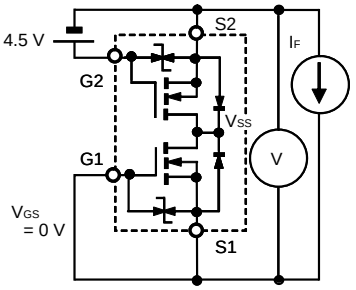
TEST CIRCUIT 5 $R_{SS(on)}$

V_{SS}/I_S

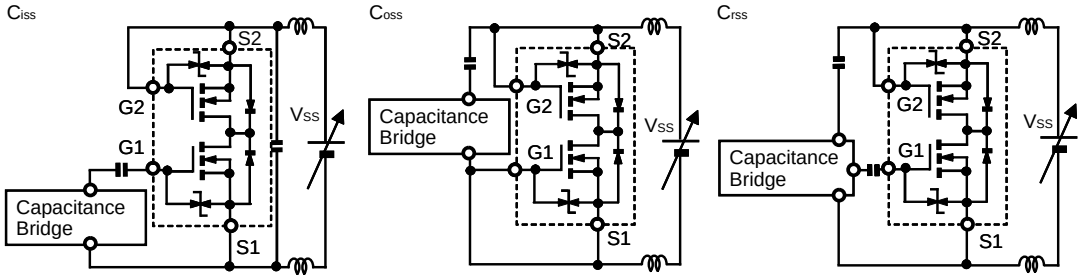


TEST CIRCUIT 6 $V_{F(S-S)}$

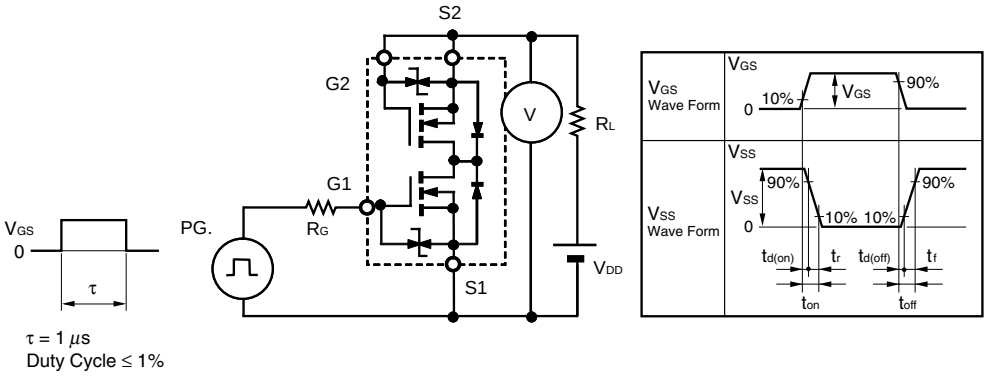
When FET1 is measured, FET2 is added V_{GS} +4.5 V.



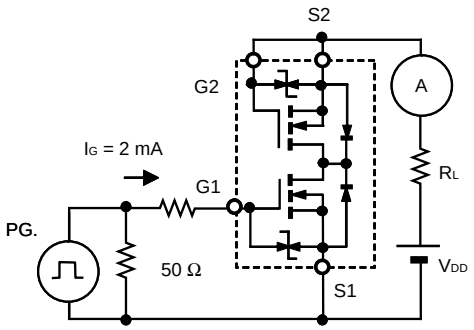
TEST CIRCUIT 7



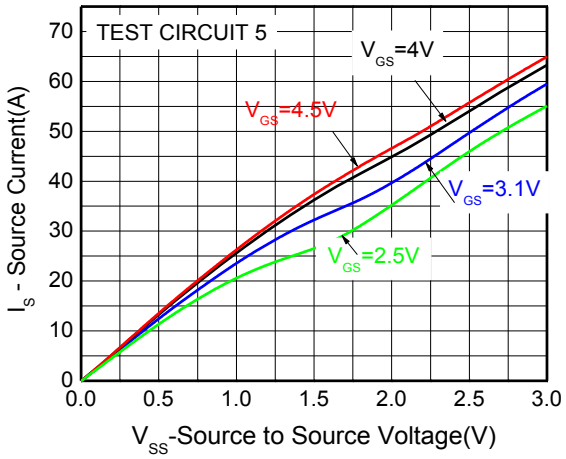
TEST CIRCUIT 8 $t_{d(on)}$, t_r, $t_{d(off)}$, t_f



TEST CIRCUIT 9 Q_G

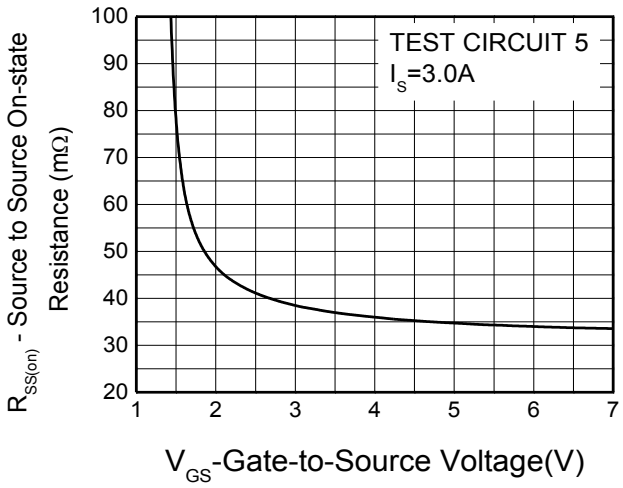


Typical Characteristics (Ta=25°C, unless otherwise noted)



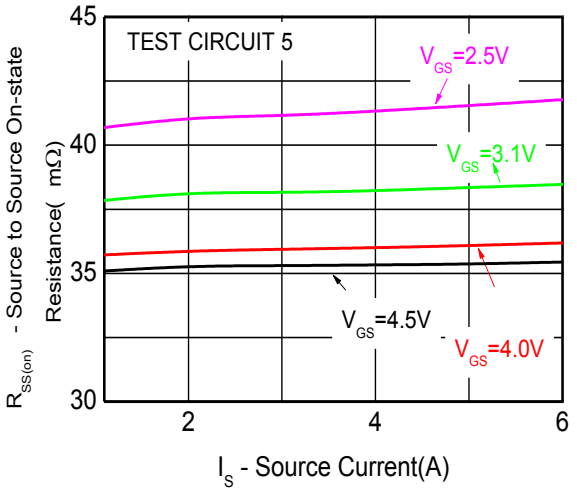
SOURCE CURRENT vs.

SOURCE TO SOURCE VOLTAGE



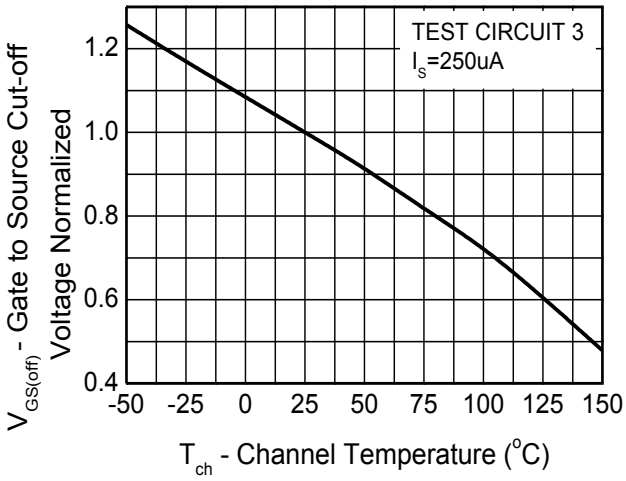
SOURCE TO SOURCE ON-STATE RESISTANCE vs.

GATE TO SOURCE VOLTAGE



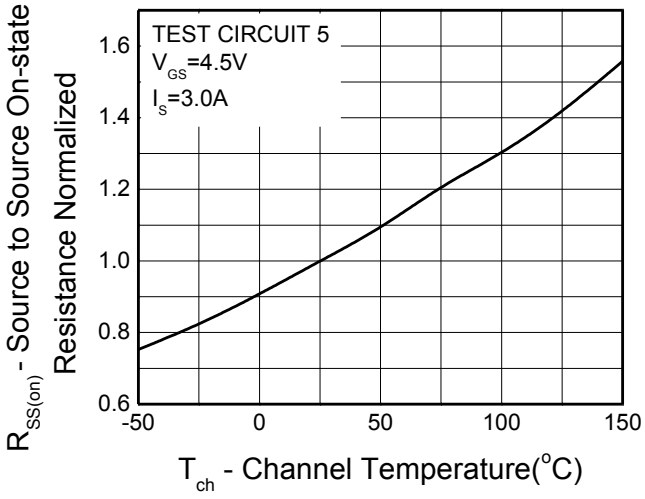
SOURCE TO SOURCE ON-STATE RESISTANCE vs.

SOURCE CURRENT



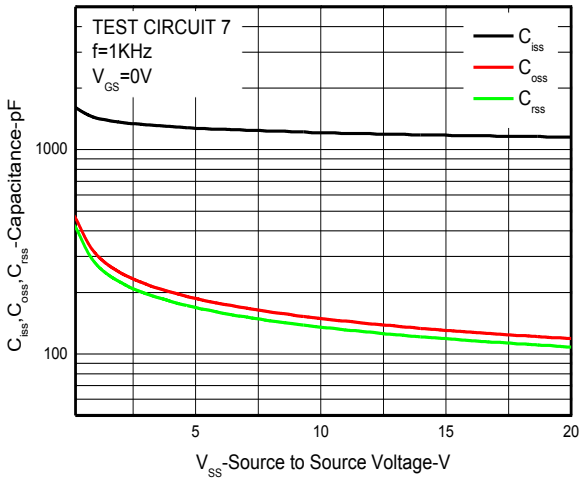
GATE TO SOURCE CUT-OFF VOLTAGE vs.

CHANNEL TEMPERATURE

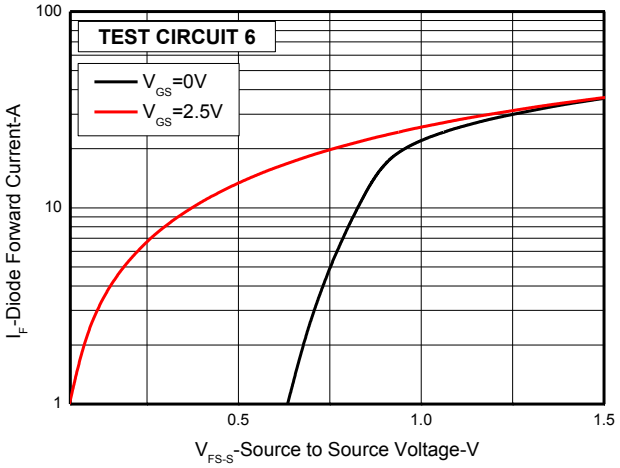


SOURCE TO SOURCE ON-STATE RESISTANCE vs.

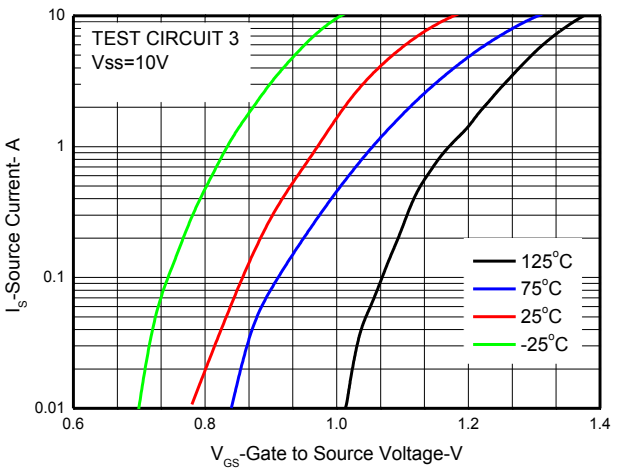
CHANNEL TEMPERATURE



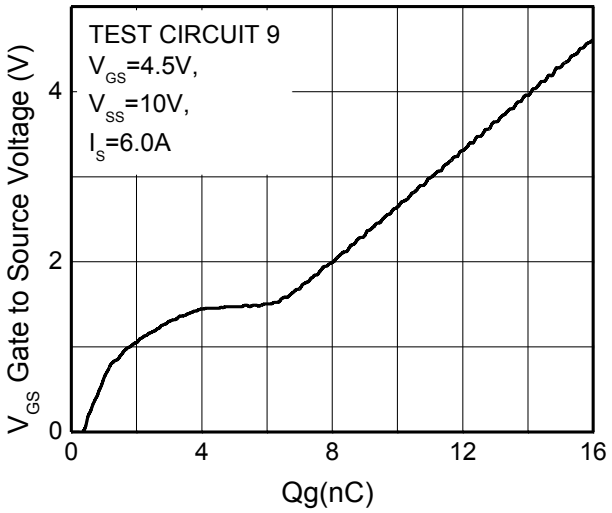
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



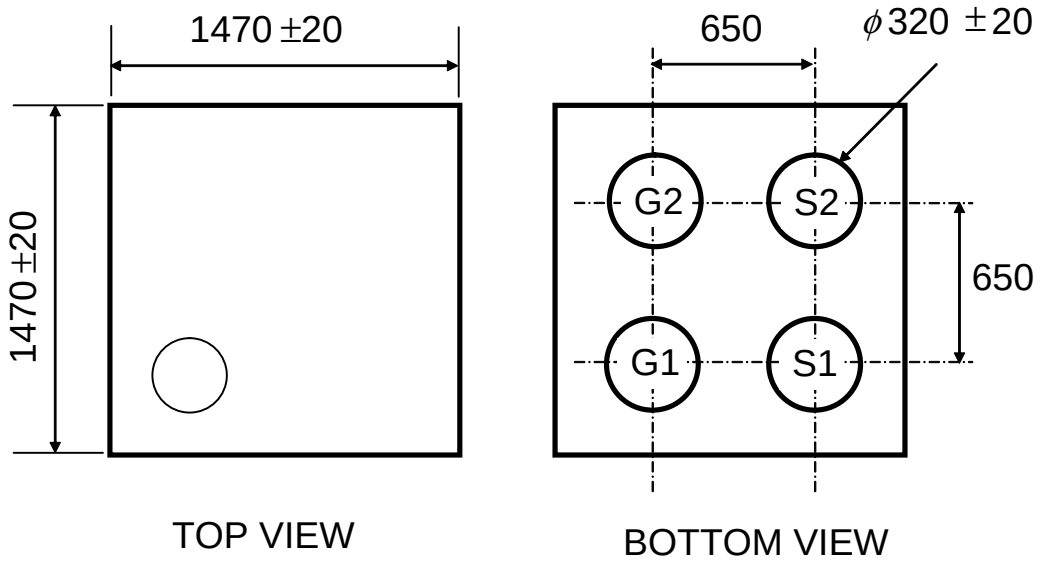
FORWARD TRANSFER CHARACTERISTICS

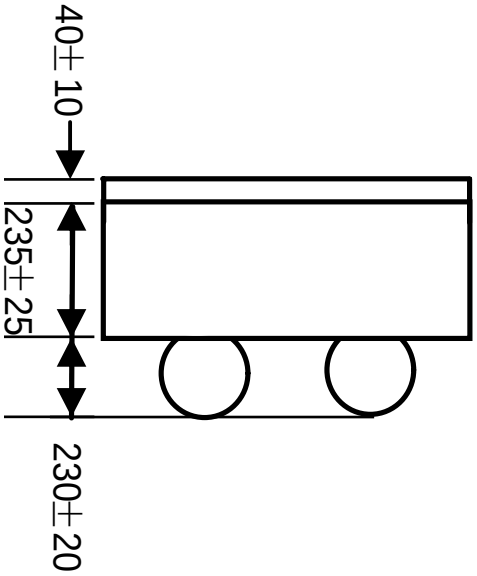


DYNAMIC INPUT CHARACTERISTICS

Package outline dimensions (Unit:um)

CSP 4L





MOSFET 1

S1: Source 1
G1: Gate 1

MOSFET 2

G2: Gate 2
S2: Source 2