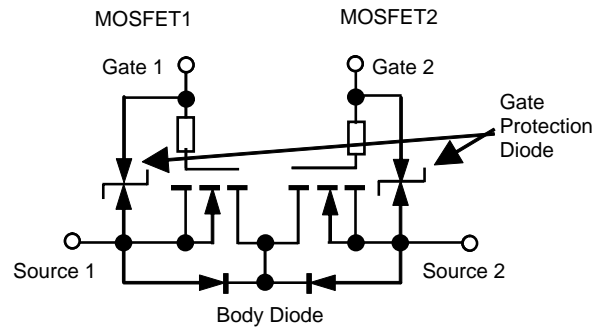
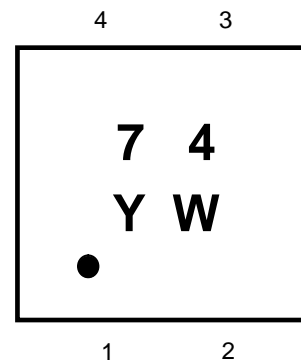


**WNMD2174**
**Dual N-Channel, 12V, 6A, Power MOSFET**
[www.sh-willsemi.com](http://www.sh-willsemi.com)

V <sub>SSS</sub> (V)	Typ R <sub>SS(on)</sub> (mΩ)
12	19@ V <sub>GS</sub> =4.5V
	20@ V <sub>GS</sub> =4.0V
	22@ V <sub>GS</sub> =3.1V
	25@ V <sub>GS</sub> =2.5V
ESD Rating:2000V HBM	


**Descriptions**

The WNMD2174 is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent R<sub>SS(ON)</sub> with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2174 is available in CSP 4L package. Standard Product WNMD2174 is Pb-free and Halogen-free.

**CSP 4L**

**Features**

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Small package CSP 4L

- 1: Source 1      74 = Device Code
- 2: Gate 1        Y = Year
- 3: Gate 2        W = Week (A~z)
- 4: Source 2

**Pin configuration (TOP view)&Marking**
**Order information**

Device	Package	Shipping
WNMD2174-4/TR	CSP 4L	3000/Reel&Tape

**Applications**

- Lithium-Ion battery protection circuit

**Electronics Characteristics (Ta=25°C, unless otherwise noted)**

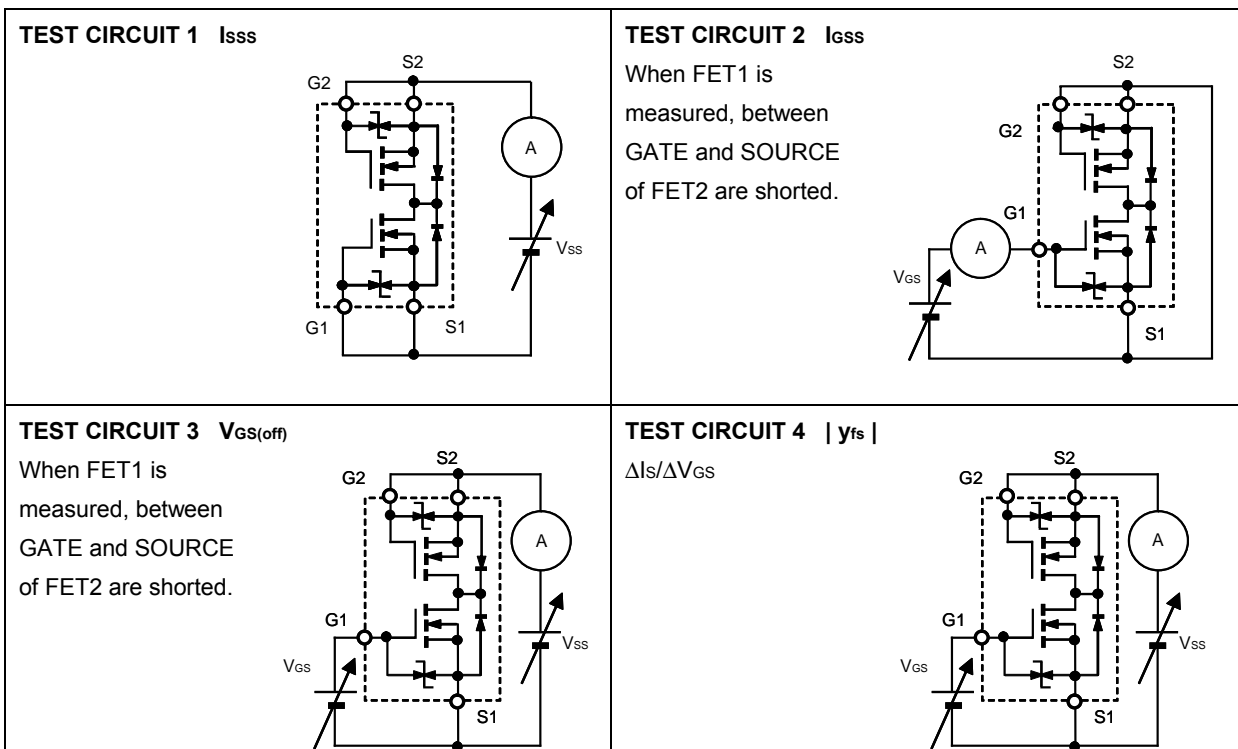
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Source to Source Voltage	V <sub>SSS</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 250uA	12			V
Zero Gate Voltage Drain Current	I <sub>SSS</sub>	V <sub>SS</sub> = 10 V, V <sub>GS</sub> = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>SS</sub> = 0 V, V <sub>GS</sub> = ±10V TEST CIRCUIT 2			±10	uA
<b>ON CHARACTERISTICS</b>						
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>GS</sub> = V <sub>SS</sub> , I <sub>S</sub> = 250uA TEST CIRCUIT 3	0.4	0.8	1.2	V
Source to Source On-state Resistance	R <sub>SS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>S</sub> = 3.0A TEST CIRCUIT 5	10	19	25	mΩ
		V <sub>GS</sub> = 4.0V, I <sub>S</sub> = 3.0A TEST CIRCUIT 5	11	20	27	
		V <sub>GS</sub> = 3.1V, I <sub>S</sub> = 3.0A TEST CIRCUIT 5	12	22	31	
		V <sub>GS</sub> = 2.5V, I <sub>S</sub> = 3.0A TEST CIRCUIT 5	14	25	35	
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>SS</sub> = 10 V, I <sub>S</sub> = 1.8A TEST CIRCUIT 4		9		S
<b>BODY DIODE CHARACTERISTICS</b>						
Body Diode Forward Voltage	V <sub>F(S-S)</sub>	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 1.0A TEST CIRCUIT 6		0.9	1.5	V
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Delay Time	td(ON)	V <sub>GS</sub> = 4.5 V, V <sub>SS</sub> = 10V, R <sub>L</sub> = 3.3 Ω, I <sub>S</sub> = 3A, R <sub>G</sub> = 6Ω TEST CIRCUIT 8		680		ns
Rise Time	tr			2960		
Turn-Off Delay Time	td(OFF)			6480		
Fall Time	tf			6760		
<b>CHARGES, CAPACITANCES AND GATE RESISTANCE</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 kHz, V <sub>SS</sub> = 10 V TEST CIRCUIT 7		1313		pF
Output Capacitance	C <sub>OSS</sub>			257		
Reverse Transfer Capacitance	C <sub>RSS</sub>			238		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>G1S1</sub> = 4.5 V, V <sub>SS</sub> = 10V, I <sub>S</sub> = 6A TEST CIRCUIT 9		17.8		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.79		
Gate-to-Source Charge	Q <sub>GS</sub>			2.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			6.4		

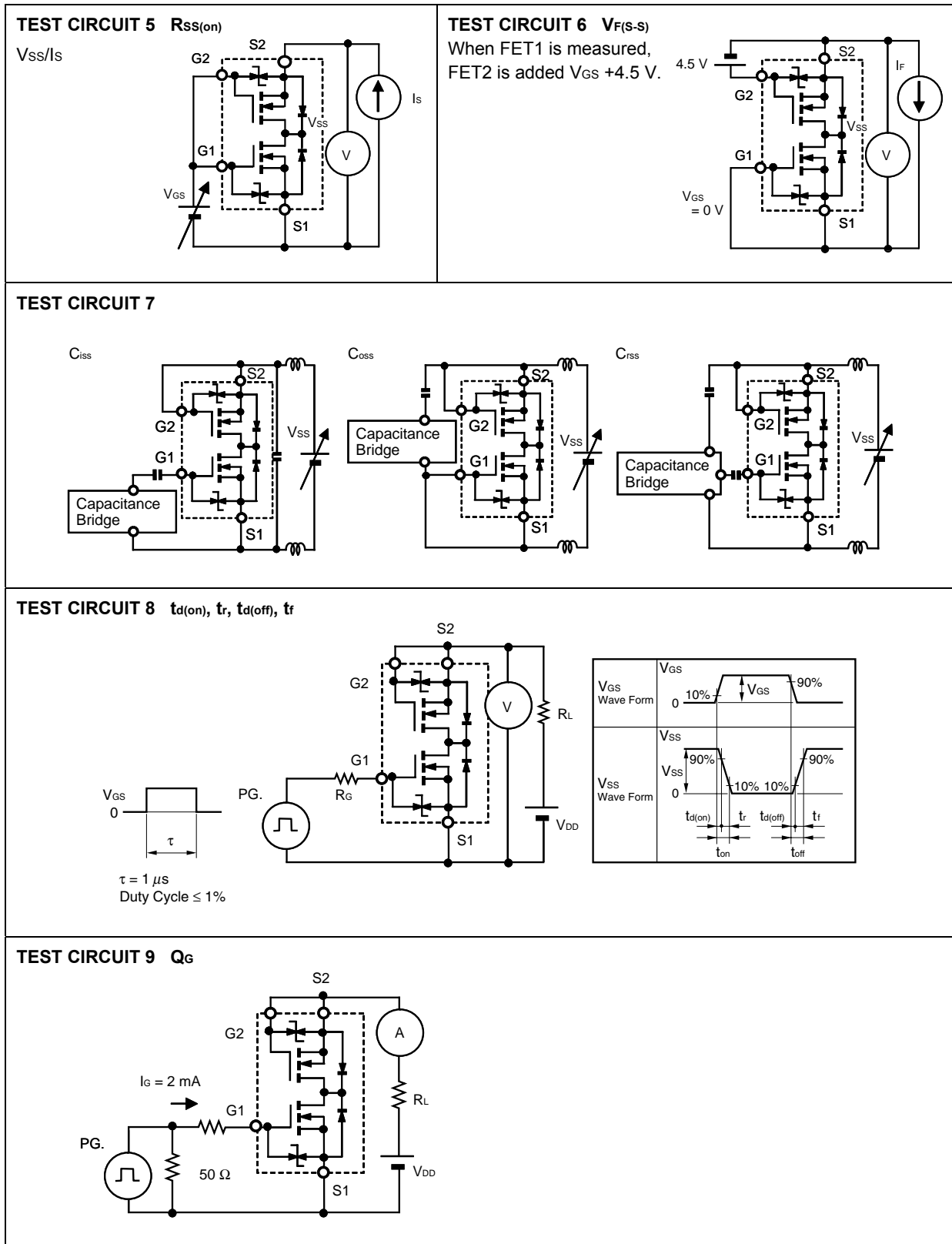
### Absolute Maximum ratings

Parameter	Symbol	10 s	Steady State	Unit
Source to Source Voltage ( $V_{GS} = 0\text{ V}$ )	$V_{SSS}$	12	V	V
Gate to Source Voltage ( $V_{SS} = 0\text{ V}$ )	$V_{GSS}$	$\pm 10$		
Source Current (pulse) <sup>Note.c</sup>	$I_{S(\text{pulse})}$	60	A	A
Source Current (DC)	$I_S$	6	A	A
Channel Temperature	$T_{ch}$	150	$^{\circ}\text{C}$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to 150	$^{\circ}\text{C}$	$^{\circ}\text{C}$

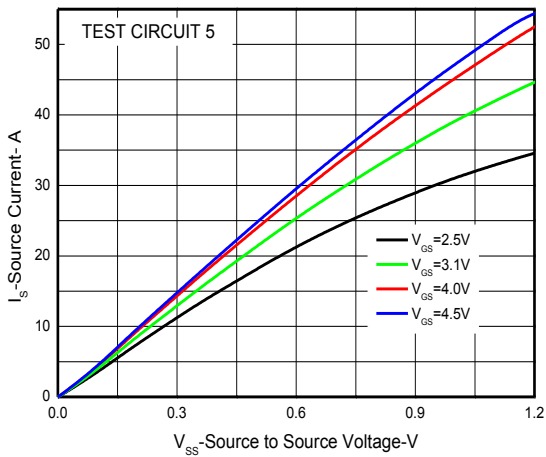
Note.c  $PW \leq 10\mu\text{s}$ , duty cycle  $\leq 1\%$ ;

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

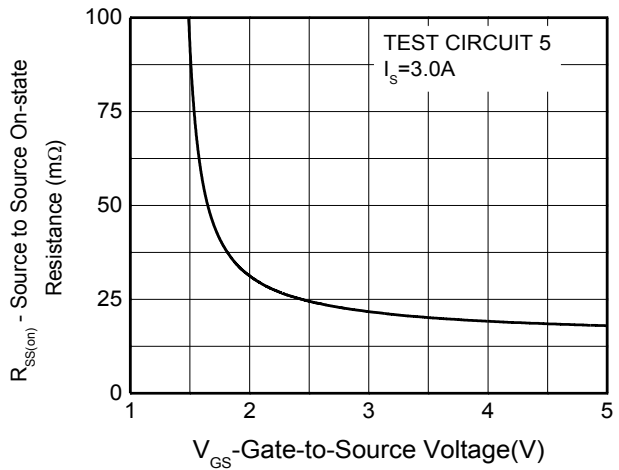




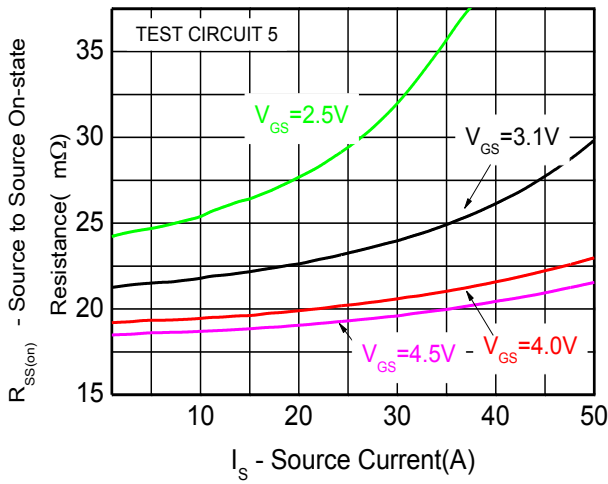
**Typical Characteristics (Ta=25°C, unless otherwise noted)**



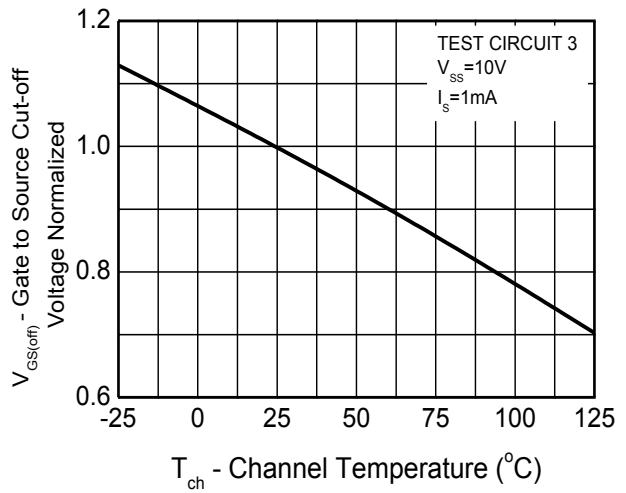
**SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE**



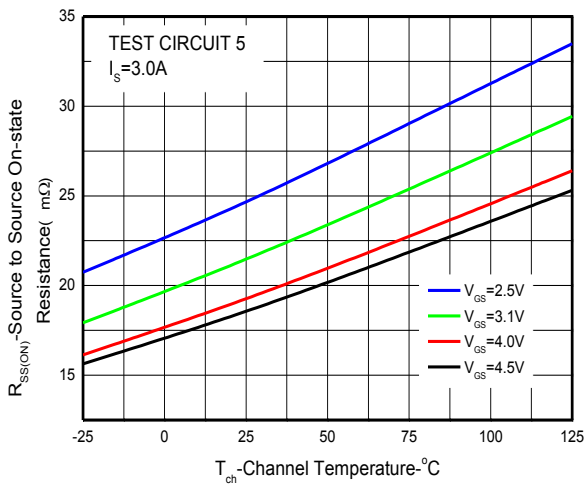
**SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE**



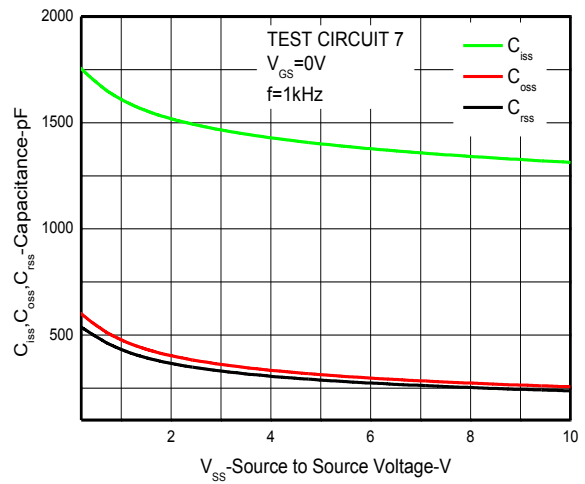
**SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT**



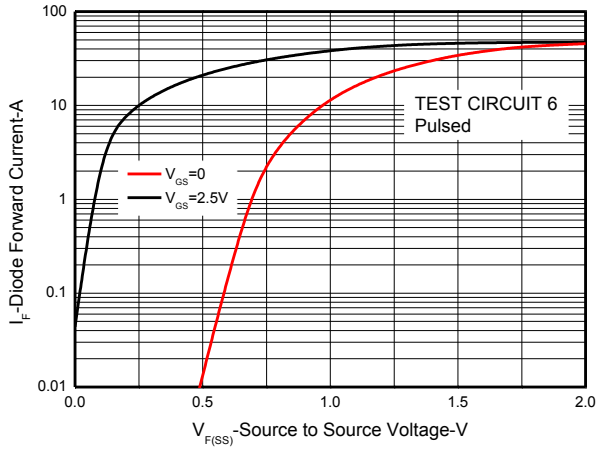
**GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE**



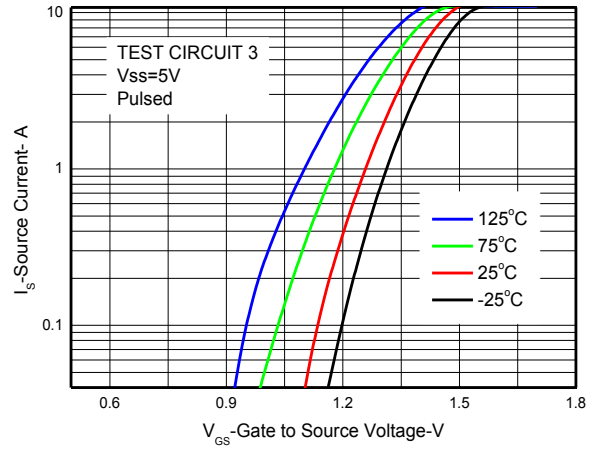
**SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE**



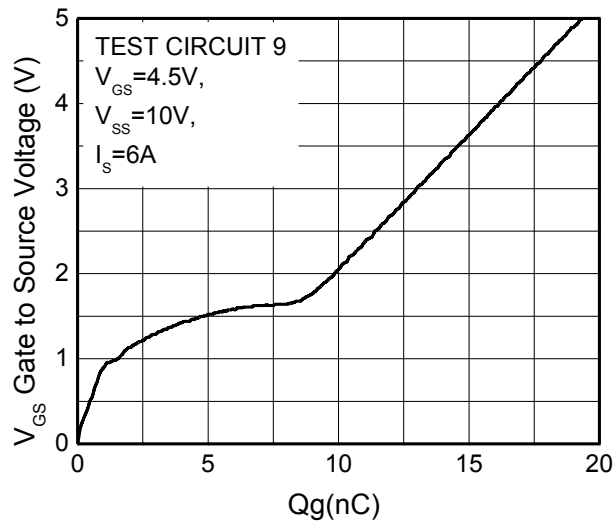
**CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE**



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS

**Package outline dimensions (Unit:um )**
**CSP 4L**
