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Over-Voltage Protection IC

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WP3881L

Description

WP3881L can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected.

The system is positive overvoltage protected up to 28V. The overvoltage thresholds (OVLO) is 5.95 V.

WP3881L internal Thermal-Shutdown Protection.

The device is packaged in advanced full-Green compliant Wafer Level Chip Scale Packaging (WLCSP12).

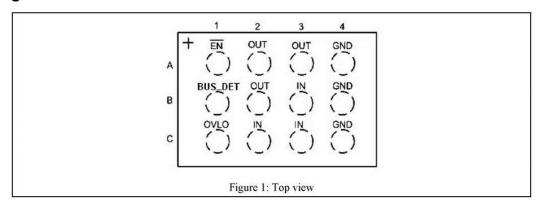
Features

- □ 4.8A Continuous Current Capability
- \square Typical R_{ON}: 35 m Ω N-Channel MOSFET
- □ V_{IN} Operating Range: 2.1V to 28V
- □ Overvoltage Lockout: OVLO=5.95V(TYP.)
- □ Overvoltage-Protection Response Time: 100ns(TYP.)
- □ OVLO Threshold Range: +4V to +20V
- ☐ Startup Debounce Time: 21ms(TYP.)
- □ Internal Thermal-Shutdown Protection
- □ Surge immunity to ± 100V
- ☐ ESD Protected: Human Body Model: JESD22-A114(All pins) ±2KV
- □ CSP12 Package (ball pitch=0.4mm)

Applications

- ☐ Smartphones, Tablet PC
- □ HDD, Storage and Solid State Memory Devices
- □ Portable Media Devices, Laptop & MID
- □ SLR Digital Cameras
- ☐ GPS and Navigation Equipment
- □ Industrial Handheld and Enterprise Equipment

Pin Configuration



SYMBOL	PARAMETERS MIN		MAX	UNIT
V _{IN}	VIN to GND	-0.3	29	V
Vouт	VOUT to GND	-0.3	V _{IN} +0.3	V
Vovlo	OVLO to GND	-0.3	14	V
$V_{\overline{\mathrm{EN}}}$	EN to GND	-0.3	7	V
I _{SW1}	Maximum Continuous Current of switch IN-OUT		4.8	А
I _{SW2}	Maximum Peak Current of switch IN-OUT(10ms)		8	А
P _D	Power Dissipation at T _A = +70 [○] C		1090	mW
T _{STG}	Storage Junction Temperature	-65	+150	°С
T _A	Operating Temperature Range	-40	+85	°C
T∟	Lead Soldering Temperature (reflow).		+260	°C
TJ	Junction Temperature		+150	°C
Surge	VIN to GND, IEC 61000-4-5, Surge Protection	-100	100	V

Pin Function

Pin	Name	Pin Function
FIII	Name	FIII FUIICUOII
A1	EN	Microphone Mode Enable. Active low.
A2, A3, B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.
B1	VBUS_DET	Regulation output of VBUS
B3, C2, C3	IN	Voltage Input. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

Absolute Maximum Ratings

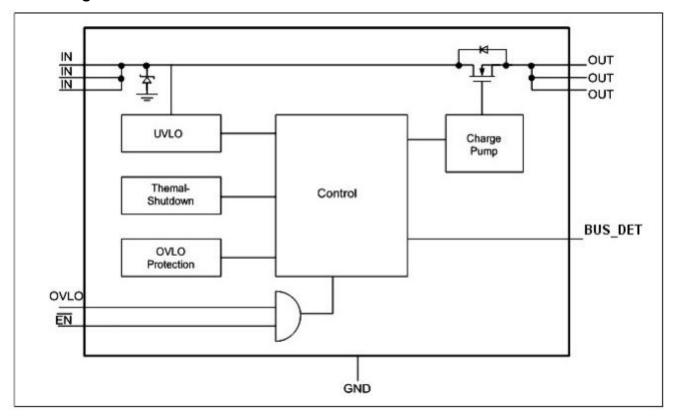
Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
Basic Operatio	n					
V _{IN}	Input Voltage		2.1		28	V
I _{IN}	V _{IN} Quiescent Current	V _{IN} =5V, OUT floating			220	μA
Ron	On-Resistance of Switch IN-OUT	V _{IN} =5.0V, I _{OUT} =1A		35	42	mΩ
V _{OVL} O	Overvoltage protect of V _{IN}	V_{IN} rise up	5.90	5.95	5.99	V
	Overvoltage protect hysteresis of V _{IN}			0.15		V
	Adjustable OVLO Threshold Range		4		20	V
V _{OVLO_TH}	OVLO Set Threshold		1.18	1.2	1.22	V
Vovlo_select	External OVLO Select Threshold		0.2		0.3	V
V _{DET}	regulation output of VBUS_DET	V_{IN} =12V, \overline{EN} =low	6		9.5	V
V _{IH}	EN Input Logic High Voltage		1.4			V
V _{IL}	EN Input Logic Low Voltage				0.3	V
	Thermal Shutdown			150		°C
	Thermal-shutdown Hysteresis			20		°C
Dynamic Chara	acteristics: see figure					
t _{DEB}	Debounce time	Time from 2.1V< V_{IN} < V_{OVLO} to V_{OUT} = 10% of V_{IN}		21		ms
t _{SS}	Soft-start time	Time from 2.1V< V_{IN} < V_{OVLO} to V_{OUT} = 90% of V_{IN}		22		ms
t _{OFF_RES}	Switch turn-off response time	V _{IN} > V _{OVLO} to V _{OUT} stop rising		100		ns

Electrical Characteristics

Unless otherwise noted, typical values are at $V_{\text{IN}}\text{=}5V$ and $T_{\text{A}}\text{=}25^{\circ}\text{C}.$

Block Diagram



Functional Description

The OVP switch with overvoltage protection feature a low 35 m Ω (TYP.) on-resistance(R_{ON}) internal FET and protect low-voltage systems against voltage faults up to $28V_{DC}$. If $\overline{\rm EN}$ is in the logic low state, when the input voltage(V_{IN}) exceeds 5.95V, the internal FET is quickly turned off to prevent damage to the protected downstream components. If $\overline{\rm EN}$ is in the logic high state,the WP3881L will feature the Microphone mode which disables the protect low-voltage system.

When input (OVLO) is set lower than 0.2V. The overvoltage protection threshold is 5.95V.

The overvoltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$$V_{IN_OVLO} = V_{OVLO_TH} * (1+R1/R2)$$
 $V_{OVLO_TH} = 1.2V(TYP.)$

The internal FET turns off when the junction temperature exceeds +150°C (TYP.). The device exits thermal shutdown after the junction temperature cools by 20°C (TYP.).

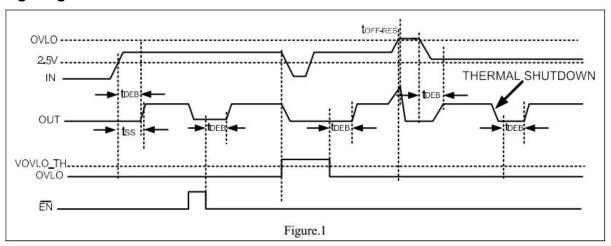
Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1µF or larger must be placed between the VIN and GND pins.

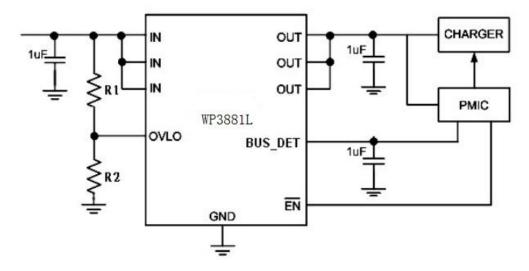
Output Capacitor

A 1µF or larger capacitor should be placed between the OUT and GND pins.

Timing Diagram



Application Circuits



Note: R1 and R2 are only required for adjustable OVLO; Otherwise OVLO is connected to GND.

*: This circuit only supplies for reference.

Package

