WP3882

Over-Voltage Protection IC

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Description

WP3882 can disconnect the systems from its output pin(OUT) in case wrong input operating conditions are detected. The system is positive overvoltage protected up to 28V. The overvoltage thresholds (OVLO) is 14 V.

WP3882 internal Thermal-Shutdown Protection.

The device is packaged in advanced full-Green compliant Wafer Level Chip Scale Packaging (WLCSP12).

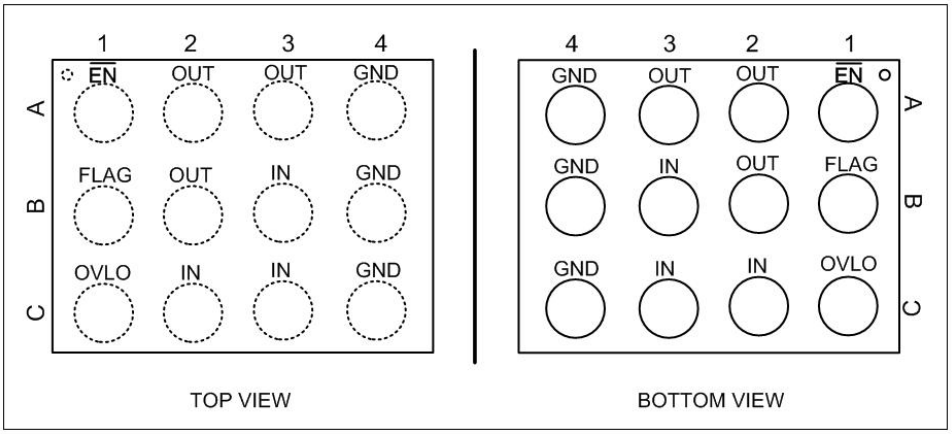
Features

- ☐ 4.8A Continuous Current Capability
- ☐ Typical R_{ON}: 30 mΩ N-Channel MOSFET
- ☐ V_{IN} Operating Range: 2.5V to 28V
- ☐ Overvoltage Lockout: OVLO=14V(TYP.)
- ☐ Overvoltage-Protection Response Time: 100ns(TYP.)
- ☐ Startup Debounce Time: 15ms(TYP.)
- ☐ Internal Thermal-Shutdown Protection
- ☐ Surge immunity to ± 100V
- ☐ ESD Protected: Human Body Model: JESD22-A114(All pins) ±2KV
- ☐ CSP12 Package (ball pitch=0.4mm)

Applications

- ☐ Smartphones, Tablet PC
- ☐ HDD, Storage and Solid State Memory Devices
- ☐ Portable Media Devices, Laptop & MID
- ☐ SLR Digital Cameras
- ☐ GPS and Navigation Equipment
- ☐ Industrial Handheld and Enterprise Equipment

Pin Configuration



SYMBOL	PARAMETERS	MIN	MAX	UNIT
V_{IN}	VIN to GND	-0.3	29	V
V_{OUT}	VOUT to GND	-0.3	V_{IN}+0.3	V
V_{OVLO}	OVLO to GND	-0.3	24	V
$V_{\overline{EN}}$	$\overline{EN}$ to GND	-0.3	7	V
V_{FLAG}	FLAG to GND	-0.3	7	V
I_{SW1}	Maximum Continuous Current of switch IN-OUT		4.8	A
I_{SW2}	Maximum Peak Current of switch IN-OUT(10ms)		6.5	A
P_D	Power Dissipation at T_A= +70 ^{O}C		1090	mW
T_{STG}	Storage Junction Temperature	-65	+150	^{O}C
T_A	Operating Temperature Range	-40	+85	^{O}C
T_L	Lead Soldering Temperature (reflow).		+260	^{O}C
T_J	Junction Temperature		+150	^{O}C
Surge	VIN to GND, IEC 61000-4-5, Surge Protection	-100	100	V

Pin Function

Pin	Name	Pin Function		
A1	$\overline{EN}$	Microphone Mode Enable. Active low.		
A2, A3, B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.		
A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.		
B1	FLAG	Power status indicator	1	V_{IN}<V_{UVLO} or V_{IN}>V_{OVLO}
			0	V_{IN} stable
B3, C2,C3	IN	Voltage Input. Connect IN pins together for proper operation.		
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
Basic Operation						
V_{IN}	Input Voltage		2.5		28	V
I_{IN}	V_{IN} Quiescent Current	V_{IN}=5V, OUT floating		90		μA
R_{ON}	On-Resistance of Switch IN-OUT	V_{IN} =5.0V, I_{OUT}=1A		35	42	mΩ
V_{OVLO}	Overvoltage protect of V_{IN}	V_{IN} rise up	13.6	14.0	14.4	V
	Overvoltage protect hysteresis of V_{IN}			0.25		V
	Adjustable OVLO Threshold Range		4		20	V
V_{OVLO_TH}	OVLO Set Threshold		1.2	1.22	1.24	V
V_{OVLO_SELECT}	External OVLO Select Threshold		0.3		0.4	V
V_{UVLO_R}	Under Voltage Lockout Threshold	V_{IN} Rising		2.0		V
V_{OL_FLAG}	FLAG Output Logic Low Voltage	V_{PU}=1.8V,I_{SINK}=1mA		0.1	0.2	V
I_{FLAG_LEAK}	FLAG Output Logic High Leakage Current	V_{FLAG}			0.5	μA
V_{IH}	$\overline{EN}$ Input Logic High Voltage		1.4			V
V_{IL}	$\overline{EN}$ Input Logic Low Voltage	V_{IN}=2.3V			0.3	V
	Thermal Shutdown			155		ºC
	Thermal-shutdown Hysteresis			20		ºC
Dynamic Characteristics: see figure						
t_{DEB}	Debounce time	Time from 2.1V< V_{IN} < V_{OVLO} to V_{OUT} = 10% of V_{IN}		15		ms
t_{SS}	Soft-start time	Time from 2.1V< V_{IN} < V_{OVLO} to 0.2×FLAG,VIO=1.8V with 10kΩ Pull-up Resistor		30		ms
t_{ON}	Switch Turn-on time	R_L=100Ω, C_L=22uF, V_{OUT} from 0.1×V_{IN} to 0.9×V_{IN}		2		ms
t_{OFF_RES}(1)	Switch turn-off response time	V_{IN} > V_{OVLO} to V_{OUT} stop rising		100		ns

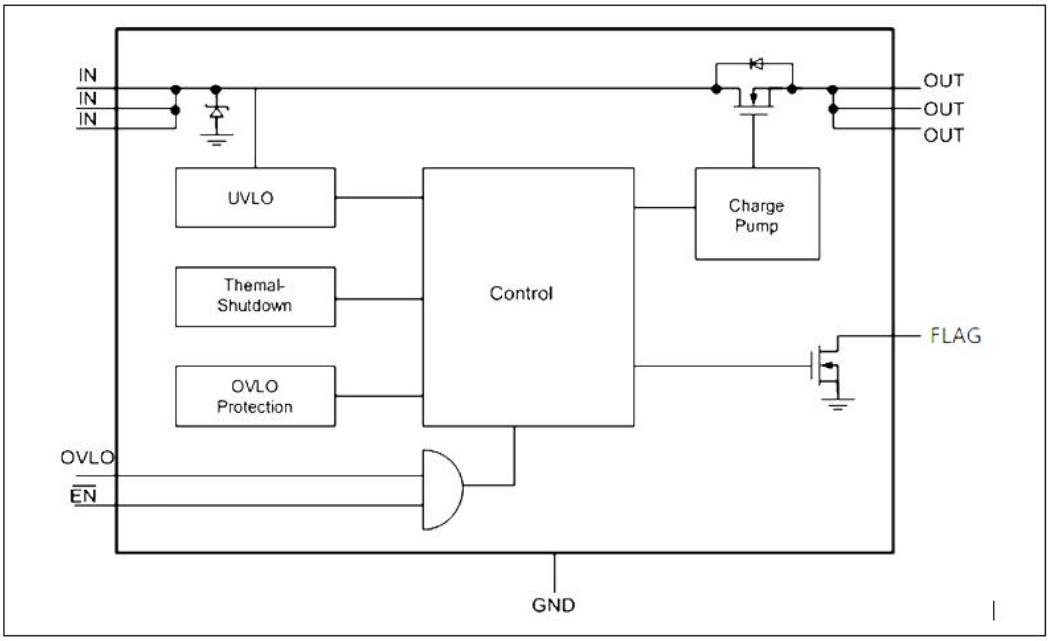
Electrical Characteristics

Unless otherwise noted, typical values are at V_{IN}=5V and T_A=25°C.

Note：

(1) Guaranteed by characterization and design.

Block Diagram



Functional Description

The OVP switch with overvoltage protection feature a low 30 mΩ (TYP.) on-resistance(R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 26V_{DC}. If $\overline{EN}$ is in the logic low state, when the input voltage(V_{IN}) exceeds 14V, the internal FET is quickly turned off to prevent damage to the protected downstream components. If $\overline{EN}$ is in the logic high state. the WP3882 will feature the Microphone mode which disables the protect low-voltage system.

When input (OVLO) is set lower than 0.3V. The overvoltage protection threshold is 14V.

The overvoltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.4V.

$V_{IN\_OVLO} = V_{OVLO\_TH} * (1+R1/R2)$ $V_{OVLO\_TH} = 1.2V(TYP.)$

The internal FET turns off when the junction temperature exceeds +150°C (TYP.). The device exits thermal shutdown after the junction temperature cools by 20°C (TYP.).

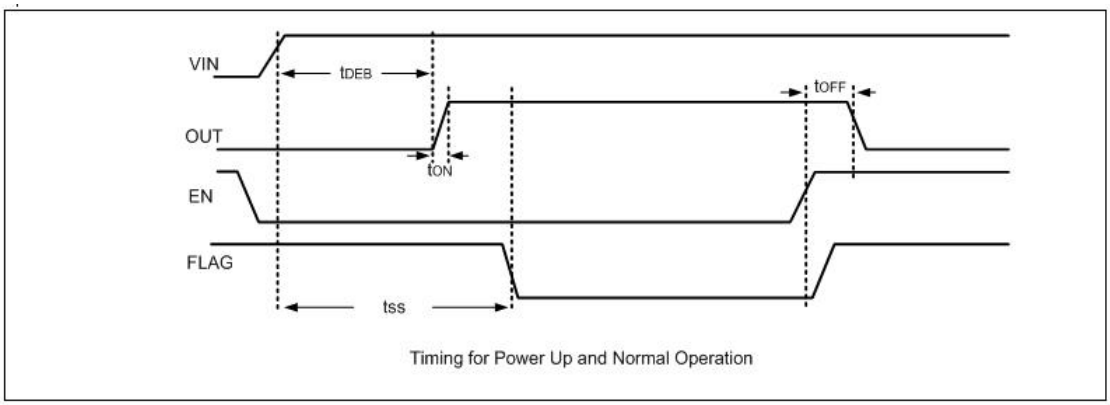
Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1μF or larger must be placed between the VIN and GND pins.

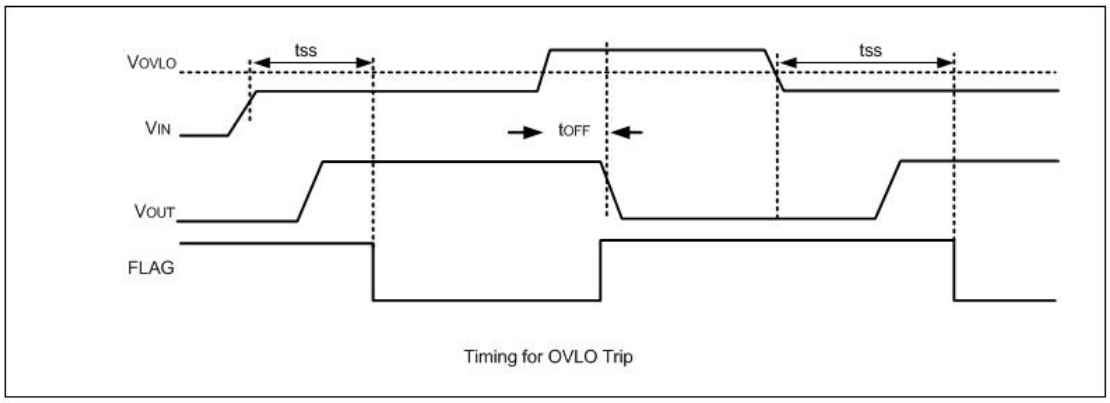
Output Capacitor

A 1μF or larger capacitor should be placed between the OUT and GND pins.

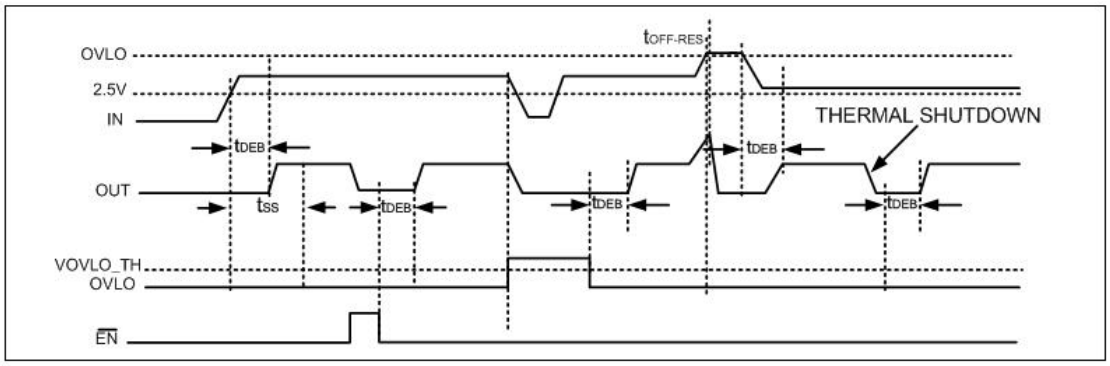
Timing Diagram



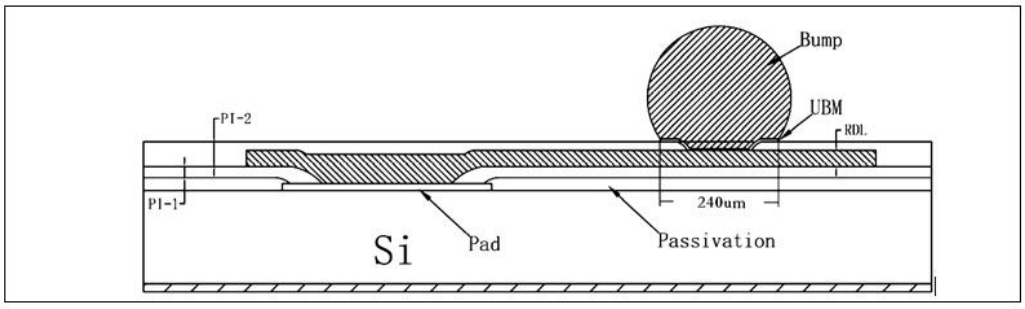
Timing for Power Up and Normal Operation



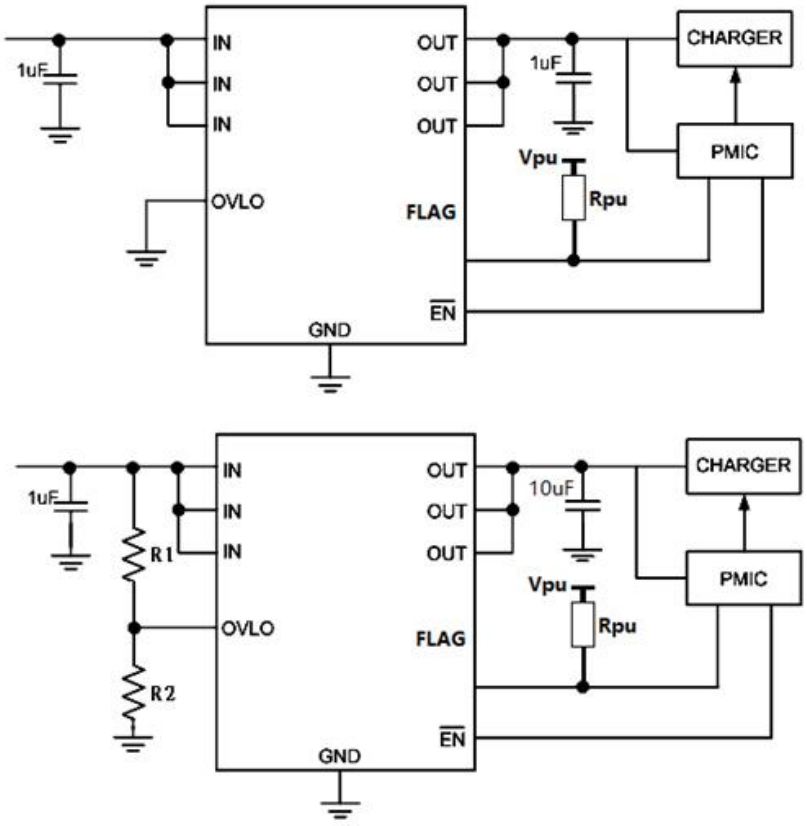
Timing for OVLO Trip



UBM Structure



Application Circuits



Note1: R1 and R2 are only required for adjustable OVLO; Otherwise OVLO is connected to GND.

Note2: Recommend 30K≤R2≤51K.

*：This electric circuit only supplies for reference.

Package