Dual Channel OVP Switch and Load Switch

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WP3899

Description

WP3899 integrated OVP switch1 and load switch2.

The OVP switch1 can disconnect the systems from its output pin(Vo) in case wrong input operating conditions are detected. The system is positive overvoltage protected up to 28V.

The load switch2 can disconnect the systems from its output pin(BAT) in case wrong input operating conditions are detected, the system is positive overvoltage protected up to 6.5V and under-voltage lockout is 2.2V. And this switch has Reverse Current Blocking(RCB) function blocking unwanted reverse current from BAT to VIF.

Features

OVP switch1

- VBUS operating Range: 2.1V to 28V
- Absolute maximum voltage of VBUS: 30V
- Low $R_{DS(ON)}$: 30mΩ typ. at VBUS=5V/0.3A
- 3A Maximum Continuous Current Capability
- Overvoltage Lock-Out: OVLO=10.0V (TYP)
- Surge immunity to ±100V

Load switch2

- 2.3V to 6.0V Input Voltage Operating Range
- Absolute maximum voltage of VIF: 6.5V
- Low RDS(on): 16 mΩ TYP @ VIF=3V/0.5A, 10mΩ TYP @VIF=4.5V/0.5A
- 6A Maximum Continuous Current Capability
- Overvoltage Lockout (OVLO=5.25V TYP)
- Under-Voltage Lockout: UVLO=2.2V TYP
- True Reverse Current Blocking (TRCB)
- Surge immunity to ±40V

All

- Compliance to IEC61000−4−2 (Level 4): With a 1.0μF or larger bypass capacitor.
  15kV(Air) 8kV (Contact); ESD Ratings: HBM >2kV.
- CSP15 Package (1.6mm*2.2mm, ball pitch=0.4mm)

Applications

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Pin Configuration

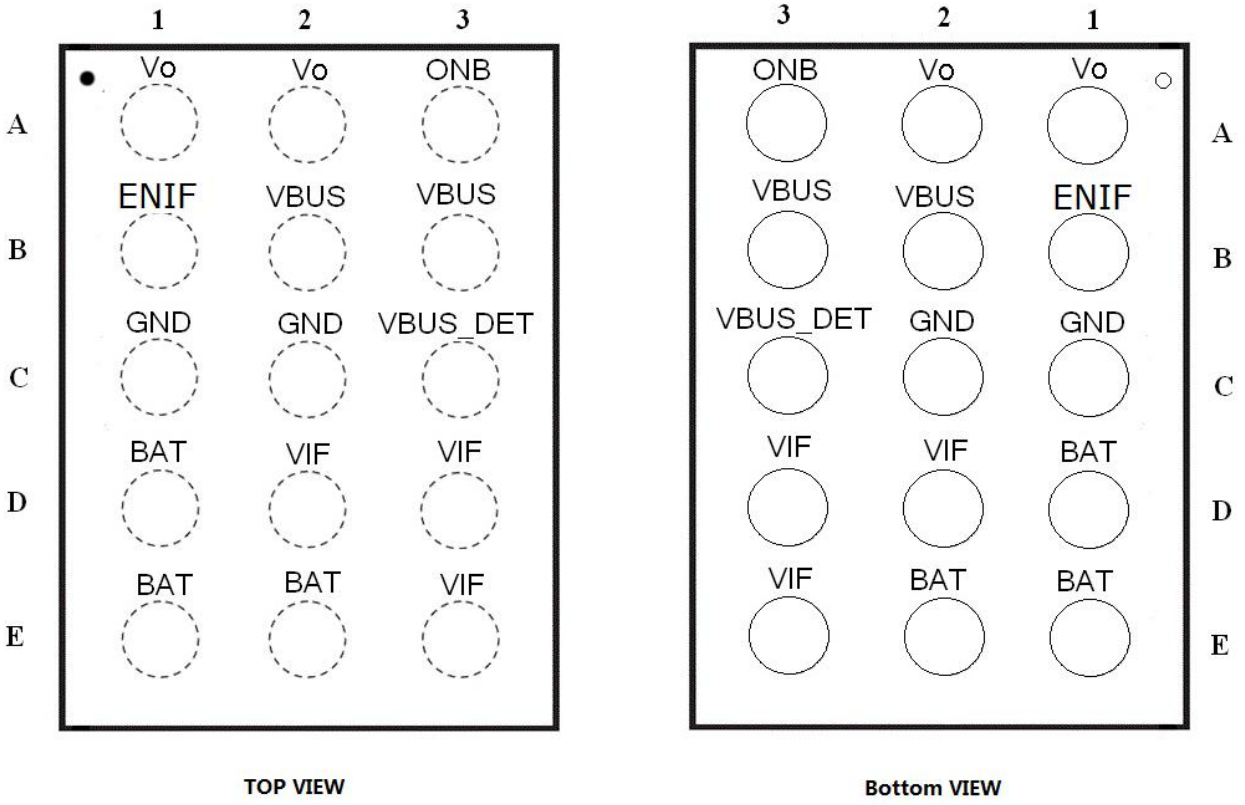


Figure 1 PIN MAP

Pin Function

Pin	Name	Pin Function
A1, A2	Vo	Output of OVP switch1
A3	ONB	OVP switch1 enable, active low
B1	ENIF	Enable of Load Switch2
B2, B3	VBUS	Input of OVP switch1
C1, C2	GND	Ground
C3	VBUS_DET	Regulation output of VBUS
D1, E1, E2	BAT	Output of switch2
D2, D3, E3	VIF	Input of switch2

Block Diagram

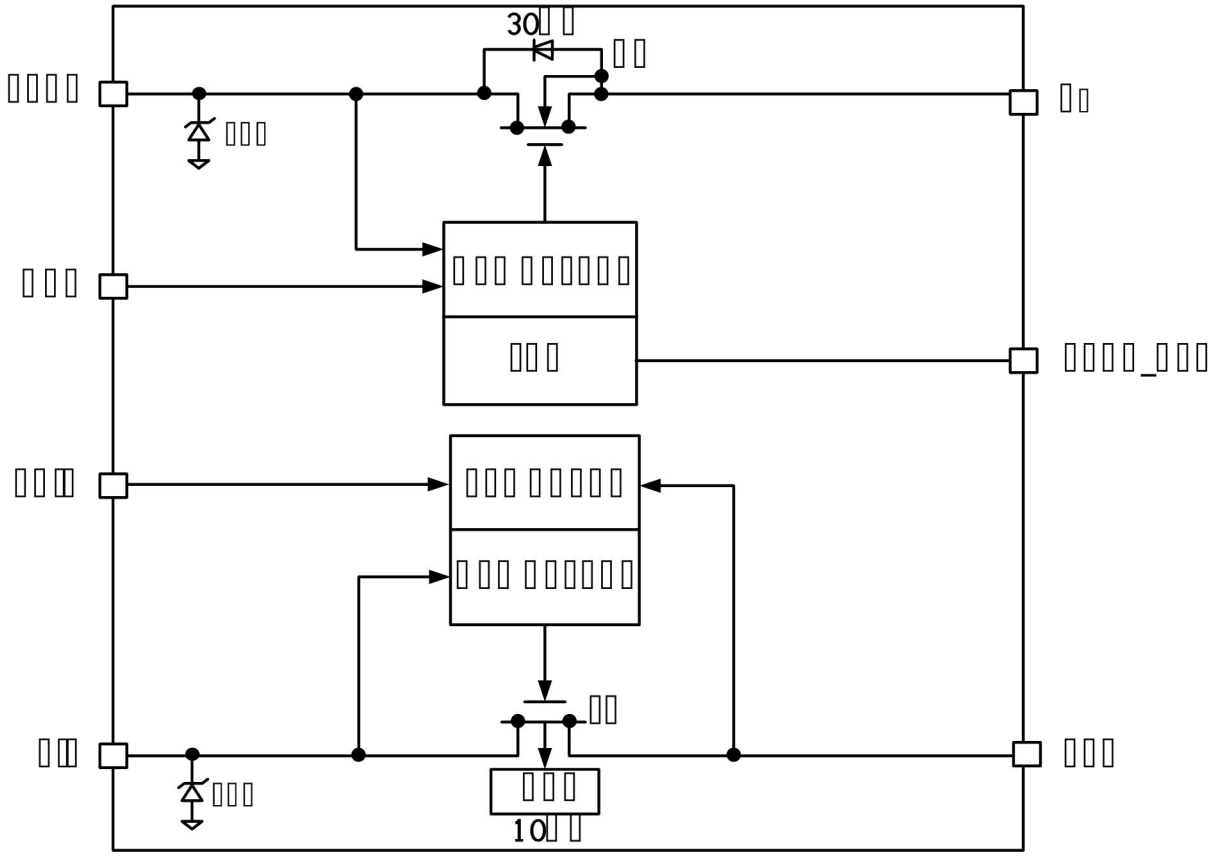


Figure 2 Block Diagram

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{BUS}	VBUS to GND	-0.3	30	V
V_{IF1}	VIF to GND	-0.3	7	V
V_{IF2}	VIF to GND, BAT<4.5V, 100mS	-2.0	4.5	V
V_{BAT}	BAT to GND	-0.3	6.5	V
V_{ONB}	ONB to GND	-0.3	6.5	V
V_{OUT}	V_{OUT} to GND	-0.3	VBUS+0.3	V
I_{SW1}	Maximum Continuous Current of switch VBUS		3	A
I_{SW2}	Maximum Continuous Current of switch VIF		6	A
I_{SW3}	Maximum Peak VBUS, Vo Current(10mS)		6	A
I_{SW4}	Maximum Peak VIF, BAT Current(5mS)		12	A
P_D	Power Dissipation at T_A=25℃		1.6	W
T_{STG}	Storage Junction Temperature	-65	+150	℃
T_A	Operating Temperature Range	-40	+85	℃
θ_{JA}	Thermal Resistance, Junction-to-Ambient		65	℃/W

ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	1.5		
Surge	VBUS to GND	IEC 61000-4-5, Surge protection	-100	100	V
	VIF to GND	IEC 61000-4-5, Surge protection	-40	40	

Recommended Operating Conditions

SYMBOL	PARAMETERS	MIN.	MAX.	UNIT
V_{BUS}	VBUS Input Voltage	2.1	28	V
V_{IF}	VIF input voltage	2.3	6.0	V
T_A	Ambient Operating Temperature	-40	+85	℃

Electrical Characteristics

OVP Switch

Unless otherwise noted, typical values are at V_{IN}=5V and T_A=25°C.

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Basic Operation						
V_{BUS}	Input Voltage		2.1		28	V
I_{Q1}	VBUS Quiescent Current	V_{ONB}=low, no load		140		μA
R_{ON1}	VBUS On-Resistance	V_{BUS}=5.0V, I_{OUT}=0.3A		30		mΩ
V_{IH}	ONB Input Logic High Voltage	V_{BUS}=2.1V to 28V	1.5			V
V_{IL}	ONB Input Logic Low Voltage	V_{BUS}=2.1V to 28V			0.5	V
R_{PD}	Pull-Down Resistance at ONB pin			1		MΩ
V_{OVLO1}	Overvoltage protect of VBUS	V_{BUS} rise up	9.8	10.0	10.2	V
	Overvoltage protect hysteresis of VBUS			0.1		V
V_{UVLO1}	Under-Voltage protect of VBUS	V_{BUS} fall down		2.0		V
V_{DET}	regulation output of VBUS_DET	ONB=low	6		9.5	V
	Thermal Shutdown			150		℃
	Thermal-shutdown Hysteresis			20		℃
Dynamic Characteristics: see figure 3						
t_{DEB}	Debounce Time	Time from 2.1V<V_{BUS}<9.9V to Vo=10% of V_{BUS}		21		ms
t_{SS}	Soft-start time	Vo=10% of V_{BUS} to soft-start off		1.2		ms
t_{OFF_RES}	Load Switch turn-off response time	R_L=100Ω, No C_L, V_{IF} > V_{OVLO2} to VBAT stop rising			150	ns

Crosstalk	VBUS to BAT	V_{BUS} =5V, V_{IS}=1V RMS , f_{VBUS}=0~100MHZ,C_{BAT}=20μF		-50		dB

Load Switch

Unless otherwise noted, typical values are at V_{IN}=5V and T_A=25°C.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
V_{IF}	VIF Input Voltage		2.3		6.0	V
I_Q	VIF Quiescent Current	No load		25	30	μA
R_{ON}	On-Resistance	V_{IF}=4.5V, I_O=0.5A		10		mΩ
		V_{IF}=3.0V, I_O=0.5A,		16		
V_{OVLO2}	Overvoltage protect of VIF	V_{IF} rise up	5	5.25	5.5	V
	Overvoltage protect hysteresis of VIF			0.3		V
V_{UVLO2}	Under-Voltage protect of VIF	V_{IF} fall down		2.2		V
V_{IH2}	ENIF Input Logic High Voltage	V_{IF}=5.0V	1.5			V
V_{IL2}	ENIF Input Logic Low Voltage	V_{IF}=5.0V			0.4	V
V_{BATH}	BAT Logic High Voltage	V_{IF}=5.0V	2.5			V
V_{BATL}	BAT Logic Low Voltage	V_{IF}=5.0V			1.0	V
I_{ENIF}	ENIF Input Leakage	V_{ENIF}=V_{IF}=5.0V			1.0	μA
True Reverse Current Blocking						
V_{T_RCB}	RCB Protection Trip Point	V_{BAT} - V_{IF}		15		mV
V_{R_RCB}	RCB Protection Release Trip Point	V_{IF} - V_{BAT}		45		mV
	RCB Hysteresis			60		mV
I_{SD_OUT}	V_O Shutdown Current	V_{BAT} =5.0V, V_{IF} =Short to GND			2	μA
T_{RCB_OFF}	RCB Response Time Device OFF	V_{BAT} - V_{IF} =100mV		4		μs
Dynamic Characteristics: see figure 4						
t_{DON+} t_{CHECK}	Turn-On Delay (1,2) + Power on check Time(3)	V_{IF} = 4.5V(power on),R_L=100Ω, C_L=22μF,V_{ENIF}=GND,T_A=25℃		4		ms
t_R	V_{OUT} Rise Time (1,2)	V_{IF} = 4.5V, R_L=100Ω, C_L=22μF,V_{ENIF}=GND,T_A=25℃		0.6		ms
t_{OFF_RES1}	Load Switch turn-off response time	R_L=100Ω, No C_L, V_{IF} > V_{OVLO2} to VBAT stop rising			150	ns

1. This parameter is guaranteed by design and characterization.
2. t_{DON} and t_R are defined in Figure 4.
3. t_{CHECK} are defined in figure 5.

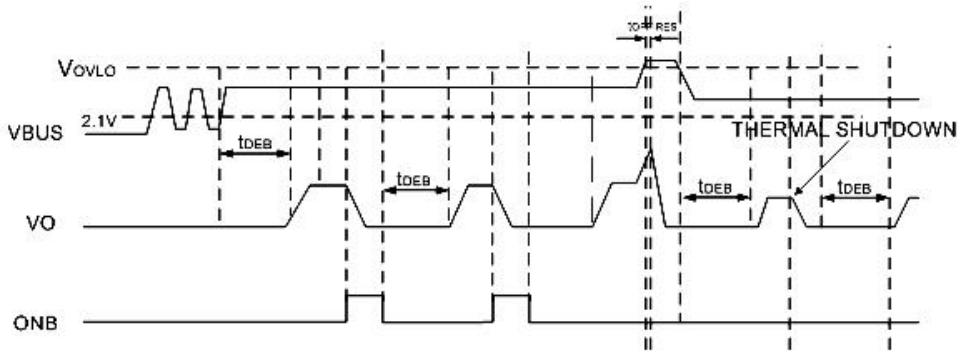


Figure 3

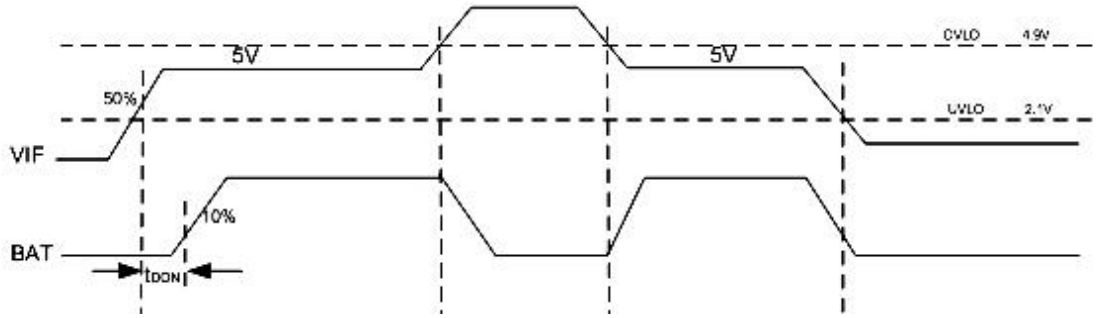


Figure 4

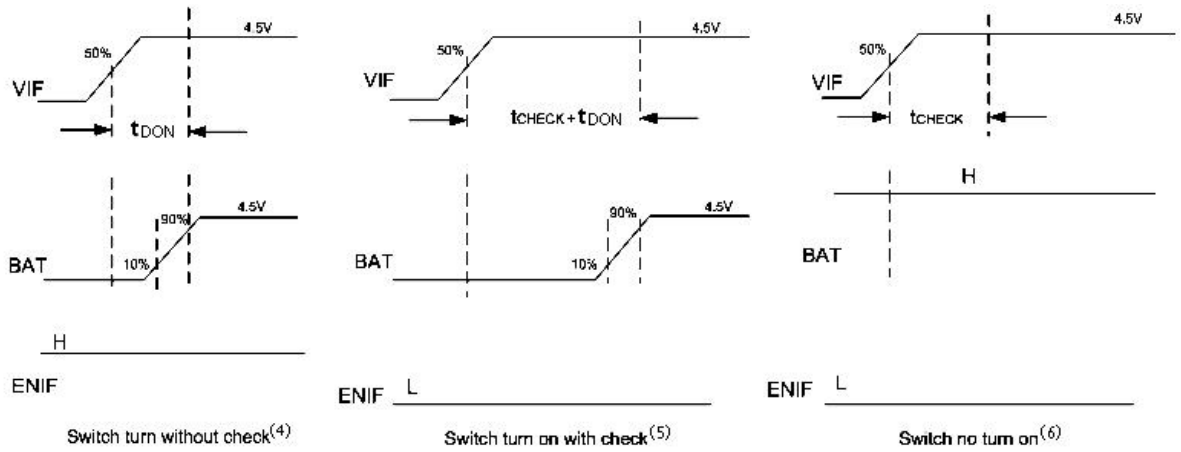


Figure 5

4.ENIF is high, the VIF power on, normally open switch;

5.ENIF if low and VBAT<1V, the VIF power on, open switch automatically;

6.ENIF if low and VBAT>2.5V，the VIF power on ,the switch remains off.

Functional Description

The WP3899 integrated two switches.

The OVP switch1 with overvoltage protection include a low 30mΩ(typ.) on-resistance(R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28V DC. When the input voltage(VBUS) exceeds 10.0V, the internal FET is quickly turned off to prevent damage to the protected downstream components. The active low pin ONB can turn off switch

when add a voltage exceeds 1.5V on this pin.

The load switch2 is a 10mΩ P-channel load switch with TRCB (True Reverse Current Blocking) between VIF and BAT.

When ENIF is low, VIF power on, the circuit will check the voltage of the BAT pin with a 300ohm pull down resistor after 3ms. If BAT is lower than 1.0V, the switch2 will turn on, and if BAT is higher than 2.5V, the switch2 will keep off.

When ENIF is high, the switch2 will turn on.

This switch is quickly turned off when the voltage of VIF exceeds 5.25V(typ.) or VIF lower than 2.2V.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1.0μF or lager must be placed between the VBUS and GND pins. Another capacitor 1.0μF or lager must be placed between the VIF and GND pins.

Output Capacitor

A 1.0μF or lager capacitor should be placed between the Vo and GND pins, anther 1.0μF or lager capacitor should be placed between the BAT and GND pins. C_{OUT} greater than C_{IN} is highly recommend.

Application Circuit

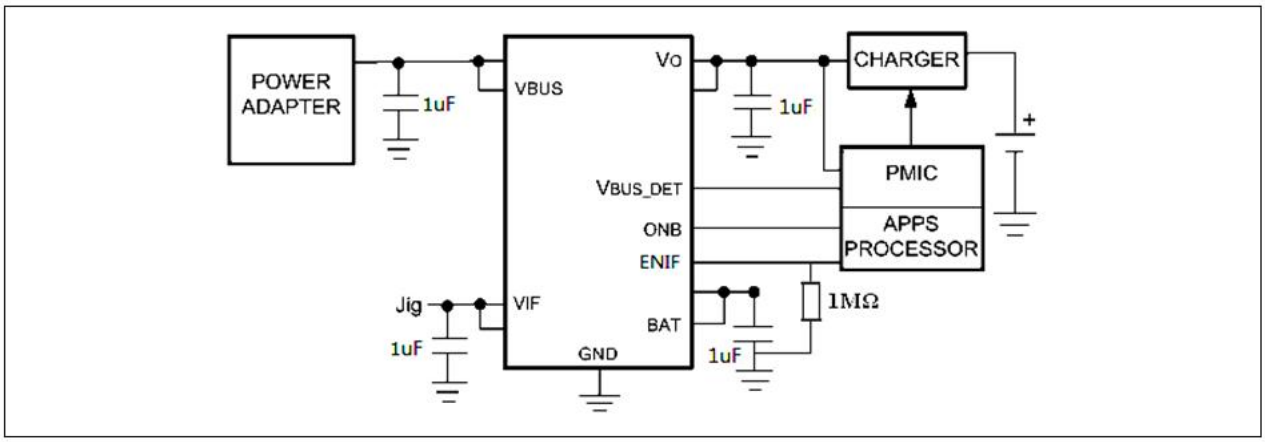
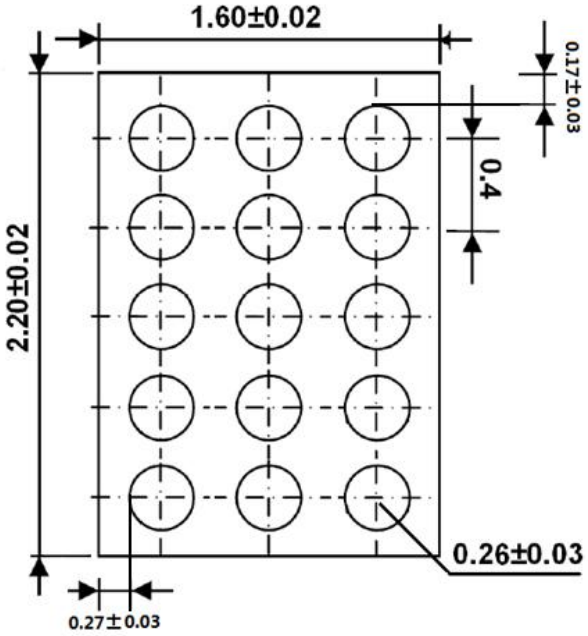


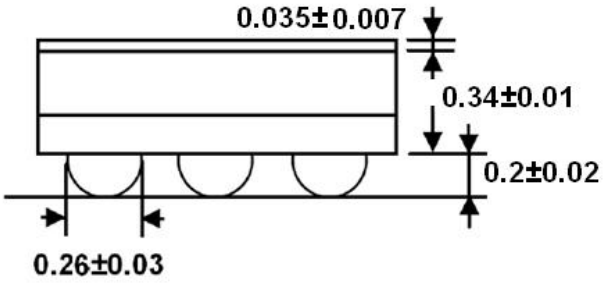
Figure 6 Typical Application

*：This electric circuit only supplies for reference

Package



Bottom View



Side View

Unit:mm