WP3891

Over-Voltage Protection IC with OTG

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Description

The WP3891 is OVP switch can disconnect the systems from its output pin in case wrong input operating conditions are detected. The system is positive overvoltage protected up to 28V.

When input (OVLO) is set lower than 0.2V. The overvoltage protection threshold is 5.9V. The overvoltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

The WP3891 provide Over Temperature Protection and also provide Reverse Current Blocking when the WP3891's switch is disabled.

The WP3891 provide OTG function allows OUT voltage to supply IN.

The device is packaged in advanced Full-Green compliant 2.1mmx1.6mm Wafer Level Chip Scale Packaging (WLCSP).

Features

- operating Range: 3V to 28V
- Absolute maximum voltage of VIN: 29V
- Low RDS(on): 60mΩ TYP at Vin=5V/0.3A
- 4.5A Maximum Continuous Current Capability
- Overvoltage Lockout :OVLO=5.9V (TYP)
- Debounce Time :20ms
- OTG Enable function
- Surge immunity to ±100V
- CSP15 Package (1.6mm*2.1mm, ball pitch=0.4mm)
- Compliance to IEC61000−4−2 (Level 4): bypassed with a 1.0μF or larger capacitor
  15kV(Air) 8kV (Contact) ; ESD Ratings: HBM >2kV

Applications

- Smartphones, Tablet PC
- HDD, Storage and Solid State Memory Devices
- Portable Media Devices, Laptop & MID
- SLR Digital Cameras
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Pin Configuration

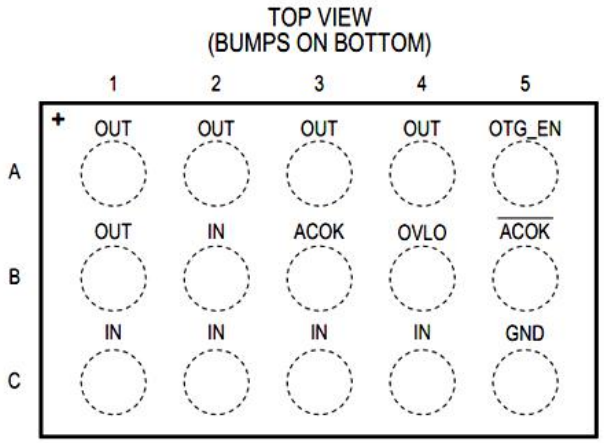


Figure1:pin map

Pin Function

PIN	NAME	DESCRIPTION
A1,A2,A3,A4,B1	OUT	Overvoltage Protection Output when OTG_EN=low and OTG output when OTG_EN=high. Bypass OUT with a 1μF ceramic capacitor.
A5	OTG_EN	Enable Input for OTG Supply Operation or Overvoltage Protection
B2,C1,C2,C3,C4	IN	Overvoltage Protection Input when OTG_EN=low and OTG output when OTG_EN=high. If desired, bypass IN with a 0.1μF ceramic capacitor as close to the device as possible.
B3	ACOK	1.8V Logic Output. It is driven high after input voltage is stable between minimum VIN and VOVLO when OTG_EN = 0. Connect a pulldown resistor from ACOK to ground.
B4	OVLO	Overvoltage Lockout Input. Connect OVLO to GND to use internal OVLO threshold. Connect OVLO to a resistor-divider for a different voltage threshold.
B5	$\overline{\text{ACOK}}$	Open-Drain Flag Output. It is driven low after input voltage is stable Between minimum VIN and VOVLO when OTG_EN = 0. Connect a pullup resistor from it to the logic I/O voltage of the host system.
C5	GND	Ground.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters	Min.	Max.	Unit
V_{IN}	IN to GND	-0.3	29	V

V_{OUT}	OUT to GND		-0.3	26	V
V_{IN-OUT}	IN-OUT		-26	29	V
V_{OTG_EN}	OTG_EN to GND		-0.3	6.0	V
V_{ACOK}	ACOK to GND		-0.3	6.0	V
$V_{\overline{ACOK}}$	$\overline{ACOK}$ to GND		-0.3	6.0	V
V_{OVLO}	OVLO to GND		-0.3	26	V
I_{SW1}	Maximum Continuous Current of switch			4.5	A
P_D	Power Dissipation at T_A=25℃			1.4	W
T_{STG}	Storage Junction Temperature		-65	+150	℃
T_A	Operating Temperature Range		-40	+85	℃
θ_{JA}	Thermal Resistance, Junction-to-Ambient			52	℃/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	1.5		
Surge	IN to GND	IEC 61000-4-5, Surge Protection	-100	100	V

Electrical Characteristics

Unless otherwise noted, Typical values are at V_{IN}=5V and T_A=25 °C.

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_Q	IN Quiescent Current	V_{OVLO} = 0V, V_{IN} = 5V, ACOK is unconnected, I_{OUT} = 0mA		95	190	μA
I_{OUT}	OUT Quiescent Current	V_{OVLO} = 0V, V_{OUT} = 5V, I_{IN} = 0mA, V_{OTG_EN} = 1.8V		80	170	μA
I_{OUT_S}	OUT Shutdown Current	V_{OVLO} = 3V, V_{OUT} = 5V, V_{IN} = 0V, V_{OTG_EN} = 0V		5	12	μA
R_{ON}	IN to OUT On-Resistance	V_{IN}=5.0V, I_{OUT}=0.1A		60	70	mΩ
		V_{IN}=5.0V, I_{OUT}=2.0A		62	72	
V_{INBT}	Input Startup Voltage			1.8	3	V
V_{INBU}	Input Sustaining Voltage	I_{OUT} = 0A		1.5	2.3	V
V_{OUTBT}	Output Startup Voltage			1.8	3	V
V_{OUTBU}	Output Sustaining Voltage	I_{IN} = 0A		1.5	2.3	V
	IN Leakage Voltage	V_{OUT} =21V, IN unconnected,			0.1	V

		V_{OTG_EN} = 0V				
V_{IN_OVLO}	Internal Overvoltage Trip Level	V_{IN} rising	5.81	5.90	6.0	V
		V_{IN} falling		5.80		
V_{OVLO_TH}	OVLO Set Threshold		1.18	1.22	1.26	V
V_{OVLO_EXT}	Adjustable OVLO Threshold Range		5		22	V
V_{OVLO_SEL}	External OVLO Select Threshold		0.20	0.25	0.30	V
V_{ACOK}	ACOK Output High Voltage	I_{SOURCE}≤100μA, V_{IN} > 3V	1.6	1.8	2.0	V
	ACOK Leakage Current	Pull down to ground, V_{OUT} = 5V, OTG_EN=high, ACOK deasserted			1	μA
V_{OL}	$\overline{ACOK}$ Output Low Voltage	V_{IO} = 3.3V, I_{SINK} = 1mA			0.4	V
V_{IH}	OTG_EN Input Logic High		1.6			V
V_{IL}	OTG_EN Input Logic Low				0.4	V
I_{OTG_EN}	OTG_EN Input Leakage Current	0V ≤ V_{OTG_EN} ≤ V_{IL} and V_{IH} ≤ V_{OTG_EN} ≤ V_{IN}, V_{IN} = 5.5V	-1		1	μA
	Thermal Shutdown			150		℃
	Thermal-shutdown Hysteresis			20		℃
Dynamic Characteristics: see figure 3						
t_{DEB}	Debounce Time	V_{IN} = 5V to charge pump on (V_{OUT} = 10% of V_{IN}), R_{LOAD} = 100Ω, C_{LOAD} = 10μF		20		ms
t_{SS}	Soft-start time	V_{IN} = 5V to V_{OUT} = 90% of V_{IN}, R_{LOAD} = 100Ω, C_{LOAD} = 10μF		25		ms
t_{ON}	IN OVP Turn-On Time During Soft-Start	V_{IN} = 5V, R_{LOAD} = 100Ω, C_{LOAD} = 10μF, V_{OUT} = 20% of V_{IN} to 80% of V_{IN}		1.5		ms
t_{OFF}	IN OVP Turn-Off Response Time	From V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{IN}, R_{LOAD} = 100Ω		1		μs
t_{OTG_ON}	OTG Turn-On Time	Time from OTG_EN high to V_{IN} = 80% of V_{OUT}, V_{OUT} = 5V, C_{IN} = 10μF		1.4		ms
	In-Discharge Pulse Duration	V_{IN} = V_{OUT} = 5V, current pulse duration after an OTG_EN transition from high to low		1.1		ms

Block Diagram

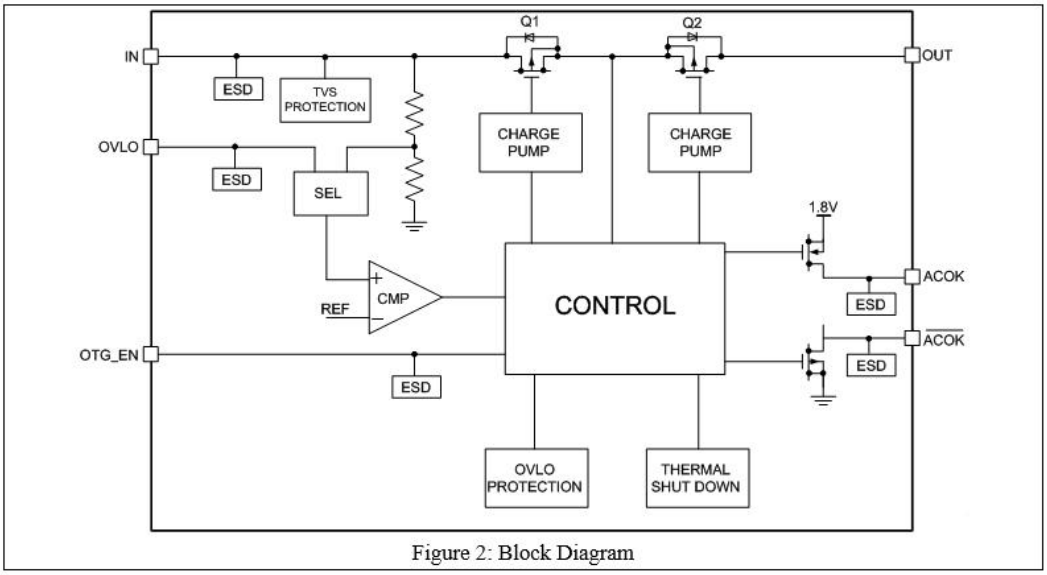


Figure 2: Block Diagram

Timing Diagram

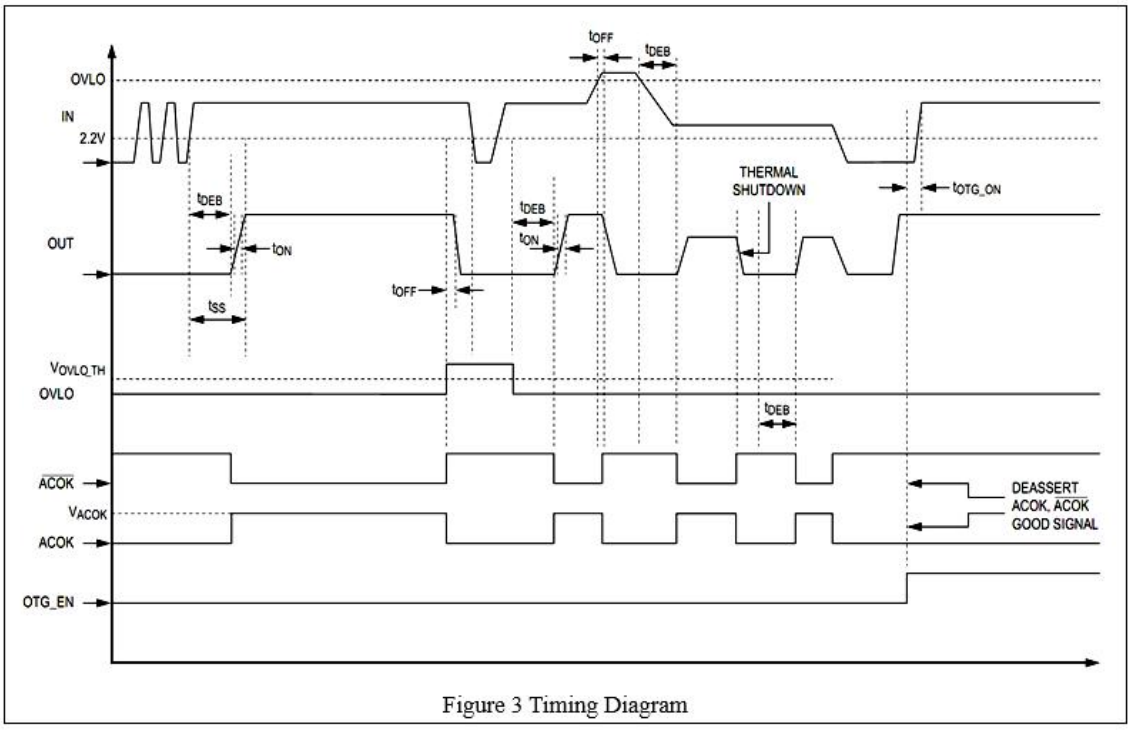


Figure 3 Timing Diagram

Functional Description

The OVP switch with overvoltage protection include a low 60mΩ(TYP) on-resistance(R_{ON}) internal FET and protect low-voltage systems against voltage faults up to 28V DC. When the input voltage(VIN) exceeds the overvoltage protection threshold, the internal FET is quickly turned off to prevent damage to the protected downstream components, the pin ACOK/ $\overline{ACOK}$ is deasserted. When IN drops below V_{IN_OVLO} OUT follows IN again and ACOK / $\overline{ACOK}$ is asserted. When OTG_EN is high, ACOK and $\overline{ACOK}$ is also deasserted.

When input (OVLO) is set lower than 0.2V. The overvoltage protection threshold is 5.9V.

The overvoltage protection threshold can also be adjusted by external resistors when input (OVLO) is set higher than 0.3V.

$V_{IN\_OVLO} = V_{OVLO\_TH} * (1+R1/R2)*$ $V_{OVLO\_TH} = 1.22$ V(TYP)

If OTG_EN is high and OUT voltage is high than the V_{OUTBT} (Output Startup Voltage), The WP3891 allows OUT voltage to supply IN. When the input voltage (VIN) exceeds the overvoltage protection threshold, the switch will be closed.

The WP3891 also provide Reverse Current Blocking when the switch is disabled.

When the junction temperature exceeds 150℃, the internal thermal sense circuit turns off the FET and allows the device to cool down. When the device's junction temperature cools by 20℃, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions.

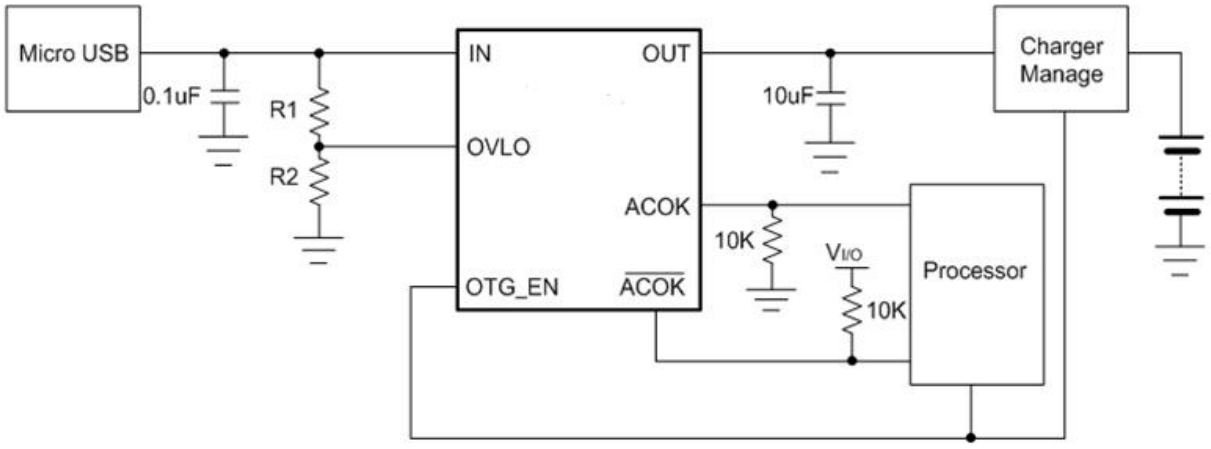
Input Capacitor

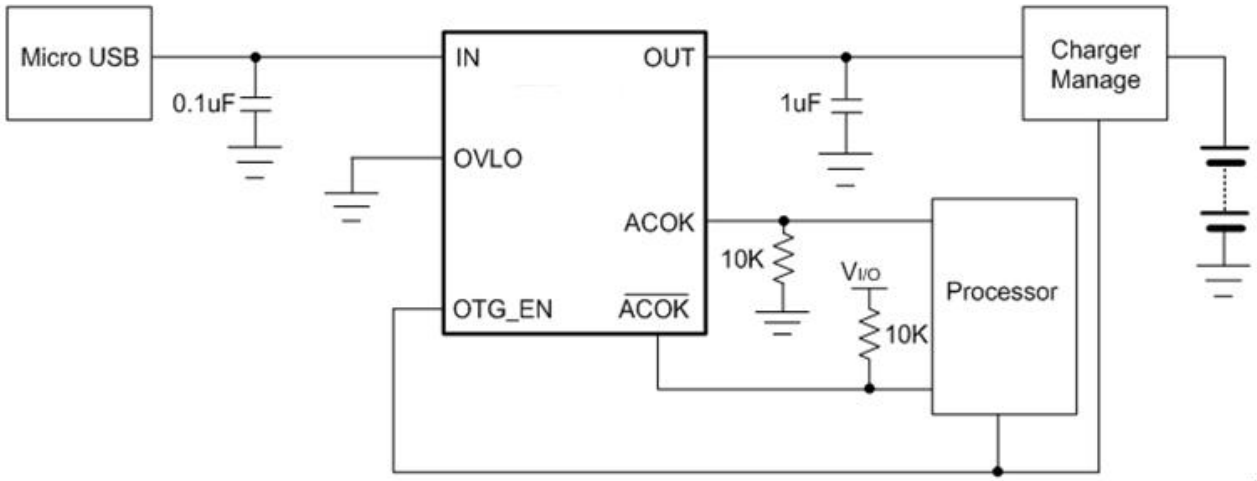
To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor 1μF must be placed between the IN and GND pins.

Output Capacitor

A 1.0μF or lager capacitor should be placed between the OUT and GND pins

Application Circuits



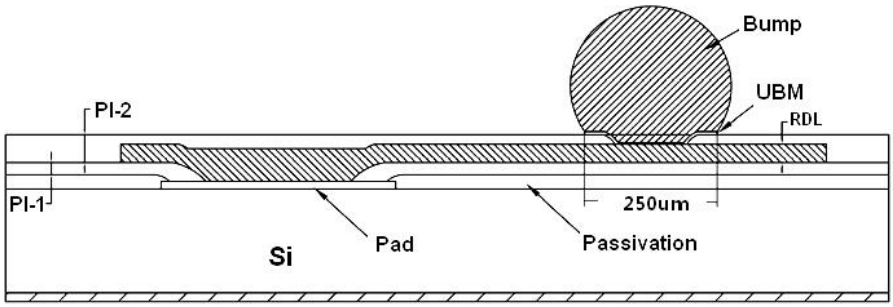


Note1: R1 and R2 are only required for adjustable OVLO; otherwise connect OVLO to GND.

Note2: Recommend 30K≤R2≤51K

*: This circuit only supplies for reference.

UBM Structure



Package

WCSP15(Unit :mm)