March 2011
Revision 1.40

WPCT301/NPCT501 Trusted Platform Module (TPM) Version 1.2 with I²C Interface

General Description

The Nuvoton WPCT301/NPCT501 family of single-chip Trusted Platform Modules (TPM) is a third-generation Nuvoton SafeKeeper™ device that implements the TCG version 1.2 specification for PC-Client TPM with the addition of a serial data interface.

The WPCT301/NPCT501 is designed to reduce system power-up time and Trusted OS loading time. It provides a complete platform security solution for a wide range of computer systems.

Features

General

- Complete, single-chip TPM solution
  - No external parts required
- Compatible with the Trusted Computing Group (TCG) TPM 1.2 Main
- Host Interface
  - TPM 1.2 Interface (TIS) emulation
  - Dedicated Interrupt signal
- Secure General-Purpose I/O (GPIO)
  - Up to three GPIO pins
  - I/O pins individually configured as input or output
  - Configurable internal pull-up resistors
  - TCG 1.2-defined interface
  - Dedicated Physical Presence (PP) pin with configurable pull-up or pull-down resistor
- Tick Counter

Bus Interface

- I²C Bus Interface
  - I²C Slave
  - Up to 400 KHz clock operation (NPCT501)

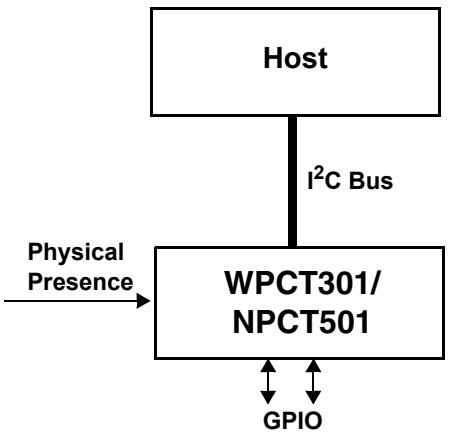
Clocking and Supply

- On-Chip Clock Generator
- Power Supply
  - 3.3V supply operation
  - Separate pins for main (V_{DD}) and standby (V_{SB}) power supplies
  - Low standby power consumption

Package

- 28-pin Thin Shrink Small Outline Package (TSSOP28)

System Block Diagram



Datasheet Revision Record

Revision Date	Status	Comments
February 2008	Revision 0.9	Preliminary Datasheet
March 2008	Revision 1.0	Preliminary Datasheet, second release
April 2008	Revision 1.01	Removed t_{WLB} requirement Fixed SPI_DO I/O definition in 1.3.1 Serial Interface Fixed signal names in 3.4.3 I^2C Timing and 3.4.4 SPI Timing diagrams In 3.4.4 SPI Timing diagram, changed Max frequency of t_{SCK} (SPI Timing) to 100 KHz
June 2008	Revision 1.02	In 3.4.4 SPI Timing diagram, changed Max frequency of t_{SCK} (SPI Timing) to 200 KHz Replaced Figures 11 and 12 (page 20)
November 2009	Revision 1.03	Nuvoton revision. Changed logos and company name.
January 2010	Revision 1.04	Order numbers changed (...0WG to ...0WX) Added description to SADD pin
August 2010	Revision 1.05	Changed power-well to V_{DD} for all pins in Section 1 (Signal/Pin Connection and Description). Changed SADD description in Section 1.3.3. Changed Section 1.4 (Internal Pull-up and Pull-down Resistors). Changed Section 4.4.2 (Reset Timing). Updated Table 1 (“Buffer Types”) and updated Section 1.3 (“Signal/Pin Description”) tables, accordingly.
December 2010	Revision 1.10	Removed references to the Nuvoton WPCT300 (SPI Interface). Added the NPCT501 device.
January 2011	Revision 1.20	Typo fixes. Added TPM Host Interface description (Section 3).
March 2011	Revision 1.30	Changed t_{SRST} max requirement from 2.5 s to none, in Power-Up Reset Timing table (Section 4.4.2). Added $t_{RST.STA}$ to I^2C Timing table (Section 4.4.3).
March 2011	Revision 1.40	Added NPCT501MA0WX order number to pinout diagram and back cover.

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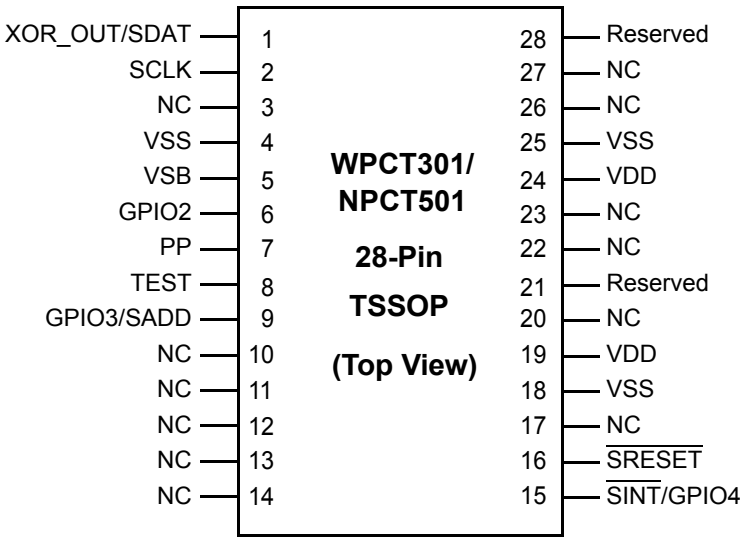
1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



NC = Not Connected

28-Pin Thin Shrink Small Outline Package (TSSOP28), JEDEC
Order Numbers: WPCT301AA0WX
NPCT501AA0WX
NPCT501MA0WX

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.3 on page 5 are denoted by buffer type symbols, which are defined in Table 1.

Table 1. Buffer Types

Symbol	Description
IN_{TS}	Input, TTL compatible, with 250 mV Schmitt Trigger
IN_{RST}	Input, Reset pin
$O_{p/n}$	Output, TTL/CMOS compatible, push-pull buffer capable of sourcing *p* mA and sinking *n* mA
OD_n	Output, TTL/CMOS compatible, open-drain buffer capable of sinking *n* mA
PWR	Power pin
GND	Ground pin

1.0 Signal/Pin Connection and Description (Continued)

1.3 SIGNAL/PIN DESCRIPTIONS

This section describes all signals of the WPCT301/NPCT501 device. The signals are organized by functional group.

1.3.1 Serial Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SDAT	1	I/O	IN_{TS}/OD_4	V_{DD}	**Serial Data In/Out.** I^2C data in/out.
SCLK	2	I/O	IN_{TS}/OD_4	V_{DD}	**Serial Clock.** I^2C clock.
$\overline{SINT}$	15	I/O	IN_{TS}/OD_8, $O_{4/8}$	V_{DD}	**Serial Communication Command Completion Interrupt.** Active low as long as there is data on the output data FIFO.
$\overline{SRESET}$	16	I	IN_{RST}	V_{DD}	**Serial Reset.** Host system reset used for the serial bus (Hardware reset).

1.3.2 Inputs and Outputs

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
PP	7	I	IN_{TS}	V_{DD}	**Physical Presence Input.** Indicates owner's physical presence.
GPIO4-2	15, 9, 6	I/O	IN_{TS}/OD_8, $O_{4/8}$	V_{DD}	**General-Purpose I/O Port.** General-Purpose I/O pins compatible with the *PC Client TPM 1.2 Specification*.

1.3.3 Configuration Straps and Testing

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
TEST	8	I	IN_{TS}	V_{DD}	**Test Mode.** Sampled at V_{DD} Power-Up reset to force the device pins into a XOR tree or TRI-STATE® configuration, as follows: – No pull-up resistor (default) - Normal device operation – 4.7 KΩ external pull-up resistor - Pins configured for Test mode.
SADD	9	I	IN_{TS}	V_{DD}	**Serial Slave Address.** Sampled at V_{DD} Power-Up reset to select the slave address, as follows: - No pull-down resistor - AEh (write) and AFh (read) - 10 KΩ external pull-down resistor - reserved for future implementation. Do not use this option. **Test Mode Selection.** Test mode (XOR tree or TRI-STATE) is selected by the sampled state of the SADD pin during VDD Power-Up reset. When SADD is sampled high, XOR Tree mode is selected. When SADD is sampled low, TRI-STATE mode is selected, floating all output pins.
XOR_OUT	1	O	$O_{4/8}$	V_{DD}	**XOR Tree Output.** This pin is the output of the XOR tree test logic.

1.3.4 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
VSS	4, 18, 25	I	GND		**Ground.** Ground connection for both core logic and I/O buffers, for the Main, Standby and Battery power supplies.
VDD	19, 24	I	PWR		**Main 3.3V Power Supply.** Powers the I/O buffers of the GPIO ports and the serial interface.
VSB	5	I	PWR		**Standby 3.3V Power Supply.** Powers the on-chip core.

1.0 Signal/Pin Connection and Description (Continued)

1.3.5 Reserved

Signal	Pin(s)	Description
NC	3, 10-14, 17, 20, 22-23, 26-27	**Not Connected.** These pins must be left unconnected.
Reserved	21, 28	**Reserved.** These pins must be connected to an external 10 KΩ pull-down resistor.

1.4 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 2 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as “Programmable”

Table 2. WPCT301/NPCT501 Internal Pull-Up and Pull-Down Resistors

Signal	Pin(s)	Power Well	Type		Comments
			WPCT301	NPCT501	
$\overline{\text{SINT}}$/GPIO4	15	V_{DD}	PU_{66}	PU_{110}	GPIO4 Programmable[1]
GPIO3-2	9, 6	V_{DD}	PU_{66}	PU_{110}	Programmable
PP	7	V_{DD}	PU_{66}/PD_{50}	PU_{110}/PD_{110}	Programmable[2]
TEST	8	V_{DD}	PD_{50}	PD_{110}	Strap
SADD	9	V_{DD}	PU_{66}	PU_{110}	Strap
SDAT	1	V_{DD}	PU_{66}	PU_{110}	

1. Controlled by TPM. Default at reset: GPIO4 disabled.
2. Controlled by TPM. Default at reset: pull-down enabled.

2.0 Trusted Platform Module (TPM) Overview

The WPCT301/NPCT501 provides TPM functionality in TCG 1.2-compliant systems and is designed to best meet the requirements of embedded computer systems.

2.1 SYSTEM CONNECTIONS

Figure 1 shows the system connections of the WPCT301/NPCT501 in a typical system.

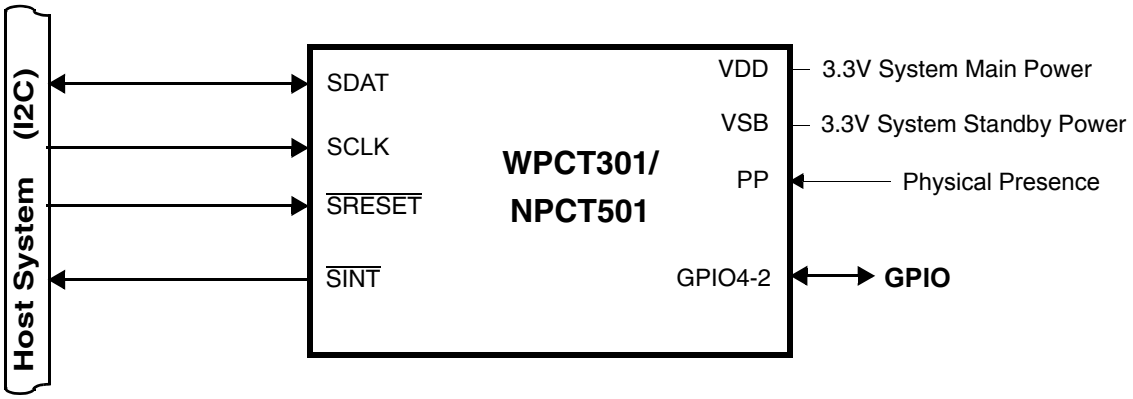


Figure 1. WPCT301/NPCT501 System Connection Diagrams

TPM functions are all integrated on-chip. The major elements of the WPCT301/NPCT501 interface are:

- Host interface based on an I^2C bus, with interrupt request.
- A physical presence input signal (PP) to indicate owner physical presence.
- GPIO signals (GPIO4-2), operated by TCG commands.

2.2 POWER MANAGEMENT (PM)

The WPCT301/NPCT501 has an advanced power management scheme. The wake-up scheme enables the WPCT301/NPCT501 to respond to any kind of event that may require its attention. Power consumption is minimized by dynamically adjusting the internal power modes to the activity required by the host commands and other operations.

The security functions (core and associated peripherals) are supplied by V_{SB} power, which should be connected to the system standby power source (if standby power exists). If the system does not have a standby power source, use the system main power source instead (i.e., connect the system main power source to the VSB pin).

2.3 HOST INTERFACE

The Host Bus Interface is based on a serial interface. This interface fully emulates the TIS registers (as defined in the *TCG PC Client-Specific Specification*.

2.4 RESET

Serial reset performs the following actions:

- Resets host interface state machine.
- Resets the TPM interface host-controlled registers.

3.0 TPM Host Interface

This chapter describes the TPM 1.2-compliant host interface.

3.1 SERIAL TPM INTERFACE PROTOCOL (TSIP)

The WPCT301/NPCT501 TSIP implements the TIS register set accessible through the serial bus (I^2C). The protocol state machine and register layout are implemented as defined in the *TIS Specification*. This section describes the state machine, sending commands to the TPM, reading results from the TPM, error handling, register mapping and communication sequences on the bus.

3.1.1 State Machine, Flow and Timeouts

The state machine follows the definition in Section 11.3.11 (“Status Register”) in the *TIS Specification*.

Use the sequence defined in *TCG PC Client Specific, Device Driver Design Principles, for TCG Version 1.2*, to send or receive command input/output parameters.

The TPM triggers $\overline{\text{SINT}}$ interrupt on the transition to Command Completion state. The $\overline{\text{SINT}}$ is an active-low signal, i.e., it goes low whenever **`TPM_STS.dataAvail`** is set (and **`TPM_STS.valid`** is set), and goes back high when **`TPM_STS.dataAvail`** is cleared.

There are two methods for the host device driver to wait for the command execution to finish:

- Interrupt (recommended) - $\overline{\text{SINT}}$ signal assertion (i.e., transition from high to low) triggers an interrupt in the host interrupt controller, followed by the host issuing the interrupt handler code.
- Polling - Host device driver performs status polling by reading **`TPM_STS`** register to check if **`dataAvail`** bit is set by TPM. In this method, it is recommended to add a delay between the consecutive reads of **`TPM_STS`** register. Table 3 shows the recommended values for delays:

Table 3. Delay Between Consecutive TPM_STS Register Reads During Command Execution State

Duration Since TPM_STS.tpmGo Set	Recommended Delay between Consecutive TPM_STS Reads
0 - 10 msec	2 msec
more than 10 msec	10 msec

When an error occurs (i.e., a timeout is reached) while in Command Reception or Execution states, abort the command at any point by setting **`TPM_STS.commandReady`**. After which the command can be resent.

When an error occurs (timeout is reached) while in Command Completion state, set **`TPM_STS.ResponseRetry`**, This causes the Nuvoton TPM to restart sending command output parameters.

The effects of setting **`TPM_STS.commandReady`** in the different TPM communication states are as follows:

- In Ready state: Ignored - stay in Ready state
- In Idle State: Enter Ready state, within **`TIMEOUT_B`**
- In Command Reception state: This is an **Abort**.
  - The TPM Write FIFO is cleared
  - TPM enters Idle state
  - Command can be resent
- In Command Completion state: This is an **Abort**
  - The TPM Read and Write FIFO are cleared
  - Enter Idle state
- In Command Execution state: This is an **Abort**
  - TPM aborts current command execution
  - The TPM Read and Write FIFO are cleared
  - Enter Idle state

3.0 TPM Host Interface (Continued)

3.1.2 TIS Register Mapping

Table 4 shows the TIS register offset mapping in the TSIP space:

Table 4. TIS Register Offset Mapping in TSIP Space

Offset	Register Name[1]	R/W	Page Size (bytes)	Description
00h	**TPM_STS**	R/W[2]	2	Status Register. Provides TIS status.
20h	**TPM_WR_FIFO**	WO	32	Write this register to send input command parameters during Command Reception state.
40h	**TPM_RD_FIFO**	RO	32	Read this register to receive output command parameters during Command Completion state.
60h	**TPM_DID_VID_RID**	RO	4	Vendor, device and revision ID: - WPCT301: 00FE1050h - NPCT501: 47FE1050h

1. For a detailed description of these registers, see the *TIS Specification.*
2. Offset 0 is R/W while offset 1 (burstCount) is RO.

Any TIS register writing or reading data is processed and **TPM_STS** register updated (including **burstCount** field) on an I^2C STOP condition.

Any part of a command's input parameter write operation to **TPM_WR_FIFO** should start at offset 20h.

Any part of a command's output parameter read operation to **TPM_RD_FIFO** should start at offset 40h.

4.0 Device Specifications

4.1 GENERAL DC ELECTRICAL CHARACTERISTICS

4.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Main 3V Supply Voltage	3.0	3.3	3.6	V
V_{SB}	Standby 3V Supply Voltage	3.0	3.3	3.6	V
T_A	Operating Temperature	0		+70	°C

4.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground (V_{SS}).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply Voltage[1]		-0.3	+4.1	V
V_I	Input Voltage		-0.3	V_{DD} + 0.5	V
V_O	Output Voltage		-0.3	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		-65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V

1. V_{SUP} is V_{DD}, V_{SB}.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

4.1.3 Capacitance

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
C_{IN}	Input Pin Capacitance			4	5	pF
C_{IO}	I/O Pin Capacitance			8	10	pF
C_O	Output Pin Capacitance			6	8	pF

1. T_A = 25°C; f = 1 MHz.

4.0 Device Specifications (Continued)

4.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions[1]	Typ	Max	Unit
I_{DD}	V_{DD} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	5	10	mA
I_{SB}	V_{SB} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V, No Load	20	50	mA
I_{SBLP}	V_{SB} Quiescent Supply Current in Idle Mode[2]	V_{IL} = V_{SS}, V_{IH} = V_{SB}, No Load	300	700	µA

1. All parameters specified for 0°C ≤ T_A ≤ 70°C; V_{DD} and V_{SB} = 3.3V ±10% unless otherwise specified.
2. Device is not performing any operation; no Serial bus activity.

4.0 Device Specifications (Continued)

4.2 DC CHARACTERISTICS OF PINS BY I/O BUFFER TYPES

The tables in this section summarize the DC characteristics of all device pins described in Chapter 1.2 on page 4. The characteristics describe the general I/O buffer types defined in Table 1 on page 4.

4.2.1 Input, TTL Compatible, with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2	V_{SUP}[1]+0.5	V
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_H	Input Hysteresis		300		mV
I_{ILK}[2]	Input Leakage Current	V_{SUP} = 3.0V - 3.6V and 0 < V_{IN} < V_{SUP}		±10	µA
		V_{SUP} = 3.0V - 3.6V and V_{SUP} < V_{IN}		±10	µA

1. V_{SUP} is V_{DD} or V_{SB} according to the power well of the input.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs. For additional conditions, see Section 4.2.5 on page 13.

4.2.2 Input, Reset Pin

Symbol: IN_{RST}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5 V_{DD}	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		–0.3	0.3 V_{DD}	V
I_{ILK}[1]	Input Leakage Current	V_{DD} = 3.0V - 3.6V and 0 < V_{IN} < V_{DD}		±10	µA
		V_{DD} = 3.0V-3.6V and V_{DD}<V_{IN}< V_{DD}+0.5V		±10	µA

1. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs. For additional conditions, see Section 4.2.5 on page 13.

4.2.3 Output, TTL/CMOS Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS Compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –*p* mA	2.4		V
		I_{OH} = –50 µA	V_{SUP}[1] – 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V
I_{OLK}[2]	Output Leakage Current	V_{SUP} = 3.0V - 3.6V and 0 < V_{IN} < V_{SUP}		±10	µA
		V_{SUP} = 3.0V - 3.6V and V_{SUP} < V_{IN} < V_{SUP}+0.5V		±10	µA

1. V_{SUP} is V_{DD} or V_{SB} according to the power well of the input.
2. Output leakage current includes the input leakage of the bidirectional buffers with TRI-STATE outputs. For additional conditions, see Section 4.2.5 on page 13.

4.0 Device Specifications (Continued)

4.2.4 Output, Open Drain Buffer

Symbol: OD_n

Output, Open Drain capable of sinking *n* mA.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V
I_{OLK}[1]	Output Leakage Current	V_{SUP} = 3.0V - 3.6V and 0 < V_{IN} < V_{SUP}		10	µA
		V_{SUP} = 3.0V - 3.6V and V_{SUP} < V_{IN} < V_{SUP}+0.5V		10	µA

1. Output leakage current includes the input leakage of the bidirectional buffers with TRI-STATE outputs. For additional conditions, see Section 4.2.5 on page 13.

4.2.5 Notes and Exceptions

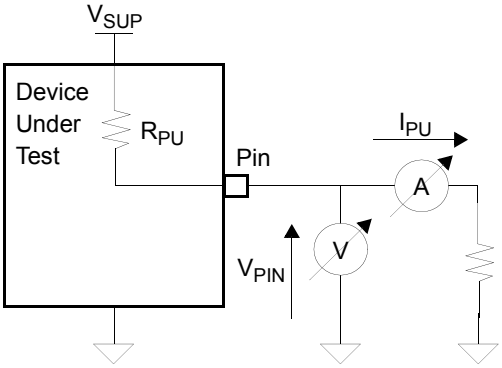
1. I_{ILK} and I_{OLK} are measured in the following cases (where applicable):
   - Internal pull-up or pull-down resistor is disabled
   - Push-pull output buffer is disabled (TRI-STATE mode)
   - Open-drain output buffer is at high level
2. Some pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current from V_{SUP} (when V_{IN} = 0). See Section 1.4 on page 6 for a list of the relevant pins.
3. Some pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to GND (when V_{IN} = V_{SUP}). See Section 1.4 on page 6 for a list of the relevant pins.
4. The following strap pins have an internal static pull-up resistor enabled during Power-Up reset and therefore may have leakage current from V_{SB} (when V_{IN} = 0): SADD, $\overline{TEST}$.
5. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
6. In XOR Tree mode, the buffer type of the input pins included in the XOR tree is IN_T (Input, TTL compatible), regardless of the buffer type of these pins in normal device operation mode.

4.0 Device Specifications (Continued)

4.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit



Pull-Down Resistor Test Circuit

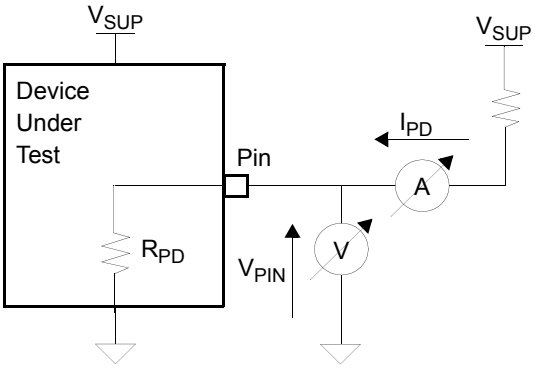
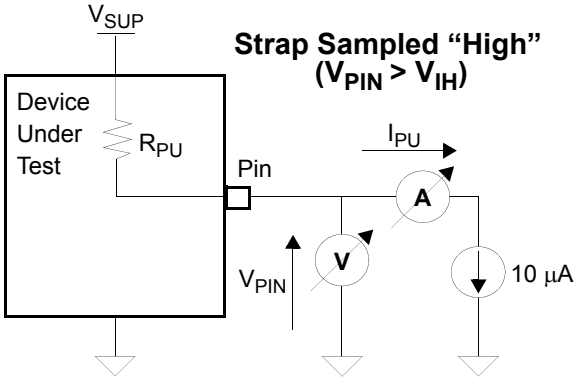


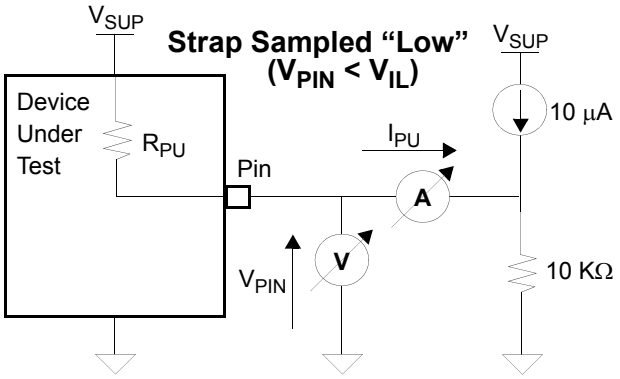
Figure 2. Internal Resistor Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.3V

Internal Pull-Up Strap

Strap Sampled "High" ($V_{PIN} > V_{IH}$)

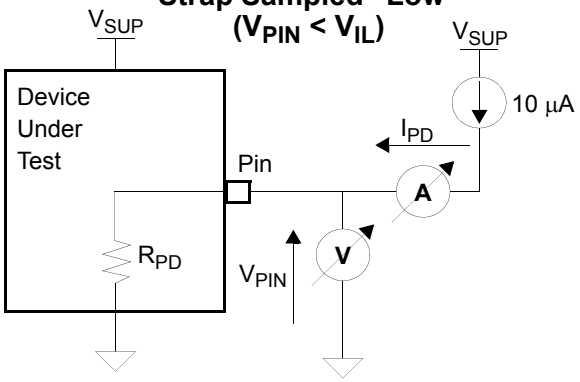


Strap Sampled "Low" ($V_{PIN} < V_{IL}$)



Internal Pull-Down Strap

Strap Sampled "Low" ($V_{PIN} < V_{IL}$)



Strap Sampled "High" ($V_{PIN} > V_{IH}$)

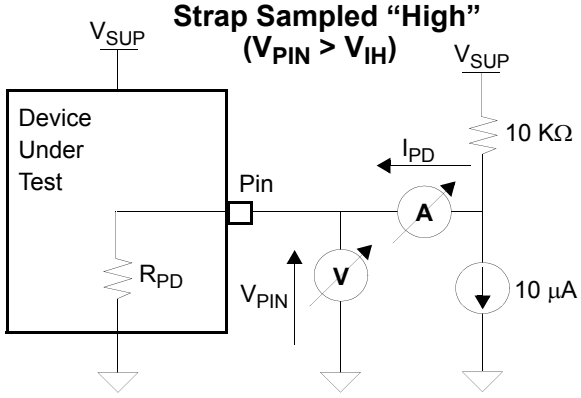


Figure 3. Internal Resistor Design Requirements, T_A = 0°C to 70°C, V_{SUP} = 3.3 V

Notes:

1. V_{SUP} is V_{DD} or V_{SB}, according to the pin power well.
2. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
3. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

4.0 Device Specifications (Continued)

4.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	V_{PIN} = 0V	*nn* – 50%	*nn*	*nn* + 66%	KΩ

1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested; guaranteed by characterization.

4.3.2 Pull-Down Resistor

Symbol: PD_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	V_{PIN} = V_{SUP}	*nn* – 50%	*nn*	*nn* + 120%	KΩ

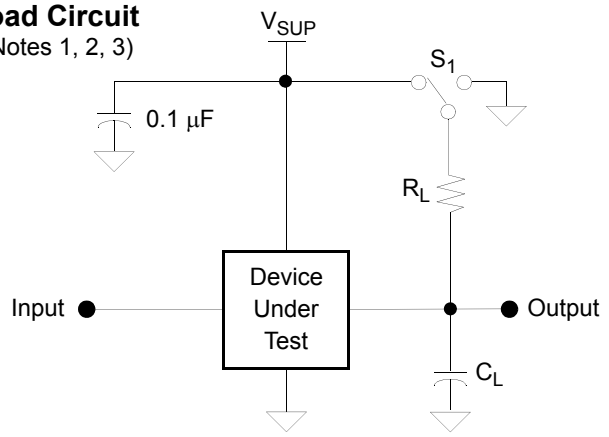
1. TA = 0°C to 70°C, V_{SUP} = 3.3V.
2. Not tested; guaranteed by characterization.

4.0 Device Specifications (Continued)

4.4 AC ELECTRICAL CHARACTERISTICS

4.4.1 AC Test Conditions

Load Circuit
(Notes 1, 2, 3)



AC Testing Input, Output Waveform

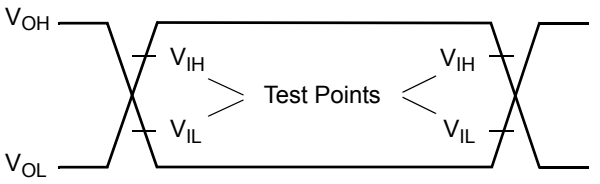


Figure 4. AC Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.0V - 3.6V

Notes:

1. V_{SUP} is V_{DD} or V_{SB} according to the power well of the pin.
2. C_L = 50 pF for all output pins except the following pin groups (values include both jig and oscilloscope capacitance):
   S_1 = Open – for push-pull output pins.
   S_1 = V_{SUP} – for high impedance to active low and active low to high-impedance transition measurements.
   S_1 = GND – for high impedance to active high and active high to high-impedance transition measurements.
   R_L = 1.0 KΩ – for all pins.
3. The following abbreviations are used in Section 4.4: RE = Rising Edge; FE = Falling Edge

Definitions

The timing specifications in this section are relative to V_{IL} or V_{IH} (according to the specific buffer type) on the rising or falling edges of all the signals, as shown in the following figures (unless specifically stated otherwise).

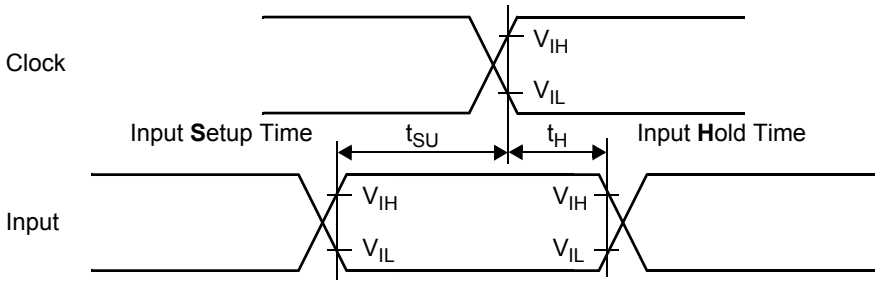


Figure 5. Input Setup and Hold Time

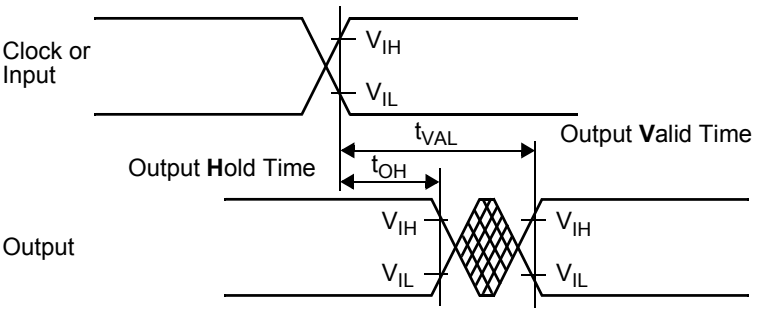


Figure 6. Clock-to-Output and Propagation Delay

4.0 Device Specifications (Continued)

4.4.2 Reset Timing

Power-Up Reset

Symbol	Description	Reference Conditions	Min[1]	Max[2]
t_{SB2DD}	Time between standby and main supply voltage	Before end of reset	0 ms	
t_{SRST}	$\overline{\text{SRESET}}$ active time	V_{DD} power-up to end of $\overline{\text{SRESET}}$	10 ms	
t_{PLV}	Strap valid time	Before end of reset	10 ms	
t_{EPLV}	External strap pull-down resistor, valid time	Before end of reset	10 ms	

1. Not Tested; Guaranteed by design.
2. Not Tested; Guaranteed by design.

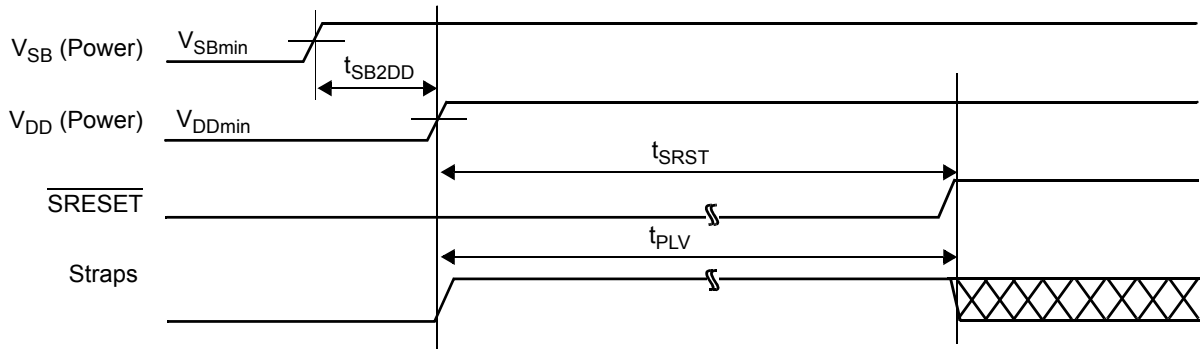


Figure 7. Power-Up Reset

4.0 Device Specifications (Continued)

4.4.3 I²C Timing

Symbol	Description	Min		Max		Units
		WPCT 301	NPCT 501	WPCT 301	NPCT 501	
f_{SCL}	Clock frequency, SCL	50	50	100[1]	400[2]	KHz
t_{LOW}	Clock pulse width, low	4.7	1.1			µs
t_{HIGH}	Clock pulse width, high	4.0	1.0			µs
t_{BUF}	Time that the bus must be available before the start of a new transmission	4.7	1.1			µs
$t_{HD.STA}$	Start hold time	4.0	1.0			µs
$t_{SU.STA}$	Start setup time	4.7	1.1			µs
$t_{HD.DAT}$	Data in hold time	0	0			µs
$t_{SU.DAT}$	Data in setup time	200	200			ns
t_R	Input rise time			1000	250	ns
t_F	Input fall time			300	250	ns
$t_{SU.STO}$	Stop setup time	4.7	1.1			µs
t_{DH}	Data out hold time	300	300			ns
t_{WR}	Write/read cycle time			20	20	µs
$t_{INIT.STA}$	Start condition after V_{SB} power-up	100	100			ms
$t_{RST.STA}$	Start condition after $\overline{SRESET}$ deassertion	30	30			ms

1. Test conditions: R_L = 1 KΩ to V_{DD}=3.3V, C_L = 400 pF to GND
2. Test conditions for 100 KHz: R_L = 1 KΩ to V_{DD}=3.3V, C_L = 400 pF to GND;
   Test conditions for 400 KHz: R_L = 1 KΩ to V_{DD}=3.3V, C_L = 100 pF to GND

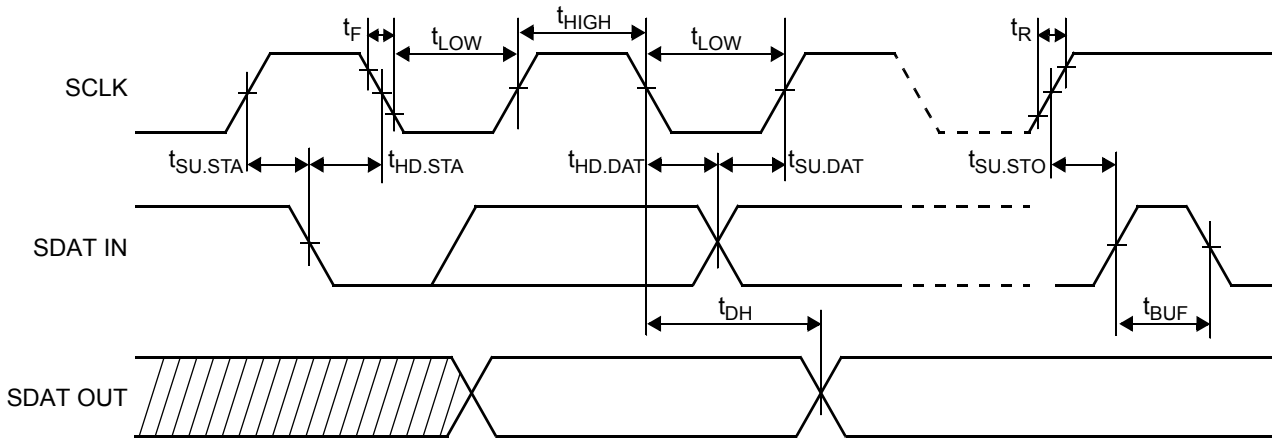
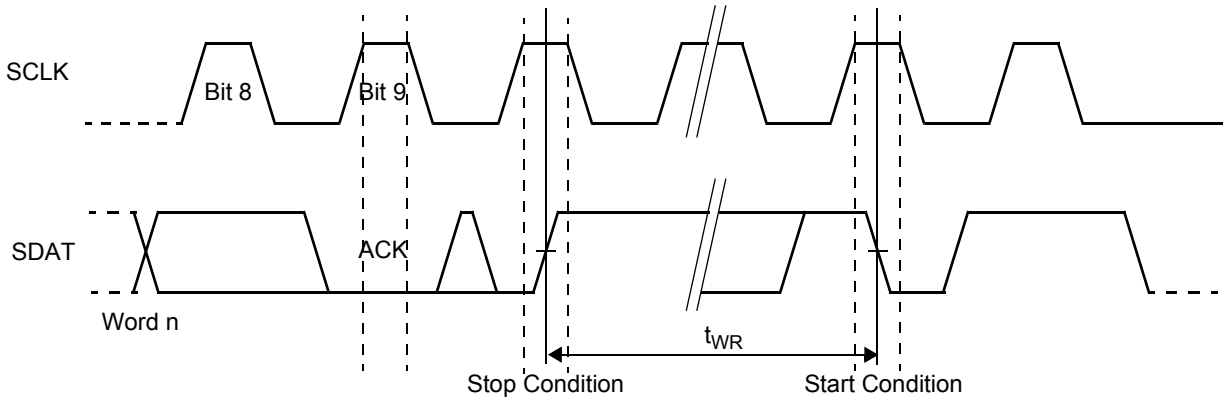


Figure 8. Bus Timing

4.0 Device Specifications (Continued)



Note: Write/read cycle time (t_{WR}) = the time from a valid write/read sequence stop condition until the end of an internal operation.

Figure 9. Cycle, Start, Stop and Acknowledge Timing

4.0 Device Specifications (Continued)

4.5 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees C/W) $Theta_{JC}$ and $Theta_{JA}$ values for the WPCT301/NPCT501 packages are as follows:

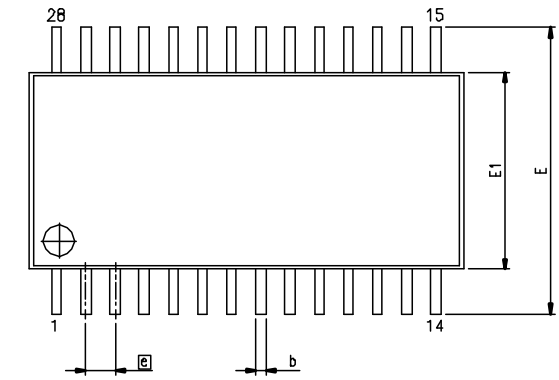
Table 5. Theta (Θ) J Values

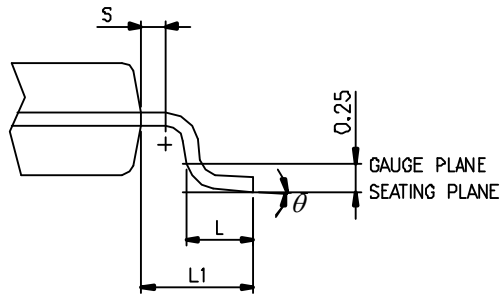
Package Type	$Theta_{JA}$@0 lfpm	$Theta_{JA}$@150 lfpm	$Theta_{JA}$@250 lfpm	$Theta_{JA}$@500 lfpm	$Theta_{JC}$
TSSOP28	29	27	25	23	10

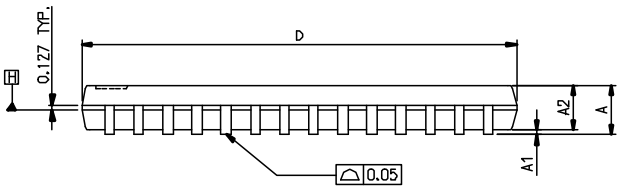
Note: Airflow for $Theta_{JA}$ values is measured in linear feet per minute (lfpm).

Physical Dimensions

All dimensions are in millimeters.







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

28-Pin Thin Shrink Small Outline Package (TSSOP28), JEDEC
Order Numbers: WPCT301AA0WX
NPCT501AA0WX
NPCT501MA0WX

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Headquarters
No. 4, Creation Rd. 3,
Science-Based Industrial Park,
Hsinchu, Taiwan, R.O.C
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.nuvoton.com.tw (Chinese)
http://www.nuvoton.com (English)

Nuvoton Technology Corporation America
2727 North First Street,
San Jose, CA 95134, U.S.A.
TEL: 1-408-544-1718
FAX: 1-408-544-1787

Nuvoton Technology (Shanghai) Ltd.
27F, 2299 Yan An W. Rd.
Shanghai, 200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-2658-8066
FAX: 886-2-8751-3579

Winbond Electronics Corporation Japan
NO. 2 Ueno-Bldg., 7-18, 3-chome
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Nuvoton Technology (H.K.) Ltd.
Unit 9-15, 22F, Millennium City 2,
378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

For Advanced PC Product Line information contact: APC.Support@nuvoton.com