

WPM3401

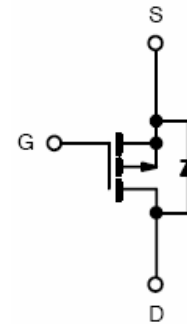
P-Channel Enhancement Mode MOSFET

<http://www.jestek.com.cn>

Description

The WPM3401 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

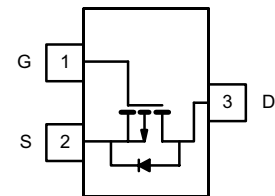
This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.



P-Channel MOSFET

Features

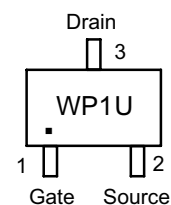
- -30V/-4.3A, RDS(ON) < 65mΩ @ VGS = -10V
- -30V/-3.4A, RDS(ON) < 90mΩ @ VGS = -4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT23 package design



Top View

Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch



U = Date Code
WP1 = Specific Device Code

Order information

Part Number	Package	Shipping
WPM3401-3/TR	SOT23	3000 Tape&Reel

Absolute Maximum Ratings (TA=25 °C unless otherwise specified)

Parameter	Symbol			Value	Unit
V _{DS}	Drain-Source voltage			-30	V
V _{GS}	Gate-Source Voltage			±20	V
I _D	Continuous Drain Current	Steady-State	TA=25°C	-4.3	A
		Steady-State	TA=70°C	-3.4	
I _{DM}	Pulse Drain Current			-20	A
P _D	Power Dissipation	TA=25°C		2.8	W
		TA=70°C		1.8	
T _J	Operating Junction Temperature Range			-55~150	°C
T _{stg}	Storage Temperature Range				
R _{θJA}	Thermal Resistance-Junction to Ambient			70	°C/W

Electrical Characteristics

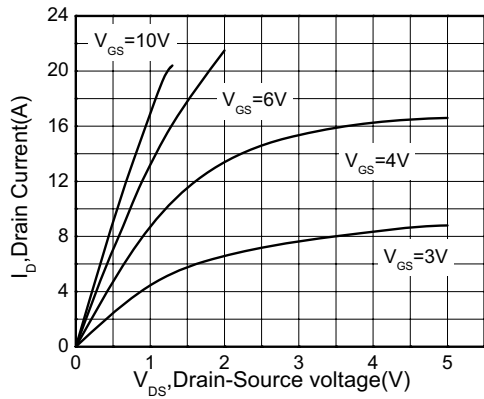
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.8	-1.37	-2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	uA
		V _{DS} =-30V, V _{GS} =0V T _J =85°C			-5	
On-State Drain Current	I _{D(on)}	V _{DS} = -5V, V _{GS} =-4.5V	-10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-7.2A		0.055	0.065	Ω
		V _{GS} =-4.5V, I _D =-5.0A		0.076	0.090	
Forward Transconductance	g _{fs}	V _{DS} =-15V, I _D =-5.7A		13		S
Diode Forward Voltage	V _{SD}	I _S =-1.3A, V _{GS} =0V		-0.72	-1.0	V

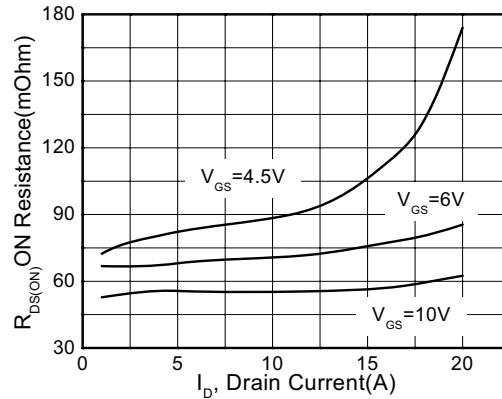
Dynamic

Total Gate Charge	Q _g	V _{DS} =-15V, V _{GS} =-10V I _D = -3.5A		14	18	nC
Gate-Source Charge	Q _{gs}			3.1		
Gate-Drain Charge	Q _{gd}			3		
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V f=1MHz		700		pF
Output Capacitance	C _{oss}			120		
Reverse Transfer Capacitance	C _{rss}			75		
Turn-On Time	t _{d(on)}	V _{DD} =-15V, R _L =15Ω I _D =-1.0A, V _{GEN} =-10V R _G =6Ω		8	18	nS
	t _r			5	18	
Turn-Off Time	t _{d(off)}			28	50	
	t _f			13	35	

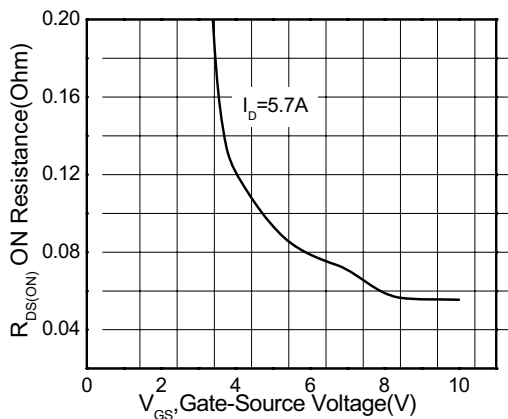
Typical Performance Characteristics



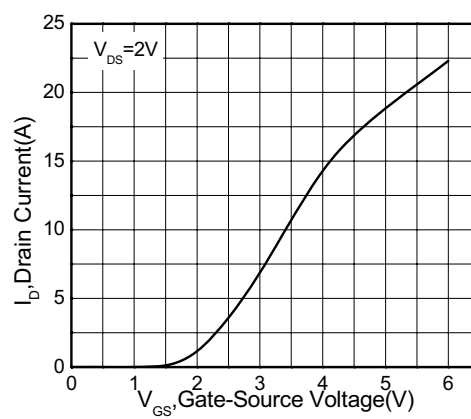
Drain Current VS Drain-Source voltage



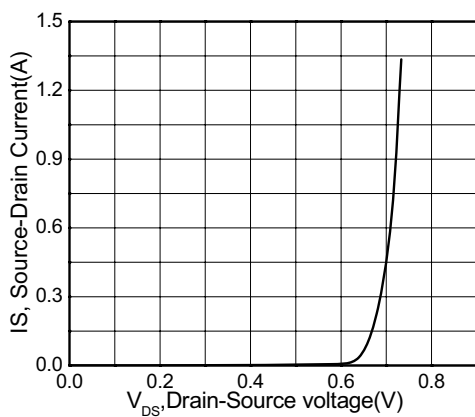
Drain Current vs ON Resistance



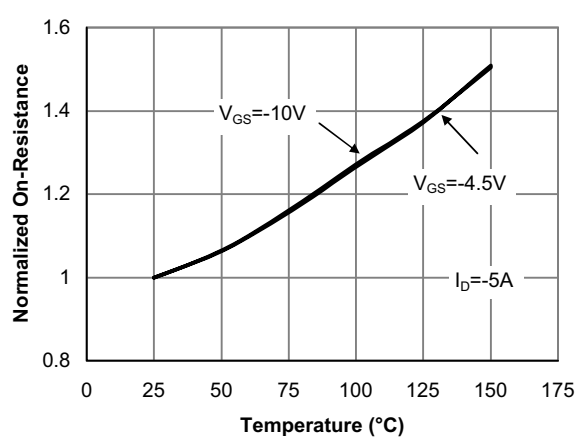
Gate-Source Voltage vs ON Resistance



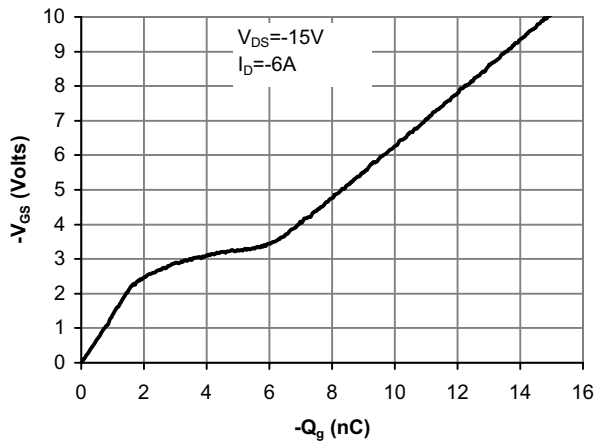
Drain Current VS Gate-Source Voltage



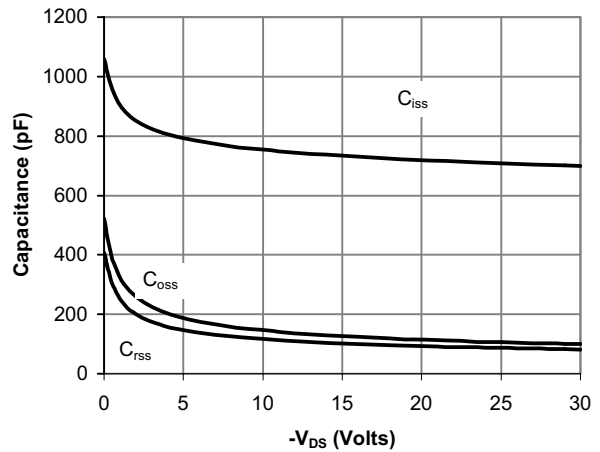
Drain Current VS Source-Drain Current



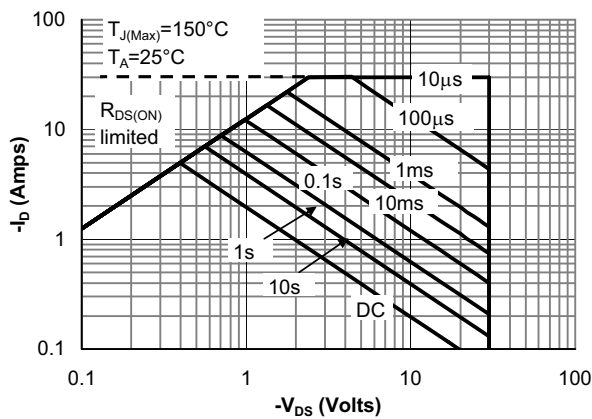
On-Resistance vs. Junction



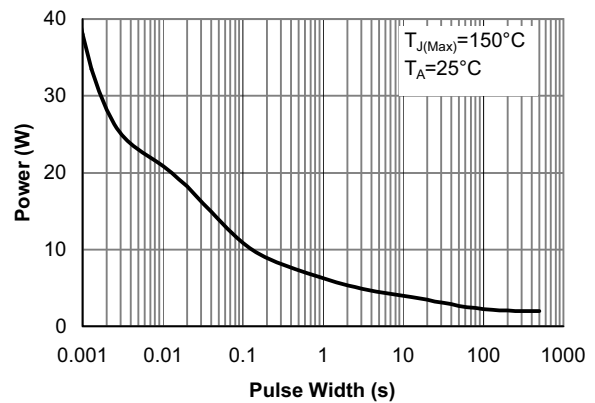
Gate-Charge Characteristics



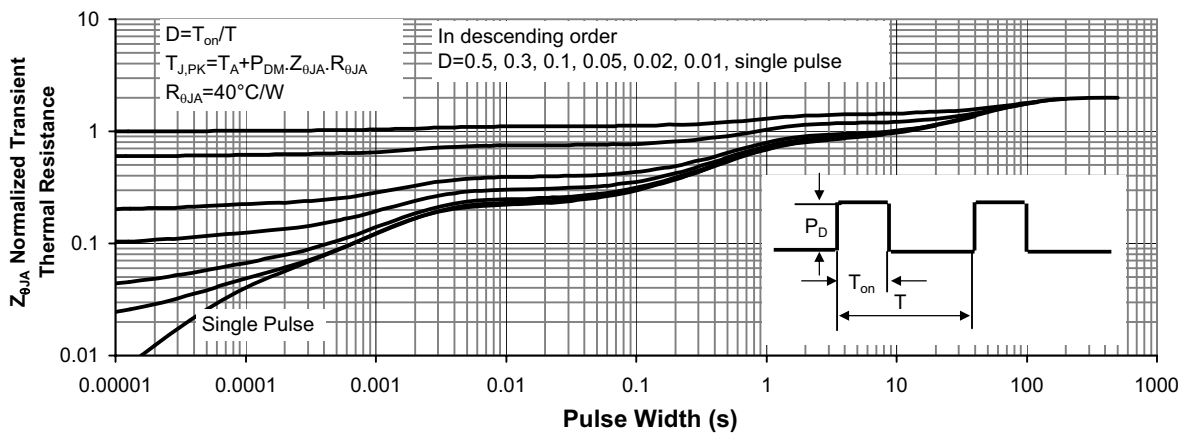
Capacitance Characteristics



Maximum Forward Biased Safe Operating Area (Note E)



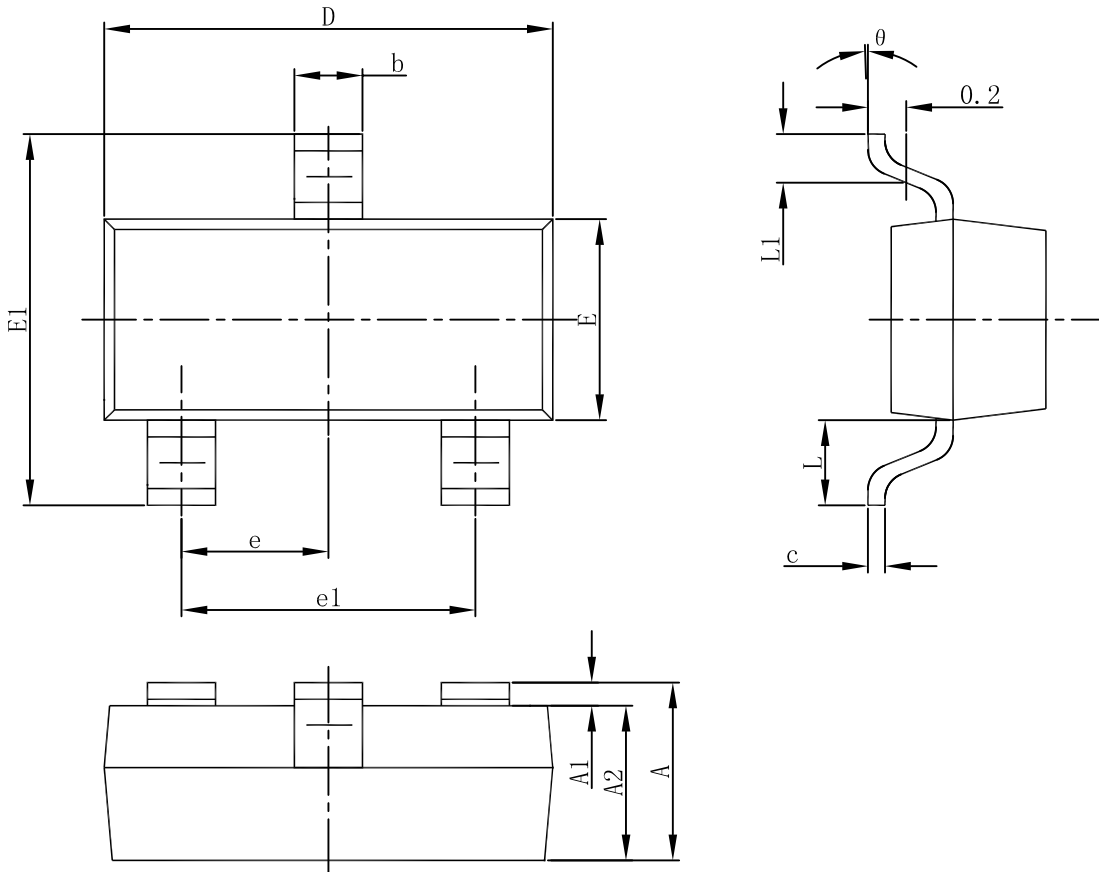
Single Pulse Power Rating Junction-to-Ambient (Note E)



Normalized Maximum Transient Thermal Impedance

Packaging Information

SOT23 Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.047
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.043
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°