# 512Kx16 SRAM MODULE

## FEATURES

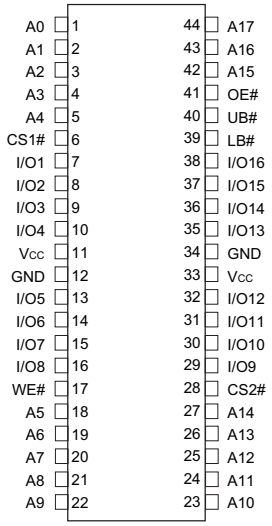
- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 44 pin Ceramic SOJ (Package 102)
  - 44 lead Ceramic Flatpack (Package 209)
- Organized as two banks of 256Kx16
- Data Byte Control:
  Lower Byte (LB#) = I/O1-8
  Upper Byte (UB#) = I/O9-16
- Data I/O Compatible with 3.3V devices
- 2V Minimum Data Retention for battery back up operation
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply (3.3V parts also available)
- Low Power CMOS
- TTL Compatible Inputs and Outputs

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

## PIN CONFIGURATION FOR WS512K16-XXX

### 44 CSOJ
### 44 FLATPACK

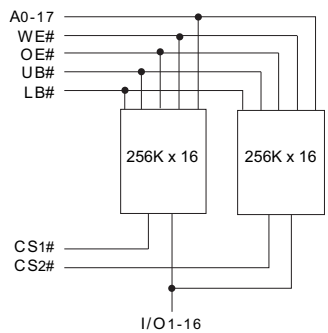
**Top View**




### Pin Description

| | |
|---|---|
| A0-17 | Address Inputs |
| LB# | Lower-Byte Control (I/O1-8) |
| UB# | Upper-Byte Control (I/O9-16) |
| I/O1-16 | Data Input/Output |
| CS1-2# | Chip Select |
| OE# | Output Enable |
| WE# | Write Enable |
| Vcc | +5.0V Power |
| GND | Ground |
| NC | No Connection |

### Block Diagram



## TRUTH TABLE

| CS1# | CS2# | WE# | OE# | LB# | UB# | Mode | Data I/O | | Power |
|---|---|---|---|---|---|---|---|---|---|
| H | H | X | X | X | X | Not Select | I/O1-8 | I/O9-16 | Standby |
| L | H | H | H | X | X | Output Disable | High Z | High Z | Active |
| H | L | | | | | | | | |
| L | H | X | X | H | H | | | | |
| H | L | | | | | | | | |
| H | L | H | L | L | H | Read | Data Out | High Z | Active |
| L | H | | | H | L | | High Z | Data Out | |
| | | | | L | L | | Data Out | Data Out | |
| H | L | L | H | L | H | Write | Data In | High Z | Active |
| L | H | | | H | L | | High Z | Data In | |
| | | | | L | L | | Data In | Data In | |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | $V_{CC}$+0.5 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 7.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |
| Opertating Temp. (MIL) | $T_A$ | -55 | +125 | °C |

## CAPACITANCE

$T_A$ = +25°C

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0V, f = 1.0 MHz | 25 | pF |
| Output capacitance | $C_{OUT}$ | $V_{OUT}$ = 0V, f = 1.0 MHz | 25 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

$V_{CC}$ = 5.0V, $V_{SS}$ = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter | Sym | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | CS# = $V_{IH}$, OE# = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | µA |
| Operating Supply Current | $I_{CC}$ | CS# = $V_{IL}$, OE# = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 290 | mA |
| Standby Current | $I_{SB}$ | CS# = $V_{IH}$, OE# = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 30 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA, $V_{CC}$ = 4.5 | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA, $V_{CC}$ = 4.5 | 2.4 | | V |

NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V

## DATA RETENTION CHARACTERISTICS

-55°C ≤ $T_A$ ≤ +125°C

| Characteristic | Sym | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Data Retention Supply Voltage | $V_{DR}$ | CS# ≥ $V_{CC}$ -0.2V | 2.0 | | 5.5 | µA |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3V | | 2.0 | 12.0* | mA |

* Also available in Low Power version. Please call factory for informaion.

## AC CHARACTERISTICS

$V_{CC}$ = 5.0V, GND = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter<br>Read Cycle | Symbol | -17 | | -20 | | -25 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 17 | | 20 | | 25 | | 35 | | ns |
| Address Access Time | $t_{AA}$ | | 17 | | 20 | | 25 | | 35 | ns |
| Output Hold from Address Change | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | $t_{ACS}$ | | 17 | | 20 | | 25 | | 35 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 10 | | 12 | | 15 | | 20 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 2 | | 5 | | 5 | | 5 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 9 | | 10 | | 12 | | 15 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 9 | | 10 | | 12 | | 15 | ns |
| LB#, UB# Access Time | $t_{BA}$ | | 10 | | 12 | | 14 | | 17 | ns |
| LB#, UB# Enable to Low Z Output | $t_{BLZ1}$ | 0 | | 0 | | 0 | | 0 | | ns |
| LB#, UB# Disable to High Z Output | $t_{BHZ1}$ | | 9 | | 10 | | 12 | | 15 | ns |

1. This parameter is guaranteed by design but not tested.

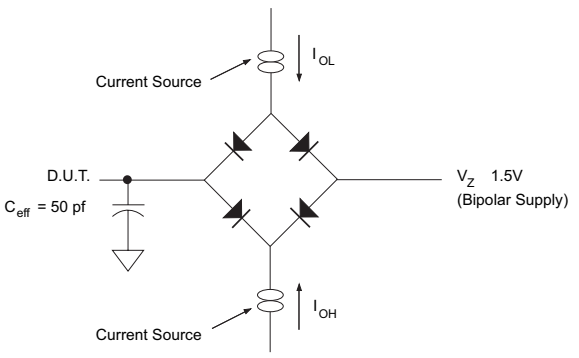
## AC CHARACTERISTICS

$V_{CC}$ = 5.0V, GND = 0V, -55°C ≤ $T_A$ ≤ +125°C

| Parameter<br>Write Cycle | Symbol | -17 | | -20 | | -25 | | -35 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 17 | | 20 | | 25 | | 35 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 14 | | 17 | | 20 | | 25 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 14 | | 17 | | 20 | | 25 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 10 | | 12 | | 15 | | 20 | | ns |
| Write Pulse Width | $t_{WP}$ | 14 | | 17 | | 20 | | 25 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | $t_{OW}$[1] | 0 | | 0 | | 0 | | 0 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | | 9 | | 10 | | 10 | | 15 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| LB#, UB# Valid to End of Write | $t_{BW}$ | 14 | | 17 | | 20 | | 25 | | ns |

1. This parameter is guaranteed by design but not tested.

## AC TEST CIRCUIT

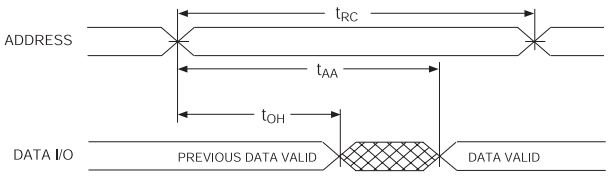



### AC Test Conditions

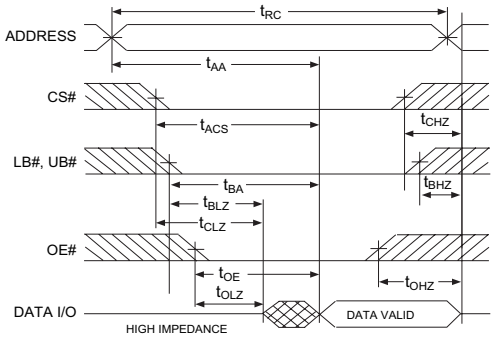
| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

Notes:
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## TIMING WAVEFORM – READ CYCLE

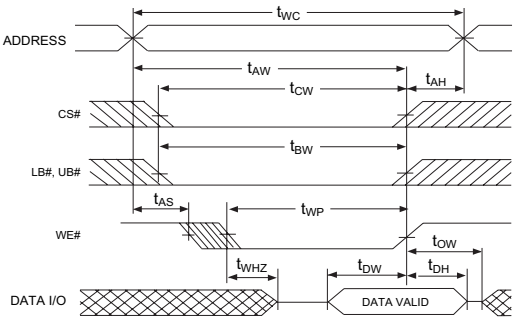



READ CYCLE 1, (CS# = OE# = $V_{IL}$, UB# or LB# = $V_{IL}$, WE# = $V_{IH}$)



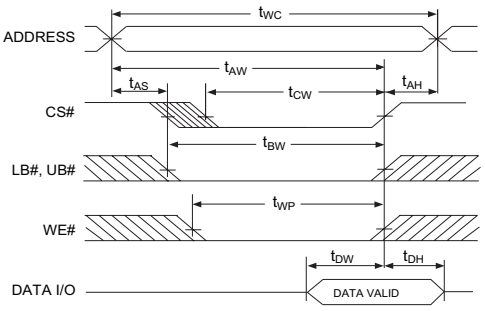

READ CYCLE 2 (WE# = $V_{IH}$)

## WRITE CYCLE – WE# CONTROLLED



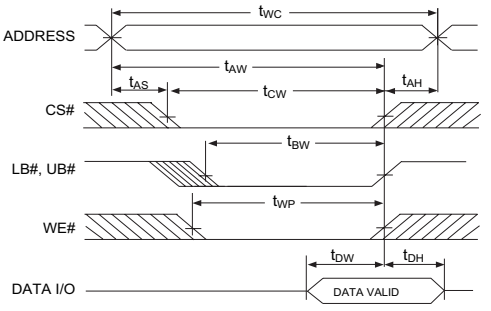

WRITE CYCLE 1, WE# CONTROLLED

## WRITE CYCLE – CS# CONTROLLED



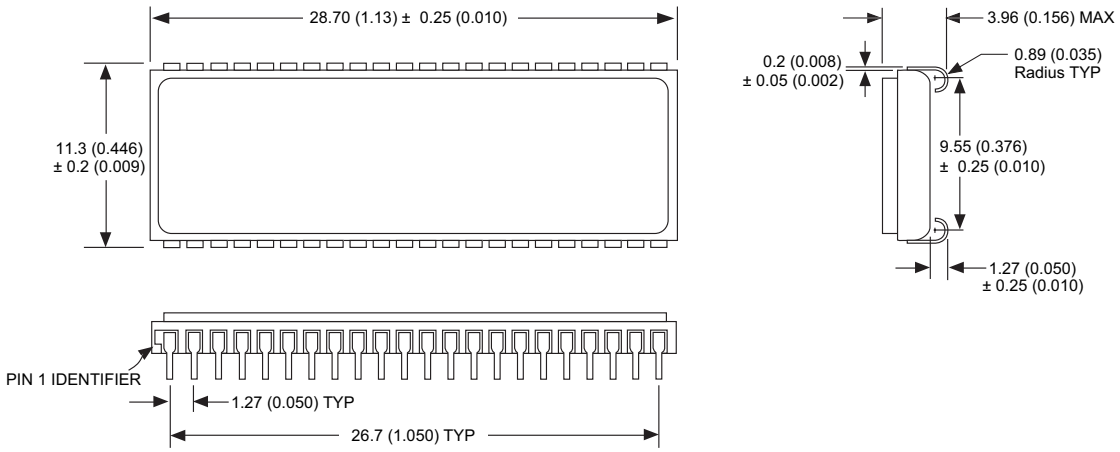

WRITE CYCLE 2, CS# CONTROLLED

## WRITE CYCLE – LB#, UB# CONTROLLED



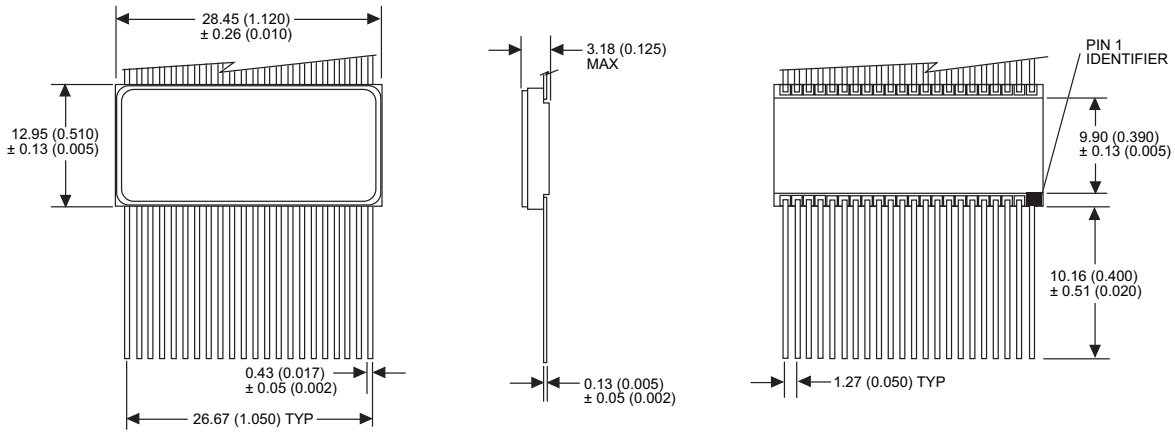

WRITE CYCLE 3, LB#, UB# CONTROLLED

## PACKAGE 102: 44 LEAD, CERAMIC SOJ




ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## PACKAGE 209: 44 LEAD, CERAMIC FLAT PACK

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## ORDERING INFORMATION