



High Speed Super Low Power SRAM

8K-Word By 8 Bit

WS6264

■ GENERAL DESCRIPTION

The WS6264 is a high performance, high speed and super low power CMOS Static Random Access Memory organized as 8,192 words by 8bits and operates from a single 4.5V to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 70ns in 5.0V operation. Easy memory expansion is provided by using two chip enable inputs (/CE1, CE2) and active LOW output enable (/OE).

The WS6264 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The WS6264 is available in JEDEC standard 28-pin SOP(300 mil) and PDIP (600 mil) packages.

■ FEATURES

- Operation voltage : 4.5 ~ 5.5V
- Ultra low power consumption:
Operating current 1mA@1MHz & CMOS standby current 1.0uA (Typ.) in Vcc=5.0V
- High speed access time: 70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 2.0V.
- Easy expansion with /CE1, CE2 and /OE options.

■ PRODUCT FAMILY

| Product Family | Operating Temp. | Vcc Range | Speed (ns) | Standby Current (Typ.) I _{CCSB1} | Package Type |
|----------------|-----------------|-----------|------------|--|--------------|
| WS6264LLFP | 0~70°C | 4.5~5.5V | 70 | 1.0uA | 28 SOP |
| WS6264LLP | | | | | 28 PDIP |
| WS6264LLFPI | -40~85°C | | 70 | 1.0uA | 28 SOP |
| WS6264LLPI | | | | | 28 PDIP |

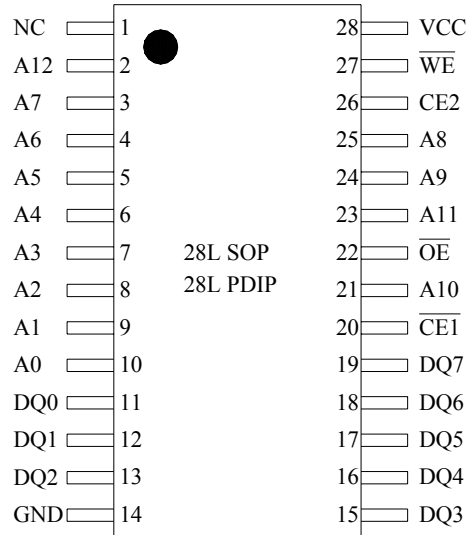


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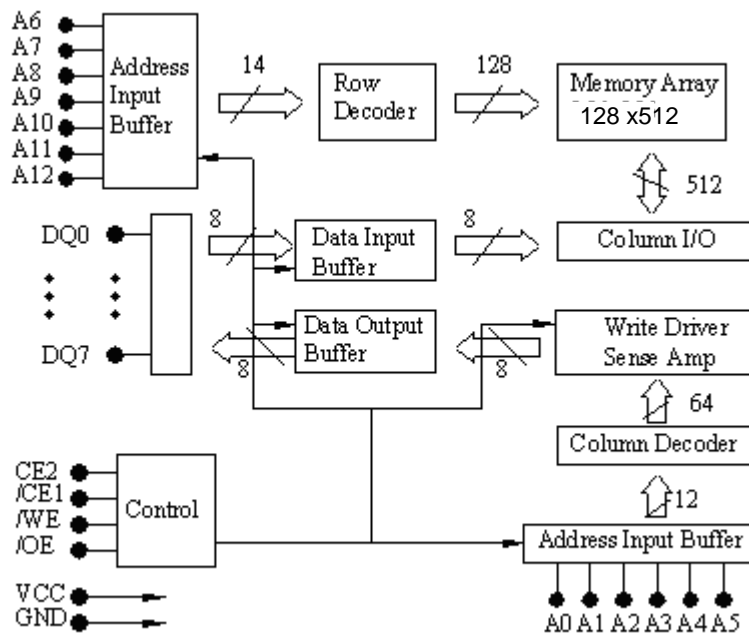
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■ PIN CONFIGURATIONS



■ FUNCTIONAL BLOCK DIAGRAM





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■ PIN DESCRIPTIONS

| Name | Type | Function |
|-----------------|-------|--|
| A0 – A12 | Input | Address inputs for selecting one of the 8,192 x 8 bit words in the RAM |
| /CE1,CE2 | Input | /CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected. |
| /WE | Input | The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location. |
| /OE | Input | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive. |
| DQ0~DQ7 | I/O | These 8 bi-directional ports are used to read data from or write data into the RAM. |
| Vcc | Power | Power Supply |
| Gnd | Power | Ground |
| NC | | No connection |

■ TRUTH TABLE

| MODE | /CE1 | CE2 | /WE | /OE | DQ0~7 | Vcc Current |
|-----------------------|------|-----|-----|-----|------------------|--|
| Standby | H | X | X | X | High Z | I _{CCSB} , I _{CCSB1} |
| | X | L | X | X | | |
| Output Disable | L | H | H | H | High Z | I _{CC} |
| Read | L | H | H | L | D _{OUT} | I _{CC} |
| Write | L | H | L | X | D _{IN} | I _{CC} |



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■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Rating | Unit |
|------------|--------------------------------------|----------------------|------|
| V_{TERM} | Terminal Voltage with Respect to GND | -0.5 to $V_{CC}+0.5$ | V |
| T_{BIAS} | Temperature Under Bias | -40 to +125 | °C |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| P_T | Power Dissipation | 1.0 | W |
| I_{OUT} | DC Output Current | 50 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|------------|
| Commercial | 0~70°C | 4.5 ~ 5.5V |
| Industrial | -40~85°C | 4.5 ~ 5.5V |

■ CAPACITANCE⁽¹⁾($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

| Symbol | Parameter | Conduction | MAX. | Unit |
|----------|--------------------------|---------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN}=0V$ | 8 | pF |
| C_{DQ} | Input/Output Capacitance | $V_{DI/O}=0V$ | 10 | pF |

1. This parameter is guaranteed, and not 100% tested.



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■ **DC ELECTRICAL CHARACTERISTICS** ($T_A = 0^\circ \sim 70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

| Name | Parameter | Test Condition | MIN | TYP ⁽¹⁾ | MAX | Unit |
|--------------------------|--|--|------|--------------------|--------------|-----------|
| V_{IL} | Guaranteed Input Low Voltage ⁽²⁾ | $V_{CC}=5.0\text{V}$ | -0.5 | | 0.8 | V |
| V_{IH} | Guaranteed Input High Voltage ⁽²⁾ | $V_{CC}=5.0\text{V}$ | 2.2 | | $V_{CC}+0.5$ | V |
| I_{IL} | Input Leakage Current | $V_{CC}=\text{MAX}$, $V_{IN}=0$ to V_{CC} | -1 | | 1 | uA |
| I_{OL} | Output Leakage Current | $V_{CC}=\text{MAX}$, /CE1= V_{IH} , or CE2= V_{IL} , or /OE= V_{IH} , or /WE= V_{IL} $V_{IO}=0\text{V}$ to V_{CC} | -1 | | 1 | uA |
| V_{OL} | Output Low Voltage | $V_{CC}=\text{MAX}$, $I_{OL} = 1\text{mA}$ | | | 0.4 | V |
| V_{OH} | Output High Voltage | $V_{CC}=\text{MIN}$, $I_{OH} = -1\text{mA}$ | 2.4 | | | V |
| I_{CC} | Operating Power Supply Current | /CE1= V_{IL} , $I_{DQ}=0\text{mA}$, $F=F_{\text{MAX}}=1/t_{RC}$ | | | 30 | mA |
| I_{CCSB} | TTL Standby Supply | /CE1= V_{IH} , $I_{DQ}=0\text{mA}$, | | | 10 | mA |
| I_{CCSB1} | CMOS Standby Current | /CE1 $\geq V_{CC}-0.2\text{V}$, CE2= 0.2V , $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$, | | 1 | 10 | uA |

1. Typical characteristics are at $T_A = 25^\circ\text{C}$.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.



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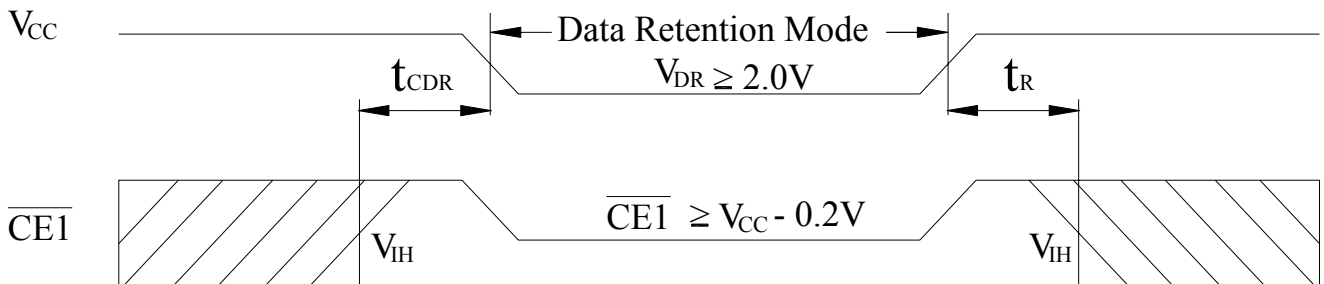
DATA RETENTION CHARACTERISTICS (TA = 0° ~70°C, VCC = 5.0V)

| Name | Parameter | Test Condition | MIN | TYP ⁽¹⁾ | MAX | Unit |
|-------------------|--------------------------------------|---|---------------------|--------------------|-----|------|
| V _{DR} | V _{CC} for Data Retention | /CE1 ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V | 2.0 | | | V |
| I _{CCDR} | Data Retention Current | /CE1 ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V | | 0.5 | 5 | uA |
| T _{CDR} | Chip Deselect to Data Retention Time | Refer to Retention Waveform | 0 | | | ns |
| t _R | Operation Recovery Time | | t _{RC} (2) | | | ns |

1. TA = 25°C

2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM(1) (/CE1 Controlled)



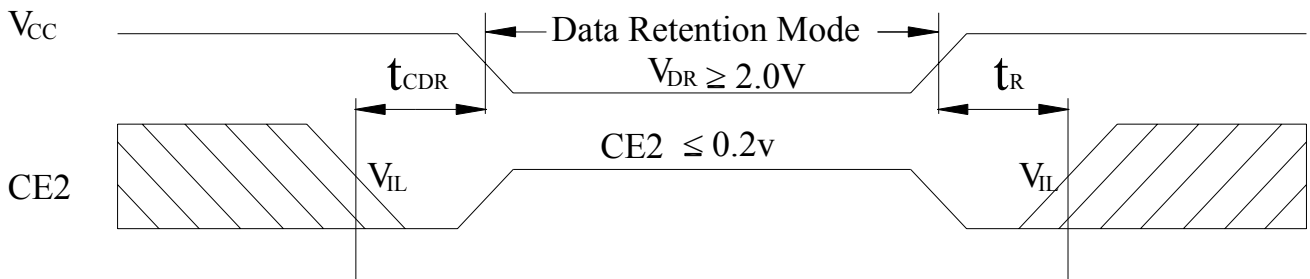


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■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



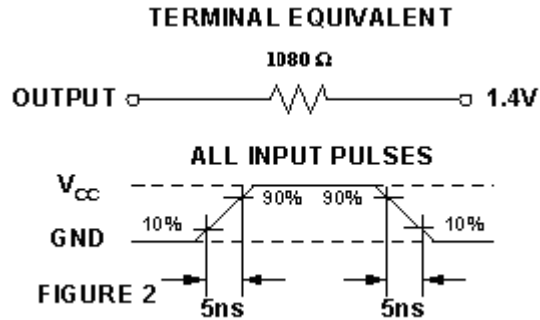
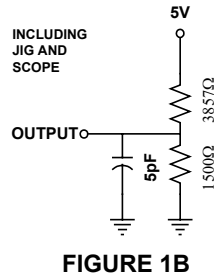
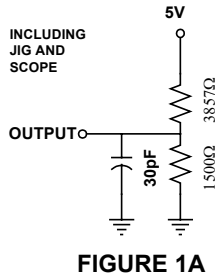
■ AC TEST CONDITIONS

| | |
|---|----------------------|
| Input Pulse Levels | V _{CC} /0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Level | 0.5V _{CC} |
| Output Load | See FIGURE 1A and 1B |

■ KEY TO SWITCHING WAVEFORMS

| WAVEFORMS | INPUTS | OUTPUTS |
|-----------|---------------------------------|---|
| | MUST BE STEADY | MUST BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGE FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGE FROM L TO H |
| | DON'T CARE ANY CHANGE PERMITTED | CHANGE STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE OFF STATE |

AC TEST LOADS AND WAVEFORMS



AC ELECTRICAL CHARACTERISTICS (0°C~70°C ; V_{CC}=5V)

< READ CYCLE >

| JEDEC Name | Symbol | Description | -70 | | Unit |
|-------------------|---------------------------------|------------------------------------|-----|-----|------|
| | | | MIN | MAX | |
| t _{AVAX} | t _{RC} | Read Cycle Time | 70 | | ns |
| t _{AVQV} | t _{AA} | Address Access Time | | 70 | ns |
| t _{ELQV} | t _{ACE} | Chip Select Access Time | | 70 | ns |
| t _{GLQV} | t _{OE} | Output Enable to Output Valid | | 40 | ns |
| t _{ELQX} | t _{CLZ} ⁽⁵⁾ | Chip Select to Output Low Z | 10 | | ns |
| t _{GLQX} | t _{OLZ} ⁽⁵⁾ | Output Enable to Output in Low Z | 5 | | ns |
| t _{EHQZ} | t _{CHZ} ⁽⁵⁾ | Chip Deselect to Output in High Z | 0 | 35 | ns |
| t _{GHQZ} | t _{OHZ} ⁽⁵⁾ | Output Disable to Output in High Z | 0 | 30 | ns |
| t _{AXOX} | t _{OH} | Address Change to Out Disable | 10 | | ns |



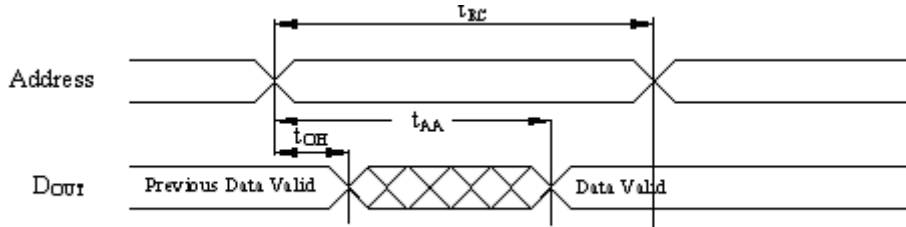
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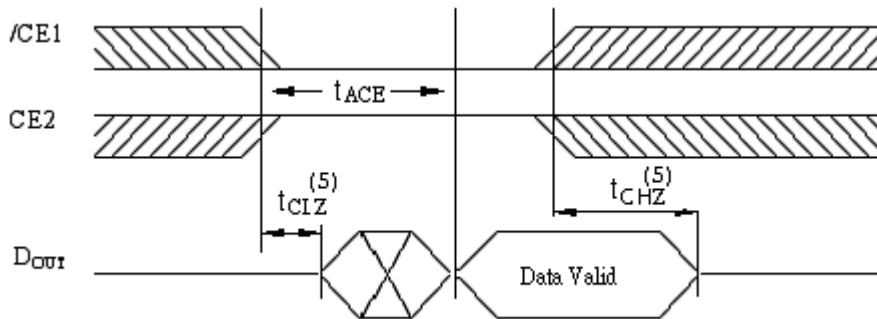
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SWITCHING WAVEFORMS (READ CYCLE)

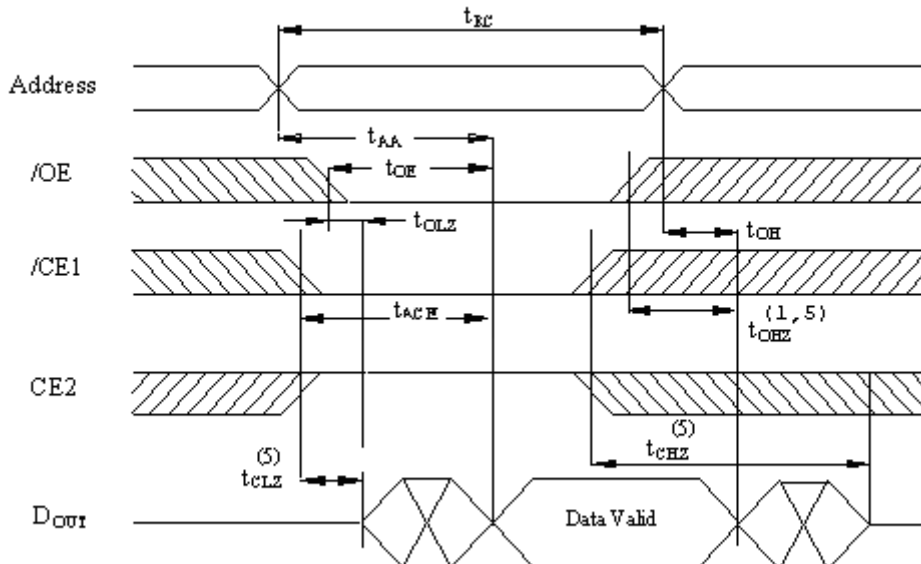
READ CYCLE 1 [1,2,4]



READ CYCLE 2 [1,3,4]



READ CYCLE 3 [1,4]





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NOTES:

1. /WE is high in read Cycle.
2. Device is continuously selected when /CE1 = V_{IL} and CE2=V_{IH}.
3. Address valid prior to or coincident with /CE1 transition low and /or CE2 transition high.
4. /OE = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

■ **AC ELECTRICAL CHARACTERISTICS (0°C~70°C ; V_{CC}=5V)**
< WRITE CYCLE >

| JEDEC Name | Symbol | Description | -70 | | Unit |
|--------------------|----------------------------------|------------------------------------|-----|-----|------|
| | | | MIN | MAX | |
| t _{AVAX} | t _{WC} | Write Cycle Time | 70 | | ns |
| t _{E1LWH} | t _{CW} | Chip Select to End of Write | 70 | | ns |
| t _{AVWL} | t _{AS} | Address Setup Time | 0 | | ns |
| t _{AVWH} | t _{AW} | Address Valid to End of Write | 70 | | ns |
| t _{WLWH} | t _{WP} | Write Pulse Width | 50 | | ns |
| t _{WHAX} | t _{WR} | Write Recovery Time | 0 | | ns |
| t _{WLQZ} | t _{WHZ} ⁽¹⁰⁾ | Write to Output in High Z | | 35 | ns |
| t _{DVWH} | t _{DW} | Data to Write Time Overlap | 40 | | ns |
| t _{WHDX} | t _{DH} | Data Hold for Write End | 0 | | ns |
| t _{GHQZ} | t _{OHZ} ⁽¹⁰⁾ | Output Disable to Output in High Z | 0 | 30 | ns |
| t _{WHOX} | t _{OW} ⁽¹⁰⁾ | End of Write to Output Active | 5 | | ns |



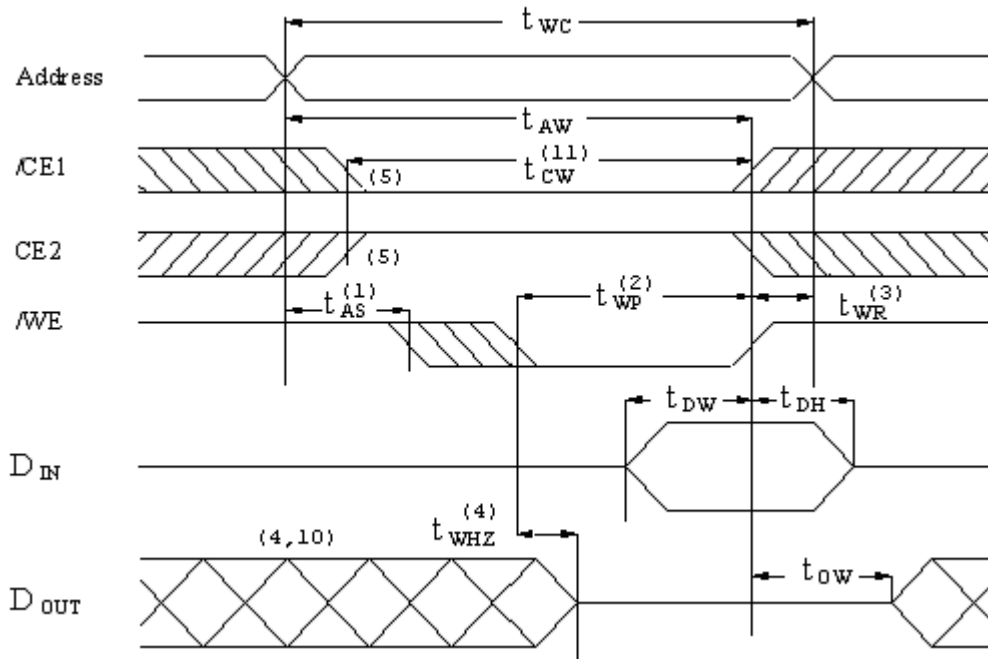
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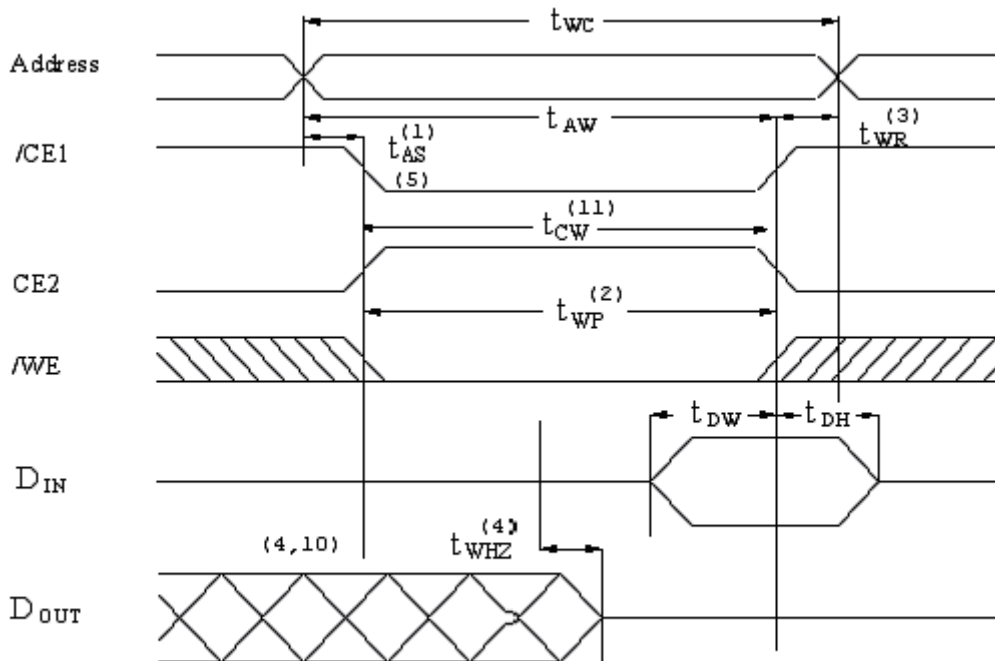
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SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)





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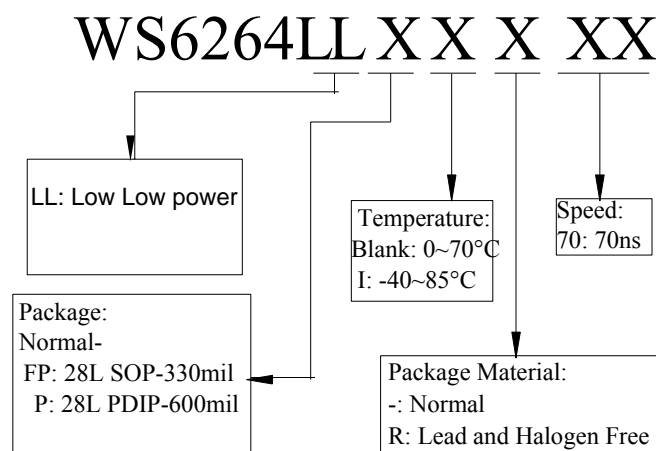
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NOTES:

1. T_{AS} is measured from the address valid to the beginning of write.
2. The internal write time of the memory is defined by the overlap of $/CE1$ and $CE2$ active and $/WE$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $/CE1$ or $/WE$ going high or $CE2$ going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $/CE1$ low transition or $CE2$ high transition occurs simultaneously with the $/WE$ low transitions or after the $/WE$ transition, output remain in a high impedance state.
6. $/OE$ is continuously low ($/OE = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $/CE1$ is low and $CE2$ is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500mV$ from steady state with $C_L = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $/CE1$ going low or $CE2$ going high to the end of write.

ORDER INFORMATION





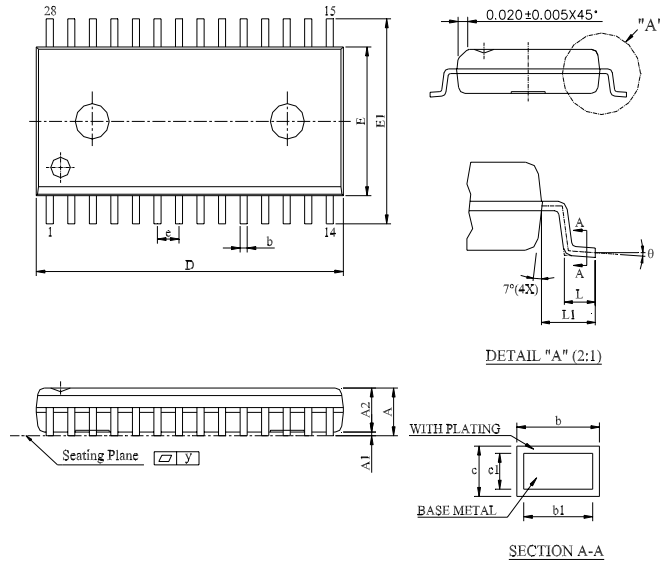
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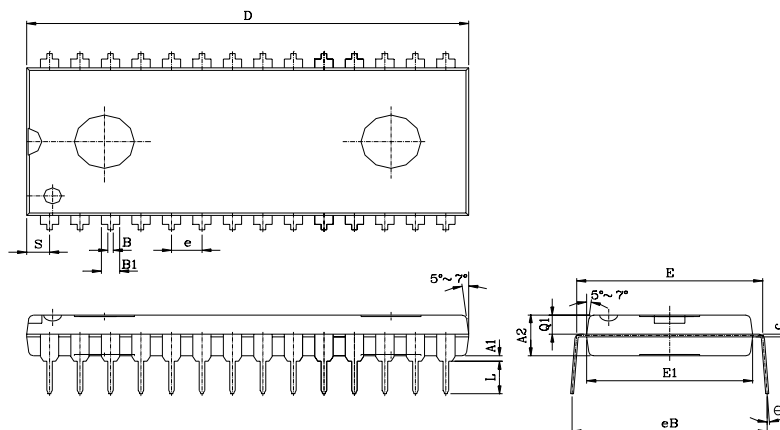
PACKAGE DIMENSIONS

28 pin SOP (330 mil) :



| SYMBOL | | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L | L1 | y | ∅ |
|--------|------|-------|-------|-------|-------|-------|-------|-------|--------|-------|--------|-------|--------|--------|-------|-----|
| mm | Min. | 2.540 | 0.102 | 2.362 | 0.35 | 0.35 | 0.20 | 0.20 | 17.983 | 8.280 | 11.506 | 1.118 | 0.700 | 1.520 | - | 0° |
| | Nom. | 2.692 | 0.226 | 2.489 | - | - | - | - | 18.110 | 8.407 | 11.811 | 1.270 | 0.964 | 1.720 | - | - |
| | Max. | 2.844 | 0.350 | 2.616 | 0.50 | 0.45 | 0.32 | 0.28 | 18.237 | 8.534 | 12.116 | 1.422 | 1.228 | 1.920 | 0.1 | 10° |
| inch | Min. | 0.100 | 0.004 | 0.093 | 0.014 | 0.014 | 0.008 | 0.008 | 0.708 | 0.326 | 0.453 | 0.044 | 0.0276 | 0.0598 | - | 0° |
| | Nom. | 0.106 | 0.009 | 0.098 | - | - | - | - | 0.713 | 0.331 | 0.465 | 0.050 | 0.0380 | 0.0677 | - | - |
| | Max. | 0.112 | 0.014 | 0.103 | 0.020 | 0.018 | 0.012 | 0.011 | 0.718 | 0.336 | 0.477 | 0.056 | 0.0484 | 0.0756 | 0.004 | 10° |

28 pin PDIP (600mil):



| SYMBOL | | A1 | A2 | B | B1 | c | D | E | E1 | e | eB | L | S | Q1 | ∅ |
|--------|------|-------|-------|-------|-------|-------|--------|--------|--------|----------------|--------|-------|-------|-------|----|
| mm | Min. | 0.254 | 3.683 | 0.330 | 1.270 | 0.152 | 36.957 | 14.986 | 13.716 | 2.540 (TYP) | 15.748 | 3.048 | 1.778 | 1.651 | 3° |
| | Nom. | - | 3.810 | 0.457 | 1.524 | 0.254 | 37.084 | 15.240 | 13.818 | | 16.256 | 3.302 | 2.032 | 1.778 | 6° |
| | Max. | - | 3.937 | 0.584 | 1.778 | 0.356 | 37.211 | 15.494 | 13.920 | | 16.764 | 3.556 | 2.286 | 1.905 | 9° |
| inch | Min. | 0.010 | 0.145 | 0.013 | 0.050 | 0.006 | 1.455 | 0.590 | 0.540 | 0.100 (TYP) | 0.620 | 0.120 | 0.070 | 0.065 | 3° |
| | Nom. | - | 0.150 | 0.018 | 0.060 | 0.010 | 1.460 | 0.600 | 0.544 | | 0.640 | 0.130 | 0.080 | 0.070 | 6° |
| | Max. | - | 0.155 | 0.023 | 0.070 | 0.014 | 1.465 | 0.610 | 0.548 | | 0.660 | 0.140 | 0.090 | 0.075 | 9° |