Bluetooth Headset IC - WS9623AB3DF

Datasheet

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OVERVIEW

WS9623AB3DF is a stereo single chip headset solution based on Bluetooth protocol. It consists of 128 MHz high performance CPU processor, SRAM, via ROM Bluetooth baseband controller, MODEM, RF, Audio CODEC, PMU, etc. The protocol stack is stored in the on-chip ROM. It is fully compliant with all the mandatory features of Bluetooth version 4.1 + EDR specification.

FEATURES

- 128 MHz high performance CPU processor.
- Internal 512KB via ROM.
- Internal 4M bit SPI flash.
- -92dBm RX sensitivity and +9dBm TX output power capability
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, and whitening and transmit pulse shaping.
- Fully qualified Bluetooth v4.1 + EDR feature including eSCO and AFH.
- Internal 128KB SRAM. Allows full-speed data transfer with full piconet support, mixed voice and data, including all EDR packet types.
- Audio transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air.
- UART interface with programmable baud rate up to 3Mbps for HCI communication.
- Multiple I^2C interface for external EEPROM.
- Boot loader with external memory interface for software debugging.
- Internal 32 KHz oscillator for low power operation.
- QFN48 package.
- SPI flash support. Operation voltage is 3.3V.
- Battery power display support. Allows user to use buttons to trigger a tone/speech tone or a led, to prompt the current battery.
- SPP support. Increased SPP protocol, which is used to transmit commands and data, realize interaction control with other equipment that supports SPP.
- AT Command support. Communicates with MCU through the UART，controlled by the MCU，or converted the command to bluetooth command，sent to the mobile phone to realize the control of the phone by MCU.
- Working temperature range -40 to +80 ℃.
- Dual Mic Acoustic Noise Cancellation. Used to eliminate the stationary and non-stationary noise on Tx.
- Single-microphone echo Cancellation. Used to cancel acoustic echo.
- Single-microphone noise suppression. Used to reduce stationary noise on Tx and Rx
- Packet Loss Concealment. Used to restore audio quality in difficult RF environment on Rx.
- Equalizer. Supports six arbitrarily frequency bands and the bandwidth can be adjusted.
- Automatic Gain Control. Performs automatic volume adjustment of the signal on Tx and Rx.
- Speech Tone. Encoded with SBC (Sub-Band Codec) format and stored in FLASH, to indicate general event from headset by specified tone directly.
- Advanced multi-point support. Allows connecting 2 devices (either phones or pads) and handling multiple calls or music at the same time.
- Bluetooth Air path parameter configuration.
- 24 bit Audio codec, -98dB SNR.
- Low radio power realizes 10+meter communication (class2).
- Fast charger: 30 minutes charging time.
- No Balun filter required for connection.
- Battery monitor designed for smart phones.
- Watch dog for link loss alarm.
- Virtual Surround Sound for headphone and loudspeakers support. Create a perceived widened or surrounding sound image.
- Bass Enhancement support. Boosts the low frequency part of the signal and leaves the remaining part of the frequency range unchanged in terms of loudness and timbre. This gives the possibility to create extreme bass enhancement.

TYPICAL APPLICATION

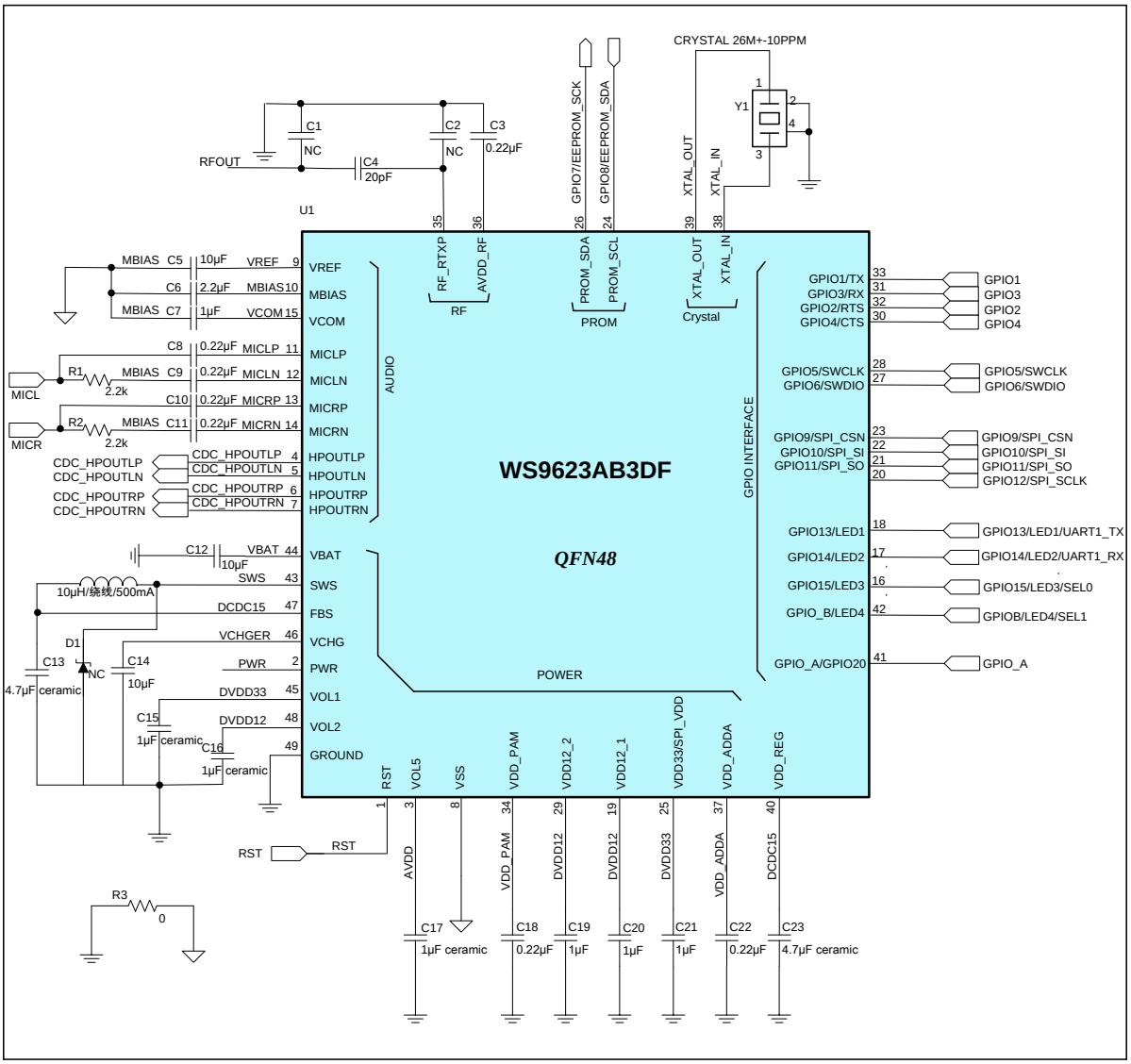


Figure 1 WS9623AB3DF Typical Application

PIN CONFIGURATIONS

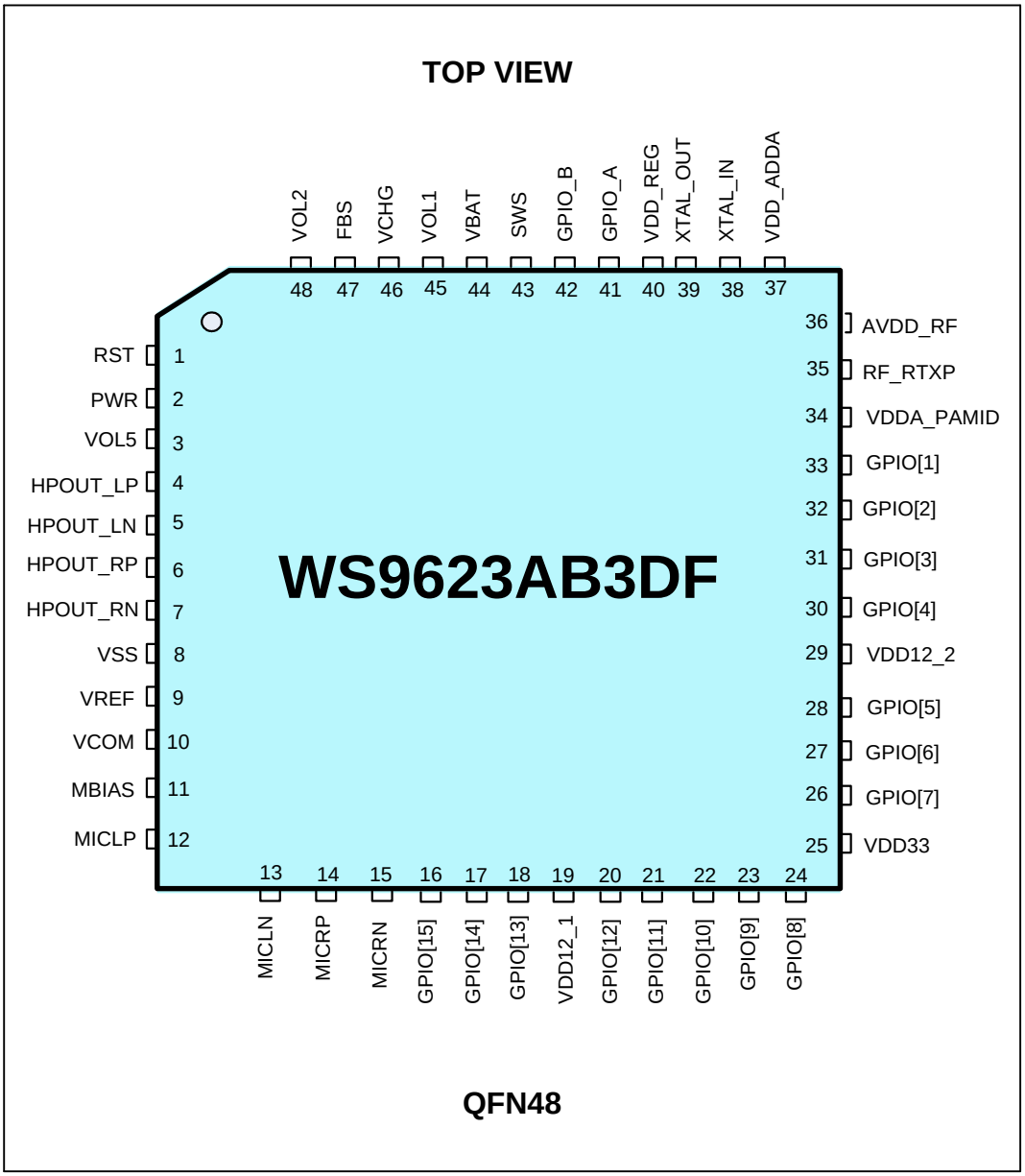


Figure 2 WS9623AB3DF Pin Assignment (Not to scale)

PIN DESCRIPTION

[Table 1] PIN Descriptions by Order

ORDER	PIN NAME	DIR	POWER	DESCRIPTION
1	RST	AI	AVDDBAT	Rest for deadlock.
2	PWR	AI	AVDDBAT	High level (BAT voltage) means button is turned on.
3	VOL5	AIO	AVDDBAT	LDO5 (3.3V) output. Power Supply for Audio an HP (AVDD33 power domain).
4	HPOUTLP	A, O	AVDD18	Headphone left channel output (Positive).
5	HPOUTLN	A, O	AVDD18	Headphone left channel output (Negative).
6	HPOUTRP	A, O	AVDD18	Headphone right channel output (Positive).
7	HPOUTRN	A, O	AVDD18	Headphone right channel output (Negative).
8	VSS	P	AVDD33	Ground for Audio.
9	VREF	AIO	AVDD33	Internal reference voltage output,
10	MBIAS	AIO	AVDD33	Microphone bias voltage output, tied 2.2μF capacitor to AVSS.
11	MICLP	A, O	AVDD33	Microphone left channel input, positive end.
12	MICLN	A, I	AVDD33	Microphone left channel input, negative end.
13	MICRP	A, I	AVDD33	Microphone right channel input, positive end.
14	MICRN	A, I	AVDD33	Microphone right channel input, negative end.
15	VCOM	A, I	AVDD33	Common mode reference voltage.
16	GPIO[15]	B	VDD33	General purpose IO.
17	GPIO[14]	B	VDD33	General purpose IO.
18	GPIO[13]	B	VDD33	General purpose IO.
19	VDD12_1	P	DVDD12	Digital core power.
20	GPIO[12]	B	VDD33	General purpose IO.
21	GPIO[11]	B	VDD33	General purpose IO.
22	GPIO[10]	B	VDD33	General purpose IO.
23	GPIO[9]	B	VDD33	General purpose IO.
24	GPIO[8]	B	VDD33	General purpose IO.
25	VDD33	P	DVDD33	Digital I/O power.
26	GPIO[7]	B	VDD33	General purpose IO.
27	GPIO[6]	B	VDD33	General purpose IO.
28	GPIO[5]	B	VDD33	General purpose IO.
29	VDD12_2	P	DVDD12	Digital core power.
30	GPIO[4]	B	VDD33	General purpose IO.
31	GPIO[3]	B	VDD33	General purpose IO.
32	GPIO[2]	B	VDD33	General purpose IO.
33	GPIO[1]	B	VDD33	General purpose IO.
34	VDDA_PAMID	P,O	AVDD125	PA supply. LDO output, connect to decoupling cap.
35	RF_RTXP	AIO	AVDD125	RF input/output, drive SAW filter. Require on board matching network.
36	AVDD_RF	P	AVDD125	RF front end supply.LDO output, connect to decoupling cap.
37	VDD_ADDA	P	AVDD125	analog vdd, LDO output, connect to decoupling cap.
38	XTAL_IN	AIO	AVDD125	XTAL input, connect to crystal.

ORDER	PIN NAME	DIR	POWER	DESCRIPTION
39	XTAL_OUT	AIO	AVDD125	XTAL output, connect to crystal
40	VDD_REG	P, I	AVDD15	XTAL/analog/RF LDO power (1.5V) input, external power supply from FBS .need 3.3uF and 4.7pF on board caps.
41	GPIO_A	B	VDD33	General purpose IO.
42	GPIO_B	B	VDD33	General purpose IO.
43	SWS	AIO	AVDDBAT	Connect the inductor of switching Buck DC-DC.
44	VBAT	P, IO	AVDDBAT	Battery positive terminal.
45	VOL1	AIO	AVDDBAT	LDO1 (3.3V) output and input for POR. Power Supply of digital I/O (DVDD33 power domain).
46	VCHG	P, I	AVDDBAT	Charger input terminal.
47	FBS	AIO	AVDDBAT	The feedback pin of switching Buck DC-DC. Source of AVDD 15 power domain.
48	VOL2	AIO	AVDDBAT	LDO2 (1.2V) output. Power Supply of core of digital logic.

[Table 2] PIN Numbers by Interface

INTERFACE	PIN NUMBER
GPIO Interface	16~18, 20~24, 26~28, 30~33, 41~42
PMU Interface	1~3, 8~10, 19, 25, 29, 34, 36~37, 40, 43~48
Audio Interface	6~7, 11~15,
Radio Interface	35
Crystal Interface	38~39

Note 1:

P	Power/Ground
A	Analog
I	Input
O	Output
B	Bi-direction
PP	Internal programmable pull up/down
Sch	Schmitt Input

FUNCTIONAL BLOCK DESCRIPTION

Radio Transceiver

The WS9623AB3DF features an integrated radio transceiver that has been optimized for Bluetooth 2.4 GHz wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification 4.1 and EDR specification, and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The WS9623AB3DF features a fully integrated zero-IF transmitter. The baseband transmits GFSK, DQPSK, 8DPSK data is digitally modulated in the modem block, and then up-converts the data to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filters, I/Q up-converters, output Power Amplifiers (PAs), and RF filters. The digital modulator performs the data modulation and filtering required for the GFSK, DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Receiver Path

The receiver path uses an innovative Adaptive-Adjustable-IF architecture (patent pending) for improved anti-interference performance and low power consumption. The front-end topology with built-in out-of-band attenuation enables the WS9623AB3DF to be used in most applications with no off-chip filtering. The digital demodulator and bit synchronizer take the down-converted received signal and perform an optimal frequency tracking and bit synchronization algorithm. The radio portion of the WS9623AB3DF also provides a Received Signal Strength Indication (RSSI) signal to the baseband so that the controller can participate in a Bluetooth power-controlled link.

Audio codec

Audio Codec includes two channel voice band 24bit ADC, which can support stereo microphone recording, with one microphone bias output. The codec also has two channel CD quality 24bit Audio DACs, which support two 16Ω headphone / speakers with two 40mW output, or two 32Ω headphone / speakers with two 40mW output.

Power Management

PMU is an integrated power solution for applications powered by one small Li-Ion battery. It provides total power solution for WS9623AB3DF. It provides one highly efficient, low output ripple step-down converter to the core voltage. Step-down converter enters PFM mode at light load for maximum efficiency over the widest possible range of load currents. The PMU also integrates three LDO regulators (with Charger bypass mode), POR, Start-up controller and a battery charger. The charger block will provide smart battery charging management, while LDO will provide a low-noise power supply for WS9623, and POR will provide reset signal for digital core.

SRAM

The SRAM of 128kB is used in WS9623AB3DF Chip. This memory stores the data generated or required by running the high performance CPU.

ROM

The VIA ROM of 512KB is employed in WS9623AB3DF Chip. This memory is used to store the firmware.

DEVICE TERMINAL DESCRIPTIONS

Power Supply

WS9623AB3DF is powered by one small Li-Ion battery via the pins VBAT and GNDS1. The voltage value range of battery is from 3.0V to 5.5V.

It can be connected to charger via the pin VCHG; the charger block will provide smart battery charging management and power supply through LDO for chip simultaneously. The Input voltage value range of charger is from 3.0V to 6.5V (From Adapter or USB).

The maximum charging current is 300mA.

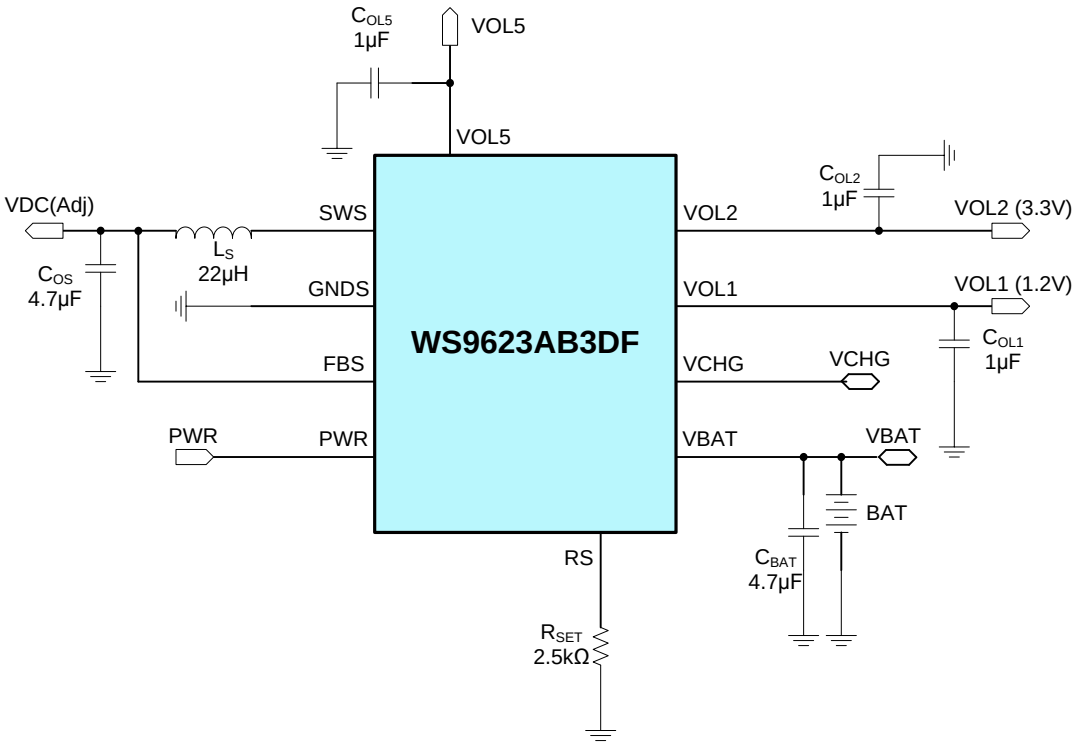


Figure 3 WS9623AB3DF Typical Power Application

Crystal Oscillator

Port XTAL_IN and XTAL_OUT need to be bonded out and connect to the on-board crystal circuit. The load cap for both pins is 4-12pF. The on-board crystal circuit needs to be placed close to the chip. The on-chip DCXO circuit can work with crystal frequency 26MHz.

The initialization time for the DCXO circuit to settle to 10ppm accuracy is 2mS. The reference clock generated by the DCXO goes to RFPLL and DPLL. However, the reference clock generated by DCXO can be directly feed to the digital baseband in that case.

The on-chip DCXO circuit has a cap tuning array that can be used to trim reference clock frequency.

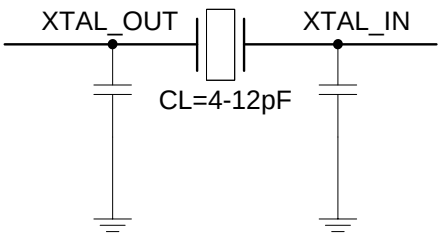


Figure 4 Typical Applications of XTAL_IN and XTAL_OUT

RF Interface

Port RFXP and AVDD_RF are the RF I/O ports and need to be bonded out. The two RF pins are connected to on-board matching network which should be placed close to the chip. The associated on–board transmission line routing should have 50Ω impedance matching.

Audio Interface

WS9623AB3DF supports Dual Microphone Audio inputs. The MICLP port is microphone left channel inputs, the MICLN port is differential inputs, the MICRP port is microphone right channel inputs and the MICRN port is differential inputs.

The stereo Audio output ports are HPOUT_RP/HPOUT_RN and HPOUT_LP/HPOUT_LN, while HPOUT_RP and HPOUT_RN are headphone right channel output, HPOUT_LP and HPOUT_LN are headphone left channel output.

UART Interface

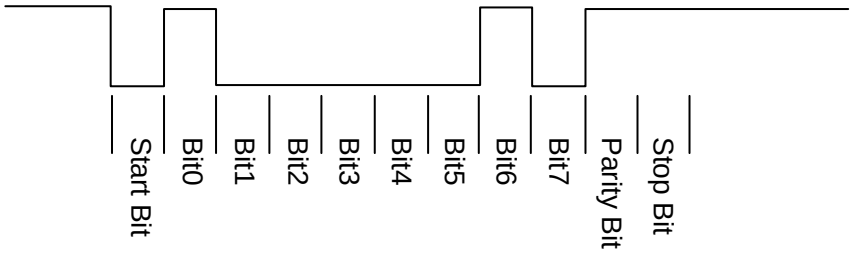
The UART ports are shared with GIPO [4:1]. Those ports are used as UART by configuring related register by SW.

Function Description

Serial Operation

The UART module has one operation mode --- non-return to zero (NRZ).

The NRZ mode is primarily associated with RS-232. Each character is transmitted as a frame delimited by a start bit at the beginning and a stop bit at the end. Data bits are transmitted least significant bit first, each bit occupies a period of time equal to 1 full bit. If parity is used, then the parity bit is transmitted after the most significant bit. Following is the waveform in NRZ mode.



NRZ mode transmits an ASCII “A” Character with Odd

Figure 5 Waveform of UART

UART External Connection for Bluetooth

The UART in WS9625ABMC can be used to transport HCI (Host Controller Interface) packets for Bluetooth. The HCI UART Transport Layer uses the following settings for RS232:

[Table 3] HCI UART Transport Layer settings

Baud rate	manufacturer-specific
Number of data bits	8
Parity bit	no parity
Stop bit	1 stop bit
Flow control	RTS/CTS (Hardware Flow Control)
Flow-off response time	manufacturer specific

The RS232 signals should be connected in a null-modem fashion.

The most expensive null modem cable is the null modem cable suitable for full handshaking. In this null modem

cable, seven wires are present. Only the ring indicator RI and carrier detect CD signal are not linked. The cable is shown in the following figure. DTR and DSR are not used in UART of WS9623AB3DF.

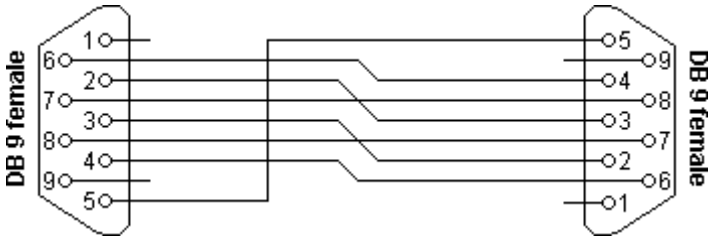


Figure 6 Null Modem Cable Connections

Connector 1	Connector 2	Function		
2	3	Rx	←	Tx
3	2	Tx	→	Rx
4	6	DTR	→	DSR
5	5	Signal ground		
6	4	DSR	←	DTR
7	8	RTS	→	CTS
8	7	CTS	←	RTS

In CTS/RTS flow, the RTS output of device1 signals device2 that device1 is capable of receiving information, so device2 will send the data out when the RTS signal of device1 is set valid. Also, device1 will send the data out when the RTS signal of device2 is set valid.

I²C Interface

WS9623AB3DF provides PROM_SCL and PROM_SDA for communication with EEPROM which comply with I²C protocol.

I²C is a two-wire, bi-directional serial bus, which provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.
The I²C interface defines 2 transmission speeds:

- Normal: 100Kbit/s
- Fast: 400Kbit/s

Only 100Kbps mode and 400Kbps mode are supported directly.

FEATURES:

- Compatible with I²C standard;
- Multi Master Operation;
- Supports 7 and 10bit addressing mode;
- Software programmable clock frequency, supports a wide range of input clock frequencies;
- Software programmable acknowledge bit;
- Interrupt or bit-polling driven byte-by-byte data-transfers;
- Arbitration lost interrupt, with automatic transfer cancellation;
- Bus busy detection;
- Clock Stretching and Wait state generation;

Interface Timing Signal with I²C bus

System Configuration

The I²C system uses the serial data line (SDA) and serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line via a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and it must be held stable during the high period of SCL. While SCL is high, the transition on the SDA line is interpreted as a command (sees START and STOP signals).

I²C Protocol

Generally, a standard communication consists of four parts:

- START signal generation
- Slave address transfer
- Data transfer
- STOP signal generation

Figure 7 I²C protocol

START Signal

When the bus is free/idle, that is no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. The START signal, usually referred as the S-bit, is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.

Repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus.

The core generates a START signal when the STA-bit in the Command Register is set and the RD or WR bits are set. Depending on the current status of the SCL line, a START or Repeated START is generated.

Slave Address Transfer

The slave address is the first byte of data transferred by the master immediately after the START signal. This is a seven-bits calling address followed by a RW bit. The RW bit signals the slave data transfer direction. The slave address is unique; no two slaves in the system can have the same address. Only the slave with an address that matches the address transmitted by the master will respond, it responds by returning an acknowledge bit which is pulled by the SDA low at the 9th SCL clock cycle.

Note: The core supports 10bit slave addresses by generating two address transfers. See the Philips I²C specifications for more details.

The core treats a Slave Address Transfer as any other write action. Store the slave device's address in the Transmit Register and set the WR bit. The core will then transfer the slave address on the bus.

Data Transfer

Once achieved the successful slave addressing, the data transfer can proceed on a byte-by-byte basis in the

direction specified by the RW bit that sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge, the master will generate a STOP signal to abort the data transfer, or generate a Repeated START signal and then start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave should release the SDA line for the master to generate a STOP or Repeated START signal.

To write data to a slave, store the data in the Transmit Register to be transmitted and set the WR bit. To read data from a slave, set the RD bit. The core set the TIP flag during a transfer, indicating that a transfer is in progress. When the transfer is done the TIP flag is reset, and generates an interrupt. The Receive Register contains valid data after the IF flag is reset. The user may issue a new write or read command when the TIP flag is reset.

STOP Signal

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred as the P-bit, is defined as a low-to-high transition of SDA while SCL is at logical '1'.

Arbitration Procedure

■ Clock Synchronization

The I^2C bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters simultaneously try to control the bus, a clock synchronization procedure determines the bus clock. Because of the wired-AND connection of the I^2C signals, a high-to-low transition affects all the devices that connected to the bus. Therefore a high–to-low transition on the SCL line causes all concerned devices to count off their low period. Once a device clock has gone low, it will hold the SCL line in low state until the clock high state is reached. Due to the wired-AND connection, the SCL line will therefore be held low by the device with the longest low period, and held high by the device with the shortest high period.

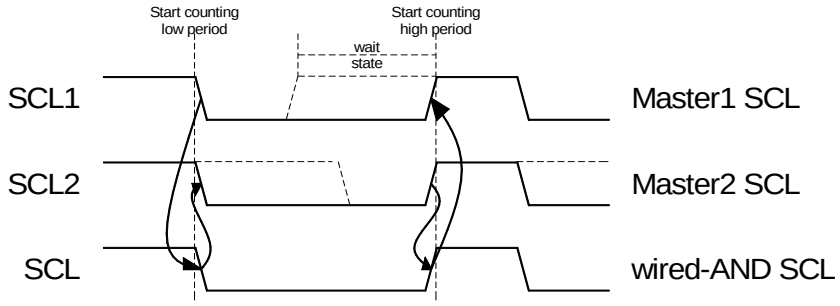


Figure 8 Arbitration Procedure

■ Clock Stretching

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate. After the master has driven SCL low, the slave can drive SCL low for the required period and then release it. If the slave's SCL low period is greater than the master's SCL low period, the resulting SCL bus signal low period will be stretched, thus inserting wait-states.

GPIO interface

The ports GPIO [15:1] / GPIO_A/ GPIO_B are general purpose IO, GPIO [15:13] / GPIO_B are used as LED.

GPIO [12:1] / GPIO_A are used as Buttons which indicate volume control, music play/stop, link statues display, etc. The special function of each port can be configured in SW.

GPIO [4:1] is shared for UART connections. GPIO [4:1] is used for UART transport by configuring related register by SW.

The PWR is voltage value high indication port and it is used as Multi function port. High level (BAT voltage) of this port means the button is turned on; it can be used for powering on, powering down, or paging scan mode of chip according of its high level and Duration of High level.

There are 17 GPIO in the GPIO module. GPIO module is used to process the transmission and receiving between GPIO pad and the core and to generate the interrupt from GPIO pad.

In WS9623, GPIO [4:1] are shared for UART connections. When GDMUX [4:1] is configured to 4'b1111, GPIO [4:1] is used for UART transport.

In WS9623, GPIO [6:5] are shared for ARM debugging port. When GDMUX [6:5] is configured to 2'b11, GPIO [6:5] is used for ARM debugging port (SWDIOTMS and SWCLKTCK) transport, which is their default setting. They are pulling up pins (other GPIO are pulling down pins).

In WS9623, GPIO [8:7] are shared for I2C connections. When GDMUX [8:7] is configured to 2'b11, GPIO [8:7] is used for I2C transport, and now GPIO [8:7] can't used as Buttons.

In WS9623, GPIO [12:9] are shared for SPI connections. When GDMUX [12:9] is configured to 4'b1111, GPIO [12:9] is used for SPI transport, and now GPIO [12:9] can't used as Buttons.

ELECTRICAL CHARACTERISTICS

RF Specifications

[Table 4] Receiver RF Specifications

Parameters	Mode and Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Rx Sensitivity	GFSK, 1Mbps, 0.1% BER	–	-92.0	-90.0	dBm
	DQPSK, 2Mbps, 0.01% BER	–	-93.0	-91.0	dBm
	8DPSK, 3Mbps, 0.01% BER	–	-86.0	-84.0	dBm
Maximum Input	–	–	–	-10.0	dBm
Interference Performance	C/I CCI (GFSK, 0.1% BER)	–	–	11.0	dB
	C/I 1MHz ACI (GFSK, 0.1% BER)	–	–	0.0	dB
	C/I 2MHz ACI (GFSK, 0.1% BER)	–	–	-30.0	dB
	C/I ≥3MHz ACI (GFSK, 0.1% BER)	–	–	-40.0	dB
	C/I image channel (GFSK, 0.1% BER)	–	–	-9.0	dB
	C/I CCI (DQPSK, 0.1% BER)	–	–	13.0	dB
	C/I 1MHz ACI (DQPSK, 0.1% BER)	–	–	0.0	dB
	C/I 2MHz ACI (DQPSK, 0.1% BER)	–	–	-30.0	dB
	C/I ≥3MHz ACI (DQPSK, 0.1% BER)	–	–	-40.0	dB
	C/I image channel (DQPSK, 0.1% BER)	–	–	-7.0	dB
	C/I CCI (8DPSK, 0.1% BER)	–	–	21.0	dB
	C/I 1MHz ACI (8DPSK, 0.1% BER)	–	–	5.0	dB
	C/I 2MHz ACI (8DPSK, 0.1% BER)	–	–	-25.0	dB
	C/I ≥3MHz ACI (8DPSK, 0.1% BER)	–	–	-33.0	dB
	C/I image channel (8DPSK, 0.1% BER)	–	–	0.0	dB
Out-of-Band Blocking Performance (CW)	30 MHz to 2000 MHz (GFSK, 0.1% BER)	–	-10.0	–	dBm
	2000 MHz to 2399 MHz (GFSK, 0.1% BER)	–	-27.0	–	dBm
	2498 MHz to 3000 MHz (GFSK, 0.1% BER)	–	-27.0	–	dBm
	3000 MHz to 12.75 GHz (GFSK, 0.1% BER)	–	-10.0	–	dBm
Intermodulation Performance	BT, Delta f = 5MHz	-39.0	–	–	dBm

[Table 5] Transmitter RF Specifications

Parameters	Mode and Conditions	Min	Typ	Max	Unit
Frequency Range	–	2402	–	2480	MHz
Channel Spacing	–	–	1	–	MHz
Maximum Output Power	Class 2	+2	+4	+9	dBm
Output Power Range	–	-30	–	>+4	dBm
In-Band Spurious Emission	±500 kHz	–	–	-20.0	dBc
	1.0MHz<|M – N|<1.5 MHz (EDR only)	–	–	-26.0	dBc
	1.5MHz<|M – N|<2.5 MHz (EDR only)	–	–	-20.0	dBm
	|M – N|>2.5 MHz (EDR only)	–	–	-40.0	dBm
LO Performance	Lock time	–	100	150	us
	Initial carrier frequency tolerance	–	±25	±75	kHz

Parameters	Mode and Conditions	Min	Typ	Max	Unit
Frequency Drift	DH1 packet	–	±20	±25	kHz
	DH3 packet	–	±20	±40	kHz
	DH5 packet	–	±20	±40	kHz
	Drift rate	–	10	20	kHz/50 us
Frequency Deviation	00001111 sequence in payload	140	160	175	kHz
	01010101 sequence in payload	115	150	165	kHz

Power Consumption

[Table 6] Power Supply Current (With a normal 3.7V battery voltage)

Operating Mode	Typical	Unit
HV3	15.0	mA
EV3	15.0	mA
2EV3	14.3	mA
A2DP Active Mode: 2DH5, 350 kbps SBC	14.5	mA
Single HFP Sniff (500ms Interval)	350	µA
Deep Sleep (off) Mode	5.0	µA

Note :
The currents are measured without an audio signal present.
The currents are measured with LEDs off.
The sniff mode current is measured with the device operating in Slave mode.
The A2DP Active mode current is with the device operating in Slave mode.

Power Meter

Power meter measures power consumption of the battery and sends the current battery level to phones. Power meter has 10 report levels. The following devices support power meter currently.

- iPhone 3/4/4S/5
- iPad 1/2/mini
- iTouch 3/4/5
- MiPhone 2/2S

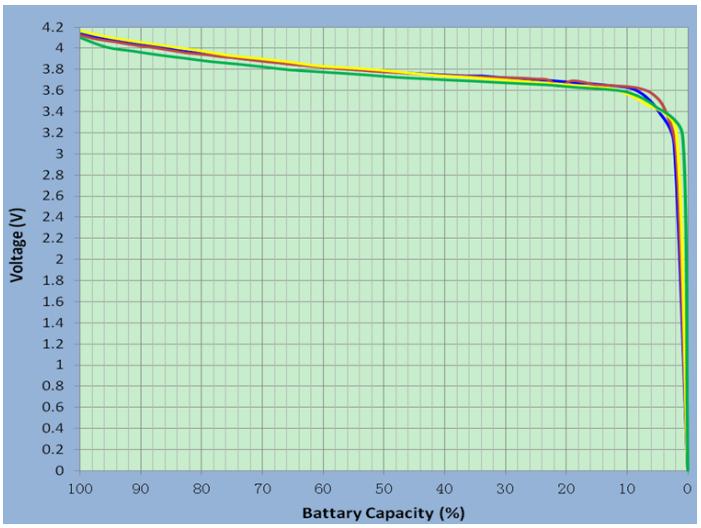


Figure 9 Power Meter Curve

PACKAGE INFORMATION

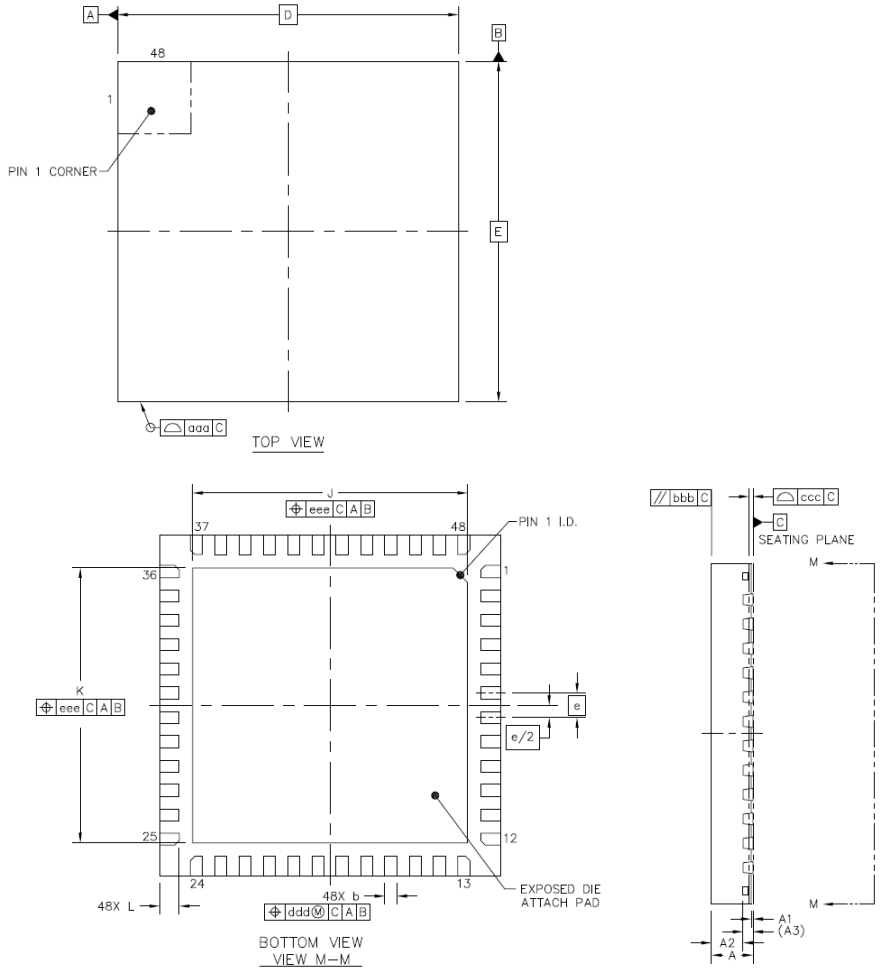


Figure 10 48-leads 7 x7 mm QFN Package

[Table 7] Physical Dimensions in figure 9 (Unit:mm)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.035	0.05
A2	---	0.65	0.67
A3		0.203 (REF)	
b	0.20	0.25	0.30
D		7 (BSC)	
E		7 (BSC)	
e		0.5 (BSC)	
J	5.55	5.65	5.75
K	5.55	5.65	5.75
L	0.35	0.40	0.45
aaa		0.1	
bbb		0.1	
ccc		0.08	
ddd		0.1	
eee		0.1	

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