

General Description

The WSP6020 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent R_{DS(on)} and gate charge for most of the synchronous buck converter applications .

The WSP6020 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

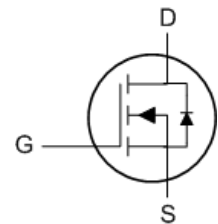
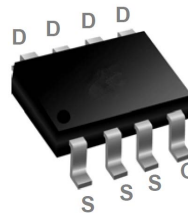
Product Summary

BVDSS	R _{DS(on)}	I _D
60V	7mΩ	18A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOP-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	18	A
I _D @T _C =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	12	A
I _{DM}	Pulsed Drain Current ²	72	A
EAS	Single Pulse Avalanche Energy ³	196	mJ
I _{AS}	Avalanche Current	16	A
P _D @T _A =25°C	Total Power Dissipation ⁴	2.5	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	72	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.2	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.044	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =15A	---	7	9	mΩ
		V _{GS} =4.5V, I _D =10A	---	8	12	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	2.0	3.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =60V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =60V, V _{GS} =0V, T _J =55°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
Q _g	Total Gate Charge (10V)	V _{DS} =24V, V _{GS} =10V, I _D =10A	---	82	---	nC
Q _{gs}	Gate-Source Charge		---	13	---	
Q _{gd}	Gate-Drain Charge		---	17	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =30V, V _{GEN} =10V, R _G =6Ω I _D =4A, R _L =30Ω	---	26	---	ns
T _r	Rise Time		---	125	---	
T _{d(off)}	Turn-Off Delay Time		---	58	---	
T _f	Fall Time		---	112	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	3760	---	pF
C _{oss}	Output Capacitance		---	340	---	
C _{rss}	Reverse Transfer Capacitance		---	200	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =25V, L=0.1mH, I _{AS} =12A	---	196	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =6.3A, dI/dt=100A/μs, T _J =25°C	---	38	---	nS
Q _{rr}	Reverse Recovery Charge		---	44	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper,t<10sec.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=12A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

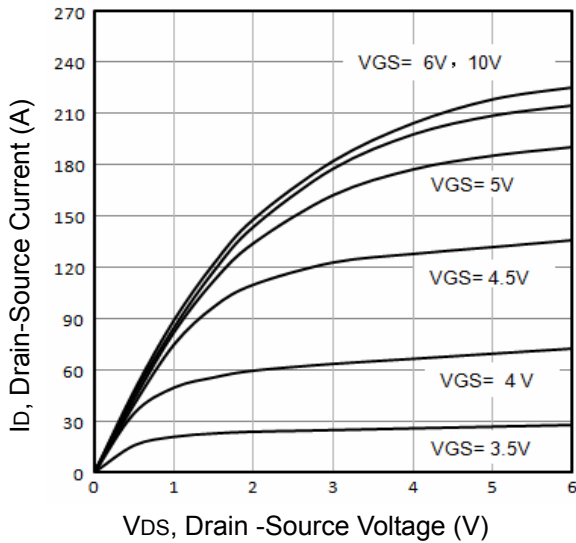


Fig1. Typical Output Characteristics

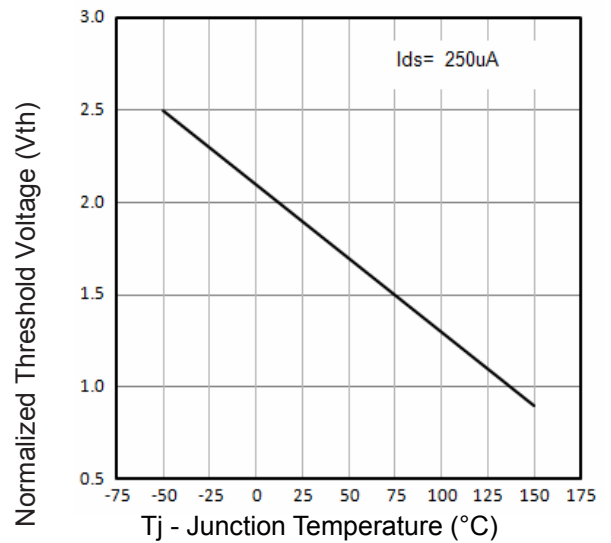


Fig2. Normalized Threshold Voltage Vs. Temperature

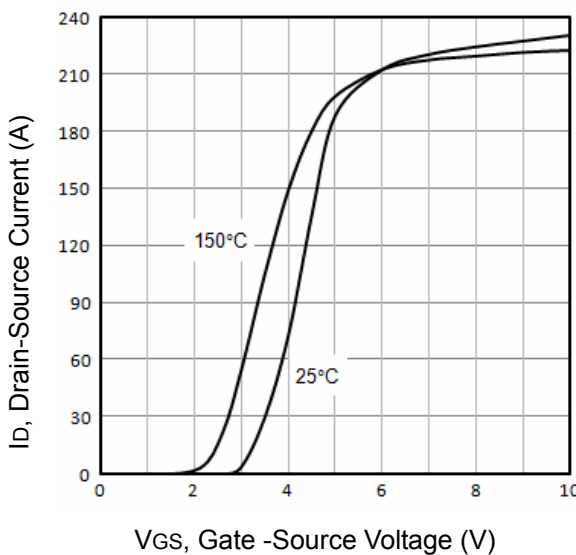


Fig3. Typical Transfer Characteristics

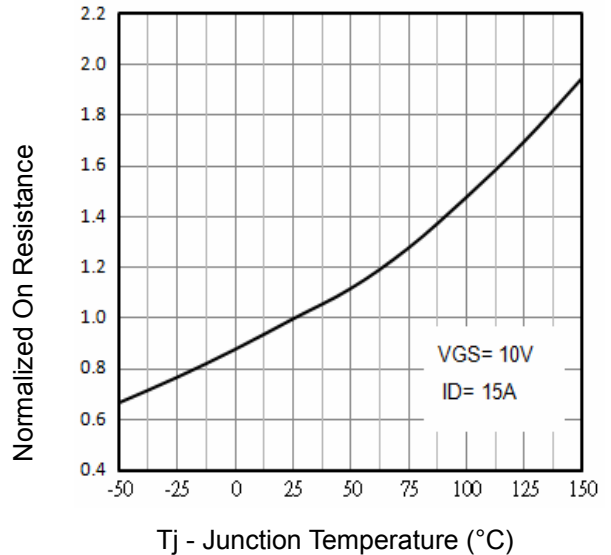


Fig4. Normalized On-Resistance Vs. Temperature

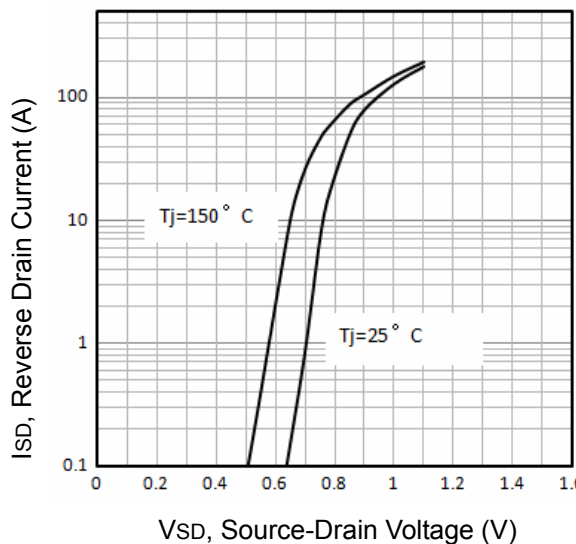


Fig5. Typical Source-Drain Diode Forward Voltage

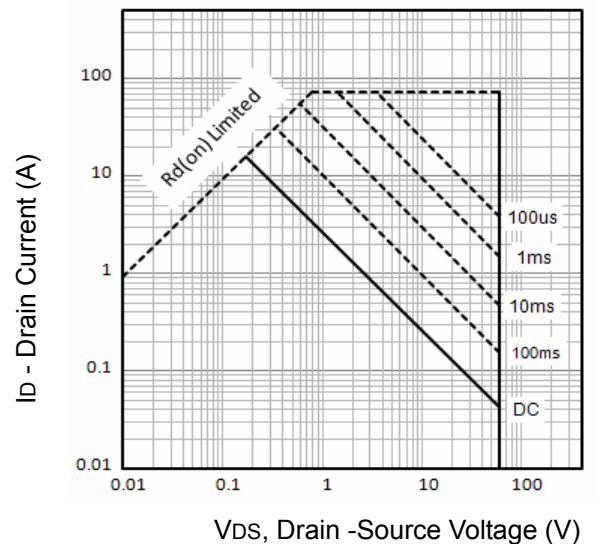
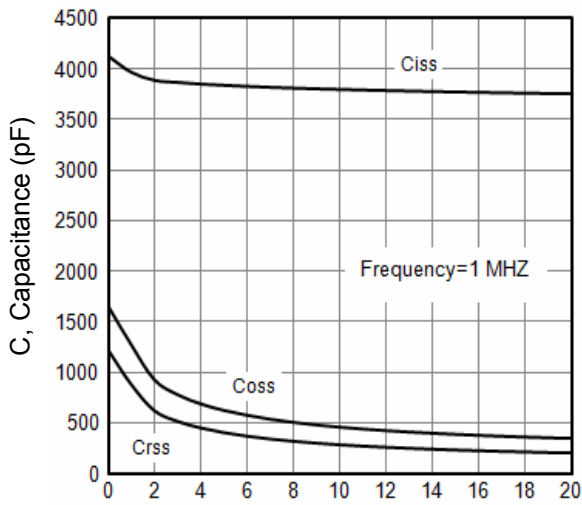
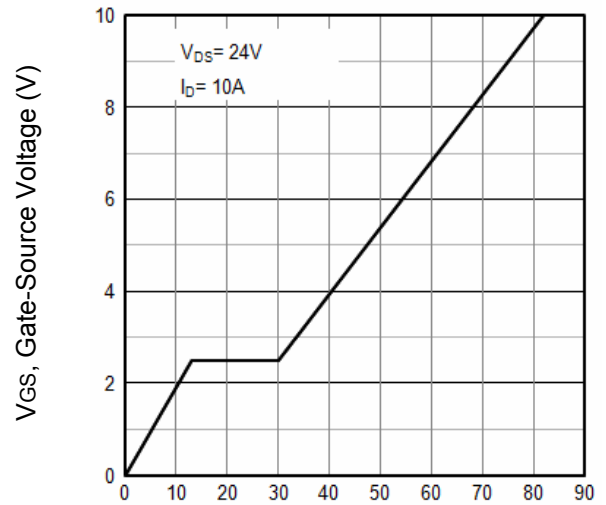


Fig6. Maximum Safe Operating Area



V_{DS} , Drain-Source Voltage (V)

Fig7. Typical Capacitance Vs.Drain-Source Voltage



Q_g -Total Gate Charge (nC)

Fig8. Typical Gate Charge Vs.Gate-Source Voltage

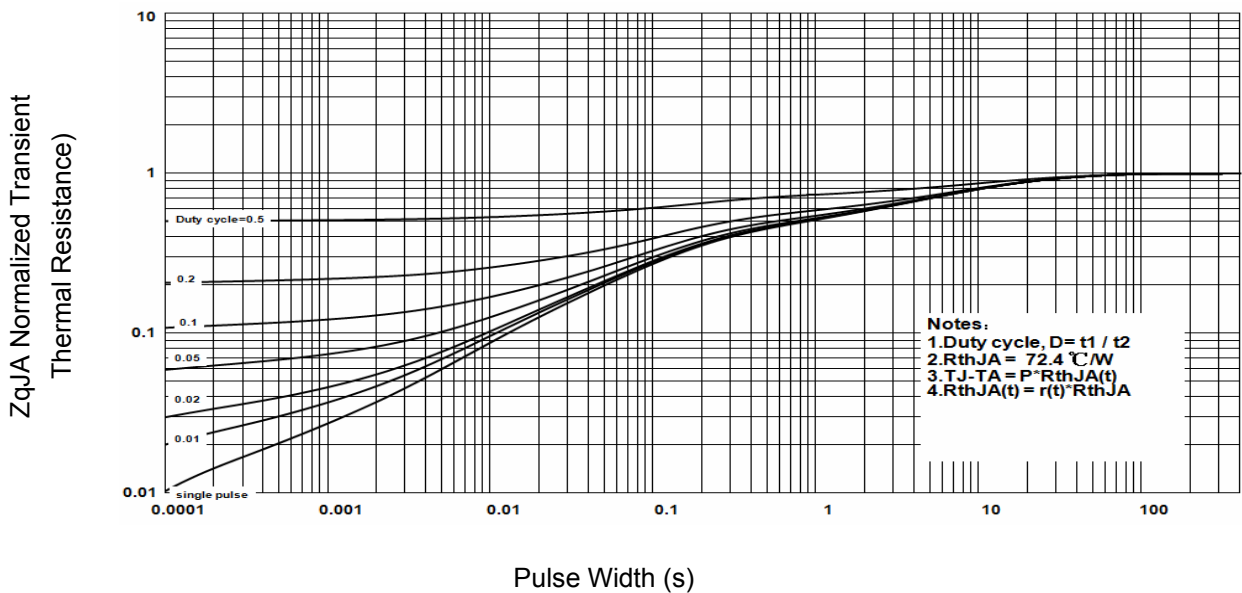


Figure 9: Normalized Maximum Transient Thermal Impedance

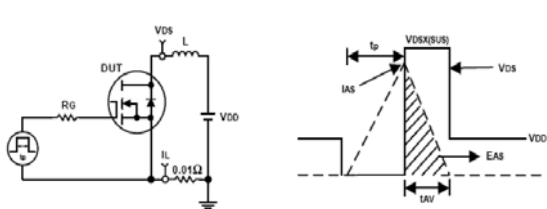


Fig10. Unclamped Inductive Test Circuit and waveforms

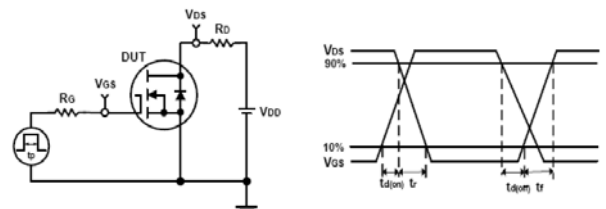
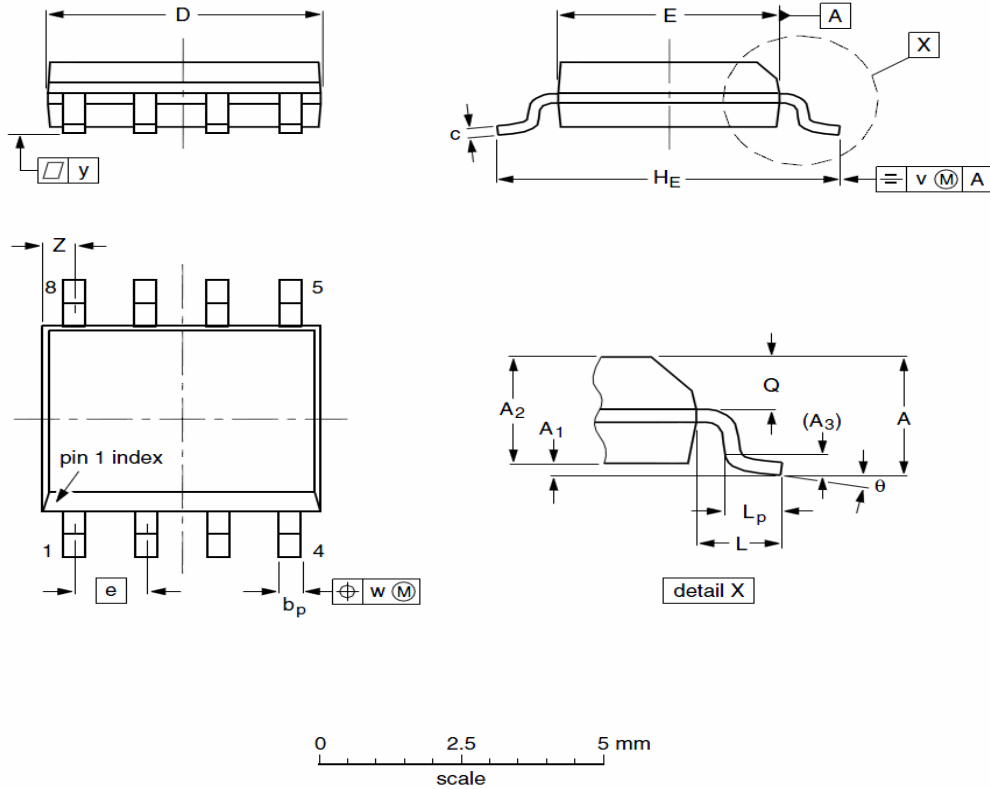


Fig11. Switching Time Test Circuit and waveforms

SOP8 Package Outline Data



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	--	1.75	--	A ₁	0.10	0.18	0.25
A ₂	1.25	1.35	1.45	A ₃	--	0.25	--
b _p	0.36	0.42	0.49	c	0.19	0.22	0.25
D	4.80	4.92	5.00	E	3.80	3.90	4.00
e	--	1.27	--	H _E	5.80	5.98	6.20
L	--	1.05	--	L _p	0.40	0.68	1.00
Q	0.60	0.65	0.70	v	--	0.25	--
w	--	0.25	--	y	--	0.10	--
Z	0.30	0.50	0.70	θ	0°		8°



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