WT51F516
Flash Type General Purpose Microcontroller

Data Sheet

Rev. 1.02

January 31, 2012

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REVISION HISTORY

V1.02 01/31/2012
1. Add « typical application circuit » section
2. Update electrical Characteristics
3. Update section 5.20 analog comparator register description.
4. Add ADC register notice at section 5.18
5. Add Temperature sensor description at section 5.19
6. Update location table description (section 9.2)
7. Modify part number “51F516-SG160WT” to “51F516-SG161WT”
8. Modify pin description

V1.01 09/15/2011
1. Update SOP 16 pin package dimension

V1.00 08/23/2011
1. Remove SG080 package type
2. Add GPIOC1 notice for UG320 package type(section 5.6.)

V0.97 07/20/2011
1. Modify section 5.4. watchdog timer description

V0.96 07/20/2011
1. Update section 7.2. QFN32 package dimension description

V0.95 07/19/2011
2. Update section 2.3. pin description for add IRQ[3:0] pin information and die information.
3. Update section 3. selection guide for add die information
4. Update section 4. function block diagram for add “IRQ process”
5. Update section 5.1.5. SFR description
6. Move 01H register bit[3-2] to 04H register
7. Add 03H register for control GPIOC[1] & GPIOA[7] SMT input buffer.
8. Add watchdog timer detect time 33m & 66ms (register 0AH)
9. Add enhance timer wake up source (register 29H)
10. Update interrupt register (30H ~ 34H)
    (a) Add enhance timer interrupt source
    (b) Add analog comparator interrupt source,
    (c) Update all-input toggle interrupt register define position
    (d) Add IRQ[3:0] interrupt source
11. Add IRQ[3:0] setting register (3AH ~ 3BH)
12. Add enhance timer function (section 5.11.)
13. Remove register 40H bit-6 “SI_TLO_EN’ (section 7.15. C touch counter)
14. Add register 38H bit-4 RTC_RESET, to reset RTC module.
15. Update section 7.2. QFN32 package dimension description
16. Add Bonding diagram and Location table for DIE.(section 7.)

V0.94 04/06/2011
1. Add SOP8 package
2. update LVD register description

V0.93 03/24/2011
Change product to WT51F516 (from WT69P5)
Note: WT51F516 V0.93 released in 2011/3/24

V0.92 02/07/2011

1. Add LQFP48 package
2. Change SPI-MISO pin to share with GPIOC6. (Original share with SDA pin)
3. Change SPI-SCK pin to share with GPIOC5. (Original share with SCL pin)
4. Add 8052 P00,P01, P02 and P03 pins to share with GPIOA0, GPIOA1, GPIOA2 and GPIOA5

Table of Contents

1. General Description

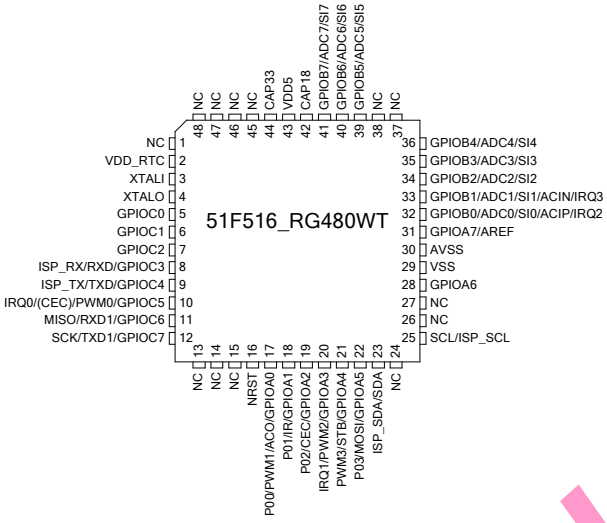
The WT51F516 is a microcontroller with 1) 1T 8052 CPU, 2) 8052 2 timers and UART, 3) 16k bytes flash memory, 4) 512 bytes SRAM, 5) watch-dog timer, 6) one enhance timer, 7) emulated EEPROM, 8) one master/slave SPI interface, 9) one slave I^2C interface, 10) hardware universal IR receiver, 11) hardware CEC, 12) 4 10-bit PWMs, 13) 8 channel 10-bit A/D converter, 14) 8 channel C-touch input, 15) on-chip analog comparator, 16) temperature sensor, 17) real time clock, 18) power down mode, 19) embedded ICE/ISP mode,

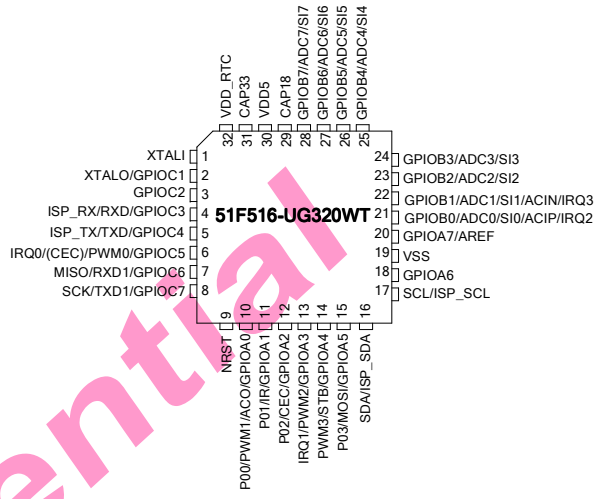
1.1. Features

- Embedded 1T 8052 CP
  - Normal operation mode :
    - 12MHz, 6MHz, 3MHz, 1MHz(internal RC OSC), 128KHz(internal RC OSC)
  - Instruction execution time : Min. =83.3ns @12Mhz
- Memory :
  - Flash memory: 16K Bytes
  - RAM: internal 256Bytes + external 256Bytes
- 3 8051 timers: Timer0, Timer1, Timer2
- 2 8051 UART, support baud rate 230400 – 1200 at RC oscillator =12MHz.
- Watchdog timer
- One enhance timer
- Emulated EEPROM by software
  - Emulated EEPROM size: 512Bytes
- One M/S SPI interface (with 8 bytes buffer)
- One slave mode IIC interface
- Hardware universal IR receiver with programmable digital filter for noise rejection
- Hardware HDMI CEC
- Tri-state I/O structure, Input state can decided by external resister (pull high or pull low)
- 4 10-bit PWM pin output (Frequency can be adjustable)
- 10-bit A/D converter with 8 selectable inputs
- 8 channel C-touch input
- Temperature sensor
- On-chip analog comparator
- Low voltage detector, low voltage reset, internal POR
- Build-in 12Mhz RC oscillator
- Build-in RTC function with 32.768KHz crystal oscillator
- Program read out protection
- Build-in ICE/ISP
- Power consumption :
  - Typical 4mA at 12Mhz normal operation mode
  - Typical 400/100uA at RC OSC stand-by mode
  - Typical 5uA at RC OSC power down mode
- Operating voltage range : 2V to 5.5V
- Operation temperature:-40℃ to + 85℃
- Package :
  - SOP8/SOP16/SSOP20
  - QFN32
  - LQFP48

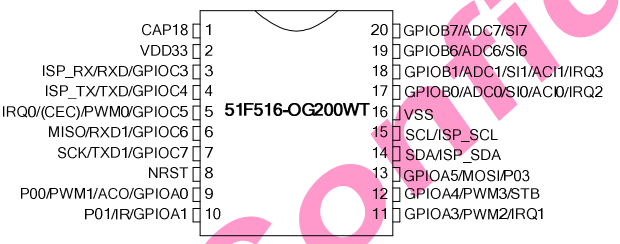
2. Pin Assignment

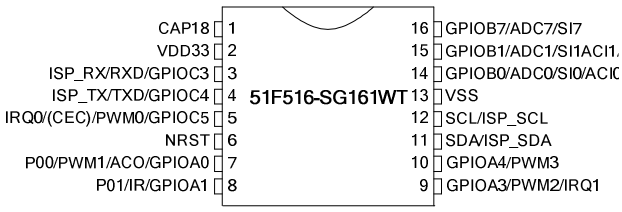
2.1. Package





*To use GPIOC1 port at UG320 package type, please see section 5.6 notice.





2.2. Ordering information

Package Type	Package Outline	Part Number
LQFP 48 pin	7*7 mm	51F516-RG480WT
QFN 32 pin	5*5 mm	51F516-UG320WT
SSOP 20 pin	150 mil	51F516-OG200WT
SOP 16pin	150 mil	51F516-SG161WT
DIE	-	51F516-HXXXWT

2.3. Pin description

RG480	UG320	OG200	SG161	DIE	Pin Name	I/O	Function Description
3	1			2	XTALI	I	32768hz crystal oscillator input
4	2			3	XTALO	O	32768hz crystal oscillator output
5				4	GPIOC0	I/O	GPIO C0
6	2			5	GPIOC1	I/O	GPIO C1
7	3			6	GPIOC2	I/O	GPIO C2
8	4	3	3	7	GPIOC3	I/O	GPIO C3 share with 8052 UART RXD or ISP RX.
9	5	4	4	8	GPIOC4	I/O	GPIO C4 share with 8052 UART TXD or ISP TX.
10	6	5	5	9	GPIOC5	I/O	GPIO C5 share with PWM0 output or HDMI CEC input or external IRQ0 interrupt input
11	7	6		10	GPIOC6	I/O	GPIO C6 share with 8052 UART RXD1 or SPI MISO
12	8	7		11	GPIOC7	I/O	GPIO C7 share with 8052 UART TXD1 or SPI SCK
16	9	8	6	12	NRES	I	Reset pin, active low (internal pull high)
17	10	9	7	13	GPIOA0	I/O	GPIO A0 share with PWM1 or analog compare output or 8052 P0.0
18	11	10	8	14	GPIOA1	I/O	GPIO A1 share with IR input or 8052 P0.1
19	12			15	GPIOA2	I/O	GPIO A2 share with HDMI CEC input or 8052 P0.2
20	13	11	9	16	GPIOA3	I/O	GPIO A3 share with PWM2 output or external IRQ1 interrupt input
21	14	12	10	17	GPIOA4	I/O	GPIO A4 share with slave SPI STB input or PWM3 output
22	15	13		18	GPIOA5	I/O	GPIO A5 share with SPI data master output/slave input or 8052 P0.3
23	16	14	11	19	SDA	I/O	Slave I2C SDA share with ISP I2C SDA
25	17	15	12	20	SCL	I/O	Slave I2C SCL share with ISP I2C SCL
28	18			21	GPIOA6	I/O	GPIO A6
29	19	16	13	22	VSS	PWR	Ground
29	19	16	13	23	VSS	PWR	Ground
29	19	16	13	24	VSS	PWR	Ground
30	19	16	13	25	AVSS	PWR	Ground for ADC
31	20			26	GPIOA7	I/O	GPIO A7 share with AREF(analog reference voltage).
32	21	17	14	27	GPIOB0	I/O	GPIO B0 share with ADC0 input or C-touch input0 or analog comparator input 0 or external IRQ2 interrupt input.
33	22	18	15	28	GPIOB1	I/O	GPIO B1 share with ADC1 input or C-touch input1 or analog comparator input 1 or external IRQ3 interrupt input
34	23			29	GPIOB2	I/O	GPIO B2 share with ADC2 input or C-touch input2.
35	24			30	GPIOB3	I/O	GPIO B3 share with ADC3 input or C-touch input3.
36	25			31	GPIOB4	I/O	GPIO B4 share with ADC4 input or C-touch input4.
				32	NC1		
39	26			33	GPIOB5	I/O	GPIO B5 share with ADC5 input or C-touch input5.
40	27	19		34	GPIOB6	I/O	GPIO B6 share with ADC6 input or C-touch input6.
41	28	20	16	35	GPIOB7	I/O	GPIO B7 share with ADC7 input or C-touch input7.
				36	NC2		
42	29	1	1	37	CAP18	PWR	1.8v LDO filter (connect with 4.7u+0.1u capacitor)

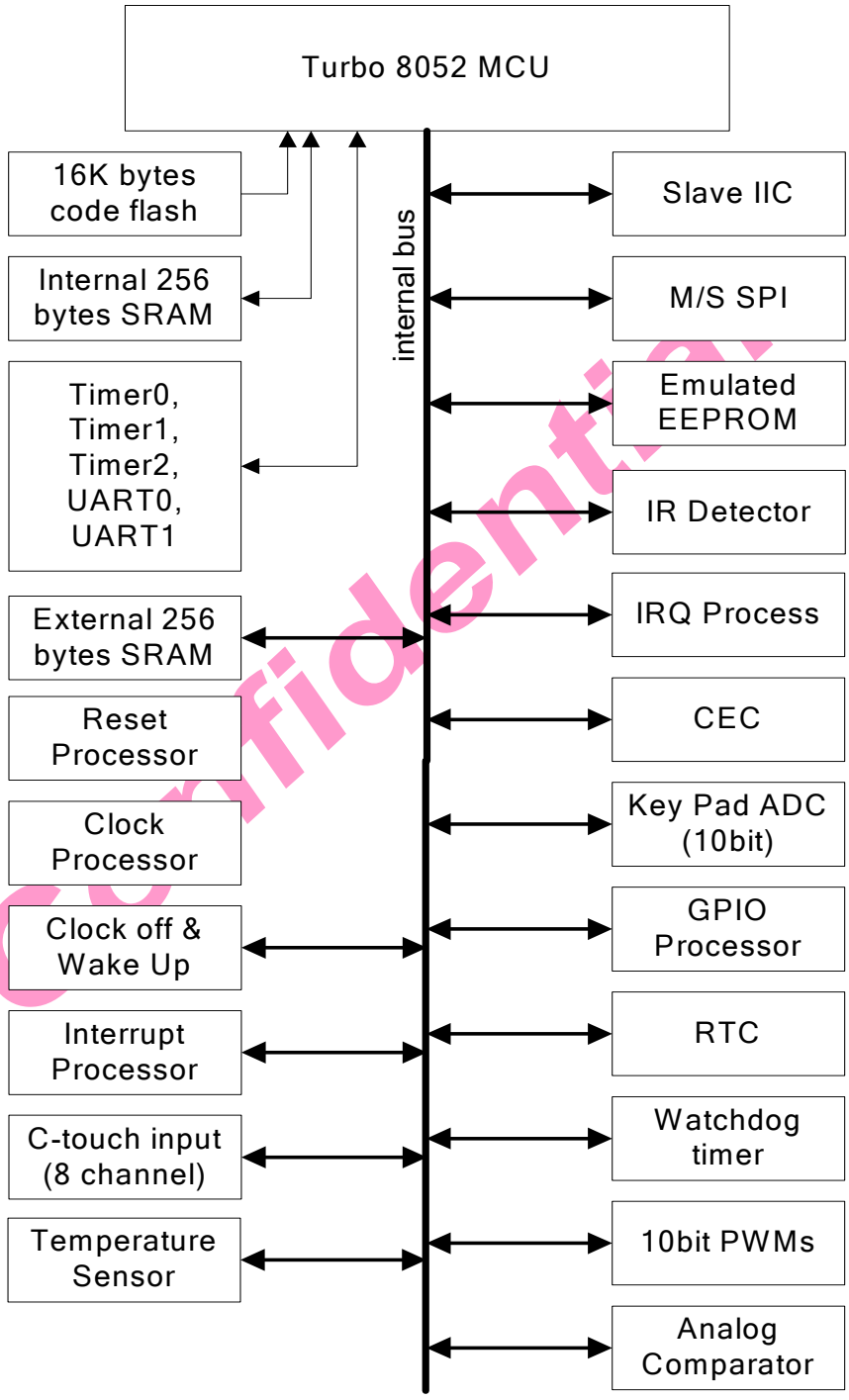
42	29	1	1	38	CAP18	PWR	
43	30	2	2	39	VDD5	PWR	Power 5v
44	31	2	2	40	CAP33	PWR	3.3v LDO filter (connect with 4.7u+0.1u capacitor)
44	31	2	2	41	CAP33	PWR	
				42	NC3		
2	32	2	2	1	VDD_RTC	PWR	RTC Power 3.3V

(a) All GPIOs have Schmitt trigger input.
(b) When use slave I2C or UART, the external circuit need pull high
(c) **GPIOA7, GPIOB7 ~ 0, GPIOC1 and XTALI MAX input are +3.6v** and the other GPIOs MAX input is +5.5v
(d) CEC pin shared with GPIOA2/GPIOC5 depends on CEC_IO_SLT register (Index 02H-bit 4)

3. Selection Guide

Part Number	51F516-RG480WT	51F516-UG320WT	51F516-OG200WT	51F516-SG161WT	51F516-HXXXWT
16K Flash Memory	V	V	V	V	V
RAM 512 Byte	V	V	V	V	V
UART	2	2	2	1	2
WDT	V	V	V	V	V
C-touch input	8	8	4	3	8
PWM output	4	4	4	4	4
Hardware universal IR Receiver	V	V	V	V	V
Hardware HDMI CEC	V	V	V	V	V
Slave I2C	V	V	V	V	V
Master/Slave SPI	V	V	V	-	V
10 bit ADC input	8	8	4	3	8
Temperature Sensor	V	V	V	V	V
Analog Comparator	V	V	V	V	V
RTC mode	V	V	-	-	V
NRST pin	V	V	V	V	V
GPIO	24	23	14	10	24
Power	5v/3.3v	5v/3.3v	3.3v	3.3v	5v/3.3v
Package	48 pin LQFP	32 pin QFN	20 pin SSOP	16 pin SOP	DIE

4. Functional Block Diagram



5. Functional Description

5.1. MCU

5.1.1. Internal MCU

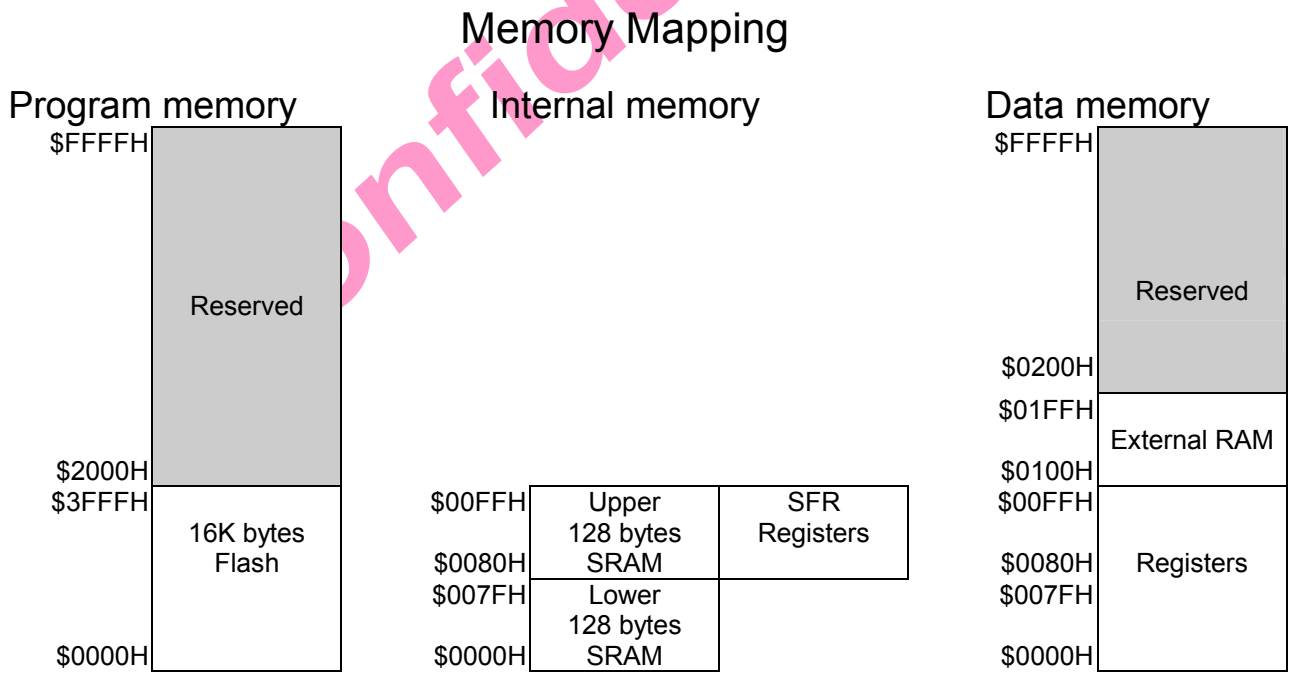
Embedded 8-bit 1T 8052 compatible CPU with 16-bit address and 8-bit data bus operates at 12MHz,6MHz, 3Mhz, 2MHz, 128KHz

5.1.2. RAM

The SRAM include :
128 bytes internal SRAM are from 0x0000H to 0x007FH (direct & indirect addressing)
128 bytes internal SRAM are from 0x0080H to 0x00FFH (indirect addressing)
256 bytes external SRAM are from 0x0100H to 0x01FFH

5.1.3. Flash Memory

MAX F/W program address is located from $0000h to $3FFFh (16k bytes).



5.1.4. 8052 Timer0, Timer1, Timer2, UART0, UART1, INT0, INT1

INT0/INT1 cause by LVD, WDT, C_TOUCH, SPI, SIIC, CEC, IR detector, Key pad ADC, RTC 1s and input toggle interruption

If UART0 is used, the EN_UART0_IO register has to be set “1”.
If UART1 is used, the EN_UART1_IO register has to be set “1”.

5.1.5. SFR(SPECIAL FUNCTION REGISTER) MAP

F8									FF
F0	B								F7
E8									EF
E0	ACC		ReP2						E7
D8	SCON1	SBUF1	SBRG1H	SBRG1L					DF
D0	PSW								D7
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CF
C0									C7
B8	IP								BF
B0									B7
A8	IE								AF
A0									A7
98	SCON	SBUF	SBRGH	SBRGL					9F
90									97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	*P0*	SP	DPL	DPH	DPL1	DPH1	DPS	PCON	87

bit addressable

6 source interrupt information:

Interrupt Source	Vector Address	Polling Sequence within Priority level	Enabled required settings	Interrupt type edge/level
External Interrupt 0	03H	1	IE.0	TCON.0
Timer 0	0BH	2	IE.1	--
External Interrupt 1	13H	3	IE.2	TCON.2
Timer 1	1BH	4	IE.3	--
Serial Port 0 (UART0)	23H	5	IE.4	--
Timer 2	2BH	6	IE.5	--
Serial Port 1 (UART1)	33H	7	IE.6	--

B: Address : F0H

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

ACC: Address : E0H

7	6	5	4	3	2	1	0

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Accumulator. The instruction use the accumulator as both source and destination for calculations and moves.

P0: Address: 80H

7	6	5	4	3	2	1	0
				P0.3	P0.2	P0.1	P0.0

ReP2: Address E2H

7	6	5	4	3	2	1	0
ReP2.7	ReP2.6	ReP2.5	ReP2.4	ReP2.3	ReP2.2	ReP2.1	ReP2.0

It will replace P2[HighByte Address] by ReP2 when the instructions, MOVX @Ri, A / MOVX A, @Ri, have been executed.

PSW(Program Status Word): Address : D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	PARITY

CY: Carry Flag, CY is set if the operation result in a carry out of (during addition) or a borrow into (during subtraction) the high-order bit of the result; otherwise CY is cleared.

AC: Auxiliary-Carry Flag. AC is set if the operation result in a carry out of the low-order 4 bits of the result (during addition) or a borrow from the high-order bits into the low-order 4 bits (during subtraction); otherwise AC is cleared.

F0: User Flag0. General-purpose flag.

RS1, RS0: Register Bank Select Bits 1 and 0. These bits select the memory locations that comprise the active bank of the register file.

RS1	RS0	Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

OV: Overflow Flag. This bit is set if an addition or signed variables results in an overflow error (i.e., if the magnitude of the sum or difference is too great for the seven LSBs in 2's-complement representation). The overflow flag is also set if multiplication product overflows one byte or if a division by zero is attempted.

PARITY: Parity Flag. This bit indicates the parity of accumulator. It is set an add number of bits in the accumulator are set. Otherwise, it is cleared. Not all instructions update the parity bit. The parity bit is set or cleared by instructions that change the contest to the accumulator.

IP (8052 interrupt priority register) Address : B8H

7	6	5	4	3	2	1	0
	PS1	PT2	PS	PT1	PX1	PT0	PX0

"PS1" : IP.6, Define the serial port 1 interrupt priority level. PS1 = 1 program it to higher priority level.

IE (8052 interrupt enable register) Address : A8H

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

ES1 :IE.6, Enables/disables the Serial Port 1 interrupt. If ES1 = 0, the Serial Port 1 interrupt is disabled.

TCON (8052 Timer 0/1 control register) Address: 88H

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

IE0: If IT0 = 1, IE0 is set/cleared automatically by hardware when interrupt is detected/serviced

IT0: External interrupt 0 is falling-edge/low-level triggered when this bit is set/cleared by software

IE1: If IT1 = 1, IE1 is set/cleared automatically by hardware when interrupt is detected/serviced

IT1: External interrupt 1 is falling-edge/low-level triggered when this bit is set/cleared by software

TF0: Timer 0 Overflow. This bit is set when Timer0 overflows. When Timer0 interrupt is enabled, this bit will cause the interrupt to be triggered.

TR0: Timer 0 Run. When set, timer 0 will be turned on. Otherwise, it is turned off.

TF1: Timer 1 Overflow. This bit is set when Timer1 overflows. When Timer0 interrupt is enabled, this bit will

cause the interrupt to be triggered.
TR1: Timer 1 Run. When set, timer 1 will be turned on. Otherwise, it is turned off.

TMOD(8052 Timer0/1 mode control register) Address: 89H

7	6	5	4	3	2	1	0
		M11	M10			M01	M00

M11	M10	MODE	
0	0	0	8-bit timer(TH1) with 5-bit prescalar (TL1)
0	1	1	16-bit timer/counter
1	0	2	8-bit auto-reload timer/counter(TL1). Reload from TH1 at overflow
1	1	3	Timer 1 halted. Retains count

M01	M00	MODE	
0	0	0	8-bit timer (TH0) with 5-bit prescalar (TL0)
0	1	1	16-bit timer
1	0	2	8-bit auto-reload timer(TL0). Reload from TH0 at overflow
1	1	3	TL0 is an 8-bit timer. TH0 is an 8 bit timer using timer 1's TR1 and TF1 bits

T2CON (8052 Timer 2 control register) Address: C8H

7	6	5	4	3	2	1	0
TF2					TR2		

TF2: Timer 2 Overflow. This bit is set when Timer2 overflows. When Timer2 interrupt is enabled, this bit will cause the interrupt to be triggered.
TR2: Timer 2 Run. When set, timer 2 will be turned on. Otherwise, it is turned off.

T2MOD (8052 Timer 2 mode control register) Address: C9H

7	6	5	4	3	2	1	0
							DCEN

DCEN: Down Count Enable Bit.

TL0 (8052 low byte of the timer 0 timer register) Address: 8AH

7	6	5	4	3	2	1	0
TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

TH0 (8052 high byte of the timer 0 timer register) Address: 8CH

7	6	5	4	3	2	1	0
TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

TL1 (8052 low byte of the timer 2 timer register) Address: 8BH

7	6	5	4	3	2	1	0
TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

TH1 (8052 high byte of the timer 2 timer register) Address: 8DH

7	6	5	4	3	2	1	0
TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

TL2 (8052 low byte of the timer 2 timer register) Address: CCH

7	6	5	4	3	2	1	0
TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

TH2 (8052 high byte of the timer 2 timer register) Address: CDH

7	6	5	4	3	2	1	0
TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

RCAP2L (8052 low byte of the Timer 2 reload/recapture register) Address: CAH

7	6	5	4	3	2	1	0
RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

This register stores 8-bit values to be loaded into or captured from the timer register TL2 in timer 2.

RCAP2H (8052 high byte of the Timer 2 reload/recapture register) Address: CBH

7	6	5	4	3	2	1	0
RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

This register stores 8-bit values to be loaded into or captured from the timer register TH2 in timer 2.

SP (Stack Point) Address: 81H

7	6	5	4	3	2	1	0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

The 8-bit SP contains the address at which the last byte was push onto the stack. This is also the address of the next byte that will be stopped. The SP is incremented before very PUSH operation. SP can be read or written to under software control.

DPL (DPTR, low byte of the 16-bit data pointer) Address: 82H

7	6	5	4	3	2	1	0
DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

DPH (DPTR, high byte of the 16-bit data pointer) Address: 83H

7	6	5	4	3	2	1	0
DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

DPL1 (DPTR, low byte of the 16-bit data pointer 1) Address: 84H

7	6	5	4	3	2	1	0
DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

DPH1 (DPTR, high byte of the 16-bit data pointer 1) Address: 85H

7	6	5	4	3	2	1	0
DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

DPS (Data point select) Address: 86H

7	6	5	4	3	2	1	0
							DPS

DPS: 0= Dph, Dpl will be selected
1= Dph-1, Dpl-1 will be selected

PCON (8052 power control register) Address : 87H

7	6	5	4	3	2	1	0
SMOD							

SCON (8052 UART0 control register) Address : 98H

7	6	5	4	3	2	1	0
SM0_1	SM0_2	SM0_3	REN_0	TB8_0	RB8_0	TI_0	RI_0

The additional serial port is similar as 8052's UART.

SBUF (8052 UART0 buffer) Address : 99H

7	6	5	4	3	2	1	0
SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0

SBRGH: Address : 9AH

7	6	5	4	3	2	1	0
SBRG_EN	BRG_M[10]	BRG_M[9]	BRG_M[8]	BRG_M[7]	BRG_M[6]	BRG_M[5]	BRG_M[4]

SBRGL: Address : 9BH

7	6	5	4	3	2	1	0
BRG_M[3]	BRG_M[2]	BRG_M[1]	BRG_M[0]	BRG_F[3]	BRG_F[2]	BRG_F[1]	BRG_F[0]

Serial Baud Rate Generator register.
When SBRG_EN (SBRGH.7) is set to high,

Baud rate, UART0 = $\frac{f_{osc}}{16*(BRG\_M[10:0]+\frac{BRG\_F[3:0]}{16})}$

Baud Rate Support Table :

	12MHz				
	Baud Rate Register	BRG_M	BRG_F	Actual	Error
2400	312.5	312	8	2400	0.0%
9600	78.125	78	2	9600	0.0%
19200	39.0625	39	1	19200	0.0%
57600	13	13	0	57692	0.16%
115200	6.5	6	8	115384	0.16%
230400	3.25	3	4	230769	0.16%

SCON1 (8052 UART1 control register) Address : D8H

7	6	5	4	3	2	1	0
SM1_1	SM1_2	SM1_3	REN_1	TB8_1	RB8_1	TI_1	RI_1

The additional serial port is similar as 8052's UART.

SBUF1 (8052 UART1 buffer) Address : D9H

7	6	5	4	3	2	1	0
SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

SBRG1H: Address : DAH

7	6	5	4	3	2	1	0
SBRG1_EN	BRG1_M [10]	BRG1_M[9]	BRG1_M[8]	BRG1_M[7]	BRG1_M[6]	BRG1_M[5]	BRG1_M[4]

SBRG1L: Address : DBH

7	6	5	4	3	2	1	0
BRG1_M[3]	BRG1_M[2]	BRG1_M[1]	BRG1_M[0]	BRG1_F[3]	BRG1_F[2]	BRG1_F[1]	BRG1_F[0]

Serial Baud Rate Generator register.
When SBRG1_EN (SBRG1H.7) is set to high,

Baud rate, UART1 = $\frac{f_{osc}}{16*(BRG1\_M[10:0]+\frac{BRG1\_F[3:0]}{16})}$

5.2. System Reset

All reset signals will last 16*12*1024*(RC Oscillator clock), For waiting system stable

RC oscillator clock = 12MHz, all reset signals will last 16*12*1024*F_{OSC} = 16.384ms

Reset sources

NRST

The NRST-Reset happens when there is a low level on the NRST pin.

*NRST pin digital filter setting by register 01H-bit7 “RST_NDF “

RST_NDF =1: Disable “NRST pin” digital filter(default)

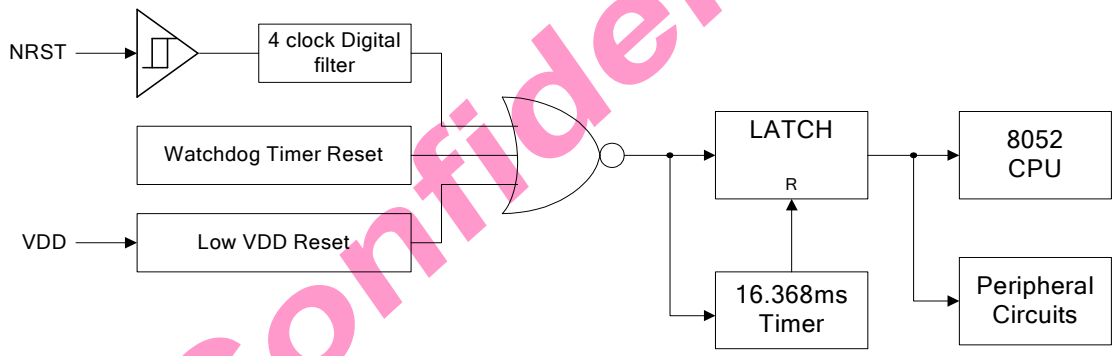
RST_NDF =0: “NRST” have digital filter (3-4 OSC clock)

Low VDD Reset

The Low-VDD-Reset is generated when VDD5 is below 1.4v.

Watchdog Timer Reset

The Watchdog-Timer-Reset happens when the watchdog timer is time out. Please refer to the watchdog timer section for more detail.



5.3. System Level Register

Index	Default	R/W	Bit	Name	Description
01	82	R/W	7	RST_NDF	1: "NRST pin" no digital filter(default) 0: "NRST pin" have digital filter
			6	OSC_OFF	FOR OSC OFF power down mode, Signals wake up MCU to MCU work after 256 RC OSC clock 1:Power down mode, turn off RC clock & system clock (system no clock) 0:Normal mode.
			5	OSC_OFF2	FOR OSC power down mode(OSC bias ON), Signals wake up MCU to MCU work after 8 RC OSC clock (at OSCOFF2_CLK_CTL=0) 1:Power down mode, turn off RC clock & system clock (system no clock) 0:Normal mode.
			4	MCU_OFF	FOR CLK OFF power down mode, Signals wake up MCU to MCU work after 4 RC OSC clock 1: Turn off all clock.(clock disable, rc oscillator on) 0: Normal mode
			3-2	Reserved	
			1	OSC32K_EN	1:32k oscillator enable. If the system is without external 32K crystal, this bit have be clear "0" 0:32k oscillator disable.
			0	PWR_SAVE	Power saving mode, Signals wake up MCU to MCU work after ΔT+ 256 RC OSC clock 1: Power saving mode 0: Normal mode
02	20	R/W	7	Reserved	
			6	OSCOFF2_CLK_CTL	OSCOFF2 wake up MCU to MCU work wait time control 1: wait 32 RC OSC clock 0: wait 8 RC OSC clock
			5	FLASH_POWER_CTL	1: Reduce flash power by timing share 0: No timing share (flash always enable)
			4	CEC_IO_SEL	1: CEC input shared with GPIOC5 0: CEC input shared with GPIOA2
			3	Reserved	
			2-0	CHG_CLK[2:0]	000 : MCU clock= 12MHz RC oscillator clock 001 : MCU clock= (12MHz RC oscillator clock)/2 010 : MCU clock= (12MHz RC oscillator clock)/4 011 : MCU clock= (12MHz RC oscillator clock)/12 1xx : MCU clock= 128KHz RC oscillator clock
03	00	R/W	7	DIS_GPC1_SMT	GPIOC1 SMT input buffer control. 1: Disable GPIOC1 SMT.(Read data =0) 0: Enable GPIOC1 SMT input.
			6	DIS_GPA7_SMT	GPIOA7 SMT input buffer control. 1: Disable GPIOA7 SMT.(Read data =0) 0: Enable GPIOA7 SMT input.
			5-0	Reserved	
04	00	R/W	7-4		For bit[3:0] write control =5: write enable Others: disable write bit[3:0] register.
			3	OSC12MRC_PD	1: 12MHz RC oscillator power down (when mcu_clk=32k)

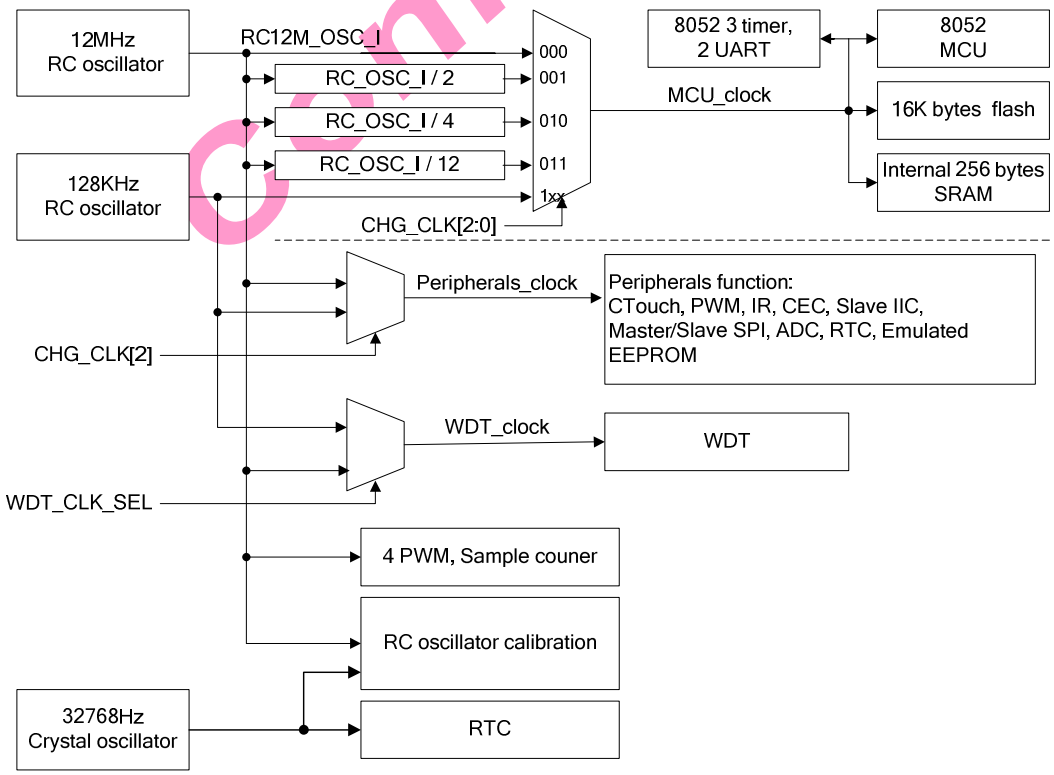
					0:12MHz RC oscillator enable
			2	OSC128KRC_PD	1:128kHz RC oscillator power down 0:128kHz RC oscillator enable
			1	PD_BPLDO33	LDO33 power control. (BIG LDO18) 1: Power down LDO33 0: Normal mode
			0	PD_LPLDO33	LPLDO33 power control (Low power LDO33) 1: Power down LPLDO33 0: Others: Normal mode
0F	20	R/W	7	PD_LVR	1: LVR disable 0: LVR enable
			6-0	TEST[6:0]	TEST[6:0] for internal test mode use. This byte must set 20H

(1) OFF mode

PWR_SAVE	OSC_OFF	MCU_OFF	RC12M_OSC_I	MCU_clock	Peripherals_ clock	Wake up wait MCU clock
0	0	0	ON	ON	ON	-
0	0	1	ON	OFF	OFF	4 clock
0	1	0	OFF	OFF	OFF	256 clock
1	0	0	OFF	OFF	OFF	ΔT+ 256 clock (*)

* Power save mode, signal wake up MCU to MCU work after internal regulator wake up + 256 RCOSC clock. Internal regulator wake up about 100ms.

(2) MCU clock option



5.4. Watchdog Timer

Watchdog timer will generate a reset pulse if CPU does not write 09H register within 8s or 1s or 2s or 33ms or 65ms. This function can be disabled by setting DIS_WDT bit.

Index	Default	R/W	Bit	Name	Description
08	00	R/W	7	DIS_WDT	1:Disable Watchdog Timer 0:Enable Watchdog Timer
			6	WDT_CLK_SEL	1:Clock source from 12MHz RC oscillator clock 0:Clock source from 128KHz RC oscillator clock
			5-1	Reserved	
		R	0	WDT_RST_EVT	H/W set and F/W clear(set DIS_WDT) 1: WDT event 0: No WDT event
09	00	R/W	7-3	Reserved	
			2-0	WDT_RST[2:0]	1xx: reset time = 8s 000:reset time = 1s (default) 001:reset time = 2s 010:reset time = 33ms 011:reset time = 65ms
0A	00	R/W	7-3	Reserved	
			2-0	WDT_DET[1:0]	1xx:detect time = 5s 000:detect time = 1s (default) 001:detect time = 2s 010:detect time = 33ms 011:detect time = 65ms

(1) WDT_DET_EVT will be clear by setting DIS_WDT bit and timing setting by WDT_DET.

(2) Reset Time with WDT_CLK_SEL

	WDT_CLK_SEL	
WDT_RST	12MHz RC oscillator clock	128KHz RC oscillator clock
000	1.05s	1.02s
001	2.10s	2.05s
010	32.77ms	32.0ms
011	65.54ms	64.0ms
1xx	8.23s	8.13s

(3) Detect Time with WDT_CLK_SEL

	WDT_CLK_SEL	
WDT_DET	12MHz RC oscillator clock	128KHz RC oscillator clock
000	1.05s	1.02s
001	2.10s	2.05s
010	32.77ms	32.0ms
011	65.54ms	64.0ms
1xx	5.24s	5.12s

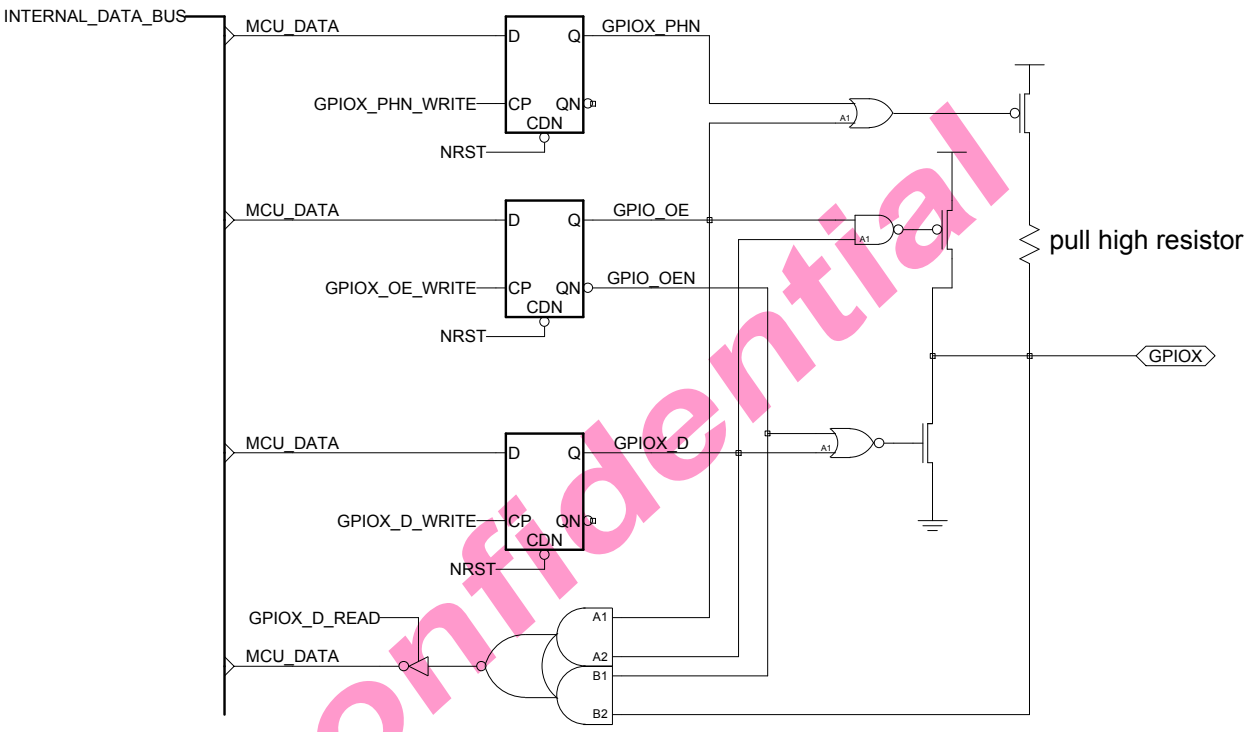
5.5. Low voltage Detect

Low voltage detector that monitors the VDD5 power supply.

Index	Default	R/W	Bit	Name	Description
0B	80	R/W	7	PD_LVD	1:Disable low voltage detect 0:Enable low voltage detect
			6-3	Reserved	
			2-1	LVD_SEL[2:0]	LVD detect voltage 00: < 2.5v 01: < 3v 10: < 3.5v 11: < 4v
			0	Reserved	

5.6. GPIO

The GPIOx0~ GPIOx7 are the general purpose IO shared with some special functions. When the special function is disabled, it is a general purpose I/O port. If it is configured as output, it could source/sink 4mA. If it is configured as input and GPIOx_PHN is “0”, it has an internal pull-up resistor. If the GPIOx is configured as input and the GPIOx_PHN is “1”, it doesn’t have an internal pull-up resistor.



Index	Default	R/W	Bit	Name	Description
10	00	R/W	7-0	GPIOA_OE[7:0]	GPIO A output enable 1: output 0: input
11	00	R/W	7-0	GPIOB_OE[7:0]	GPIO B output enable 1: output 0: input
12	00	R/W	7-0	GPIOC_OE[7:0]	GPIO C output enable 1: output 0: input
13	00	R/W	7-0	GPIOA_D[7:0]	Write : GPIO A output data Read : if GPIOA_OE=1, GPIO A output data if GPIOA_OE=0, GPIO A pin input data
14	00	R/W	7-0	GPIOB_D[7:0]	Write : GPIO B output data Read : if GPIOB_OE=1, GPIO B output data if GPIOB_OE=0, GPIO B pin input data
15	00	R/W	7-0	GPIOC_D[7:0]	Write : GPIO C output data Read : if GPIOC_OE=1, GPIO B output data if GPIOC_OE=0, GPIO B pin input data
16	FF	R/W	7-0	GPIOA_PHN[7:0]	1:Disable GPIO A[x] pull high 0:Enable GPIO A[x] pull high
17	FF	R/W	7-0	GPIOB_PHN[7:0]	1:Disable GPIO B[x] pull high 0:Enable GPIO B[x] pull high

18	FF	R/W	7-0	GPIOC_PHN[7:0]	1:Disable GPIO C[x] pull high 0:Enable GPIO C[x] pull high
19	FF	R/W	7-0	GPIOA_TPY[7:0]	1:GPIOA[x] output type push-pull. 0:GPIOA[x] output type open-drain.
1A	FF	R/W	7-0	GPIOB_TPY [7:0]	1:GPIOB[x] output type push-pull. 0:GPIOB[x] output type open-drain.
1B	FF	R/W	7-0	GPIOC_TPY [7:0]	1:GPIOC[x] output type push-pull. 0:GPIOC[x] output type open-drain.
1C	00	R/W	7	EN_SIIC_IO	1:Enable SIIC IO pad 0:Disable SIIC IO pad
			6	EN_SPI_IO	1:Enable SPI IO pad 0:Disable SPI IO pad
			5	EN_CEC_IO	1:Enable CEC IO pad 0:Disable CECIO pad
			4	EN_UART0_IO	1:Enable UART0 IO pad 0:Disable UART0 IO pad
			3-0	EN_PWM_IO[3:0]	1:Enable PWMx IO pad 0:Disable PWMx IO pad
1D	00	R/W	7-0	EN_AD_IO[7:0]	1:Enable ADC[x] IO pad 0:Disable ADC[x] IO pad
1E	00	R/W	7-0	EN_CTOUCH_IO [7:0]	1:Enable CTOUCH[x] IO pad 0:Disable CTOUCH [x] IO pad
1F	00	R/W	7	EN_ACOMP_IO	1:Enable analog comparator IO PAD 0:Disable analog comparator IO PAD
			6	EN_UART1_IO	1:Enable UART1 IO pad 0:Disable UART1 IO pad
			5-4	Reserved	
			3-0	EN_P0_IO[3:0]	1: Enable 8051 P0[x] IO pad (*a) 0: Disable 8051 P0[x] IO pad

(*a) EN_P0_IO[3:0]: enable P0[3:0] IO PAD, IO Type depend on GPIOx_TYP [x] setting.
(*b) GPIOC1 notice for UG320 package type, PIN#1(XTALI) must be tied low when PIN#2(GPIOC1/XTALO) is assigned to GPIO port.
(*c) Some GPIO port have not bonding at 20pin or 16pin package type. These pins must enable pull high for power saving.

5.7. Wake-up & toggle Register

Index	Default	R/W	Bit	Name	Description
20	00	R/W	7	I2C_WAKE	1:MCU wake up by SCL/SDA toggle 0:Disable MCU wake up SCL/SDA toggle
			6	WDT_WAKE	1:MCU wake up by WDT detect event (*c) 0:Disable MCU wake up WDT detect event
			5	ACOMP_WAKE	1:MCU wake up by analog comparator 0:Disable MCU wake up by analog comparator
			4	RTC_500MS_ WAKE	1:MCU wake up by RTC 500ms (*d) 0:Disable MCU wake up by RTC 500ms
			3	LVD_WAKE	1:MCU wake up by LVD 0:Disable MCU wake up by LVD
			2	CTOUCH_WAKE	1:MCU wake up by C Touch event 0:Disable MCU wake up by C Touch event
			1	Reserved	
			0	IR_WAKE	1:MCU wake up by IR 0:Disable MCU wake up by IR
21	00	R/W	7-0	GPIOA_WK[7:0]	1: MCU wake up by GPIOA[x] toggle 0: Disable MCU wake up by GPIOA[x] toggle
22	00	R/W	7-0	GPIOB_WK[7:0]	1: MCU wake up by GPIOB[x] toggle 0: Disable MCU wake up by GPIOA[x] toggle
23	00	R/W	7-0	GPIOC_WK[7:0]	1: MCU wake up by GPIOC[x] toggle 0: Disable MCU wake up by GPIOC[x] toggle
24	00	R	7	I2CPIN_TOG	1:I2C pin toggle 0: No I2C pin toggle
			6	WDT_EVT	1 : WDT detect event 0 : No WDT detect event
			5	ACOMP_TOG	1:Analog comparator toggle 0:Analog comparator toggle
			4	RTC_500MS_ TOG	1:RTC 500ms toggle 0:No RTC 500ms toggle
			3	LVD_EVT	1 : LVD event 0 : No LVD event
			2	CTOUCH_EVT	1 : CTOUCH counter event 0 : No CTOUCH counter event
			1	Reserved	
			0	IR_ TOG	1:IR toggle 0:No IR toggle
25	00	R	7-0	GPIOA_TOG[7:0]	1: GPIOA[x] toggle 0: No GPIOA[x] toggle
26	00	R	7-0	GPIOB_TOG[7:0]	1: GPIOB[x] toggle 0: No GPIOB[x] toggle
27	00	R	7-0	GPIOC_TOG[7:0]	1: GPIOC[x] toggle 0: No GPIOC[x] toggle
28	00	R	7	CLR_IN_TOG	1:Clear all input toggle 0:Disable clear all input toggle
			6-1	Reserved	
			0	IN_TOG	1:Or all input toggle 0:No input toggle
29	00	R/W	7-5	reserved	
			4	ETM_WAKE	1:MCU wake up by enhance Timer event 0:Disable MCU wake up enhance Timer event
			3-1	Reserved	

			0	ETM _TOG	1: Enhance Timer event 0: No Enhance Timer event

(a) OSC_OFF wake up source including I2C, WDT, ACOMP, RTC, LVD, GPIOA, GPIOB and GPIOC; power down procedure :
(1) Set RST_NDFILT=1,
(2) Disable watchdog timer reset
(3) Select wake up source
(4) Set CLR_IN_TOG
(5) Set OSC_OFF =1 & OSC_OFF =0
(6) Signals wake up MCU to MCU work : 256* MCU_clock
If XTAL clock is 12MHz, Signals wake up MCU to MCU work: 21.33us

(b) MCU_OFF wake up source including I2C, WDT, ACOMP, RTC, LVD, CTOUCH, IR, GPIOA, GPIOB and GPIOC, enhance Timer; power down procedure :
(1) Set RST_NDFILT=1,
(2) Disable watchdog timer reset
(3) Select wake up source
(4) Set CLR_IN_TOG
(5) Set MCU_OFF =1 & MCU_OFF =0
(6) Signals wake up MCU to MCU work : 4*MCU_clock
If XTAL clock is 12MHz, Signals wake up MCU to MCU work: 333.33ns

(*c) WDT detect event timing setting by WDT_DET.(index 0A-bit 1:0)

(*d) RTC_500MS_WAKE: wake up time depend on RTC_FS[2:0] (index BE-bit 2:0)

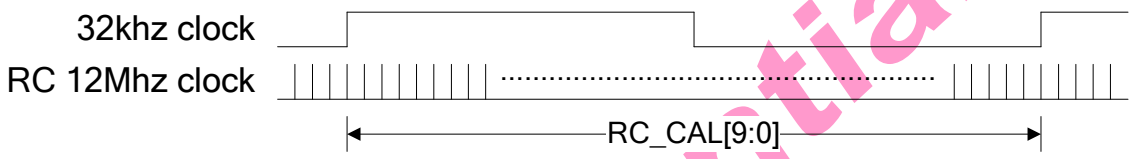
RTC_FS[2:0]	Wake up time
000	No
001	2s
010	500ms
011	62.5ms
100	7.8125ms
101	0.9765625ms
110	488.28125us
111	15.2587890625us

5.8. RC Oscillator Calibration

RC12MHz oscillator clock calibration clock source from 32768Hz crystal oscillator

Index	Default	R/W	Bit	Name	Description
2A	00	R	7-0	RC_CAL[9:2]	RC counter [9:2] calibrate with external clock
2B	00	R	7-2	Reserved	
			1-0	RC_CAL[1:0]	RC counter [1:0] calibrate with external clock
2C	40	R/W	7	Reserved	
			6-4	RC_IADJ_C[2:0]	RCOSC coarse current selection. Default is 100.
			3-0	RC_IADJ_F[3:0]	RCOSC fine current selection. Default is 0000

(*) When read register 2AH/2BH, F/W have to read RC_CAL[9:0] twice, for MCU read high byte & low byte is not simultaneous



5.9. 8051 Interrupt

INT0 is cause by enhance timer, LVD, WDT, ACOMP, C_TOUCH, SPI, SIIC, CEC, IR detector, Key pad ADC, RTC 1s and input toggle interruption.. Each interrupt can be enabled/disabled independently by programming IE0_XXX register and identified by IF0_XXX register.

INT1 is cause by enhance timer, LVD, WDT, ACOMP, C_TOUCH, SPI, SIIC, CEC, IR detector, Key pad ADC, RTC 1s and input toggle interruption.. Each interrupt can be enabled/disabled independently by programming IE1_XXX register and identified by IF1_XXX register.

Index	Default	R/W	Bit	Name	Description
30	00	R/W	7	IE0_ETM	1:Enable enhance timer event interrupt 0:Disable enhance timer event interrupt
			6	IE0_IN_TOG	1:Enable all-input toggle interrupt 0:Disable all-input toggle interrupt
			5	IE0_LVD	1:Enable LVD interrupt 0:Disable LVD interrupt
			4	IE0_WDT	1:Enable WDT interrupt 0:Disable WDT interrupt
			3	IE0_ACOMP	1:Enable ACOMP interrupt 0:Disable ACOMP interrupt
			2	IE0_CTOUCH	1:Enable C touch interrupt 0:Disable C touch interrupt
			1	IE0_SPI	1:Enable SPI interrupt 0:Disable SPI interrupt
			0	IE0_SIIC	1:Enable SIIC interrupt 0:Disable SIIC interrupt
31	00	R/W	7-4	IE0_IRQ[3:0]	1: Enable external IRQ[3:0] interrupt 0: Disable external IRQ[3:0] interrupt
			3	IE0_RTC_1S	1:Enable RTC 1s interrupt 0:Disable RTC 1s interrupt
			2	IE0_KADC	1:Enable key pad ADC interrupt 0:Disable key pad ADC interrupt
			1	IE0_IR	1:Enable IR detect interrupt 0:Disable IR detect interrupt
			0	IE0_CEC	1:Enable CEC interrupt 0:Disable CEC interrupt
32	00	R/W	7	IE1_ETM	1:Enable enhance timer event interrupt 0:Disable enhance timer event interrupt
			6	IE1_IN_TOG	1:Enable all-input toggle interrupt 0:Disable all-input toggle interrupt
			5	IE1_LVD	1:Enable LVD interrupt 0:Disable LVD interrupt
			4	IE1_WDT	1:Enable WDT interrupt 0:Disable WDT interrupt
			3	IE1_ACOMP	1:Enable ACOMP interrupt 0:Disable ACOMP interrupt
			2	IE1_CTOUCH	1:Enable C touch interrupt 0:Disable C touch interrupt
			1	IE1_SPI	1:Enable SPI interrupt 0:Disable SPI interrupt
			0	IE1_SIIC	1:Enable SIIC interrupt 0:Disable SIIC interrupt
33	00	R/W	7-4	IE1_IRQ[3:0]	1: Enable external IRQ[3:0] interrupt 0: Disable external IRQ[3:0] interrupt

			3	IE1_RTC_1S	1:Enable RTC 1s interrupt 0:Disable RTC 1s interrupt
			2	IE1_KADC	1:Enable key pad ADC interrupt 0:Disable key pad ADC interrupt
			1	IE1_IR	1:Enable IR detect interrupt 0:Disable IR detect interrupt
			0	IE1_CEC	1:Enable CEC interrupt 0:Disable CEC interrupt

(a) IE0_xx : enable 8051 INT0 interrupt
IE1_xx : enable 8051 INT1 interrupt

Interrupt1 Flag Register

Index	Default	R/W	Bit	Name	Description
34	00	R	7	IF_ETM	1:Event of enhance timer interrupt 0:No event of enhance timer interrupt
			6	IF_IN_TOG	1:Event of all-input toggle interrupt 0:No all-input toggle interrupt
			5	IF_LVD	1:Event of low voltage detect 0:No event of low voltage detect
			4	IF_WDT	1:Event of WDT 0:No event of WDT
			3	IF_ACOMP	1:Event of ACOMP 0:No event of ACOMP
			2	IF_CTOUCH	1:Event of C touch interrupt 0:No event of C touch interrupt
			1	IF_SPI	1:Event of SPI interrupt 0:No event of SPI interrupt
			0	IF_SIIC	1:Event of SIIC interrupt 0:No event of SIIC interrupt
35	00	R	7-4	IF_IRQ[3:0]	1: Event of external IRQ[3:0] interrupt 0: No event of external IRQ[3:0] interrupt
			3	IF_RTC_1S	1:Event RTC 1s interrupt 0:No event of RTC 1s interrupt
			2	IF_KADC	1:Event of key pad ADC interrupt 0:No event of key pad ADC interrupt
			1	IF_IR	1:Event of IR detect interrupt 0:No event of IR detect interrupt
			0	IF_CEC	1:Event of CEC interrupt 0:No event of CEC interrupt

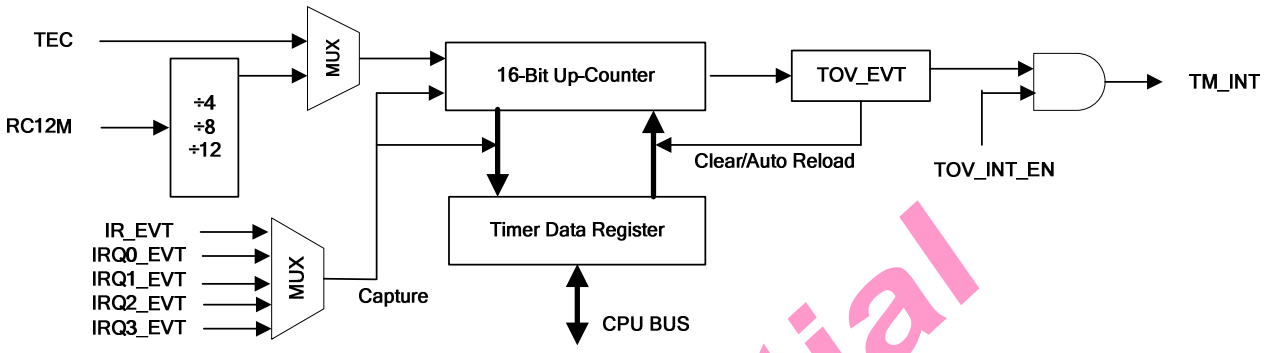
5.10. External IRQ Interrupt

IRQ Polling Flag Register

Index	Default	R/W	Bit	Name	Description
3A	00	R	7-4	EVT_IRQ[3:0]	1: Event of external IRQ[x] 0: No event of external IRQ[x]
		W	3-0	CLR_IRQ[3:0]	1: Clear event of external IRQ[x] 0: No clear event of external IRQ[x]
3B	00	R/W	7-4	IRQ_CHG[3:0]	1: rising & falling trigger 0: single edge trigger
			3-0	IRQ_EDGE[3:0]	1: falling trigger 0: rising trigger

5.11. Enhance Timer/Counter

16-bit Timer/Counter with capture mode



Control Register 1

Index	Default	R/W	Bit	Name	Description
80	00	R/W	7	TC_EN	Timer/Counter Enable
			6	EXC_EN	External clock enable =1, clock source is TEC(GPIOA0), ignore TCC_SEL =0, clock source is RC OSC
			5-4	TCC_SEL[1:0]	Timer/Counter Clock Source Select =00, RC clock =01, ÷4 =10, ÷8 =11, ÷12
			3	CAP_RL_SEL	Capture Mode/Auto Reload Mode Select =1, Capture Mode =0, Timer with auto reload, ignore CAP_SEL
			2-0	CAP_SEL[2:0]	Capture Source Select Bit[2:0] =1xx, IR edge event =000, IRQ0 event =001, IRQ1 event =010, IRQ2 event =011, IRQ3 event

Control Register 2

Index	Default	R/W	Bit	Name	Description
81	00	R/W	7	TCOV_INT_EN	Timer/Counter Overflow Interrupt Enable
			6-4	Reserved	
			3	TCOV_EVT (1)	Timer/Counter Overflow Flag
			2-0	Reserved	

* (1) TCOV_EVT will be clear by setting 81H-bit 3.

Timer/Counter Data

Index	Default	R/W	Bit	Name	Description
82	00	R/W	7-0	TCDR[15:8]	Capture Mode : Capture value high byte Auto-Reload Mode : auto-reload value high byte
83	00	R/W	7-0	TCDR[7:0]	Capture Mode : Capture value low byte Auto-Reload Mode : auto-reload value low byte

5.12. C Touch Counter

Index	Default	R/W	Bit	Name	Description
40	00	R/W	7	SMP_CNT_EN	"1": Enable C touch sample counter "0": Disable C touch counter sample (Power-down Digital)
			6-3	Reserved	
			2-0	SCAN_IN_SEL [2:0]	Select sensor input channel "000" select SI0 input "001" select SI1 input … "111" select SI7 input
41	08		7-0	SCAN_TIME[7:0]	Numbers of scan time per-channel 0000_0000: 1 time 0000_0001: 2 times …. 1111_1111: 256 times

Index	Default	R/W	Bit	Name	Description
42	00	R/W	7	SCAN_CMP_EN	1: Enable SCAN_CMP event 0: Disable SCAN_CMP event
			6	SCAN_OV_THR_ EN	1: Enable SCAN_OV_THR_EN event 0: Disable SCAN_OV_THR_EN event
			5-0	Reserved	
43	00	R	7	SCAN_CMP	1: Scan complete 0: No event
			6	SCAN_OV_THR	1: Sample counter large than the threshold counter 0: No event
			5-0	Reserved	
44	00	W	7	CLR_SCAN_INT	Clear interrupt 1: Clear interrupt 0: No even
			6-0	Reserved	

Index	Default	R/W	Bit	Name	Description
45	FF	R/W	7-0	SMP_CNT_THR [7:0]	Sample counter threshold low byte
46	FF	R/W	7-0	SMP_CNT_THR [15:8]	Sample counter threshold high byte

Index	Default	R/W	Bit	Name	Description
47	00	R	7-0	SMP_CNT[7:0]	Sample counter low byte
48	00	R	7-0	SMP_CNT[15:8]	Sample counter high byte

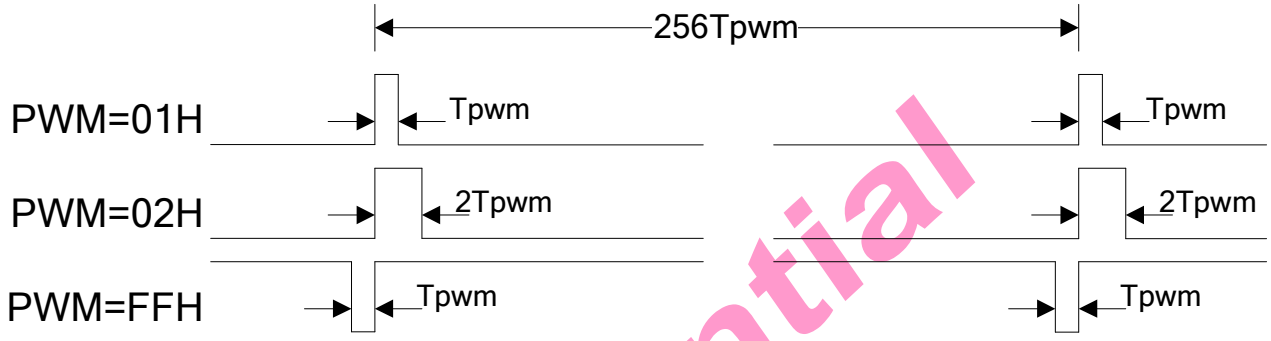
Index	Default	R/W	Bit	Name	Description
49	02	R/W	7-4	Reserved	
			3-0	SMP_I_SEL[3:0]	Set sample counter RC charge current Bit0 : 4uA Bit1 : 4uA Bit2 : 4uA Bit3 : 4uA "0001": 4uA "0011": 8uA

					“0111”: 12uA “1111”: 16uA
4A	1B	R/W	7-5	Reserved	
			4-3	SMP_RC_PL[1:0]	Discharge path select, select NMOS path PL[0]:Small PL[1]:Middle
			2-1	SMP_RC_PL_ DLY[1:0]	Sample counter RC pull low delay “00” 3us “01” 6us “10” 8us “11” 12us
			0	SMP_RC_APL_ EN	1: Enable sample RC analog pull low 0: Enable sample RC digital pull low

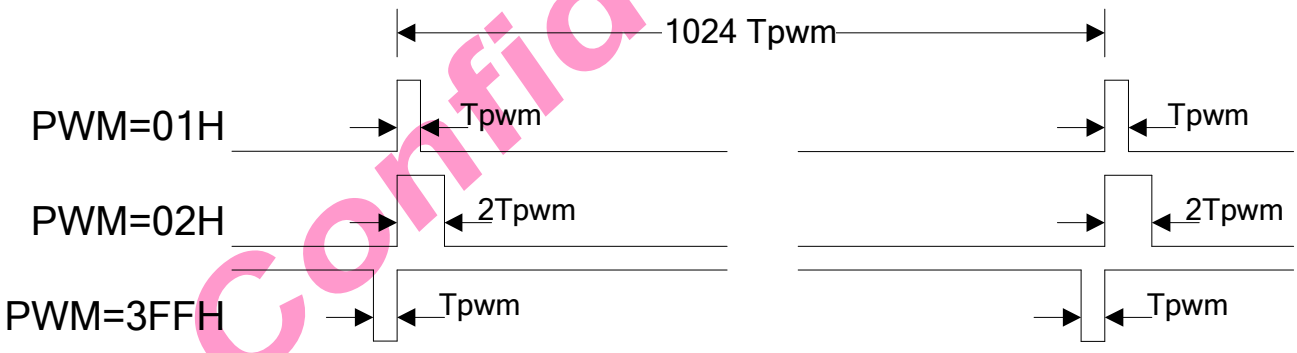
5.13. PWM

PWM0 ~ PWM3 : 8-bit/10bit PWM and 3.3V push-pull / open drain output, select by GPIOx_TYP[x], shared with I/O GPIOC5, GPIOA0, GPIOA3 and GPIOA4

(a) 8 bit PWM, the corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/256 to 255/256. PWM output clock=PWM_BAS_CLK / ((PWM_CLKx +1)* 256)



(b) 10 bit PWM, the corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/1024 to 1023/1024. PWM output clock=PWM_BAS_CLK / ((PWM_CLKx +1)* 1024)

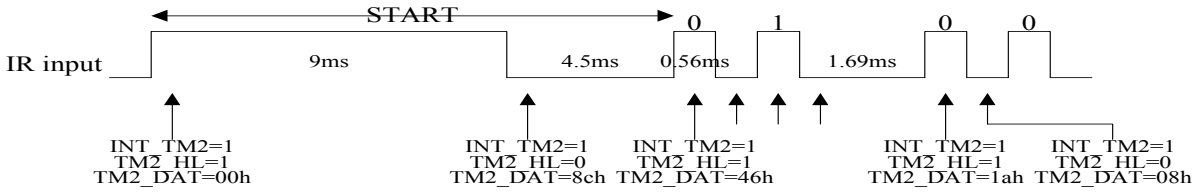


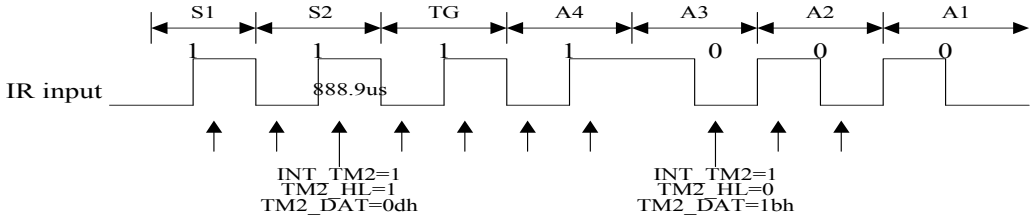
Index	Default	R/W	Bit	Name	Description
50	00	R/W	7-4	PWM_EN[3:0]	1: Enable PWMx function 0: Disable PWMx function
			3-0	PWM_BIT_SEL [3:0]	Select PWMx resolution 1: PWM[x] = 8 bit 0: PWM[x] = 10 bit
51	00	R/W	7-2	Reserved	
			1-0	PWM_BAS_CLK	PWM base clock select 00: RC12MHz oscillator clock 01: RC12MHz oscillator clock /2 10: RC12MHz oscillator clock /4 11: RC12MHz oscillator clock /12
52	00	R/W	7	Reserved	
			6-0	PWM_CLK0[6:0]	Select PWM0 clock
53	00	R/W	7	Reserved	
			6-0	PWM_CLK1[6:0]	Select PWM1 clock
54	00	R/W	7	Reserved	
			6-0	PWM_CLK2[6:0]	Select PWM2 clock
55	00	R/W	7	Reserved	

			6-0	PWM_CLK3[6:0]	Select PWM3 clock
56	80	R/W	7-0	PWM0[7:0]	Select duty cycle of PWM 0 output. 00000000: duty cycle = 0 00000001: duty cycle = 1/1024 00000010: duty cycle = 2/1024 : 11111110: duty cycle = 254/1024 11111111: duty cycle = 255/1024
57	02	R/W	7-2	Reserved	
			1-0	PWM0[9:8]	Select duty cycle of PWM 0 output [9:8]:
58	80	R/W	7-0	PWM1[7:0]	Select duty cycle of PWM 1 output [7:0]
59	02	R/W	7-2	Reserved	
			1-0	PWM1[9:8]	Select duty cycle of PWM 1 output [9:8]
5A	80	R/W	7-0	PWM2[7:0]	Select duty cycle of PWM 2 output [7:0]
5B	02	R/W	7-2	Reserved	
			1-0	PWM2[9:8]	Select duty cycle of PWM 2 output [9:8]
5C	80	R/W	7-0	PWM3[7:0]	Select duty cycle of PWM 3 output [7:0]
5D	02	R/W	7-2	Reserved	
			1-0	PWM3[9:8]	Select duty cycle of PWM 3 output [9:8]

5.14. Remote Control

Index	Default	R/W	Bit	Name	Description
60	00	R/W	7	EN_IR	1:Enable IR 0:Disable IR
			6	IR_SEDG	1:single edge trigger 0:both edge trigger
			5	IR_RF	1:rising edge trigger 0:falling edge trigger
			4	EN_OV_INT	1:Enable over flow interrupt 0:Disable over flow interrupt
			3-1	PRE_SCAL[2:0]	IR Pre scaler time 000: 1us 001: 8us 010: 32us 011: 64us 100: 128us 101: 256us 110: 512us 111: 1024us
			0	CLR_IR_INT	1:Clear interrupt “IR_INT 0:No clear interrupt “IR_INT
61	04	R	7-3	Reserved	
			2	IR_HL	Read IR input H/L
			1	IR_OVFLW	1:IR over flow interrupt 0:No IR over flow interrupt
			0	IR_INT	1: IR interrupt = edge trigger + over flow 0:No IR interrupt
62	00	R	7-0	IR_CNT[7:0]	IR counter
63	00	R/W	7-4	Reserved	
			3-0	IR_FILTER[3:0]	IR digital filter =0H : 2*84ns = 168ns digital filter =1H : 1*32us = 32us digital filter =FH : 15*32us = 480us digital filter

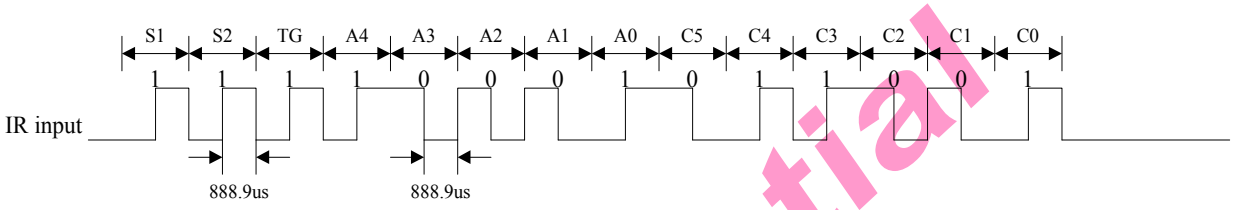




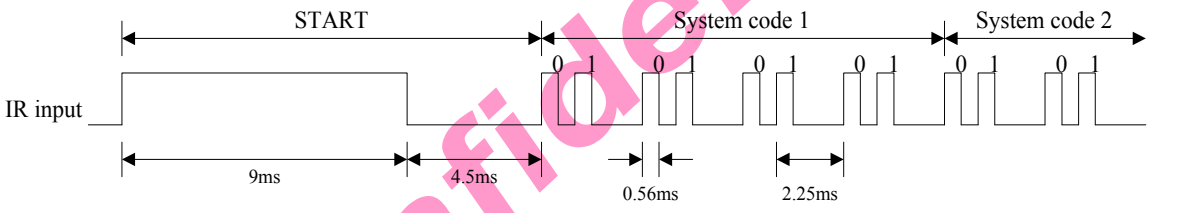
IR Timing Table

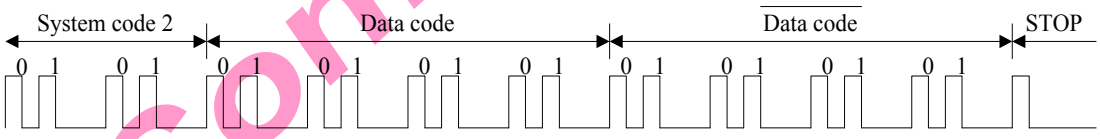
		STARTH	STARTL	pulse	H period	L period
TC9290	data	9	4.5	0.56	2.25	1.125
(TC9243)	keep	9	4.5	0.56	2.25	
NEC uPD6P5	data	9	4.5	0.56	2.25	1.125
	keep	9	2.25	0.56		
Philips RC5	data	0.889	0.889	0.889	0.889	0.889

PHILIPS RC5

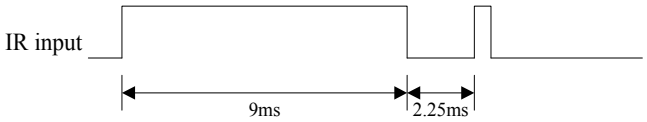


NEC & TOSHIBA Data

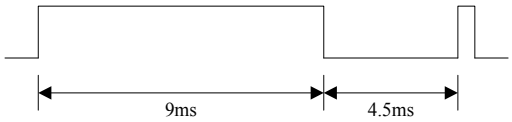




TOSHIBA Data Keep



NEC Data Keep



5.15. HDMI CEC Control

Control

Index	Default	R/W	Bit	Name	Description
70	00	R/W	7	EN_CEC	1: Enable HDMI CEC 0: Disable HDMI CEC
			6-5	Reserved	
		R	4	CEC_BUSY	1: CEC line busy 0: CEC line no busy
		W	3	CEC_L_4800US	1: Force CEC line= “L” 4.8ms 0: Disable force CEC line= “L” 4.8ms
		W	2	CEC_L_3600US	1: Force CEC line= “L” 3.6ms 0: Disable force CEC line= “L” 3.6ms
			1-0	Reserved	

EN_CEC =0, will force state to IDLE.

Initiator

Index	Default	R/W	Bit	Name	Description
71	10	R/W	7	CEC_TR	1: Enable initiator state and transmit data 0: Follower state
		R/W	6	CEC_O_EOM	Transmit EOM
		R	5	CEC_RXACK	Receive ACK
			4-0	Reserved	

Follower

Index	Default	R/W	Bit	Name	Description
72	00	R	7	CEC_I_STR	Receive START Phase
		R	6	CEC_I_EOM	Receive EOM
		R/W	5	CEC_TXACK	Transmit ACK
		R/W	4	CEC_NACK_INT	When NACK, next RX_INT will be set.
			4-0	Reserved	

Clear CEC_I_STR by (CLR_RX_INT or CLR_TX_INT) register to write 1.

Interrupt & Clear Interrupt

Index	Default	R/W	Bit	Name	Description
73	00	R	7	CEC_INT	1: Event CEC interrupt “OR” (tx_int, rx_int, dloss, tm_out, line_error) 0: No event CEC interrupt
			6	CEC_TX_INT	1: Event transmit interrupt (after time of data bit) 0: No event transmit interrupt
			5	CEC_RX_INT	1: Event receive interrupt (after time of data bit) 0: No event receive interrupt
			4	CEC_DLOSS	1: Event arbitrate loss interrupt 0: No event arbitrate loss interrupt
			3	CEC_TM_OUT	1: Event time out interrupt (one bit time over 6.144ms) 0: No event time out interrupt
			2	CEC_LINE _ERROR	1: Event LINE error interrupt(bit width < 1.9ms) 0: No event LINE error interrupt
			1-0	Reserved	
74	00	W	7	Reserved T	
			6	CLR_TX_INT	1: Clear transmit interrupt 0: No clear transmit interrupt
			5	CLR_RX_INT	1: Clear receive interrupt 0: No clear receive interrupt
			4	CLR_DLOSS	1: Clear arbitrate loss interrupt 0: No clear arbitrate loss interrupt

			3	CLR_ TM_OUT	1: Clear time out interrupt 0: No clear time out interrupt
			2	CLR_ LINE_ERROR	1: Clear line error interrupt 0: No clear line error interrupt
			1-0	Reserved	

1. Clear interrupt need to write 1;
2. CEC_DLOSS == 1.
    1. Initiator state will go to IDLE, and CEC_TR = 0.
    2. Initiator wants to send next data, need to wait “signal free time” (註一) and re-set CEC_TR.
3. CEC_LINE_ERROR ==1 (Bit time <1.9ms) or CEC_TM_OUT ==1.
    1. Need to set CEC_L_4800US==1.

Transmit/Receive buffer

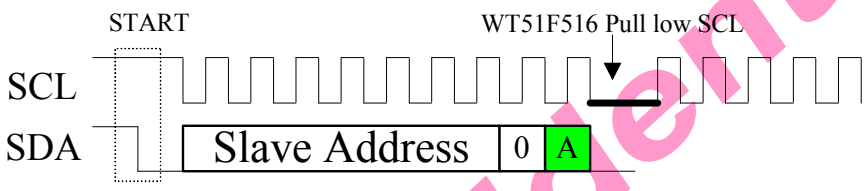
Index	Default	R/W	Bit	Name	Description
75	FF	R/W	7-0	CEC_DTX[7:0]	CEC transmit buffer
76	00	R	7-0	CEC_DRX[7:0]	CEC receive buffer

5.16. Slave IIC

Support 8 transmit buffers and 8 receive buffers.
Slave IIC Control Register

Index	Default	R/W	Bit	Name	Description
A0	00	R/W	7	SIIC_EN	1: Enable SIIC function, clear the reset of SIIC H/W 0: Disable SIIC function,
			6	EN_INT_RT	Enable Read/Write phase interrupt
			5	EN_INT_STOP	Enable STOP phase interrupt
			4	EN_INT_RSTR	Enable reStart phase interrupt
			3	SIIC_WAIT	1: Enable pull low SCL when 9th bit 0: Disable pull low SCL when 9th bit
			2-1	Reserved	
			0	SIIC_TXNAK	1: Slave I2C return NACK 0: Slave I2C return ACK

(1) If IIC speed is over F/W process data time, F/W have to set "IIC_WAIT". WT51F516 pulls low 9th SCL and handshakes master IIC (host)



Slave IIC Interrupt Timing Setting

Index	Default	R/W	Bit	Name	Description
A1	00	R/W	7-4	Reserve	
			3-2	TX_INT_NUM[1:0]	TX interrupt each #-byte 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt
			1-0	RX_INT_NUM[1:0]	RX interrupt each #-byte 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt

Slave IIC Clear Register

Index	Default	R/W	Bit	Name	Description
A2	00	R/W	7	SIIC_CLR_RT	1: Clear transmit/receive interrupt 0: No clear transmit/receive interrupt
			6	SIIC_CLR_STOP	1: Clear STOP phase interrupt 0: No clear STOP phase interrupt
			5	SIIC_CLR_RSTR	1: Clear reStart phase interrupt 0: No clear reStart phase interrupt
			4-0	Reserved	

Slave IIC Status Register

Index	Default	R/W	Bit	Name	Description
A3	00	R	7	SIIC_AL_RDY	1: Event interrupt from SIIC_INT_RT or IIC_INT_STOP 0: No interrupt from SIIC_INT_RT or SIIC_INT_STOP
			6	SIIC_INT_RT	1: Event Slave SIIC interrupt after 9th bit 0: No Slave SIIC interrupt after 9th bit
			5	SIIC_INT_STOP	1: Event "STOP" phase interrupt 0: No "STOP" phase interrupt
			4	SIIC_INT_RSTR	1: Event "reStart" phase interrupt 0: No "reStart" phase interrupt
			3	Reserve	
			2	SIIC_FIRST	1: Event "FIRST" phase 0: No "FIRST" phase
			1	SIIC_ALRW	1: Slave SIIC in TX mode 0: Slave SIIC in RX mode
			0	SIIC_RXNAK	Receive ACK bit 1: NACK 0: ACK

Slave IIC Slave Address Register

Index	Default	R/W	Bit	Name	Description
A4	00	R/W	7-1	SIIC_SADR[6:0]	Slave address
			0	Reserve	

IIC FIFO (8-RX_FIFO, 8-TX_FIFO)

IIC FIFO Control Register

Index	Default	R/W	Bit	Name	Description
A8	0	R/W	7	CLR_IIC_TX_FIFO_INDEX	Clear IIC Tx FIFO index
			6	CLR_IIC_RX_FIFO_INDEX	Clear IIC Rx FIFO index
			5-0	Reserved	

IIC FIFO Tx Status Register

Index	Default	R/W	Bit	Name	Description
A9	80	R	7	IIC_FIFO_TX_EMPTY	IIC Tx FIFO empty flag
			6-4	Reserved	
			3-0	IIC_FIFO_TX_INDEX[3:0]	IIC Tx FIFO index (indicate how many data in IIC TX FIFO)

IIC FIFO Rx Status Register

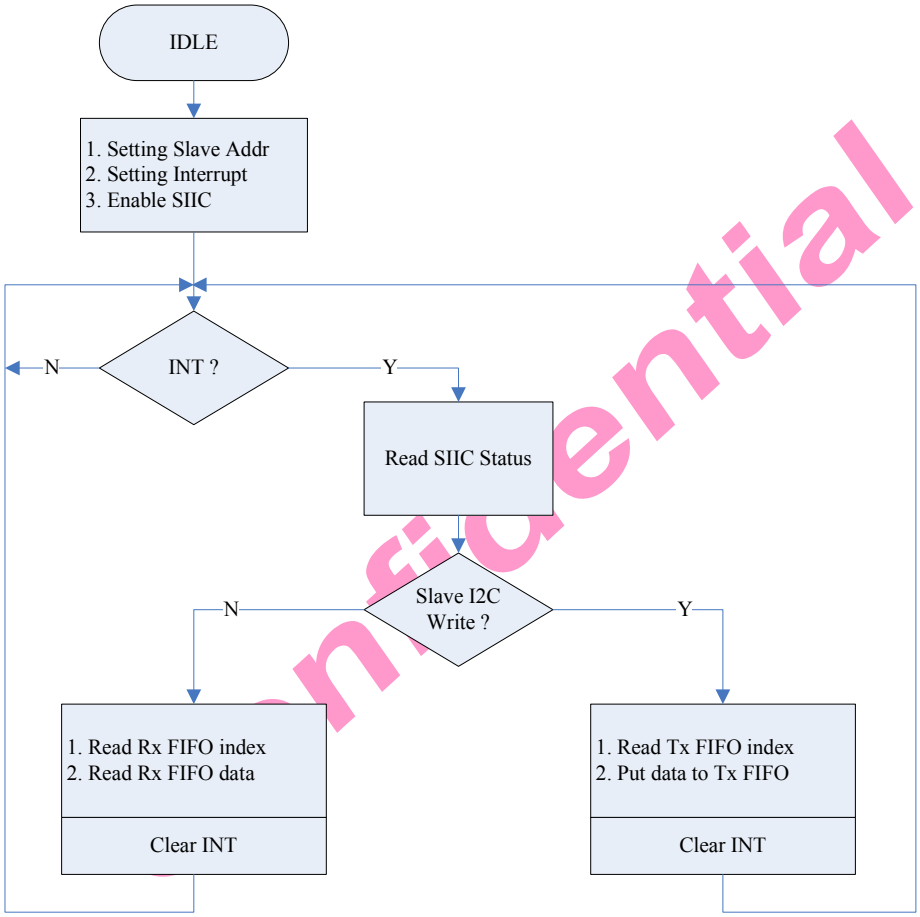
Index	Default	R/W	Bit	Name	Description
AA	0	R	7	IIC_FIFO_RX_FULL	IIC Rx FIFO full flag
			6-4	Reserved	
			3-0	IIC_FIFO_RX_INDEX[3:0]	IIC Rx FIFO index (indicate how many data in IIC RX FIFO)

IIC FIFO data Register

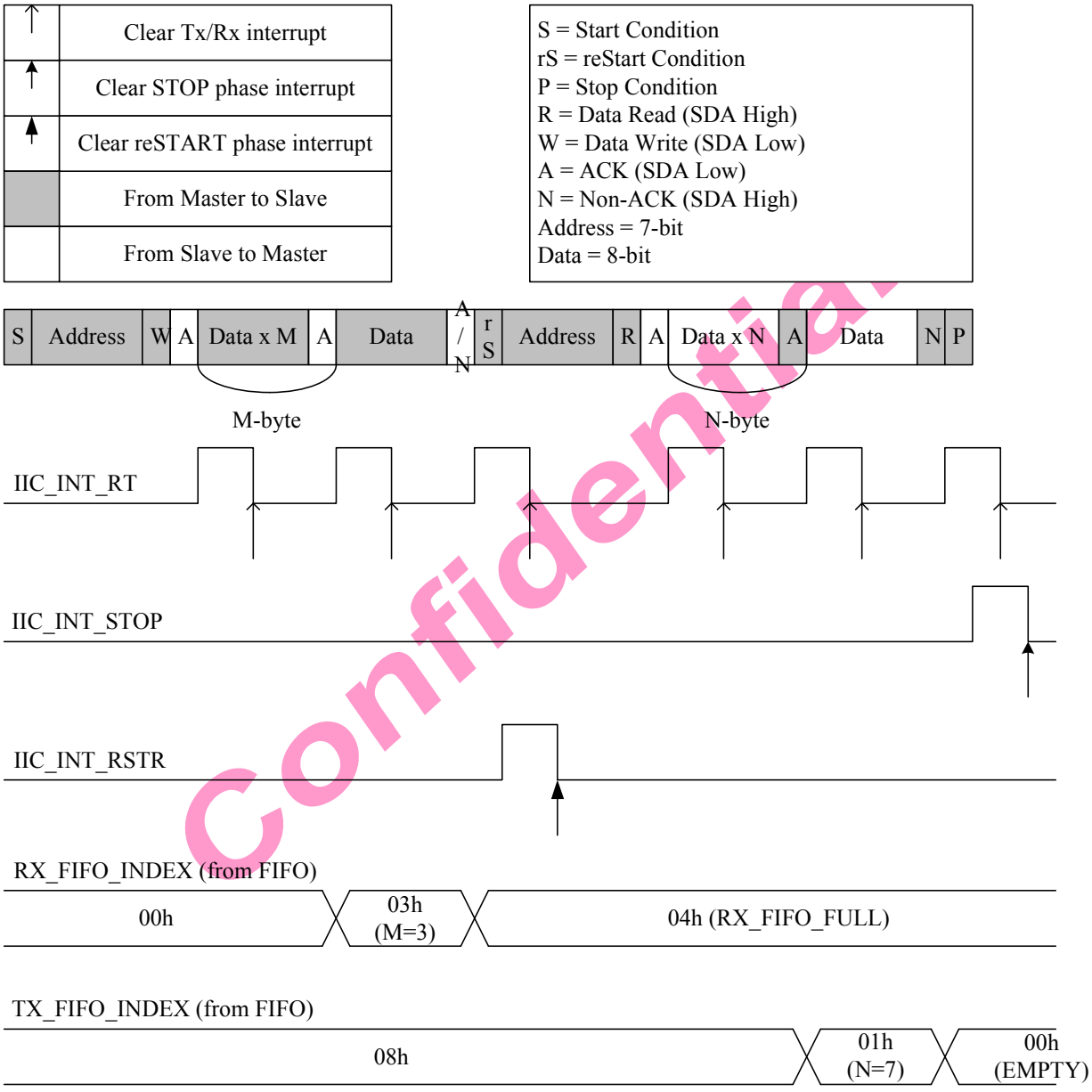
Index	Default	R/W	Bit	Name	Description
AB	FF	R/W	7-0	IIC FIFO_DAT[7:0]	R: Read data from IIC Rx FIFO W: Write data to IIC Tx FIFO

Note:
Data output FFh when Send empty TX FIFO (IIC read)
Data output FFh when Read empty RX FIFO (mcu read)
Data ignore when write more than TX FIFO size. (mcu write)
Data ignore when write more than Rx FIFO size. (IIC write

WT51F516 Slave IIC with 8-FIFO Flow Chart



WT51F516 Slave IIC with 8-FIFO Interrupt Timing



5.17. Master/Slave SPI

SPI Control Register

Index	Default	R/W	Bit	Name	Description
C0	00	R/W	7	SPI_EN	1: Enable SPI system
			6	SPI_MASTER	SPI Master/Slave Select 1: SPI in Master Mode 0: SPI in Slave Mode
			5	SPI_CPOL	SPI Clock Polarity Bit 1: Active-low clock select 0: Active-high clock select
			4	SPI_CPHA	SPI Clock Phase Bit 1: Sampling data at even edge of input SPI clock 0: Sampling data at odd edge of input SPI clock
			3	SPI_MODFEN	Mode Fault Enable bit (slave mode only) 1: STB port pin with MODF feature 0: STB port pin is not used by SPI
			2	SPI_LSBFE	LSB-First Enable 1: Data is Transferred LSB bit first 0: Data is Transferred MSB bit first
			1	SPI_SPC	Serial Pin Control 1: Enable SPI bidirectional pin config 0: Disable SPI bidirectional pin config
			0	SPI_BIDIROE	SPI Output Enable in Bidirectional Mode 1: SPI Output Enable 0: SPI Output Disable

* SPI mode select by SPI_CPOL and SPI_CPHA
mode_0 = (SPI_CPOL, SPI_CPHA) = (0, 0)
mode_1 = (SPI_CPOL, SPI_CPHA) = (0, 1)
mode_2 = (SPI_CPOL, SPI_CPHA) = (1, 0)
mode_3 = (SPI_CPOL, SPI_CPHA) = (1, 1)

Note:

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

SPI Interrupt Control Register

Index	Default	R/W	Bit	Name	Description
C1	00	R/W	7	SPI_TXIE	Enable SPI Transmitter Interrupt
			6	SPI_RXIE	Enable SPI Receiver Interrupt
			5	SPI_STPIE	Enable SPI Sequence Finish Interrupt
			4	Reserved	
			3-2	TX_INT_NUM[1:0]	TX interrupt each #-byte 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt

			1-0	RX_INT_NUM[1:0]	RX interrupt each #-byte 00: 1-byte interrupt 01: 2-byte interrupt 10: 4-byte interrupt 11: 8-byte interrupt

SPI Control Register 2

Index	Default	R/W	Bit	Name	Description
C2	00	R	7	CLR_TXIF	1: Clear SPI Tx interrupt flag
			6	CLR_RXIF	1: Clear SPI Rx interrupt flag
			5	CLR_STPIF	1: Clear SPI sequence finish interrupt flag
			4-0	Reserved	

SPI Status Register

Index	Default	R/W	Bit	Name	Description
C3	00	R	7	SPI_TXIF	SPI Tx interrupt flag
			6	SPI_RXIF	SPI Rx interrupt flag
			5	SPI_STPIF	SPI Tx/Rx data finish flag (STB pin go high) 1: SPI Tx/Rx finish 0: SPI Tx/Rx not finish
			4	SPI_MODF	Mode Fault Flag * 1: Mode fault has occurred 0: Mode Fault has not occurred
			3-0	Reserved	

* Clear SPI mode fault flag (SPI_MODF) by disable SPI module

SPI Bit Rate Selection

Index	Default	R/W	Bit	Name	Description
C4	0	R/W	7-0	SPI_BRS[7:0]	SPI Bit Rate Selection (SPI Max Frequency = 2Mhz) SCLK / (SPI_BRS[7:0]+1)x2 BRS[7:0]=0: SPI speed = 12Mhz/(255+1)x2 = 23.4375Mhz BRS[7:0]=1: SPI speed = 12Mhz/(255+1)x2 = 23.4375Mhz BRS[7:0]=2: SPI speed = 12Mhz/(2+1)x2 = 2Mhz BRS[7:0]=3: SPI speed = 12Mhz/(3+1)x2 = 1.5Mhz …… BRS[7:0]=255: SPI speed = 12Mhz/(255+1)x2 = 23.4375Mhz

SPI FIFO (8-RX_FIFO, 8-TX_FIFO)

SPI FIFO Control Register

Index	Default	R/W	Bit	Name	Description
C8	00	R/W	7	CLR_SPI_TXFIFO_INDEX	Clear SPI Tx FIFO index
			6	CLR_SPI_RXFIFO_INDEX	Clear SPI Rx FIFO index
			5-0	Reserved	

SPI FIFO Tx Status Register

Index	Default	R/W	Bit	Name	Description
C9	80	R	7	SPI_FIFO_TX_EMPTY	SPI_Tx FIFO empty flag
			6-4	Reserved	

			3-0	SPI_FIFO_TX_INDEX[3:0]	SPI _Tx FIFO index (indicate how many data in SPI TX FIFO)

SPI FIFO Rx Status Register

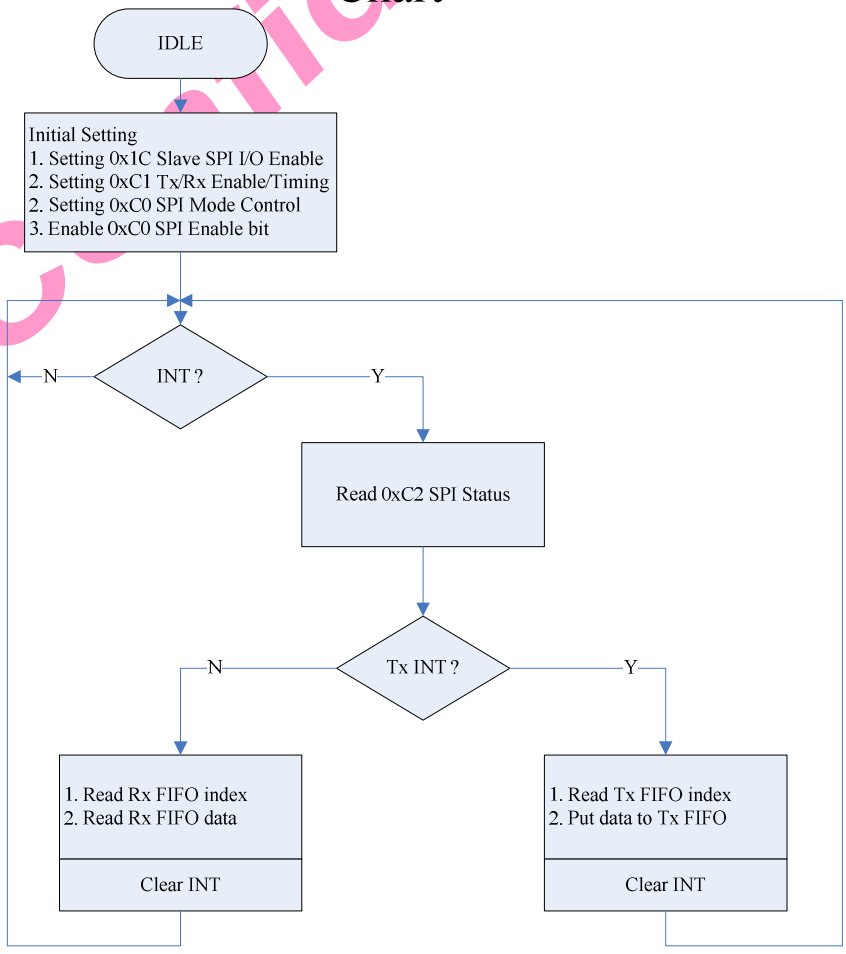
Index	Default	R/W	Bit	Name	Description
CA	00	R	7	SPI_FIFO_RX_FULL	SPI Rx FIFO full flag
			6-4	Reserved	
			3-0	SPI_FIFO_RX_INDEX[3:0]	SPI Rx FIFO index (indicate how many data in RX FIFO)

SPI FIFO Data Register

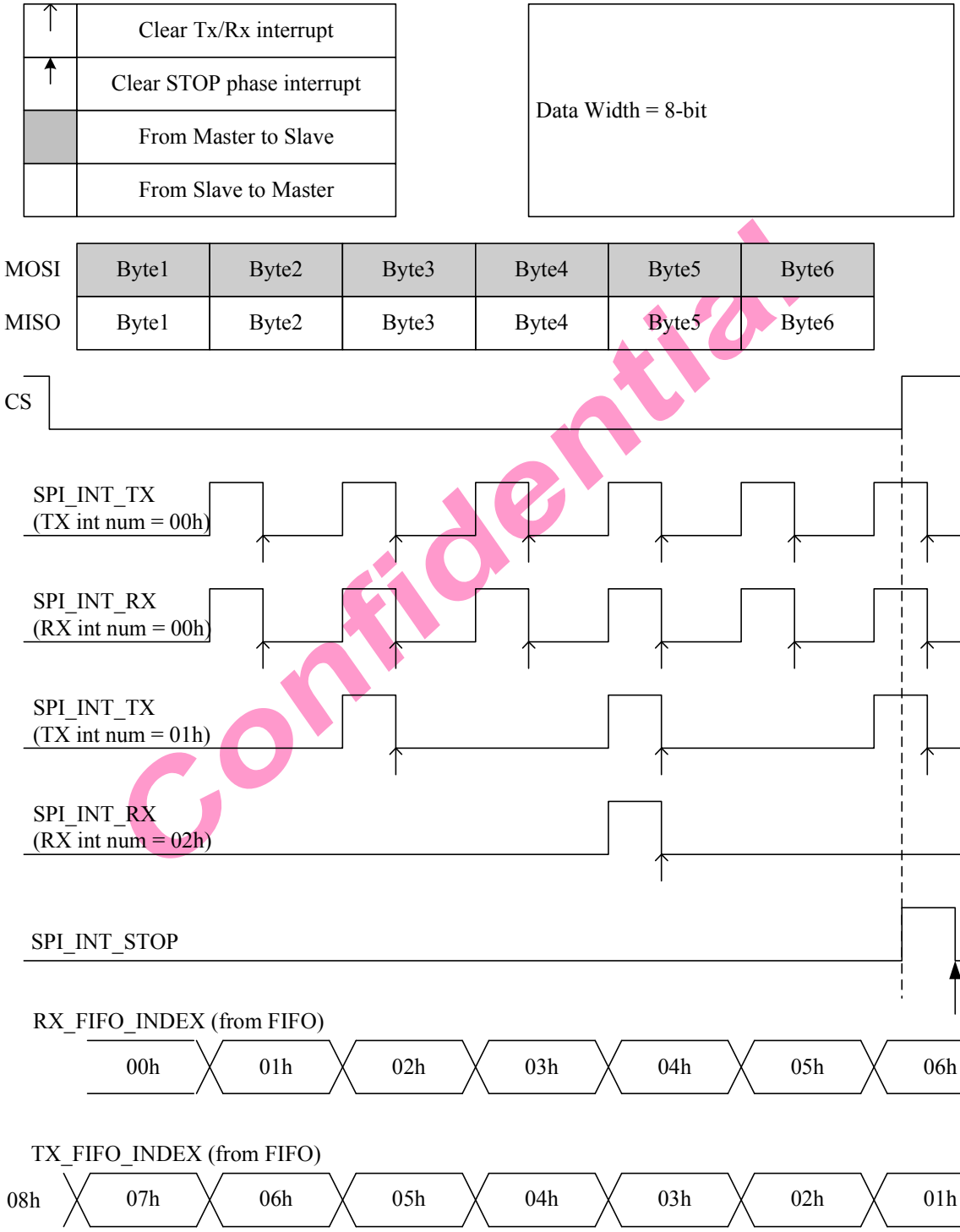
Index	Default	R/W	Bit	Name	Description
CB	FF	R/W	7-0	FIFO_DAT[7:0]	R: Read data from SPI Rx FIFO W: Write data to SPI Tx FIFO

Note:
Data output FFh when Send empty TX FIFO (SPI read)
Data output FFh when Read empty RX FIFO (mcu read)
Data ignore when write more than TX FIFO size. (mcu write)
Data ignore when write more than Rx FIFO size. (SPI write)

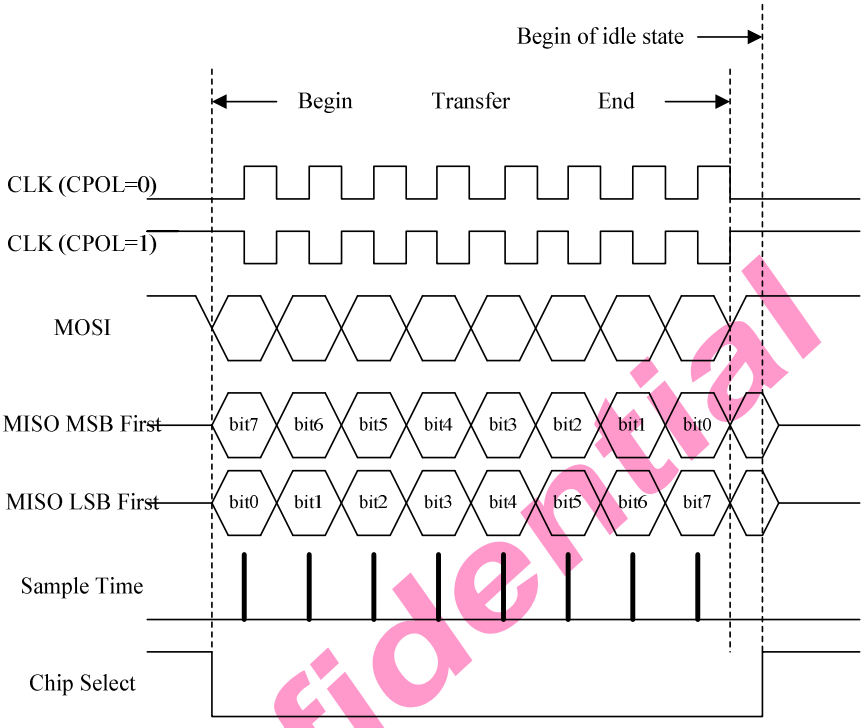
WT51F516 Slave SPI with 8-FIFO Flow Chart



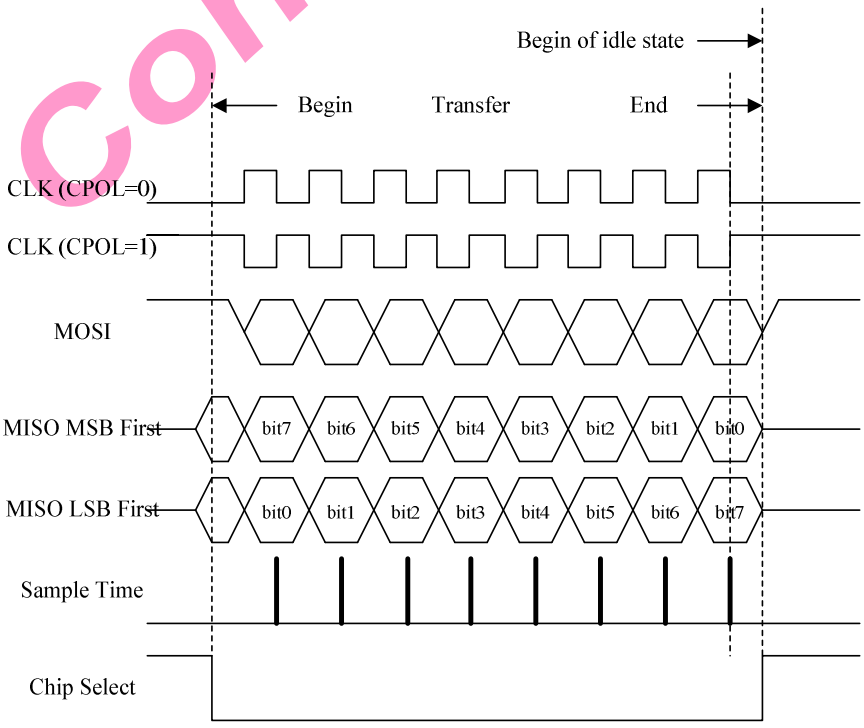
WT51F516 SPI with 8-FIFO Interrupt Timing



WT51F516 SPI Mode Timing



(CPHA = 0)



(CPHA = 1)

5.18. Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) is 10-bit resolution with four selectable input channels. When EN_AD_IO[7:0] is set, IO PAD is configured as ADC input and IO PAD pull-high resistor is disabled. When EN_AD[7:0] select which channel is converted and STR_CVT is set, it will reset the AD_DATA register and start converting. After the conversion is done, the STR_CVT bit is clear and valid data is stored in AD_DATA. The total conversion time is 16us when channel convert time base is 1MHz(If ADC_CLK_SEL=0). If program wants to make a new conversion, it writes STR_CVT register again and it will start another conversion.

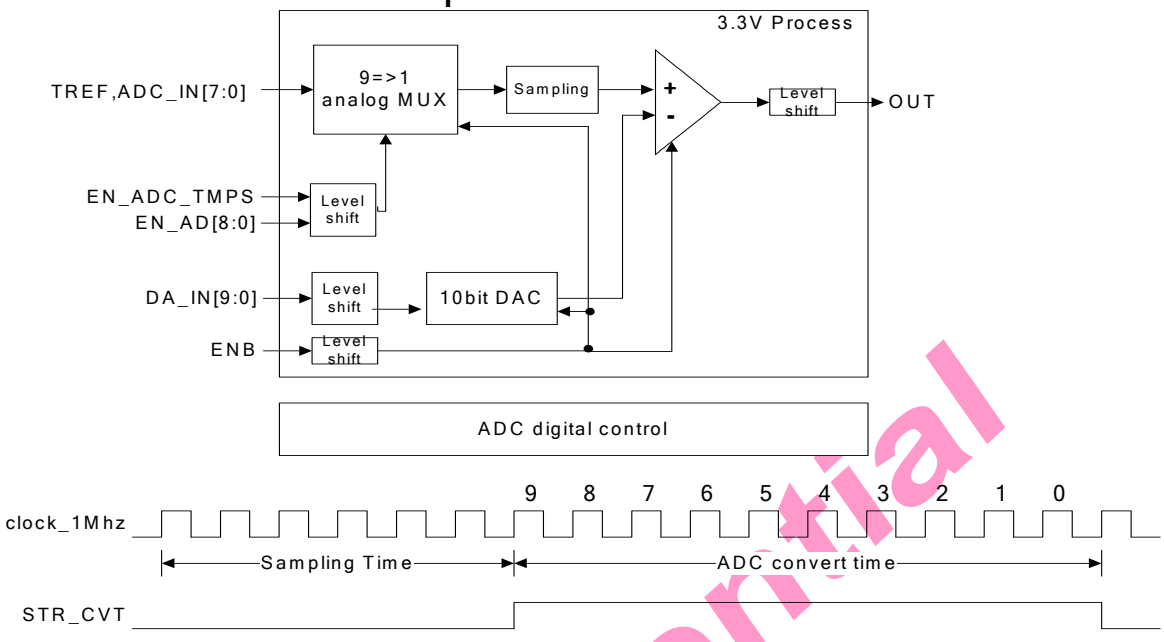
Index	Default	R/W	Bit	Name	Description
D0	80	R/W	7	PD_LADC	1:Power down low speed ADC(default) 0:Enable low speed ADC
			6	STR_CVT	1:Start ADC converter 1 => 0 : convert finish
			5	ADC_BIG	1:Select wake up ADC compare bigger
			4	EN_ADC_WK	1:Enable ADC wake up mode 0:Disable ADC wake up mode
			3	SLT_FLT_CVT	1:select 3x84ns=250ns filtered convert data 0:no filter
			2	ADC_CLK_SEL	1: Channel convert time base: 250kHz 0: Channel convert time base: 1MHz
			1	RDNOISE	1: Reduce noise when ADC convert cycle to halt 8051 0: no halt 8051
			0	Reserved	
D1	00	R	7-0	AD_DATA[9:2]	ADC convert data 10bit high bit
D2	80	R/W	7-0	ADC_WK_V[9:2]	ADC wake up compare voltage 10bit high bit
D3	00	R/W	7-0	EN_AD[7:0]	1:Enable ADC IO of CH[x] 0:Disable ADC IO of CH[x]
D4	00	R	7-2	Reserved	
			1-0	AD_DATA[1:0]	ADC convert data 10bit low bit
D5	00	R/W	7-2	Reserved	
			1-0	ADC_WK_V[1:0]	ADC wake up compare voltage 10bit low bit
D6	00	R/W	7-1	Reserved	
			0	EN_ADC_TMPS	1:Enable ADC transmit gate for temperature sensor 0:Disable ADC transmit gate for temperature sensor
D7	04	R/W	7-3	Reserved	
			2-0	VREF_SEL[2:0]	100:VREF voltage from AVDD 010:VREF voltage from AREF pin 001:VREF voltage from internal reference voltage *(d) (Need clear PD_TMPS, D8H-bit7) Others: Don't support

(a) Read register "D1H" to clear ADC wake up interrupt
(b) EN_AD[7:0] & EN_ADC_TMPS only can enable one channel at the same time.
(c) When convert temperature sensor voltage, please need set ADC_CLK_SEL=10 or 11.
(d) Flash memory XDATA 0xFFCH-bit[7:0] are stored internal reference offset voltage value. VREF_D[7:0] is the internal reference voltage sampling by VREF 3.3V 10-Bit ADC and saving last 8 LSB code in XDATA 0xFFCH-bit[7:0]. The first 2 MSB is 11.

Ex: XDATA 0xFFCH = 2BH, the fully VREF_D code is 32BH,

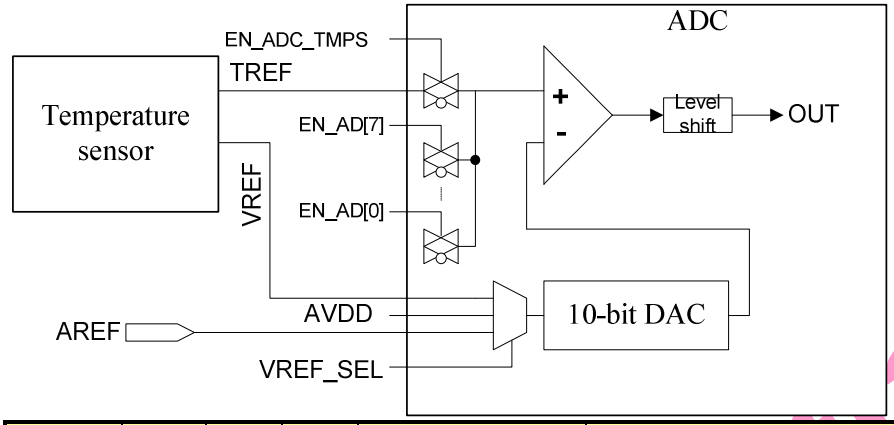
Internal reference voltage= $\frac{1024}{VREF\_D} = \frac{1024}{32BH}$ = 1.263v

Low speed ADC Block



5.19. Temperature sensor

The temperature sensors consists of a band-gap type temperature sensor, a ΣΔ Analog-to-Digital Converter.



Index	Default	R/W	Bit	Name	Description
D8	80	R/W	7	PD_TMPS	1:Power down temperature sensor(default) 0:Enable temperature sensor
			6-0	Reserved	
			1-0	TMPS_GAIN[1:0]	The selector of gain control 00: 0.9486~0.5600V (388.6mV) 01: 1.5777~0.9338V (643.9mV) 10: 2.2070~1.3040V (903.0mV) 11: 2.8377~1.6783V (1159.4mV)

(a) Flash memory XDATA 0xFFDH-bit[7:0] are stored temperature sensor offset voltage value. TS_TREF_D[7:0] is the temperature sensor sampling in room temperature by VREF 3.3V 10-Bit ADC and saving last 8 LSB code in XDATA 0xFFDH-bit[7:0] to calibrate the temperature sensor. The first 2 MSB is 10, and the ideal code in room temperature is 2E7H.

Ex: XDATA 0xFFDH = DFH, the fully TREF_D code is 2DFH,

$$Calibrated\_Temp = \frac{(2E7H - 2DFH) * 3.223mV}{-0.0066} = -3.9067\ ℃$$

*3.223mV is a ADC VLSB in 10-Bit VREF 3.3V condition, -0.0066 is the "TMPS_GAIN=11" slope, both value is determined in FT., no need to be changed in other applications.

TMPS_GAIN	Temp.(℃) - Equation	Note
00	$\frac{TS\_TREF\_Voltage - 0.85}{-0.00213} + Calibrated\_Temp$	ADC Vref>1.2V
01	$\frac{TS\_TREF\_Voltage - 1.42}{-0.00375} + Calibrated\_Temp$	ADC Vref>1.8V
10	$\frac{TS\_TREF\_Voltage - 1.98}{-0.0052} + Calibrated\_Temp$	ADC Vref>2.4V
11	$\frac{TS\_TREF\_Voltage - 2.55}{-0.0066} + Calibrated\_Temp$	ADC Vref>3.0V

TS_TREF voltage is the voltage value read by ADC converting result,

Ex: ADC VREF=3.3v, and TMPS_GAIN = 11, if the ADC code is 2AAH and TREF_D[7:0]=DFH

TS_TREF Voltage= $\frac{AD\_DATA}{1024} * ADC\_VREF = \frac{2AAH}{1024} * 3.3v$ = 2.198V

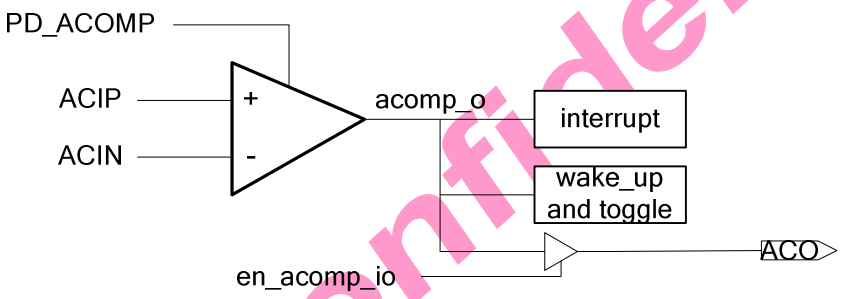
$$Temperature = \frac{TS\_TREF\_Voltage - 2.55}{-0.0066} + Calibrated\_Temp = \frac{2.198 - 2.55}{-0.0066} + (-3.9067) = 49.43\ ℃$$

5.20. Analog Comparator

The Analog Comparator compares the input values on the positive pin ACIP and negative pin ACIN. When the voltage on the positive pin ACIP is higher than the voltage on the negative pin ACIN, the Analog Comparator output ACO is set.

Index	Default	R/W	Bit	Name	Description
D9	C0	R/W	7	PD_ACOMP	1: Power down analog comparator 0: Enable analog comparator
			6	ACOMP_EDGE	1: ACIP voltage > ACIN voltage, ACOMP_EVENT=1 0: ACIP voltage < ACIN voltage, ACOMP_EVENT=1 When ACOMP_PD=1, ACOMP_EVENT=0
			5	CLR_ACOMP_EVENT	1: clear comparator event 0: no clear comparator event
			4	Reserved	
			3	ACOMP_EVENT	1: analog comparator event 0: no analog comparator event
			2-0	Reserved	

(1) After enable ACOMP, need to set CLR_ACOMP_EVENT to clear event flag due to unstable power-on statue.



5.21. RTC(Real Time Clock)

Notice:

(1) If VDD_RTC is connected with super-cap at RTC mode. When CAP33 starts to be turned on, the voltage of VDD_RTC rises slowly because CAP33 charges capacitor through "Diode". The MCU must wait to VDD_RTC power stability, then MCU can read/write RTC registers (B0H~BFH). MCU must wait to check whether written RTC data and read RTC data are equal. If data is equal, the VDD_RTC power is stable and MCU starts to read/write all RTC registers.

(2) Before using the RTC function, F/W needs to set RTC_RESET to reset RTC module.
Procedure: Set RTC_RESET -> Clear RTC_RESET -> Enable RTC_EN

Index	Default	R/W	Bit	Name	Description
38	00	R	7	RTC_1S	1:Event of RTC 1s 0:No event of RTC 1s
		R/W	6	RTC_CS	1:Enable Chip select of RTC WR/RD 0:Disable chip select of RTC WR/RD
			5	RTC_EN	1:Enable access RTC 0:Disable RTC
			4	RTC_RESET	1: Enable RTC reset 0: Disable RTC reset
			3-1	Reserved	
		W	0	CLR_RTC_1S	1:Clear event RTC 1s interrupt 0:No clear event RTC 1s interrupt

Index	Default	R/W	Bit	Name	Description
B0	00	R/W	7	Reserved	
			6-0	RTC_SEC[6:0]	Second coded in BCD, range is 0~59. SEC [6:4] represents 10 seconds. SEC[3:0] represents seconds.
B1	00	R/W	7	Reserved	
			6-0	RTC_MIN[6:0]	Minute coded in BCD, range is 0~59. MIN[6:4] represents 10 minutes. MIN[3:0] represents minutes.
B2	00	R/W	7-6	Reserved	
			5-0	RTC_HOUR[5:0]	Hour coded in BCD, range is 0~23. HOUR[5:4] represents 10 hours. HOUR[3:0] represents hours.
B3	01	R/W	7-6	Reserved	
			5-0	RTC_DAY[5:0]	Day of month coded in BCD, range is 1~31. DAY[5:4] represents 10 days. DAY[3:0] represents days.
B4	00	R/W	7-3	Reserved	
			2-0	RTC_WEEK[2:0]	Day of week. 000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday
B5	01	R/W	7-4	Reserved	
			3-0	RTC_MONTH [3:0]	Month. 0001: January 0010: February 0011: March 0100: April 0101: May 0110: June 0111: July 1000: August

					1001: September 1010: October 1011: November 1100: December
B6	00	R/W	7-0	RTC_YEAR[7:0]	Year coded in BCD, range is 0~99. YEAR[7:4] represents 10 years. YEAR [3:0] represents years.
B8	00	R/W	7-0	RTC_BAKUP1	Back up register 1
B9	00	R/W	7-0	RTC_BAKUP2	Back up register 2
BA	00	R/W	7-0	RTC_BAKUP3	Back up register 3
BB	00	R/W	7-0	RTC_BAKUP4	Back up register 4
BD	00	R/W	7-0	RTC_CA[7:0]	Calibration bits. CA[7]=1, Add clocks. CA[7]=0, skip clocks. CA[6:0] = number which add/skip clock within 128 minutes. (add/skip 128 crystal clocks in one second of minute)
BE	81	R/W	7	RTC_ PDOSC	0: 32768Hz oscillator enable 1: 32768Hz oscillator power down
			6	RTC_STOP	0: Enable RTC. 1: Stop RTC counting
			5-4	Reserved	
			3	RTC_PDOSCSU	1:Power down 32768Hz oscillator start up circuit (*1)
			2-0	RTC_FS[2:0]	Clock output frequency 000: No output 001: 0.25Hz 010: 1Hz 011: 8Hz 100: 64Hz 101: 512Hz 110: 1024Hz 111: 32768Hz
BF	62	R/W	7-4	RX[3:0]	Bias resistor selection 0000: 50k 0001: 300k 0010: 350k 0011: 400k 0100: 450k 0101: 500k 0110: 550k 0111: 600k 1000: 650k 1001: 700k 11xx: 750k
			3-2	Reserved	
			1	DRV2(*2)	Crystal bias current control. “1” : Enlarge the crystal bias current.
			0	DRV1	Crystal driver gain control. “1” : Enlarge the gain of crystal driver.
BC	00	R/W	7-4	Reserved	
			3-0	AMP[3:0]	Amplifier stages options to adjust current. AMP[3:2]: Enlarge the 2nd amplifier stage current AMP[1:0]: Enlarge the 1nd amplifier stage current “11”: four units “10”: three units “01”: two units “00”: one unit

(*1) When crystal oscillate stably, MCU can program RTC_PDOSCSU=1 to reduce power.
(*2) DRV2=1, crystal can oscillate fast, when crystal oscillate stably, MCU can program DRV2 =0 to reduce power.

5.22. Emulated EEPROM

Emulated EEPROM by software. The details please reference WT51F516_ProgrammingFlashSolution document.

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DC Supply Voltage (VDD5)	-0.3	5.5	V
Storage temperature	-60	125	°C
Operating temperature	-40	85	°C

***Note: Stresses above those listed may cause permanent damage to the devices**

6.2. Power Supply (VDD5=5v) at RC oscillator = 12MHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{VDD12M}	Normal operation current at 12Mhz operating	No load on output		4		mA
I_{VDD6M}	Normal operation current at 6Mhz operating	No load on output		2.5		mA
I_{VDD3M}	Normal operation current at 3Mhz operating	No load on output		1.5		mA
I_{VDD1M}	Normal operation current at 1Mhz operating	No load on output		1		mA
I_{VDDS1}	Standby current (Note 1)	No load on output		400		uA
I_{VDDS2}	Standby current (Note 2)	No load on output		100		uA
I_{VDDS3}	Power down mode (Note 3)	No load on output		5		uA
I_{VDDRTC}	RTC mode	No load on output		1		uA

Note 1: RC oscillator Stand-by mode, CPU & Flash memory shut down, wake up time 4 MCU CLK
Note 2: RC oscillator Stand-by mode, CPU & Flash memory shut down, wake up time 256 MCU CLK.
Note 3: RC oscillator power down mode(Internal 12MHz RC oscillator and 128KHz RC oscillator power down), CPU & Flash memory shut down and disable LVR.
Note 4: These parameters are presented for design guidance only and not tested or guaranteed

6.3. Digital I/O

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{T1+}	Schmitt trigger Low-to-High threshold point (Note 1)		1.9		5.5	V
V_{T2+}	Schmitt trigger Low-to-High threshold point (Note 2)		1.9		3.6	V
V_{T-}	Schmitt trigger High-to-Low threshold point (Note 1)				1.2	V
V_{OH4}	Output high voltage(Note 3)	I_{OH} = 4mA	2.4			V
V_{OL4}	Output low voltage(Note 3)	I_{OL} = 4mA			0.4	V
V_{OH8}	Output high voltage (Note 4)	I_{OH} = 8mA	2.4			V
V_{OL8}	Output low voltage (Note 4)	I_{OL} = 8mA			0.4	V
I_{VDD}	Total current into V_{DD} power lines (source)				50	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)				90	mA
I_{OZ}	Tri-state leakage current	V_O = 0 or 3.3V		±0.01	±1	μA
R_{PD}	Pull up resistor			50		KΩ

Note 1: Including GPIOA0~A6, GPIOC0~C7 and NRST pin, MAX input are +5.5v and GPIOC1 MAX input is +3.6v in UG320 package.
Note 2: Including **GPIOA7, GPIOB0~GPIOB7, GPIOC1, XTALI MAX input are +3.6v**.

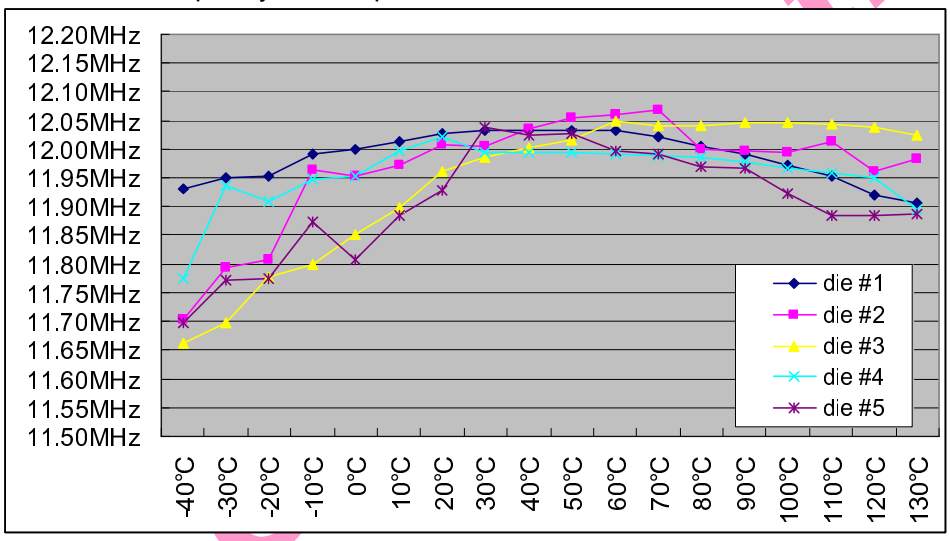
Note 3: Including all pin except GPIOA0,GPIOA3, GPIOA4 and GPIOC5, maximum sink/source current are 10mA
Note 4: Including GPIOA0,GPIOA3, GPIOA4, GPIOC5, maximum sink/source current are 20mA
Note 5: These parameters are presented for design guidance only and not tested or guaranteed

6.4. High speed internal RC Oscillator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{RCH}	RC frequency (@VDD5=5V)			12		Mhz
$\Delta F_{RCH1}/F_{RCH}$	Frequency tolerance with factory calibration	25℃		±1		%
		0℃ ~ 70℃		±2		%
		-40℃ ~ 85℃		±3		%
$\Delta F_{RCH2}/F_{RCH}$	Frequency tolerance with user Calibration	-40℃ ~ 85℃			±1	%

Note 1: These parameters are presented for design guidance only and not tested or guaranteed

RC oscillator frequency vs. Temperature.



6.5. Low speed internal RC Oscillator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{RCL}	RC frequency (@VDD5=5V)		110	128	145	Mhz
$\Delta F_{RCL}/F_{RCL}$		-40℃ ~ 85℃			±5	%

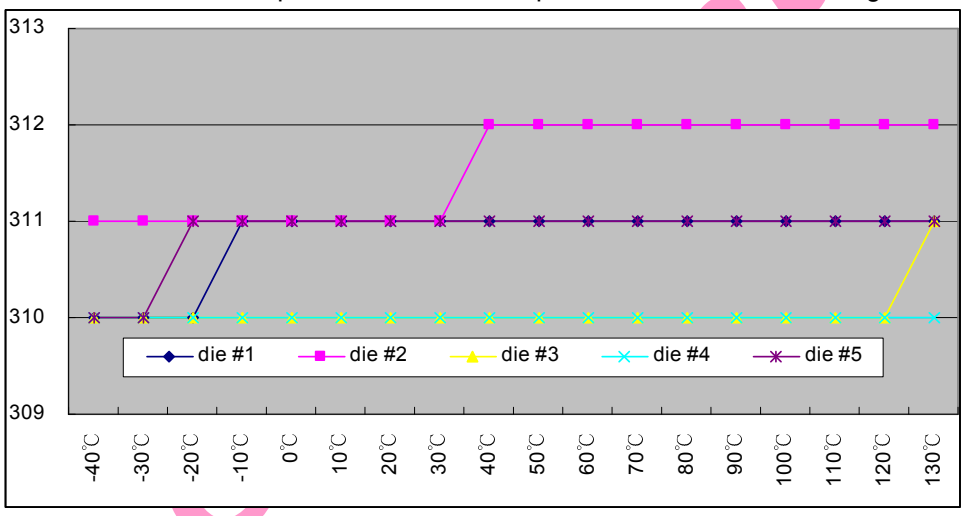
Note 1: These parameters are presented for design guidance only and not tested or guaranteed

6.6. Analog-to-Digital Converter characteristics

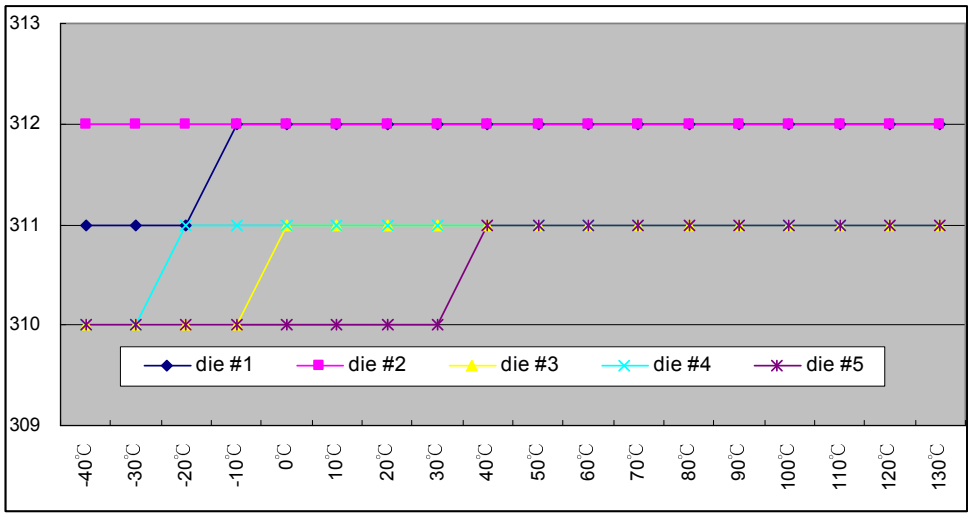
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	Resolution				10	bit
E_{IL}	Integral Error	AREF=3.3v			±2	Lsb
E_{DL}	Differential Error	AREF=3.3v			±1	Lsb
E_{OFS}	Offset Error	AREF=3.3v			±1	Lsb
E_{GAN}	Gain Error	AREF=3.3v			±3	Lsb
V_{AN}	Analog input voltage range	VDD5=5v	VSS		CAP33 (AREF)	V
		VDD33 = 3.3v	VSS		VDD33 (AREF)	V
V_{REF}	Analog Reference Voltage		2		CAP33 (VDD33)	V
IADC1	ADC current @ normal mode	VDD33 = 3.3V		600		μA

Note 1: These parameters are presented for design guidance only and not tested or guaranteed

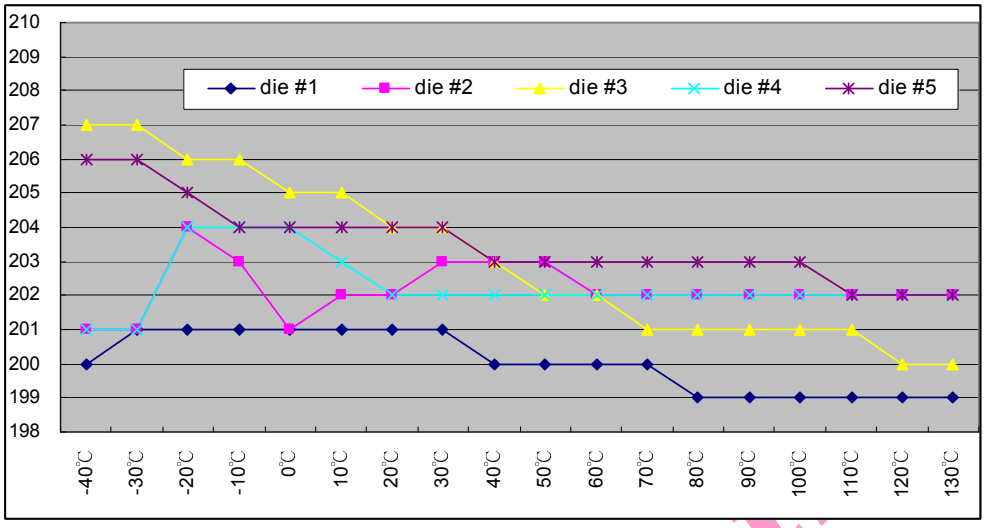
(a) Converter data vs. Temperature, When V_{AN} input =1v at "ADC VREF voltage = CAP33/VDD33 power =3.3v"



(b) Converter data vs. Temperature, When V_{AN} input =1v at "ADC VREF voltage = AREF pin =3.3v"



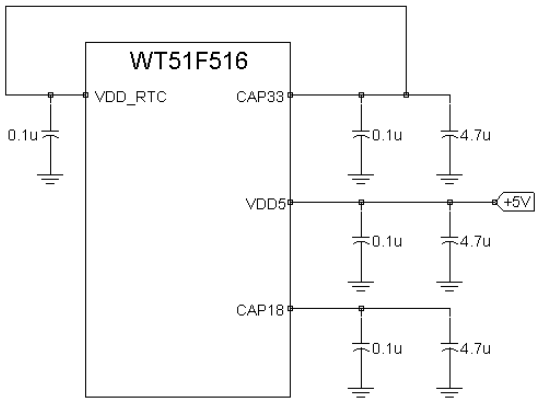
(c) Converter data vs. Temperature, When V_{AN} input =1v at “VREF voltage = internal bandgap voltage”

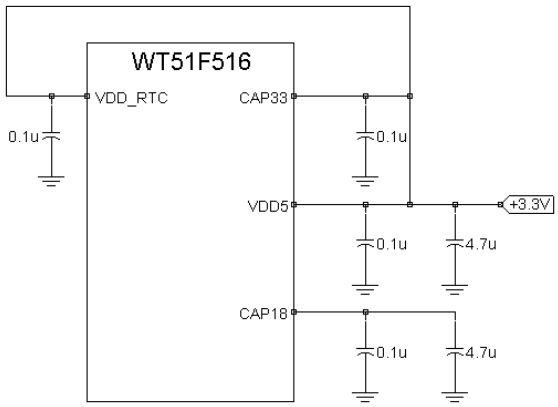


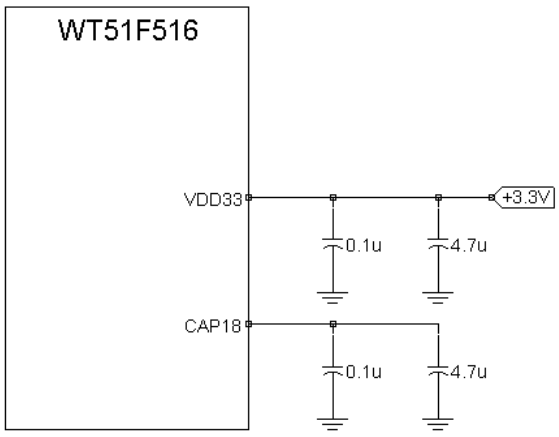
7. Typical application circuit

7.1. Power Supply

(1) Power pin application circuit

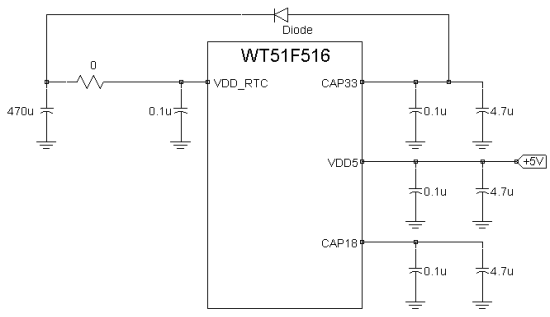
<table>
<tr><th>+5V Power supply</th><th>+3.3V power supply</th></tr>
<tr><td> 

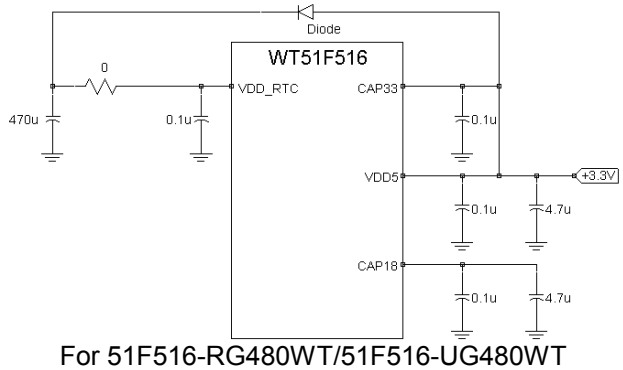
For 51F516-RG480WT/51F516-UG320WT</td><td> 

For 51F516-RG480WT/51F516-UG320WT</td></tr>
<tr><td></td><td> 

51F516-OG200WT/51F516-SG161WT</td></tr>
</table>

(2) For support battery or super-cap back up of RTC mode

<table>
<tr><th>+5V Power supply</th><th>+3.3V power supply</th></tr>
<tr><td> 

For 51F516-RG480WT/51F516-UG480WT</td><td> 

For 51F516-RG480WT/51F516-UG480WT</td></tr>
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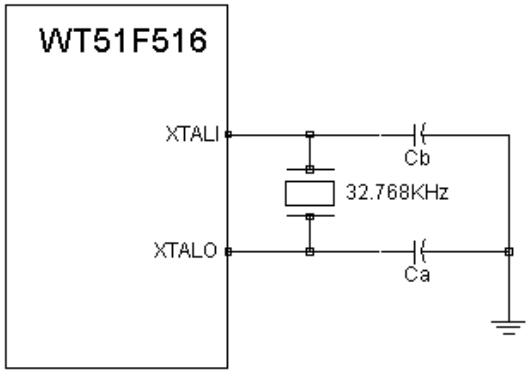
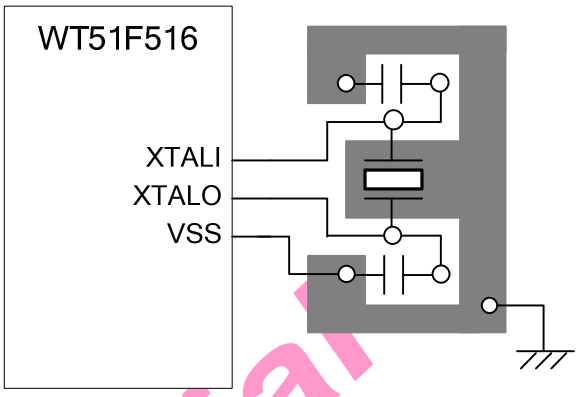
7.2. Crystal Oscillator



Oscillator Connections

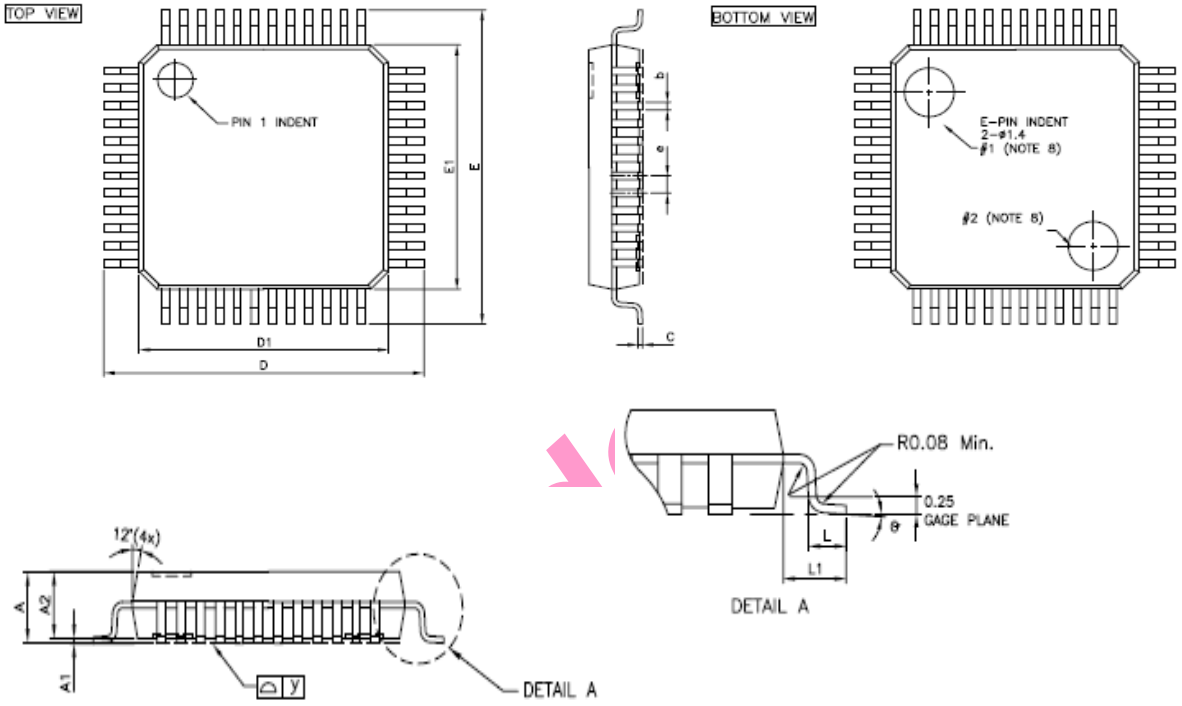


Layout of Oscillator PCB circuit

* Crystal load capacitance $C_L = \frac{Ca * Cb}{(Ca + Cb)} + Cs$ (C_S is stray capacitances and Crystal load capacitance value to look for in the data sheet of the crystal is C_L.)

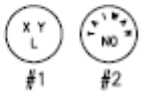
8. Package Dimension

8.1. LQFP48



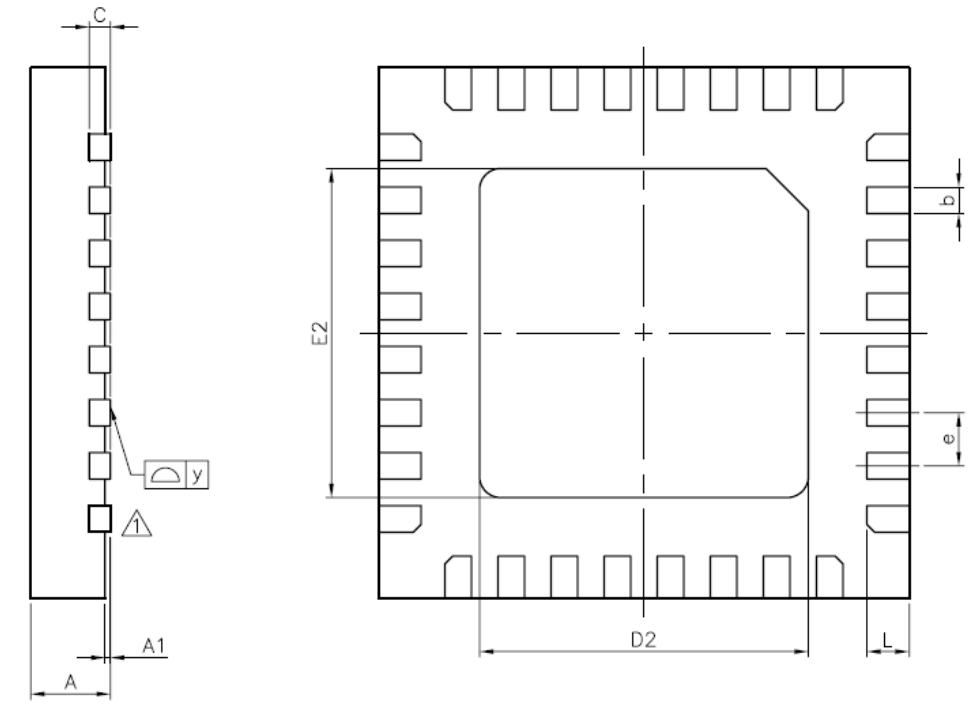
SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.60
A1	0.05	——	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.09	——	0.20
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
e	——	0.50	——
L	0.45	0.60	0.75
L1	——	1.00	——
θ	0°	3.5°	7°
y	0.0	——	0.08

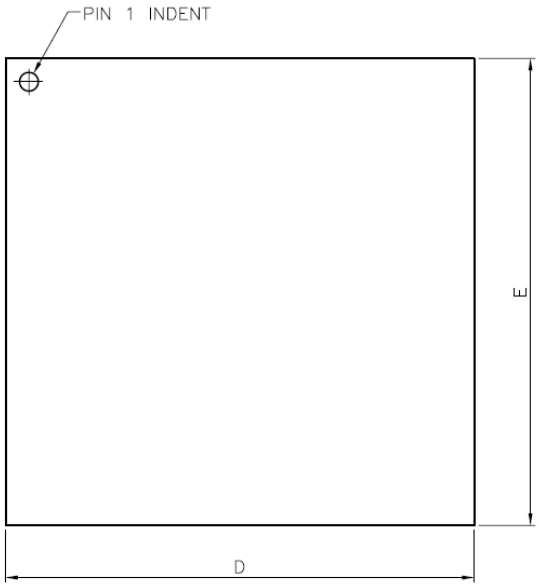
NOTE :
1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER 7025
3. DIMENSION "D1 AND E1" DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-026-BBC
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :



X : A, B, C,...
Y : 1 ~ 12
NO : DENOTE MOLD SET NUMBER

8.2. QFN32



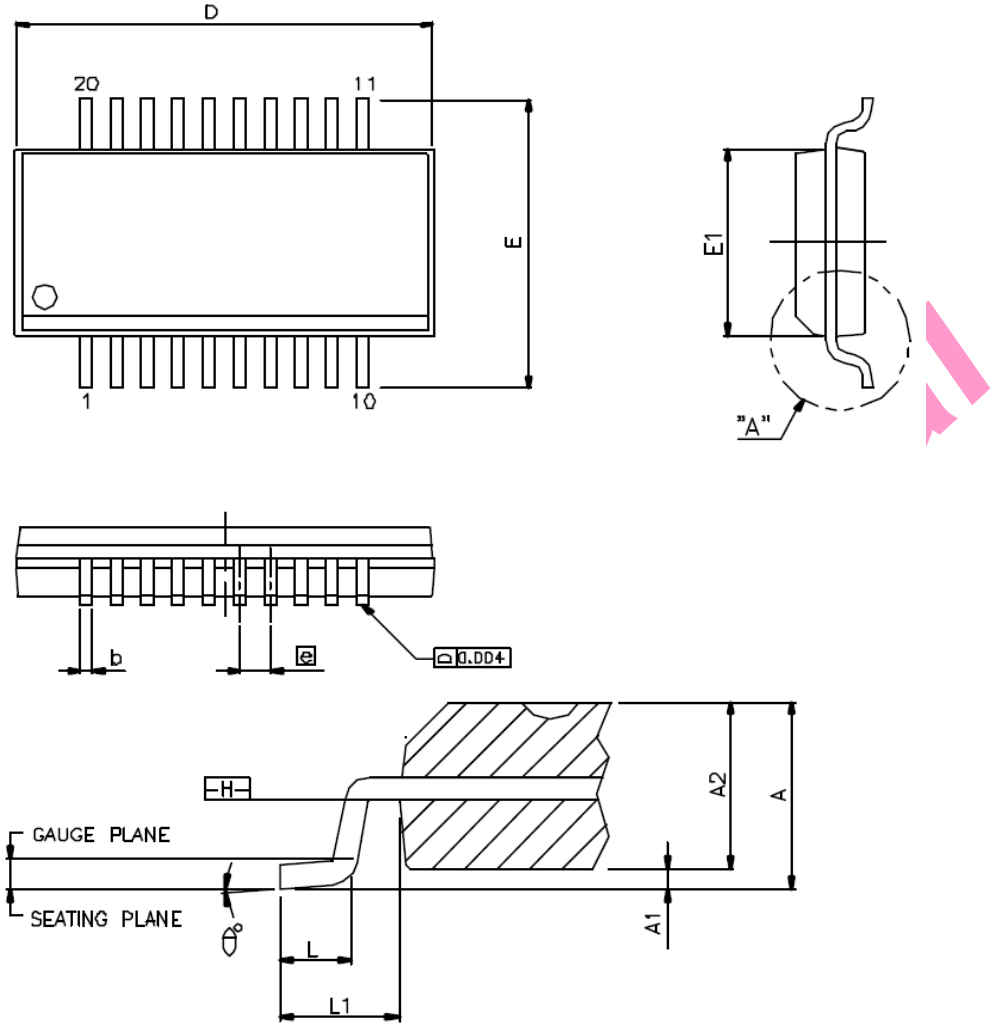


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	——	0.20 REF.	——
D	4.90	5.00	5.10
D2	3.05	3.10	3.15
E	4.90	5.00	5.10
E2	3.05	3.10	3.15
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075

NOTE:

1.THE TERMINAL #1 IDENTIFIER
IS A LASER MARKED FEATURE

8.3. SSOP20



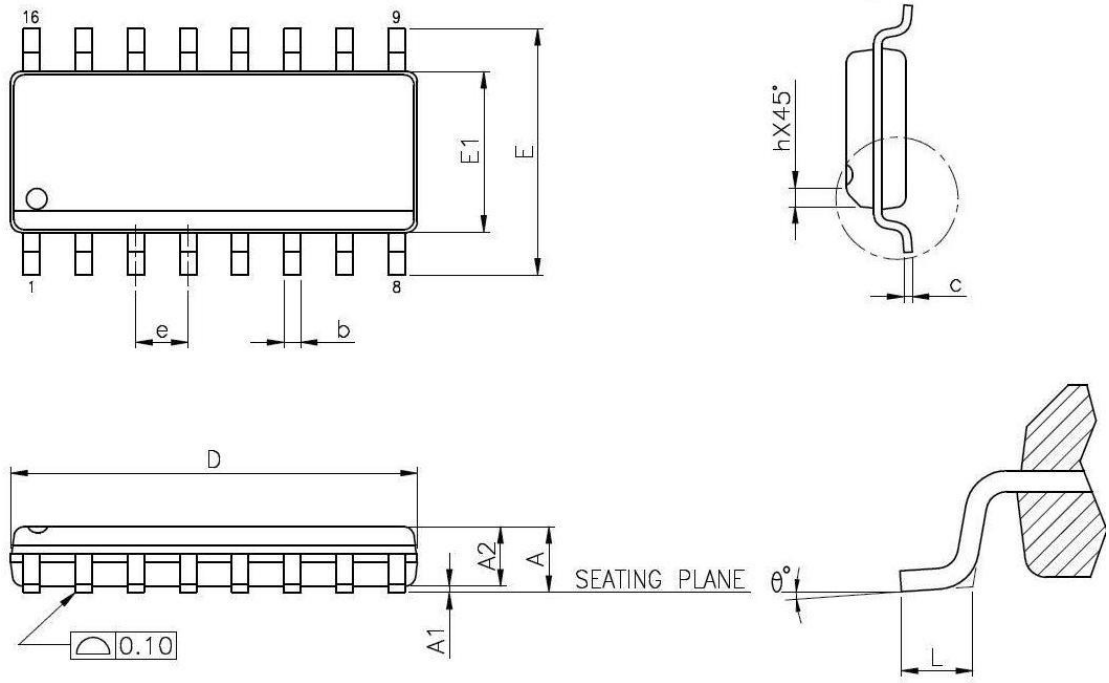
DETAIL : A

SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
b	0.008	–	0.012
C	0.007	–	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MO-137 AD
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST

8.4. SOP16



	STANDARD	
SYMBOLS	**MIN.**	**MAX.**
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

UNIT: mm

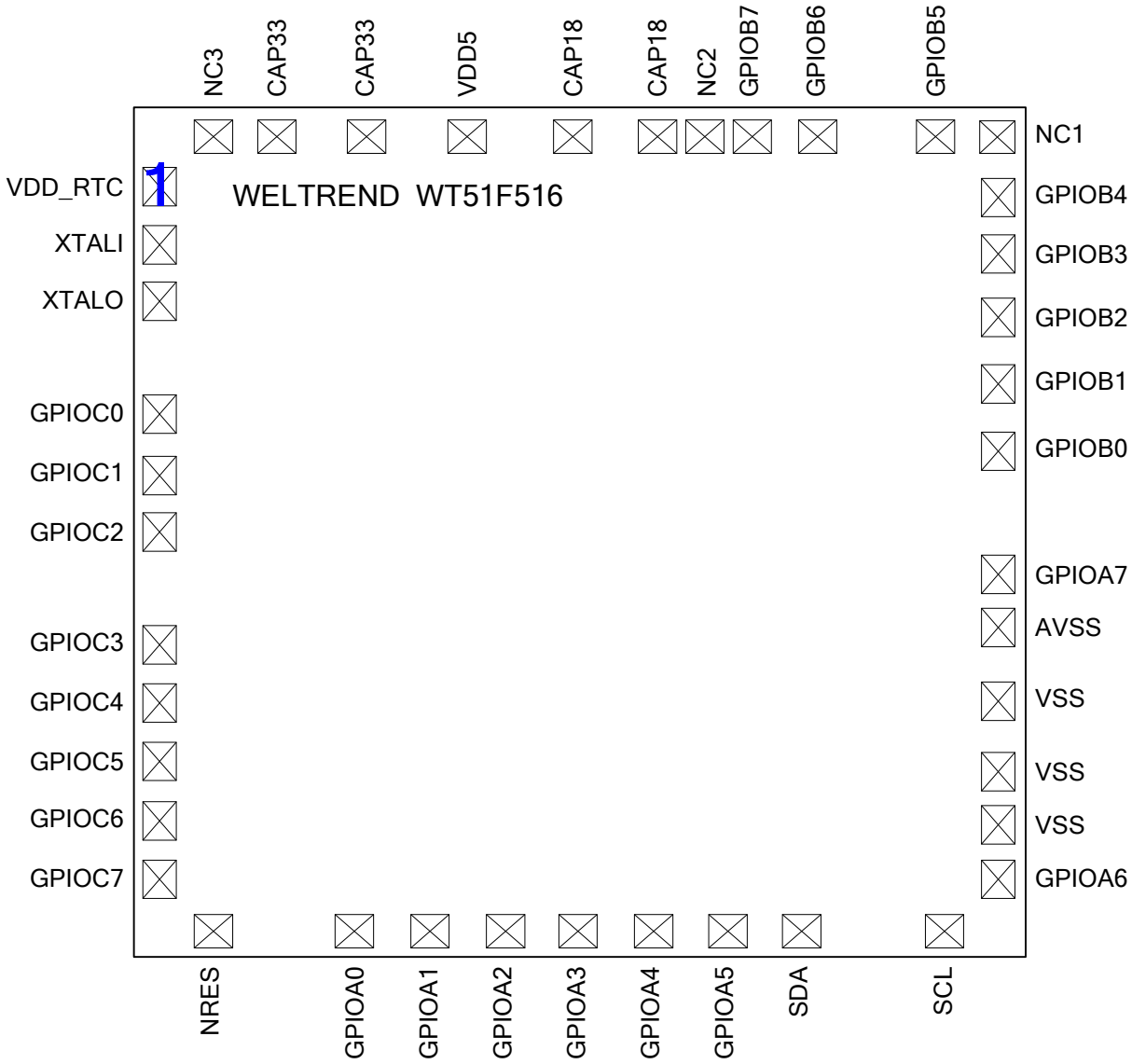
NOTES:

1. JEDEC OUTLINE:
   MS-012 AC REV.F (STANDARD)
2. DIMENSIONS “D” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE

DIMENSIONS “E1” DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE

9. Pad diagram and Location Table

9.1. Pad diagram



9.2. Location Table

No	Name	X	Y	*	No	Name	X	Y	*
1	VDD_RTC	46.18	1606.82	A	22	VSS	1803.82	268.53	A
2	XTALI	46.18	1487.12	A	23	VSS	1803.82	376.88	A
3	XTALO	46.18	1367.42	A	24	VSS	1803.82	528.05	A
4	GPIOC0	46.18	1129.69	A	25	AVSS	1803.82	681.95	A
5	GPIOC1	46.18	1006.99	A	26	GPIOA7	1803.82	795.61	A
6	GPIOC2	46.18	884.29	A	27	GPIOB0	1803.82	1055.415	A
7	GPIOC3	46.18	645.71	A	28	GPIOB1	1803.82	1192.735	A
8	GPIOC4	46.18	523.01	A	29	GPIOB2	1803.82	1330.055	A
9	GPIOC5	46.18	400.31	A	30	GPIOB3	1803.82	1467.375	A
10	GPIOC6	46.18	277.61	A	31	GPIOB4	1803.82	1587.185	A
11	GPIOC7	46.18	154.91	A	32	NC1	1805.32	1713.82	C
12	NRES	154.45	46.18	B	33	GPIOB5	1677.62	1713.82	B
13	GPIOA0	458.43	46.18	B	34	GPIOB6	1425.81	1713.82	B
14	GPIOA1	613.83	46.18	B	35	GPIOB7	1286.53	1713.82	B
15	GPIOA2	769.23	46.18	B	36	NC2	1188.79	1713.82	B
16	GPIOA3	924.63	46.18	B	37	CAP18	1091.79	1713.82	B
17	GPIOA4	1080.03	46.18	B	38	CAP18	913.595	1713.82	B
18	GPIOA5	1235.43	46.18	B	39	VDD5	696.225	1713.82	B
19	SDA	1390.83	46.18	B	40	CAP33	478.87	1713.82	B
20	SCL	1695.55	46.18	B	41	CAP33	291.68	1713.82	B
21	GPIOA6	1803.82	154.45	A	42	NC3	153.18	1713.82	B

Note 1: The origin of pad location shown here is at lower-left corner of die.
*Note 2: *PAD Window.*
A: 66 um x 73um
B: 73um x 66um
C: 63um x 66um
Note 3: To stabilize the supply voltages, please connect 0.1uF and 4.7uF bypass capacitors between CAP18/ CAP33/VDD5/VDD_RTC and VSS.
Note 4: NC1,NC2,NC3 pin no connection for normal application.
Note 5: All VSS pin need connect together. (No: 22, 23, 24, 25)
Note 6: All CAP18 pin need connect together. (No:37, 38)
Note 7: All CAP33 pin need connect together. (No:40, 41)
Note 8: VDD_RTC pin may be connect with CAP33, except it has its own power source.