Weltrend Semiconductor, Inc.

WT61P6

Embedded Micro-Controller for Monitor

(Flash Memory Type)

Data Sheet

REV. 1.01

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GENERAL DESCRIPTION

The WT61P6 is a microcontroller for digital controlled monitor with 1) 8051 compatible cpu, 2) 128K bytes Flash memory, 3) 1536 bytes SRAM, 4) 16 PWMs, 5) SYNC signal processor, 6) 2 timers, 7) two DDC1/2B interface, 8) master/slave I^2C interface, 9) 8-bit A/D converter, 10) watch-dog timer, 11) ISP, 12) power down mode, 13) embedded ICE mode.

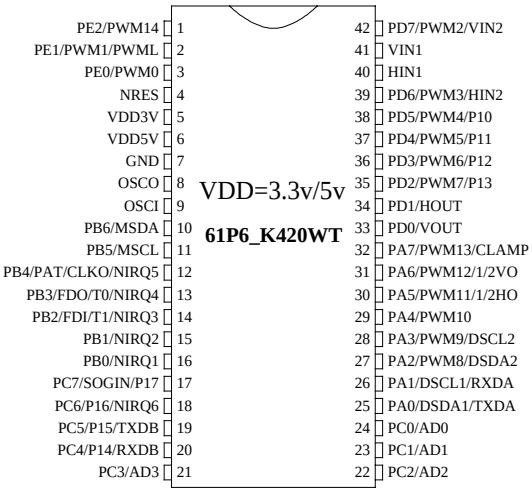
FEATURES

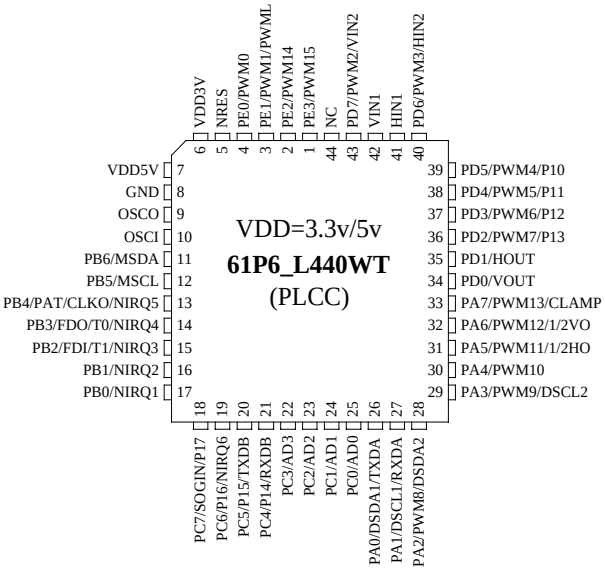
- 8-bit 8051 compatible CPU with 12/24MHz operating frequency
- 128K bytes flash memory, 1536 bytes SRAM (256 bytes internal + 1280 bytes external)
- 12/24MHz crystal oscillator
- 16 channels PWM outputs (15/ 8-bit + 1/ 12-bit), 1/ 8-bit also support low speed 60Hz PWM output
- Sync signal processor with H+V separation, H/V frequency counter, H/V polarity detection/control and clamp pulse output
- Programmable free-running SYNC signal output & White video pattern (Horizontal frequency up to 250KHz with programmable H pulse width and V pulse width)
- Programmable H and V overflow interrupt for fast blanking
- Two timers compatible to 8051
- Two DMA DDC1/2B module for EDID1.3, EDID2.0 (A2/A3, A6/A7) and Enhance EDID (60/61)
- Fast mode master/slave I^2C interface (up to 400KHz)
- 8-bit A/D converter with 4 selectable inputs
- Watchdog timer
- Maximum 35 programmable I/O pins (PLCC package)
- Two external interrupt request input
- 5/3.3 volt operate voltage supported
- Low V_{DD} reset supported
- ISP function supported
- Power down mode supported
- C compiler supported
- Embedded ICE mode supported

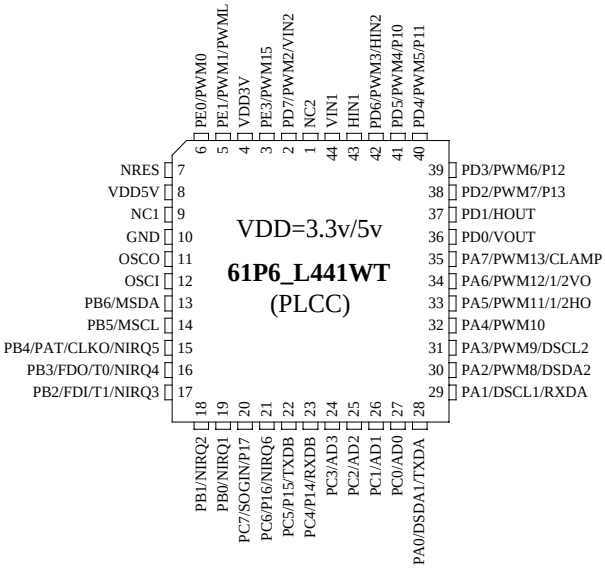
ORDERING INFORMATION

Package Type	Part Number
42-pin Shrink PDIP	61P6-K420WT(3.3v/5v)
44-pin PLCC	61P6-L440WT(3.3v/5v) 61P6-L441WT(3.3v/5v)

PIN ASSIGNMENT AND PACKAGE TYPE







PIN DESCRIPTION (5V-package)

Pin No.			Pin	I/O	Description
441	**440**	**42**	**Name**		
3	1	-	PE3/PWM15	I/O	Port E3 or PWM15
	2	1	PE2/PWM14	I/O	Port E2 or PWM14
5	3	2	PE1/PWM1/PWML	I/O	Port E1 or PWM1 or PWML (low speed)
6	4	3	PE0/PWM0	I/O	Port E0 or PWM0 (12 bits)
7	5	4	NRES	I	Reset input
4	6	5	VDD3V	P	+3.3V power supply
8	7	6	VDD5V	P	+5V power supply
10	8	7	GND	P	Ground
11	9	8	OSCO	O	12Mhz oscillator output
12	10	9	OSCI	I	12Mhz oscillator input
13	11	10	PB6/MSDA	I/O	Port B6 or master IIC SDA
14	12	11	PB5/MSCL	I/O	Port B5 or master IIC SCL
15	13	12	PB4/PAT/CLKO/NIRQ5	I/O	Port B4 or test pattern output or CPU clock output or External interrupt 5 request input
16	14	13	PB3/FDO/T0/NIRQ4	I/O	Port B3 or frequency divider output or External interrupt 4 request input
17	15	14	PB2/FDI/T1/NIRQ3	I/O	Port B2 or frequency divider input or External interrupt 3 request input
18	16	15	PB1/NIRQ2	I/O	Port B1 or External interrupt 2 request input
19	17	16	PB0/NIRQ1	I/O	Port B0 or External interrupt 1 request input
20	18	17	PC7/SOGIN/P17	I/O	Port C7 or Sync on Green input or 8031 P1.7
21	19	18	PC6/P16/NIRQ6	I/O	Port C6 or 8031 P1.6 or External interrupt 6 request input
22	20	19	PC5/P15/TXDB	I/O	Port C5 or 8031 P1.5 or UART TXDB
23	21	20	PC4/P14/RXDB	I/O	Port C4 or 8031 P1.4 or UART RXDB
24	22	21	PC3/AD3	I/O	Port C3 or ADC input 3
25	23	22	PC2/AD2	I/O	Port C2 or ADC input 2
26	24	23	PC1/AD1	I/O	Port C1 or ADC input 1
27	25	24	PC0/AD0	I/O	Port C0 or ADC input 0
28	26	25	PA0/DSDA1/TXDA	I/O	Port A0 or DDC SDA1 or UART TXDA (open drain)
29	27	26	PA1/DSCL1/RXDA	I/O	Port A1 or DDC SCL1 or UART RXDA (open drain)
30	28	27	PA2/PWM8/DSDA2	I/O	Port A2 or PWM8 or DDC SDA2 (open drain)
31	29	28	PA3/PWM9/DSCL2	I/O	Port A3 or PWM9 or DDC SCL2 (open drain)
32	30	29	PA4/PWM10	I/O	Port A4 or PWM10
33	31	30	PA5/PWM11/1/2HO	I/O	Port A5 or PWM11 or 1/2 HOUT
34	32	31	PA6/PWM12/1/2VO	I/O	Port A6 or PWM12 or 1/2 VOUT
35	33	32	PA7/PWM13/CLAMP	I/O	Port A7 or PWM13 or CLAMP output
36	34	33	PD0/VOUT	I/O	Port D0 or VSYNC output
37	35	34	PD1/HOUT	I/O	Port D1 or HSYNC output
38	36	35	PD2/PWM7/P13	I/O	Port D2 or PWM7 or 8031 P1.3
39	37	36	PD3/PWM6/P12	I/O	Port D3 or PWM6 or 8031 P1.2
40	38	37	PD4/PWM5/P11	I/O	Port D4 or PWM5 or 8031 P1.1
41	39	38	PD5/PWM4/P10	I/O	Port D5 or PWM4 or 8031 P1.0
42	40	39	PD6/PWM3/HIN2	I/O	Port D6 or PWM3 or HSYNC **II** Input
43	41	40	HIN1	I	HSYNC **I** Input.
44	42	41	VIN1	I	VSYNC **I** input.
2	43	42	PD7/PWM2/VIN2	I/O	Port D7 or PWM2 or VSYNC **II** Input

FUNCTIONAL DESCRIPTION

CPU

8-bit 8051 compatible CPU with 16-bit address bus and 8-bit data bus operates at 12/24MHz.

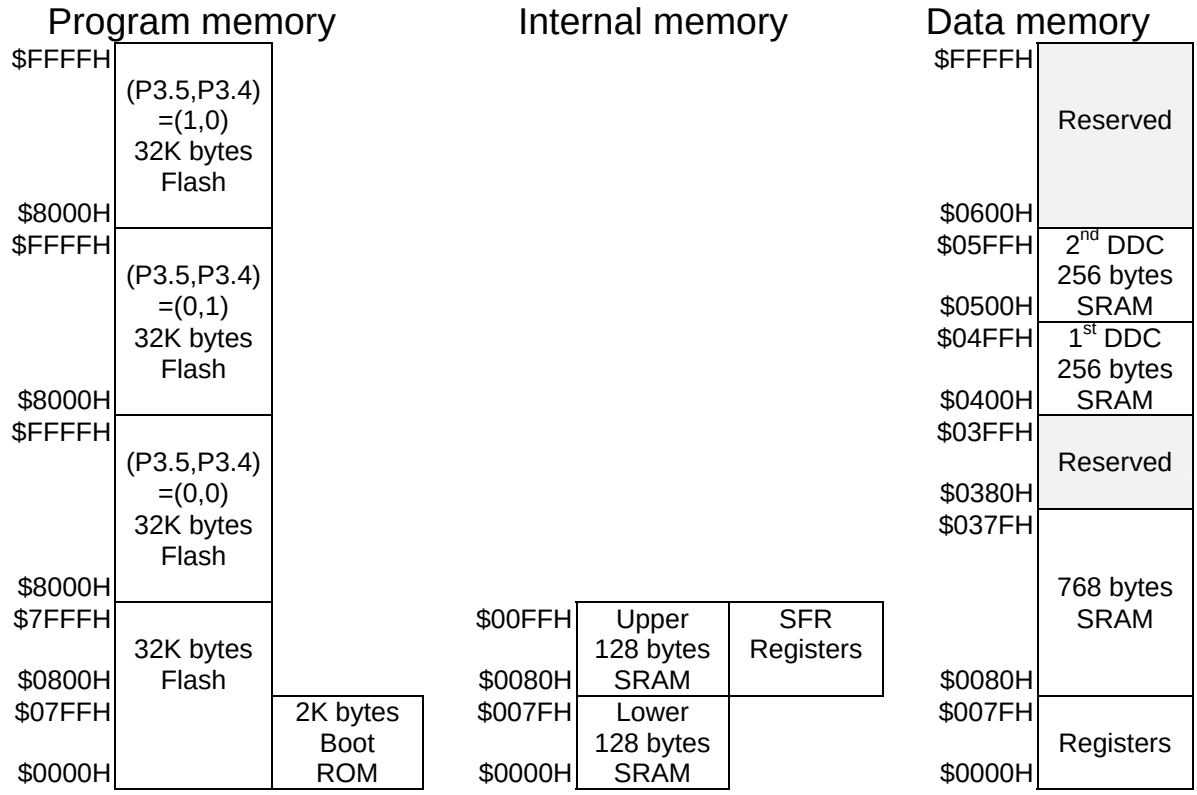
RAM

The 1536 bytes SRAM include:
128 bytes internal SRAM are from $0000H to $007FH (direct & indirect addressing)
128 bytes internal SRAM are from $0080H to $00FFH (indirect addressing)
768 bytes external SRAM are from $0080H to $037FH
256 bytes external SRAM are from $0400H to $04FFH for 1st DDC EDID
256 bytes external SRAM are from $0500H to $05FFH for 2nd DDC EDID

Flash Memory

128K bytes flash memory for program. Address is located from $00000h to $1FFFFh.
8031 (P3.5,P3.4) ports switch the flash memory bank.
When 8031 address[15]=0, (P3.5,P3.4)=(x,x) => flash address[16:0]=00000h-07FFFh.
When 8031 address [15]=1, (P3.5,P3.4)=(0,0) => flash address[16:0]=08000h-0FFFFh.
When 8031 address [15]=1, (P3.5,P3.4)=(0,1) => flash address[16:0]=10000h-17FFFh.
When 8031 address [15]=1, (P3.5,P3.4)=(1,0) => flash address[16:0]=18000h-1FFFFh.

Memory Mapping



System Reset

There are three reset sources of this controller. All reset signals will last 1.024ms. Fig.1 shows the block diagram of reset logic.

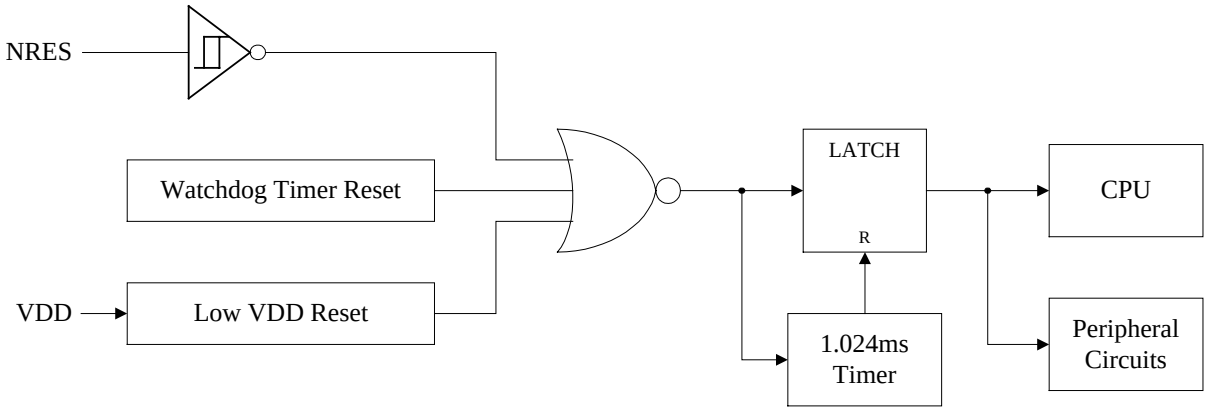


Fig. 1 Reset Signals

NRES

The NRES-Reset happens when there is a low level on the NRES pin.

Low VDD Reset

The Low-VDD-Reset is generated when VDD3V is below 2.7V either VDD=5v or VDD=3.3v. The reset signal will last 1.024ms after the voltage is higher than 2.7V.

Watchdog Timer Reset

The Watchdog-Timer-Reset happens when the watchdog timer is time out. Please refer to the watchdog timer section for more detail.

I/O Port

I/O Port A

The PA0 and PA1 are general purpose IO shared with DDC interface and 8031 UART interface. They are the IO port only when both ENDDC and REN are “0”. If the PA0OE is “1”, Pin PA0 is an **open-drain** output port. If the PA0OE is “0”, Pin PA0 is an input port **without** internal pull-up resistor. The PA1 is the same as the PA0. Fig. 2 shows the structure of PA0.

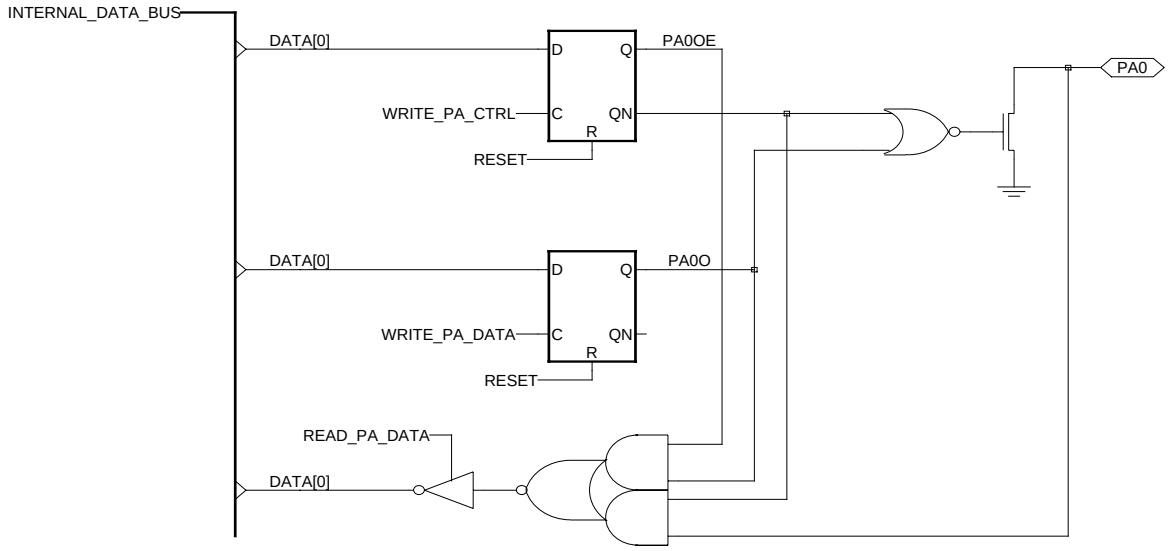


Fig.2 Structure of PA0, PA1,PA2,PA3

The PA4 to PA7 are general purpose IO shared with PWM output and some special functions. When the EPWMn is “0” and the special function is disabled, PAn is a general purpose I/O port. If the PAnOE is “1”, the PAn is configured as an output port in a push-pull type which can source or sink 6mA. If the PAnOE is “0”, the PAn is configured as an input port with internal pull-up resistor.

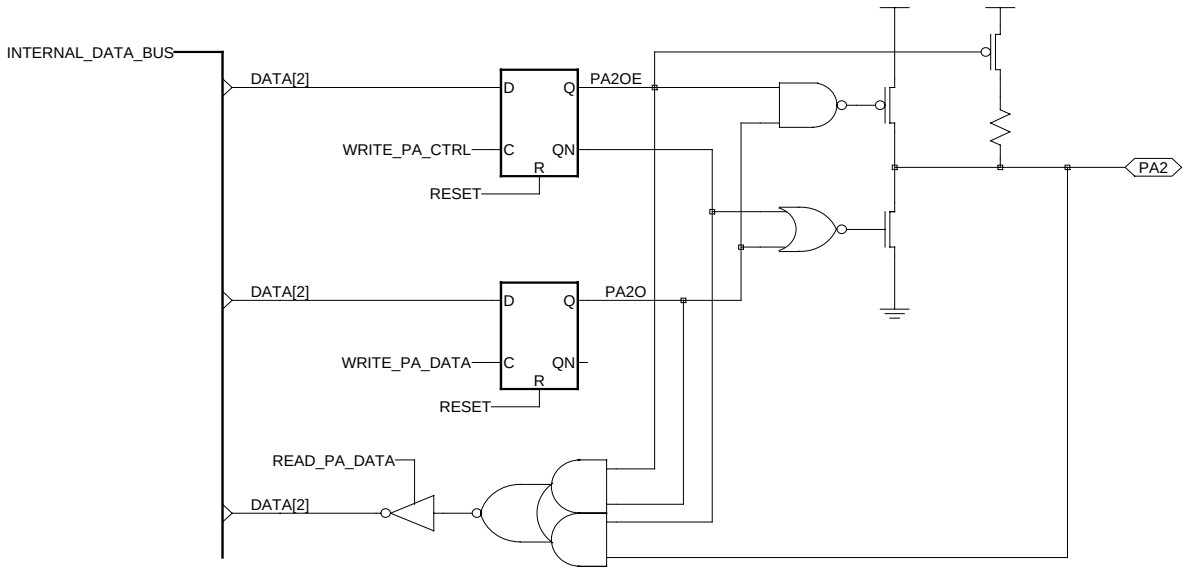


Fig.3 Structure of PA4

Port A control and data register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PA_CTRL	0000h	W	00h	PA7OE	PA6OE	PA5OE	PA4OE	PA3OE	PA2OE	PA1OE	PA0OE
PA_DATA	0001h	R	ffh	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W	ffh	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Bit Name	Description
PAnOE	Port An Output Enable. When it is set, PAn is configured as an output pin. When it is cleared, PA2~PA7 are configured as the input pin with internal pull-up resistor. PA0 and PA1 are configured as the input pin without internal pull-up resistor.
PAn (W)	This bit controls the output level when the corresponding PAnOE bit is set. When PAn=1, PAn pin outputs high level. (PA0 and PA1 are open-drain output) When PAn=0, PAn pin outputs low level.
PAn (R)	When PAnOE=1 (i.e. output port), the data of this bit is the same to PAn (W). When PAnOE=0, this bit indicates the input level. “1” is high and “0” is low.

I/O Port B

The PB0~PB6 are general purpose IO shared with some special functions. When the special function is disabled, the PBn is a general purpose I/O port and is same as PA2. If it is configured as an output, it could source/sink 6mA. If it is configured as an input, there is an internal pull-up resistor enabled.

Port B control and data register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PB_CTRL	0002h	W	00h	--	PB6OE	PB5OE	PB4OE	PB3OE	PB2OE	PB1OE	PB0OE
PB_DATA	0003h	R	xfh	--	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		W	Xfh	--	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Bit Name	Description
PBnOE	Port Bn Output Enable. When it is “1”, PBn is configured as an output pin. When it is “0”, PBn is configured as an input pin with internal pull high
PBn (W)	This bit controls the output level when the corresponding PBnOE bit is set. When PBn=1, the PBn pin outputs high level. When PBn=0, the PBn pin outputs low level.
PBn (R)	When PBnOE=1 (i.e. output port), the data of this bit is the same to PBn (W). When PBnOE=0, this bit indicates the input level. “1” is high and “0” is low.

I/O Port C

The PC0~PC7 are general purpose IO shared with some special functions. When the function is disabled, the PCn is a general purpose I/O port and is the same as PA2. If it is configured as output, it could source 6mA and sink 10mA. If it is configured as an input, it has an internal pull-up resistor.

Port C control and data register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PC_CTRL	0004h	W	00h	PC7OE	PC6OE	PC5OE	PC4OE	PC3OE	PC2OE	PC1OE	PC0OE
PC_DATA	0005h	R	ffh	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		W	ffh	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Bit Name	Description
PCnOE	Port Cn Output Enable. When it is “1”, PCn is configured as an output pin. When it is “0”, PCn is configured as an input pin with internal pull-up resistor.
PCn (W)	This bit controls the output level when the corresponding PCnOE bit is set. When PCn=1, PCn pin outputs high level. When PCn=0, PCn pin outputs low level.
PCn (R)	When PCnOE=1 (i.e. output port), the data of this bit is the same as PCn (W). When PCnOE=0, this bit indicates the input level. “1” is high and “0” is low.

I/O Port E

The PE0~PE3 are the general purpose IO shared with PWM output. When the corresponding EPWMn bit is “0”, it is a general I/O port and is the same as PA2. If it is configured as an output, it could source/sink 6mA. If it is configured as an input, it has an internal pull-up resistor.

Port E control and data register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PE_CTRL	0008h	W	00h	--	--	--	--	PE3OE	PE2OE	PE1OE	PE0OE
PE_DATA	0009h	R	xfh	--	--	--	--	PE3	PE2	PE1	PE0
		W	xfh	--	--	--	--	PE3	PE2	PE1	PE0

Bit Name	Description
PEnOE	Port En Output Enable. When it is “1”, the PEn is configured as an output pin. When it is “0”, the PEn is configured as an input pin with internal pull-up resistor.
PEn (W)	This bit controls the output level when the corresponding PEnOE bit is set. When PEn=1, PEn pin outputs high level. When PEn=0, PEn pin outputs low level.
PEn (R)	When PEnOE=1 (i.e. output port), the data of this bit is the same as PEn (W). When PEnOE=0, this bit indicates the input level. “1” is high and “0” is low.

I/O Port D

The PD0~PD7 are the general purpose IO shared with some special functions. When the special function is disabled, it is a general purpose I/O port. If it is configured as output, it could source/sink 6mA. If it is configured as input and PdnHE is “0”, it has an internal pull-up resistor. If the PDn is configured as input and the PDnHE is “1”, it doesn’t have an internal pull-up resistor.

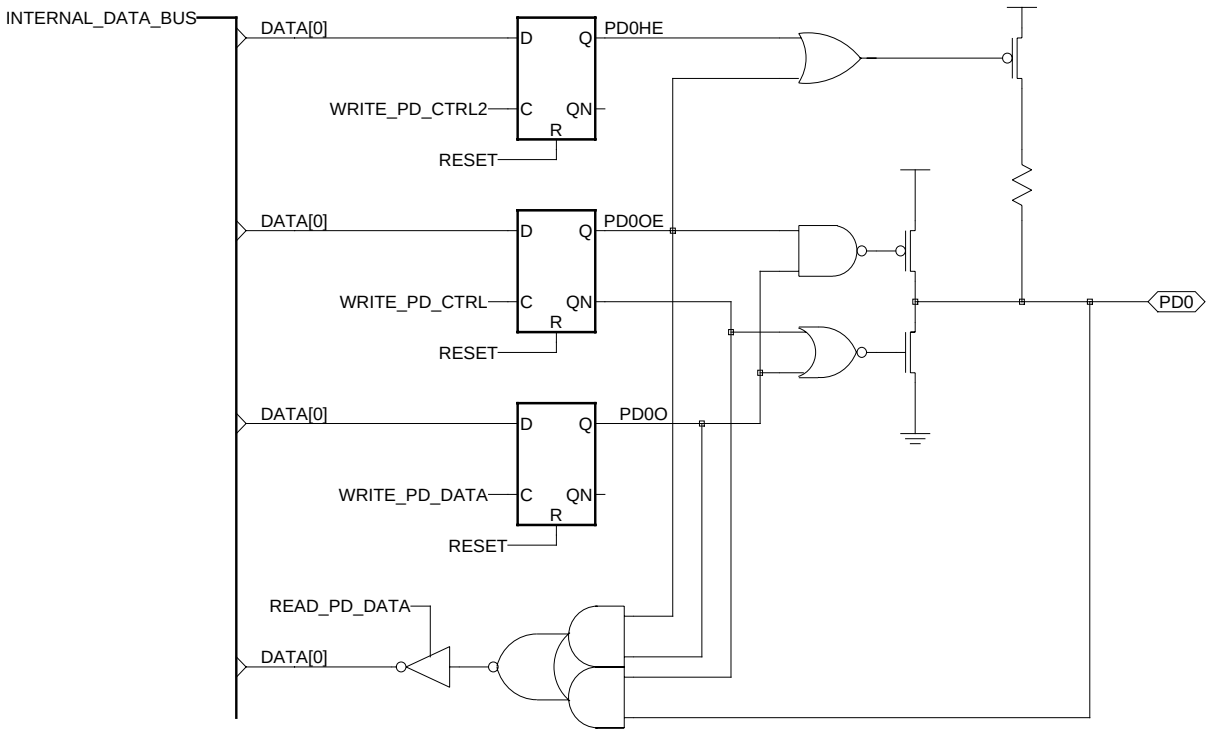


Fig.4 Structure of PD0

Port D control and data register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PD_CTRL	0006h	W	00h	PD7OE	PD6OE	PD5OE	PD4OE	PD3OE	PD2OE	PD1OE	PD0OE
PD_DATA	0007h	R	ffh	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
		W	ffh	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PD_CTRL2	000Ah	W	00h	PD7HE	PD6HE	PD5HE	PD4HE	PD3HE	PD2HE	PD1HE	PD0HE

Bit Name	Description
PDnOE	Port Dn Output Enable. When it is “1”, PDn is configured as an output pin. When it is “0”, PDn is configured as an input pin with internal pull-up resistor.
PDn (W)	This bit controls the output level when the corresponding PDnOE bit is set. When PDn=1, PDn pin outputs high level. When PDn=0, PDn pin outputs low level.
PDn (R)	When PDnOE=1 (i.e. output port), the data of this bit is same as PDn (W). When PDnOE=0, this bit indicates the input level. “1” is high and “0” is low.
PDnHE	Configured the Port Dn pull-up resistor. When PDnHE =1, PDn pin without pull-up resistor. When PDnHE =0, PDn pin with pull-up resistor.

SYNC Processor

The functional block diagram of Sync Processor is shown in Fig.5. It contains H and V polarity detection circuit, H and V frequency counter, composite sync signal separation circuit, free-running H and V sync signal generator, video signal generation circuit for burn-in test and clamp pulse generator.

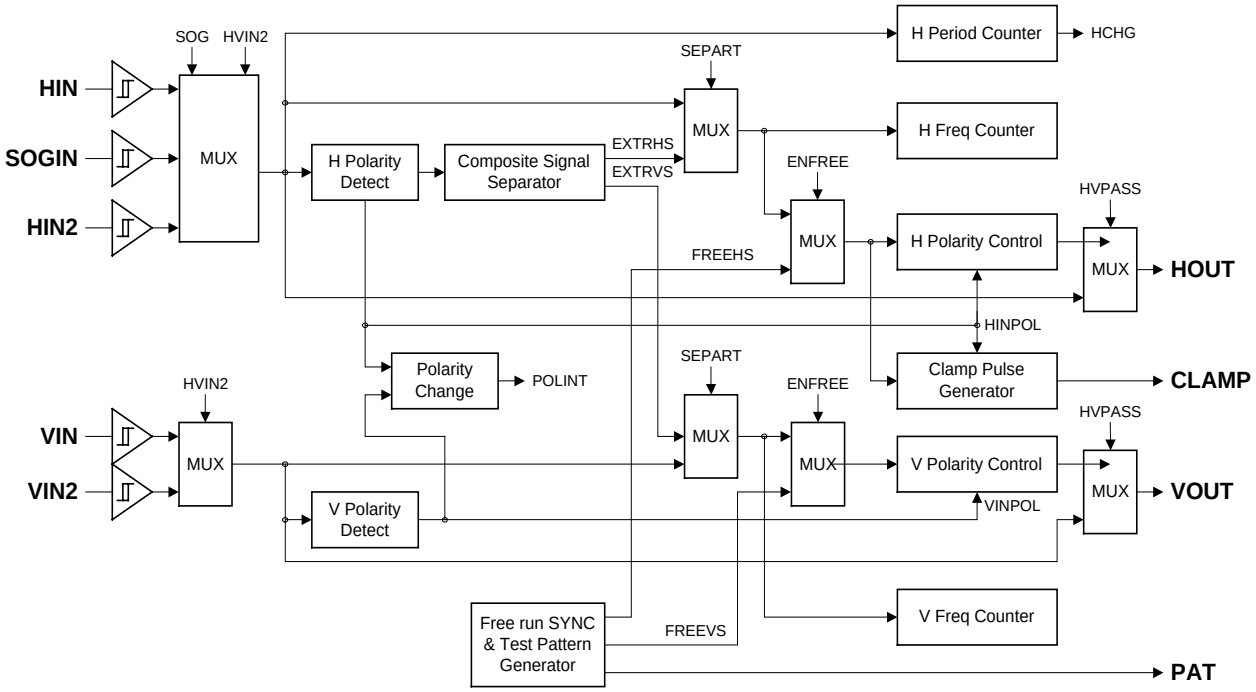


Fig.5 Block diagram of sync signal processor

Horizontal Frequency Counter

A 13-bit counter is used to measure horizontal frequency.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
HFREQ_L	0010h	R	xxh	HLVL	HINPOL	HCHG	HFL4	HFL3	HFL2	HFL1	HFL0
HFREQ_H	0011h	R	xxh	HFH7	HFH6	HFH5	HFH4	HFH3	HFH2	HFH1	HFH0

Bit Name	Description
HLVL	"1": Indicates Hsync pin is high level. "0": Indicates Hsync pin is low level.
HINPOL	"1": Indicates Hsync input is positive polarity. "0": Indicates Hsync input is negative polarity.
HCHG	"1": If the H period has been changed.
HFH7~ HFH0	Indicates the Hsync frequency in kHz.
HFL4~ HFL0	When QUICK="0", HFL4 ~ HFL0 indicates the Hsync frequency in 31.25Hz unit. When QUICK="1", HFL4 ~ HFL1 indicates the Hsync frequency in 62.5Hz.

Horizontal polarity detect
The horizontal polarity is detected by sampling HIN signal with a delay time after rising and falling edge of HIN. When the 126kHz<HIN, sample level at 3.5us – 4.5us after HIN transition edge. When the 23kHz<HIN<126kHz, sample level at 5.5us – 6.5us after HIN transition edge. When the HIN<23khz, sample level at 8.5us – 9.5us after HIN transition edge.

Horizontal frequency detect
User can choose 16ms or 32ms time interval to count pulse number of Hsync every 16.384ms or 32.768ms. For example, if QUICK bit is set, when a 16.384ms time frame begins, it resets the counter and starts counting Hsync pulses till 16ms reached, then loads the counter value to HFREQ_H and HFREQ_L registers. If the H frequency is over 192kHz, the H counter will stop counting.
The sync processor interrupt is generated every 16.384ms or 32.768ms for checking H frequency. This interrupt will be cleared after reading the HFREQ_H register.

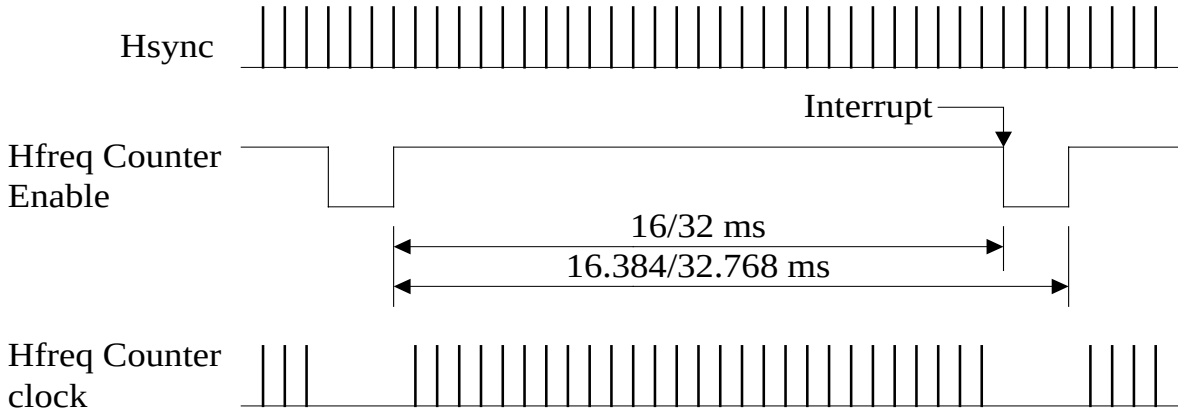


Fig.6 Horizontal Frequency Counter timing

Example of Hsync Frequency Calculation

QUICK="0"				QUICK="1"			
HFH6..0	**HFL4..0**	**Max. Freq**	**Min. Freq**	**HFH6..0**	**HFL4..0**	**Max. Freq**	**Min. Freq**
$40h	$00010b	64.0938KHz	64.0312KHz	$40h	$0001xb	64.1250KHz	64.0000KHz
$40h	$00011b	64.1250KHz	64.0625KHz				
$51h	$10000b	81.5313KHz	81.4687KHz	$51h	$1000xb	81.5625KHz	81.4375KHz
$51h	$10001b	81.5625KHz	81.5000KHz				
$51h	$10010b	81.5938KHz	81.5312KHz	$51h	$1001xb	81.6250KHz	81.5000KHz
$51h	$10011b	81.6250KHz	81.5625KHz				

Vertical Frequency Counter

A 13-bit counter is used to measure the time interval between two vertical sync pulses.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
VFREQ_L	0012h	R	xxh	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
VFREQ_H	0013h	R	xxh	VLVL	VINPOL	VOVF	VF12	VF11	VF10	VF9	VF8

Bit Name	Description
VLVL	"1": Indicates Vsync pin is high level. "0": Indicates Vsync pin is low level.
VNPOL	"1": Indicates Vsync input is positive polarity. (SEPART in HV_CR1 also make it "1") "0": Indicates Vsync input is negative polarity.
VOVF	"1": Indicates V counter is overflowed. Vsync frequency is lower than 15.25Hz. "0": Vsync frequency is over 15.25Hz.
VF12 ~ VF0	Indicates the Vertical Total Time. Vertical frequency is [125000 / (counter value $\pm$1)] Hz

Vertical polarity detect

Vertical polarity is detected by sampling VIN level at 2.048ms after rising edge of VIN. If the level is low, the polarity is positive (VINPOL=1). If the level is high, the polarity is negative (VINPOL=0). But if SEPART bit is set, the VINPOL bit is "1" because the Vsync from composite signal separator is always positive polarity.

Vertical frequency detect

It will be updated every vertical frame. The clock of this counter is 125kHz. So the frequency of Vsync is [125000 / (counter value $\pm$ 1)] Hz. When V frequency is lower than 15.25Hz, this counter stops counting and set VOVF bit to "1".

Vertical polarity is detected by sampling VIN level at 2.048ms after rising edge of VIN.

Example of Vsync frequency calculation

VF12..0	Max. Freq	Min. Freq	VF12..0	Max. Freq	Min. Freq
$05BDh	85.15Hz	85.034Hz	$0783h	65.036Hz	64.969Hz
$05BEh	85.092Hz	84.976Hz	$0784h	65.003Hz	64.935Hz
$05BFh	85.034Hz	84.918Hz	$0785h	64.969Hz	64.901Hz
$0681h	75.12Hz	75.03Hz	$0823h	60.038Hz	59.981Hz
$0682h	75.075Hz	74.985Hz	$0824h	60.01Hz	59.952Hz
$0683h	75.03Hz	74.94Hz	$0825h	59.981Hz	59.923Hz
$06C7h	72.088Hz	72.005Hz	$1FFDh	15.266Hz	15.262Hz
$06C8h	72.046Hz	71.963Hz	$1FFEh	15.264Hz	15.260Hz
$06C9h	72.005Hz	71.921Hz	$1FFFh	15.262Hz	15.258Hz

Hsync Period Counter

The H_PERD is an 8-bit counter to detect the cycle time of the Hsync input.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
H_PERD	0014h	R	xxh	HPRD7	HPRD6	HPRD5	HPRD4	HPRD3	HPRD2	HPRD1	HPRD0

This is an 8-bit counter that uses 6MHz clock to measure time interval between two H pulses. If the H frequency is lower than 23437.5Hz, this counter will overflow and register H_PERD value is zero.

Hsync Counter In One Vsync Period

Enumerate the H pulses between two V pulses.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
HF_VL	0015h	R	00h	HFV7	HFV6	HFV5	HFV4	HFV3	HFV2	HFV1	HFV0
HF_VH	0016h	R	x0h					HFV11	HFV10	HFV9	HFV8

The register can be used as H total.

Vsync overflow control register

The VFQ_OVF is used in blanking for Vertical frequency changed.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
VFQ_OVF	0010h	W	FFh	OVVF7	OVVF6	OVVF5	OVVF4	OVVF3	OVVF2	OVVF1	OVVF0

If the VIN frequency is lower than (7812.5Hz/OVVFn), the vertical frequency overflow flag of the interrupt will be set.

VFQ_OVF reference table

VFQ_OVF	Frequency	VFQ_OVF	Frequency	VFQ_OVF	Frequency	VFQ_OVF	Frequency
100	78.125 Hz	**120**	65.104 Hz	**140**	55.803 Hz	**160**	48.828 Hz
102	76.593 Hz	**122**	64.037 Hz	**142**	55.017 Hz	**162**	48.225 Hz
104	75.120 Hz	**124**	63.004 Hz	**144**	54.253 Hz	**164**	47.637 Hz
106	73.703 Hz	**126**	62.004 Hz	**146**	53.510 Hz	**166**	47.063 Hz
108	72.338 Hz	**128**	61.035 Hz	**148**	52.787 Hz	**168**	46.503 Hz
110	71.022 Hz	**130**	60.096 Hz	**150**	52.083 Hz	**170**	45.955 Hz
112	69.754 Hz	**132**	59.185 Hz	**152**	51.398 Hz	**172**	45.421 Hz
114	68.530 Hz	**134**	58.302 Hz	**154**	50.730 Hz	**174**	44.899 Hz
116	67.934 Hz	**136**	57.445 Hz	**156**	50.080 Hz	**176**	44.389 Hz
118	66.207 Hz	**138**	56.612 Hz	**158**	49.446 Hz	**178**	43.890 Hz

Sync Processor Control Register

The HV_CR1 and HV_CR2 control the HOUT, VOUT and Clamp model.

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
HV_CR1	0011h	W	00h	ENHOUT	ENVOUT	HOPOL	VOPOL	QUICK	SEPART	ENFREE	ENPAT
HV_CR2	0012h	W	00h	ENCLP	CLPEG	CLPPO	CLPPW1	CLPPW0	SOG	HVPASS	BYPASS

Bit Name	Description
ENHOUT	"1": Enable HOUT. "0": Disable HOUT. Pin is configured as I/O port PD1.
ENVOUT	"1": Enable VOUT. "0": Disable VOUT. Pin is configured as I/O port PD0.
HOPOL	"1": HOUT is positive polarity. "0": HOUT is negative polarity.
VOPOL	"1": VOUT is positive polarity. "0": VOUT is negative polarity.
QUICK	"1": Select 16ms time interval to count H pulses every 16.384ms. "0": Select 32ms time interval to count H pulses every 32.768ms.
SEPART	When H+V mode, the falling edge of extracted Vsync is synchronized with Hsync leading edge. "1": Enable sync separator circuit and use the extracted Vsync signal as VOUT. "0": VOUT pin outputs Vsync from VIN pin
ENFREE	Enable free-running sync signal output on HOUT and VOUT pins when this bit is set.
ENPAT	"1": Enable self-test pattern output on PAT pin when this bit is set. "0": Disable test pattern output. Pin is configured as I/O port PB3.
ENCLP	"1": Enable clamp pulse output on CLAMP pin. "0": Disable clamp pulse output. Pin is configured as I/O port PA7.
CLPEG	"1": Clamp pulse follows HOUT signal's rising edge. "0": Clamp pulse follows HOUT signal's falling edge.
CLPPO	"1": Clamp pulse is positive polarity. "0": Clamp pulse is negative polarity.
CLPPW1 ~ CLPPW2	(CLPPW1,CLPPW0)=(0,0) : clamp pulse width=125ns – 208ns (CLPPW1,CLPPW0)=(0,1) : clamp pulse width=208ns – 292ns (CLPPW1,CLPPW0)=(1,0) : clamp pulse width=458ns – 542ns (CLPPW1,CLPPW0)=(1,1) : clamp pulse width=958ns – 1042ns
SOG	Select composite sync signal input source. "1" : Composite sync signal comes from SOGIN pin. "0" : Composite sync signal comes from HIN pin.
HVPASS	Select bypass HSYNC & VSYNC. "1" : HOUT = HIN & VOUT=VIN without polarity changed. "0" : HOUT = HIN & VOUT=VIN with polarity changed.
BYPASS	Select bypass the composite signal separator or not. "1" : HOUT pin outputs sync signal bypass the composite signal separator. "0" : HOUT pin outputs sync signal from the composite signal separator.

Output Polarity Control
HOPOL and VOPOL bits control the polarities of HOUT and VOUT. When the bit is “1”, the output polarity is positive. When the bit is “0”, the output polarity is negative.

HVPASS
HVPASS will deliver the Hsync and Vsync from HIN and VIN to HOUT and VOUT without polarity changed.

Composite Sync Signal Separator
The composite sync signal separator can handle H+V and H exclusive-OR V signals. It will extract Vsync signal from HIN or SOGIN input pin by filtering abnormal pulses. The output Vsync signal will be widened about 4.5~5.5us. The output Hsync will be replaced by 2us pulse during Vsync pulse. Fig.7 shows the relationship of the extracted H and V sync signals.

If inserting the pseudo H pulses (Extracted HS signal) during Vsync pulse is not necessary, set BYPASS bit can make HOUT pin output waveform the same as Hsync input (Note: polarity can be controlled by HOPOL bit), set HVPASS can make HOUT pin output waveform fully the same to Hsync input.

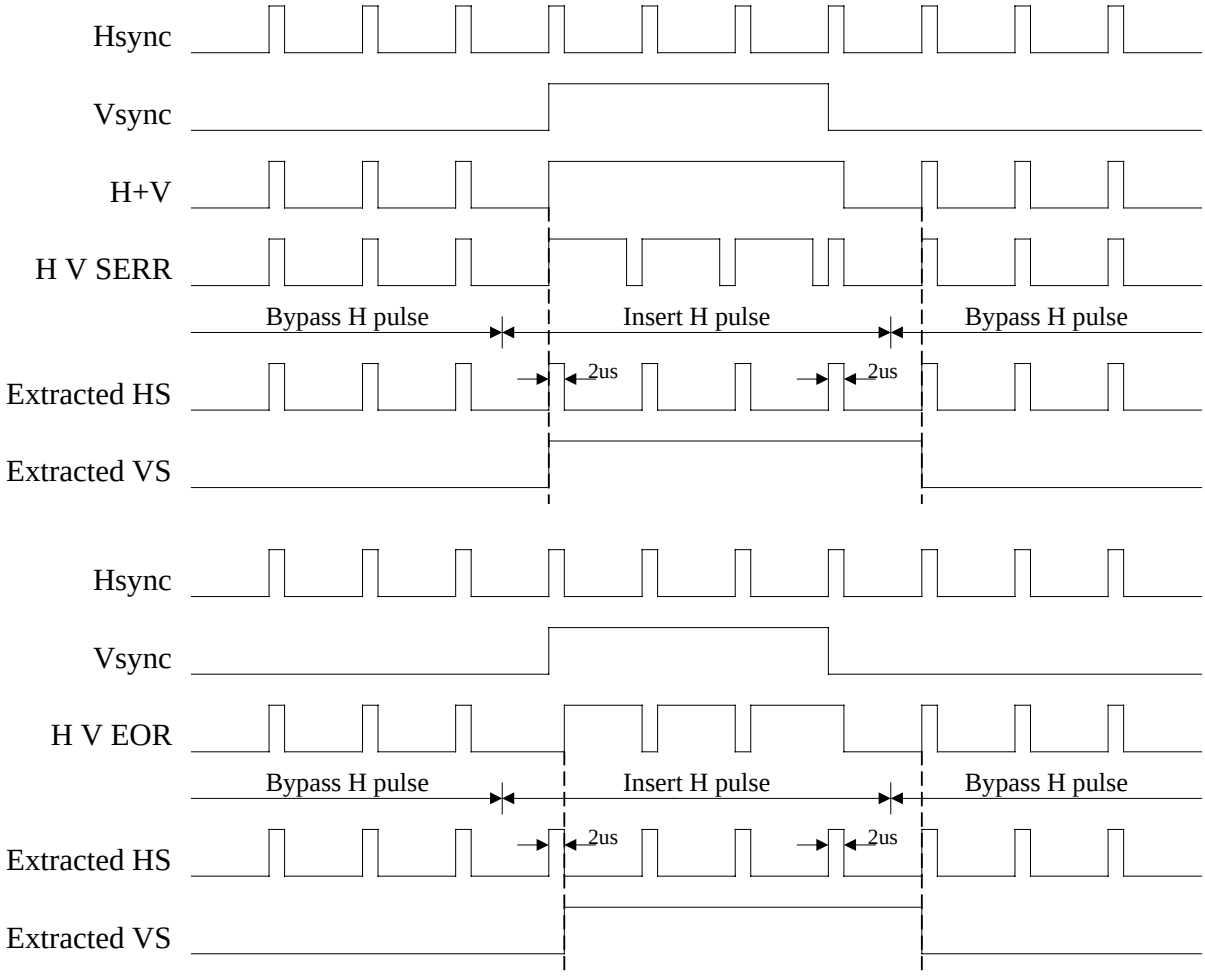


Fig.7 Timing relationship of composite SYNC signal separator

Free-Run Frequency Control Registers

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
FRH_CR	0013h	W	00h			FRH5	FRH4	FRH3	FRH2	FRH1	FRH0
FRHD_CR	0014h	W	00h	FRHB4	FRHD6	FRHD5	FRHD4	FRHD3	FRHD2	FRHD1	FRHD0
FRHB_CR	0015h	W	00h	FRHB3	FRHB2	FRHB1	FRHB0	FRHW3	FRHW2	FRHW1	FRHW0
FRV_CR	0016h	W	00h	FRV7	FRV6	FRV5	FRV4	FRV3	FRV2	FRV1	FRV0
FRVD_CR	0017h	W	00h	FRVD7	FRVD6	FRVD5	FRVD4	FRVD3	FRVD2	FRVD1	FRVD0
FRVB_CR	0018h	W	00h	FRVB4	FRVB3	FRVB2	FRVB1	FRVB0	FRVW2	FRVW1	FRVW0

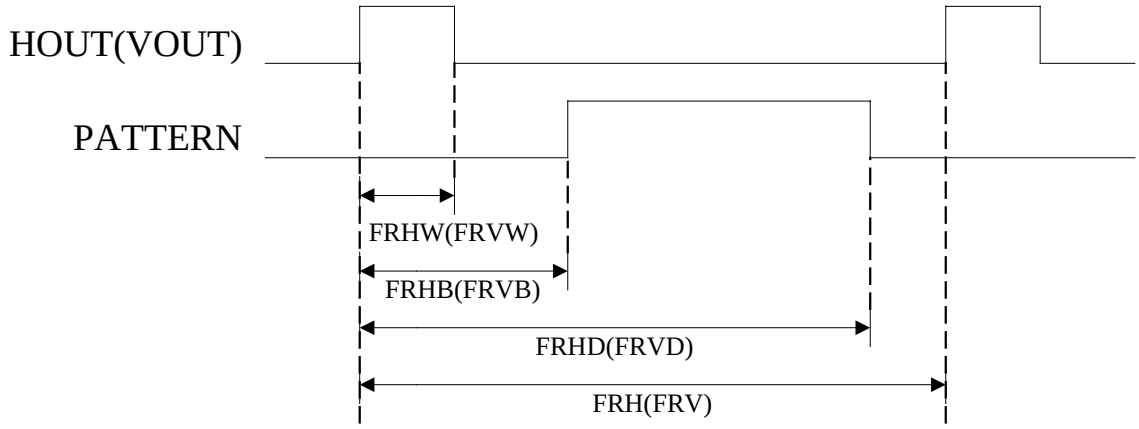


Fig. 8 Free-running SYNC signal and test pattern timing

Bit Name	Description
FRH	The FRH defines the horizontal free run frequency as HF_{FREE}=750K/FRH_CR.
FRHD	The FRHD defines the time from the horizontal blanking to the pattern end. T_{FRHD}=FRHD*0.667μs=H display+ H back porch+ H blanking
FRHB	The FRHB defines the time from the horizontal blanking to the pattern start. T_{FRHB}=FRHB*0.333μs=H back porch+ H blanking
FRHW	The FRHW defines the time for the horizontal blanking. T_{FRHW}=FRHW*0.333μs=H blanking width
FRV	The FRV defines the vertical free run frequency as VF_{FREE}=HF_{FREE}/(FRV_CR*8)
FRVD	The FRVD defines the time from the vertical blanking to the vertical pattern end. T_{FRVD}=HF_{FREE}/(FRVD*8)=V display+ V back porch+ V blanking
FRVB	The FRVB defines the time from the vertical blanking to the pattern start. T_{FRVD}=HF_{FREE}/(FRVB*2)=V back porch+ V blanking
FRVW	The FRVW defines the time for the vertical blanking. T_{FRVW}=HF_{FREE}/(FRVW*2)=V blanking width

H pulse & period = X + 83.3ns
V pulse & period = 2xn H + 1H

FRH reference table

FRH	Frequency	FRH	Frequency	FRH	Frequency	FRH	Frequency
0	--	**16**	46.88 kHz	**32**	23.44 kHz	**48**	15.63 kHz
1	750 kHz	**17**	44.12 kHz	**33**	22.73 kHz	**49**	15.31 kHz
2	375 kHz	**18**	41.67 kHz	**34**	22.06 kHz	**50**	15 kHz
3	250 kHz	**19**	39.47 kHz	**35**	21.43 kHz	**51**	14.76 kHz
4	187.5 kHz	**20**	37.5 kHz	**36**	20.83 kHz	**52**	14.42 kHz
5	150 kHz	**21**	35.71 kHz	**37**	20.27 kHz	**53**	14.15 kHz
6	125 kHz	**22**	34.09 kHz	**38**	19.74 kHz	**54**	13.89 kHz
7	107.14 kHz	**23**	32.6 kHz	**39**	19.23 kHz	**55**	13.64 kHz
8	93.75 kHz	**24**	31.25 kHz	**40**	18.75 kHz	**56**	13.39 kHz
9	83.33 kHz	**25**	30 kHz	**41**	18.29 kHz	**57**	13.16 kHz
10	75 kHz	**26**	28.85 kHz	**42**	17.86 kHz	**58**	12.93 kHz
11	68.18 kHz	**27**	27.78 kHz	**43**	17.44 kHz	**59**	12.71 kHz
12	62.5 kHz	**28**	26.79 kHz	**44**	17.05 kHz	**60**	12.5 kHz
13	57.69 kHz	**29**	25.86 kHz	**45**	16.67 kHz	**61**	12.30 kHz
14	53.57 kHz	**30**	25 kHz	**46**	16.30 kHz	**62**	12.10 kHz
15	50 kHz	**31**	24.19 kHz	**47**	15.96 kHz	**63**	11.90 kHz

Clamp pulse

Clamp pulse is generated on either rising or falling edge of HOUT pin by setting the CLPEG bit. The pulse width of clamp is defined by CLPPW bit. Output polarity is specified by CLPPO bit.

(CLPPW1, CLPPW0)=(0,0): clamp pulse width=125ns – 208ns
(CLPPW1, CLPPW0)=(0,1): clamp pulse width=208ns – 292ns
(CLPPW1, CLPPW0)=(1,0): clamp pulse width=458ns – 542ns
(CLPPW1, CLPPW0)=(1,1): clamp pulse width=958ns – 1042ns

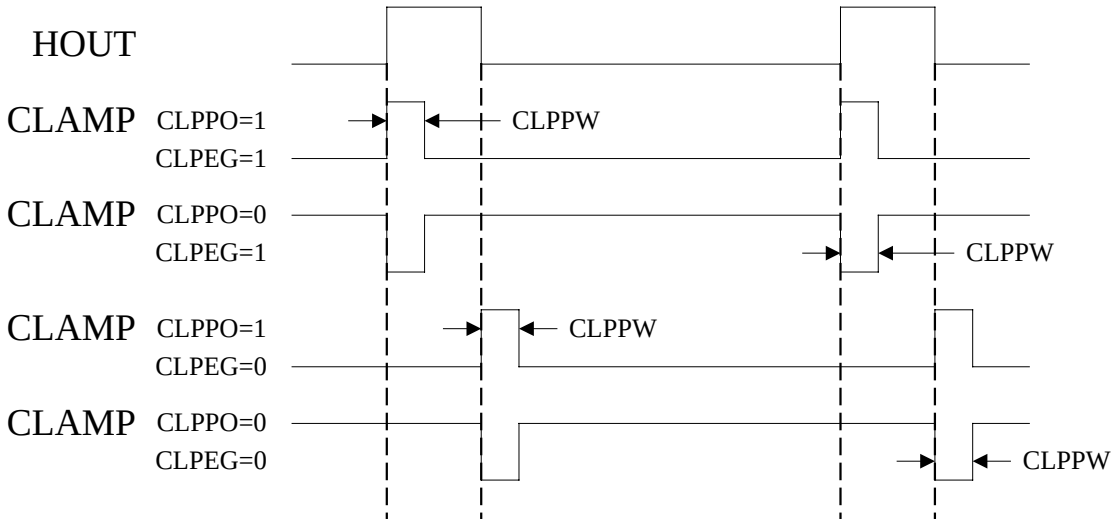


Fig. 9 Clamp pulse waveform

H Period Interrupt Control

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
HPD_CHG	0019h	W	00h					EN_LMT	HCNT2	HCNT1	HCNT0

Bit Name	Description
EN_LMT	Enable H period change interrupt.
HCNT	The range of the H_PERD changed.

1/2HIN, 1/2VIN control

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
1/2HV_CR	001Ah	W	00h	ENH2D	ENV2D	HVEDG					HVIN2

Bit Name	Description
ENH2D	Enable the 1/2 HIN output at the PA5 pin.
ENV2D	Enable the 1/2 VIN output at the PA6 pin.
HVDEG	HIN & VIN trigger edge control. HVEDG=0: leading edge trigger HVEDG=1: tailing edge trigger The duty cycle of both the 1/2HIN and 1/2VIN output are 50%.
HVIN2	Select the 2nd HIN & VIN as sync processor frequency source.

Frequency Divide Function

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
FDM_CON	0040h	W	00h	ENFDM	FDMEG	FDMPOL			FO1M	FO2D	FO3D

Bit Name	Description
ENFDM	Enable the FDM input and output..
FDMEG	"1": the output is synchronized with rising edge of input. "0": the output is synchronized with falling edge of input.
FDMPOL	"1": polarity inverted to input. "0": polarity same as input.
FO1M	Output Frequency = 1x input frequency.
FO2D	Output Frequency = (1/2) x input frequency.
FO3D	Output Frequency = (1/3) x input frequency.

The frequency range of FDI is between 20khz and 180khz and the pulse width of (1/3) input frequency & (1/2) input frequency is a input period (1T).

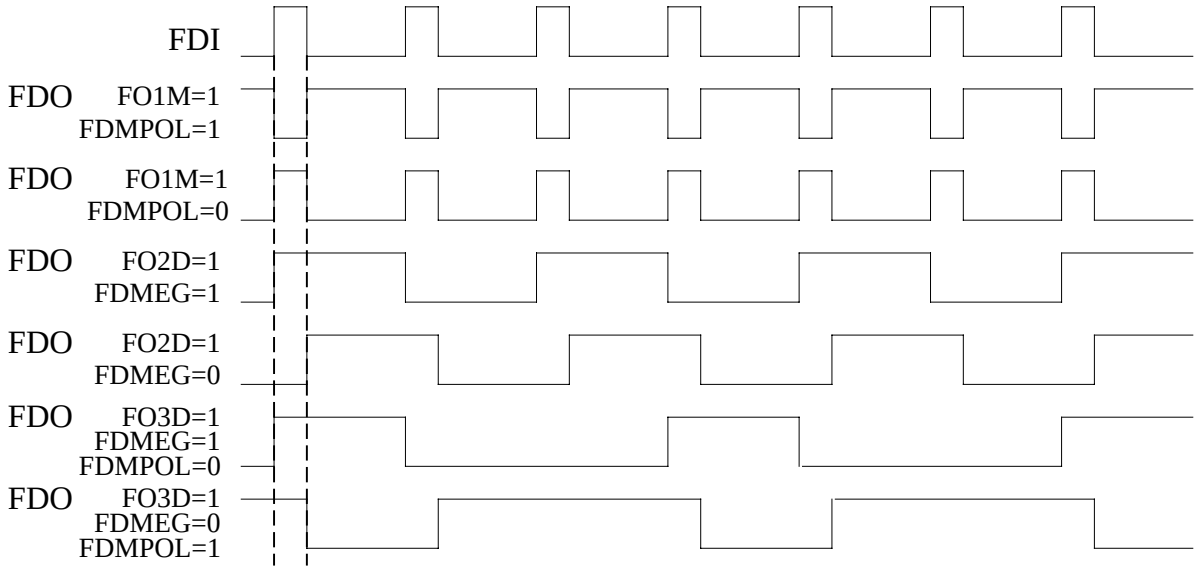


Fig. 10 FDI and FDO waveform

1st DDC & Alignment I2C Interface (PA0,PA1)

DDC Status Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
DDCA_ST1	0024h	R	01h	ALRDYA	BBA	DDC2A	FIRSTA	STOPA	ALGRWA	MATCHA	DRXNKA
DDCA_ST2	0025h	R	00h						IN_CMDA	WR_D3A	

Bit Name	Description
ALRDYA	DDC_AR1 or DDC_AR2 ready. Write the DDC_AR1 will clear this flag.
BBA	Bus busy.
DDC2A	"1": DDC2 selected "0": DDC1 selected
FIRSTA	Indicates the first byte (address) is received when this bit is set.
STOPA	Indicates STOP condition is received when this bit is set.
ALGRWA	Indicates the received R/W bit after 7-bit address. "1": Read "0": Write
MATCHA	0: DDC_ADR1 1: DDC_ADR2
DRXNKA	Received the NAK by DDC_AR1 or DDC_AR2.
IN_CMDA	DDC_ADR0, DDC_ADR1 or DDC_ADR2 have been received. Written 0 to DDC2 will clear this flag.
WR_D3A	H/W DDC data has been updated. Written 1 to CLR_WD3 then 0 to CLR_WD3 will clear this flag.

DDC Control Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
DDCA_CN1	0024h	W	00h	ENDDCA		DDC2A			DTXA		DTXNKA
DDCA_CN2	0025h	W	80h				RAMAH	RAMAL	CL_ADRA	CL_WD3A	WR_ENA

Bit Name	Description
ENDDCA	Enable the H/W DDC function of DDC_AR0.
DDC2A	DDC2=0: DDC1 selected DDC2=1: DDC2 selected
DTXA	"1": Set transmit direction. "0": Set received direction.
DTXNKA	Transmit NAK and IRQ may happen with DDC_AR1 and DDC_AR2.
RAMAH RAMAL	RAMAH=0, RAMAL=1: 128bytes format H/W DDC from 0400h to 047Fh RAMAH=1, RAMAL=1: 256bytes format H/W DDC from 0400h to 04FFh
CL_ADRA	Reset all DDC address pointer to 0.
CL_WD3A	Clear the flag indicated that the H/W DDC data has been changed.
WR_ENA	Enable the H/W DDC_WRITE.

DDC receive & transmit buffer register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
DDCA_RTX	0026h	R/W	FFh	DRXA7	DRXA6	DRXA5	DRXA4	DRXA3	DRXA2	DRXA1	DRXA0

DDC port control register

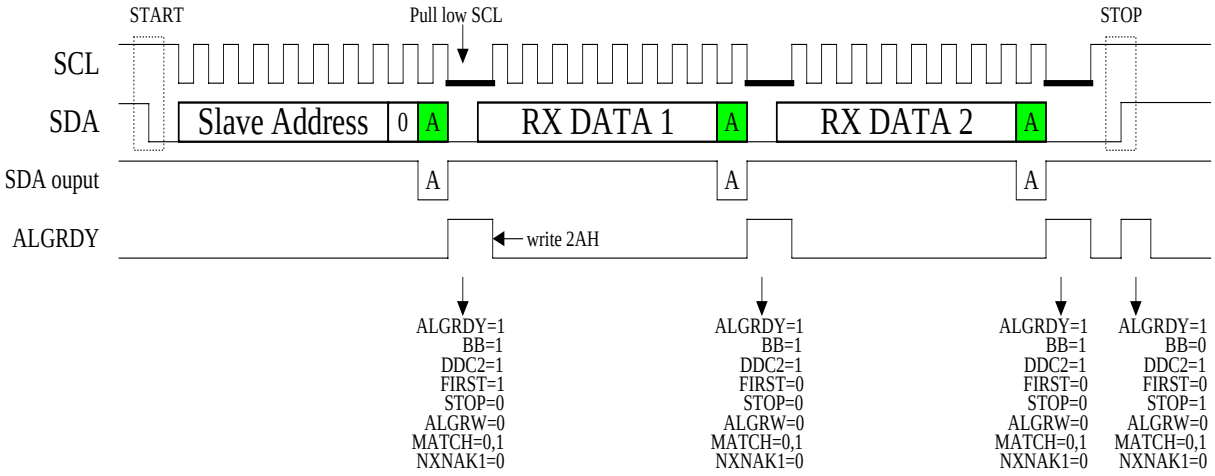
Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
DDCA_AAE	0027h	W	FFh	EN_AN7A	EN_AN6A	EN_AN5A	EN_AN4A	EN_AN3A	EN_AN2A	EN_AN1A	EN_AN0A
DDCA_AR0	0029h	W	X0h	DAR07A	DAR06A	DAR05A	DAR04A	--	--	--	ENAR0A
DDCA_AR1	002Ah	W	X0h	DAR17A	DAR16A	DAR15A	DAR14A	DAR13A	DAR12A	DAR11A	ENAR1A
DDCA_AR2	002Bh	W	X0h	DAR27A	DAR26A	DAR25A	DAR24A	DAR23A	DAR22A	DAR21A	ENAR2A

Bit Name	Description
DDCA_AAE	Optional address as DDC_AR0 bit0~bit3.
DDCA_AR0	The I^2C slave address0 defines by user as DDC port. The bits from bit0 to bit3 are defined by DDCA_AAE. Refer to 24h and 25h for hardware DDC setting.
DDCA_AR1	The I^2C slave address1 defines by user and shares with DDC port.
DDCA_AR2	The I^2C slave address2 defines by user and shares with DDC port.

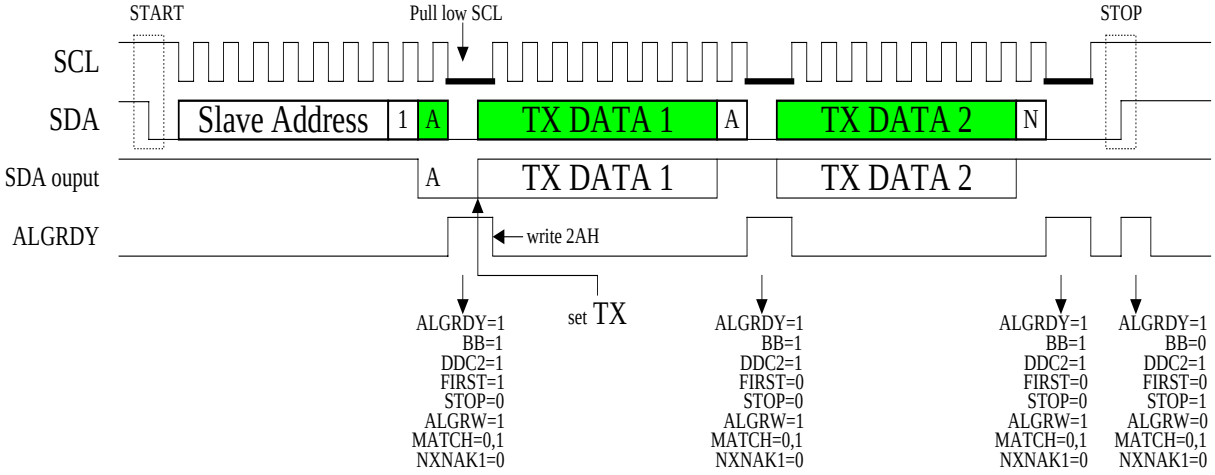
2nd DDC & Alignment I2C Interface (PA2,PA3)

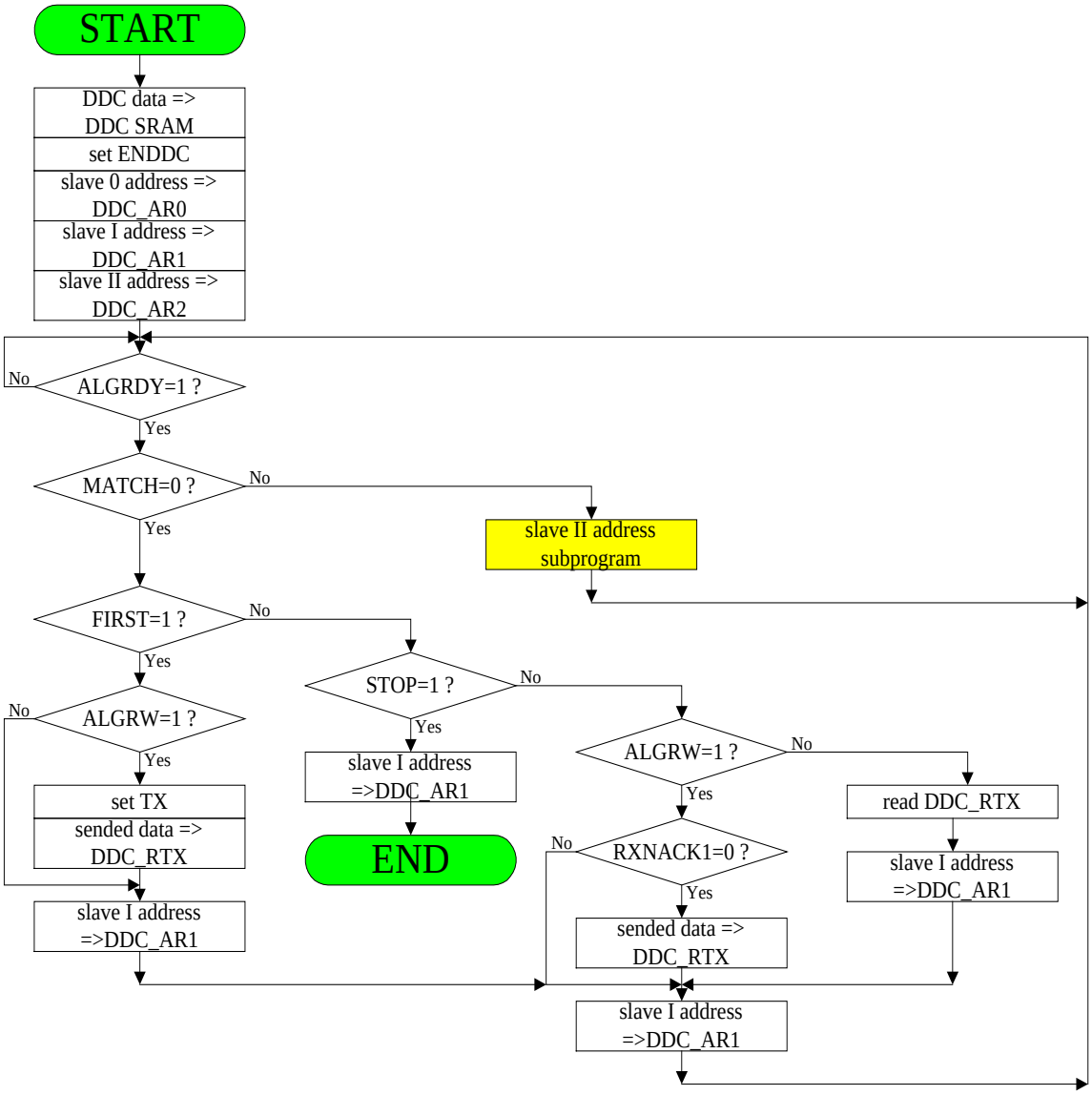
Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
DDCB_ST1	0044h	R	01h	ALRDYB	BBB	DDC2B	FIRSTB	STOPB	ALGRWB	MATCHB	DRXNKB
DDCB_ST2	0045h	R	00h						IN_CMDB	WR_D3B	
DDCB_CN1	0044h	W	00h	ENDDCB		DDC2B			DTXB		DTXNKB
DDCB_CN2	0045h	W	80h				RAMBH	RAMBL	CL_ADRB	CL_WD3B	WR_ENB
DDCB_RTX	0046h	R/W	FFh	DRXB7	DRXB6	DRXB5	DRXB4	DRXB3	DRXB2	DRXB1	DRXB0
DDCB_AAE	0047h	W	FFh	EN_AN7B	EN_AN6B	EN_AN5B	EN_AN4B	EN_AN3B	EN_AN2B	EN_AN1B	EN_AN0B
DDCB_AR0	0049h	W	X0h	DAR07B	DAR06B	DAR05B	DAR04B	--	--	--	ENAR0B
DDCB_AR1	004Ah	W	X0h	DAR17B	DAR16B	DAR15B	DAR14B	DAR13B	DAR12B	DAR11B	ENAR1B
DDCB_AR2	004Bh	W	X0h	DAR27B	DAR26B	DAR25B	DAR24B	DAR23B	DAR22B	DAR21B	ENAR2B

(1) DDC2 slave I, II write mode :



(2) DDC2 slave I, II read mode :




START
DDC data => DDC SRAM
set ENDDC
slave 0 address => DDC_AR0
slave I address => DDC_AR1
slave II address => DDC_AR2
No
ALGRDY=1 ?
Yes
MATCH=0 ?
No
Yes
slave II address subprogram
FIRST=1 ?
No
Yes
STOP=1 ?
No
Yes
slave I address =>DDC_AR1
END
ALGRW=1 ?
No
Yes
set TX
sended data => DDC_RTX
slave I address =>DDC_AR1
ALGRW=1 ?
No
Yes
read DDC_RTX
slave I address =>DDC_AR1
RXNACK1=0 ?
No
Yes
sended data => DDC_RTX
slave I address =>DDC_AR1

Master/Slave I²C Interface

I²C interface Status Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
I2C_STA	0020h	R	22h			BB	SFIRST	SSTOP	SRW	RXNAK2	I2CRDY

Bit Name	Description
BB	"1": Bus busy. "0": Bus idle. Both SDA2 and SCL2 pins keep in high level for 5us after STOP condition.
SFIRST	This bit is set when received START and first byte in slave mode.
SSTOP	This bit is set when received STOP condition in slave mode.
SRW	Received R/W bit in slave mode. "1": Read command is received. "0": Write command is received.
RXNAK2	"1": NACK is received. "0": ACK is received.
I2CRDY	This bit is set when a byte is received, transmitted or STOP condition is detected.

I²C interface Control Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
I2C_CON	0020h	W	02h	ENI2C	MCLK1	MCLK0	MSTR	MSTOP	I2CRW	TXNAK2	SLAVE

Bit Name	Description
ENI2C	"1": Enable I2C interface. "0": Pin PB5 and pin PB4 are I/O port.
MCLK1, 0	Select SCL clock in master mode "00": 400KHz "01": 200KHz "10": 100KHz "11": 50KHz
MSTR	Output START condition in master mode when this bit is set.
MSTOP	Output STOP condition in master mode when this bit is set.
I2CRW	"0": Transmitter, "1": Receiver in master mode. "1": Transmitter, "0": Receiver in slave mode ("0": I2C write mode, "1": I2C read mode.)
TXNAK2	"1": Output NACK. "0": Output ACK. It will pull low the SDA2 pin on acknowledge bit.
SLAVE	"1": Slave mode. "0": Master mode.

I²C interface Transmit/Receive Buffer Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
I2C_TX	0021h	W	xxh	MTX7	MTX6	MTX5	MTX4	MTX3	MTX2	MTX1	MTX0
I2C_RX	0021h	R	xxh	MRX7	MRX6	MRX5	MRX4	MRX3	MRX2	MRX1	MRX0

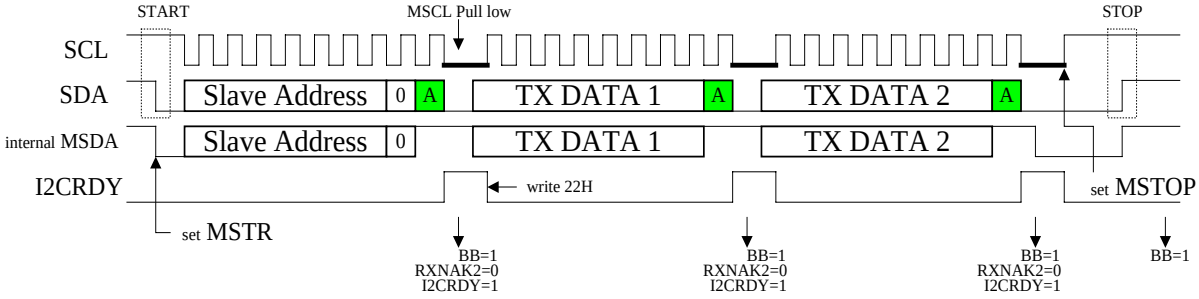
I²C interface Address Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
I2C_ADR	0022h	W	X0h	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	DLYHLD

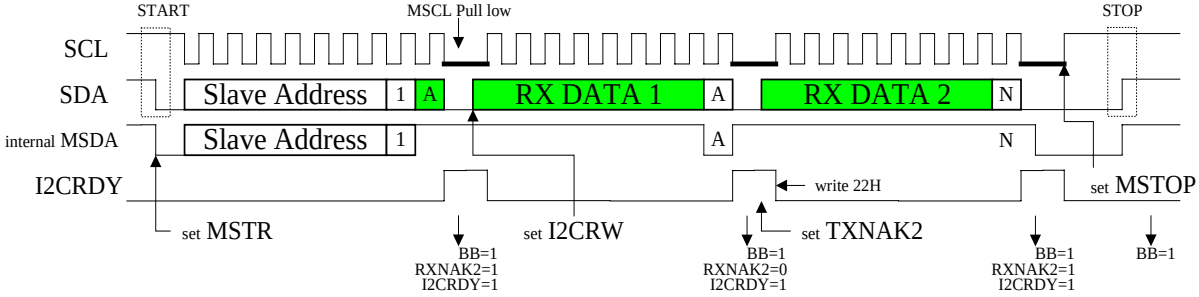
Bit Name	Description
SAR7 ~ SAR1	7-bit address to be compared in slave mode.
DLYHLD	Delay 1/2 SCL clock hold time.

I²C Data Sequence

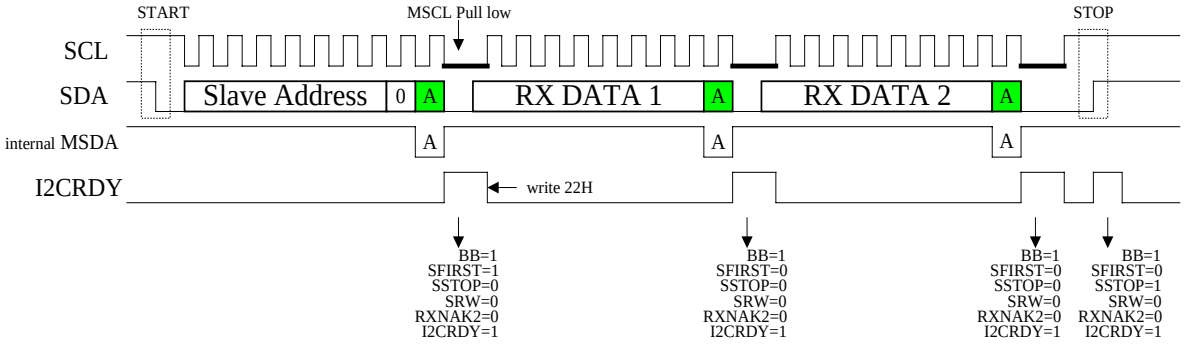
(1) Master write mode :



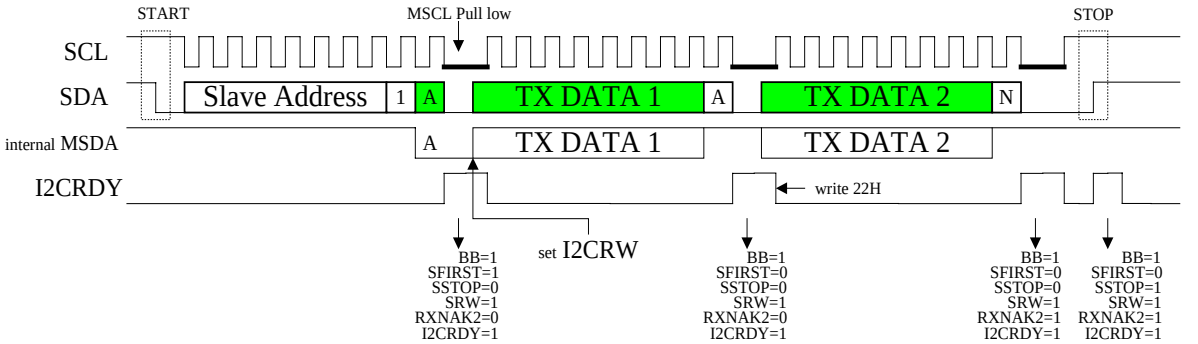
(2) Master read mode :



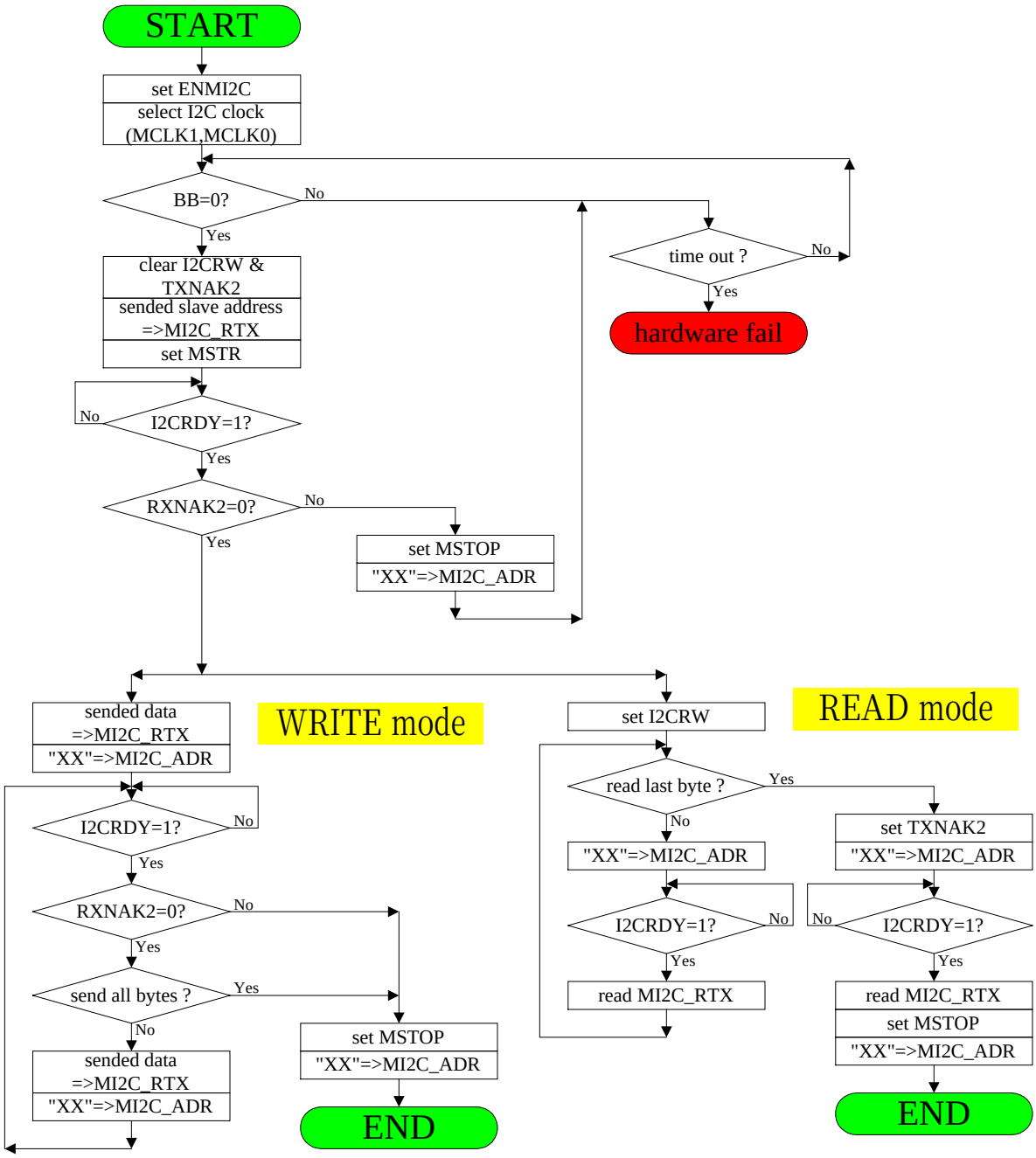
(3) Slave write mode :



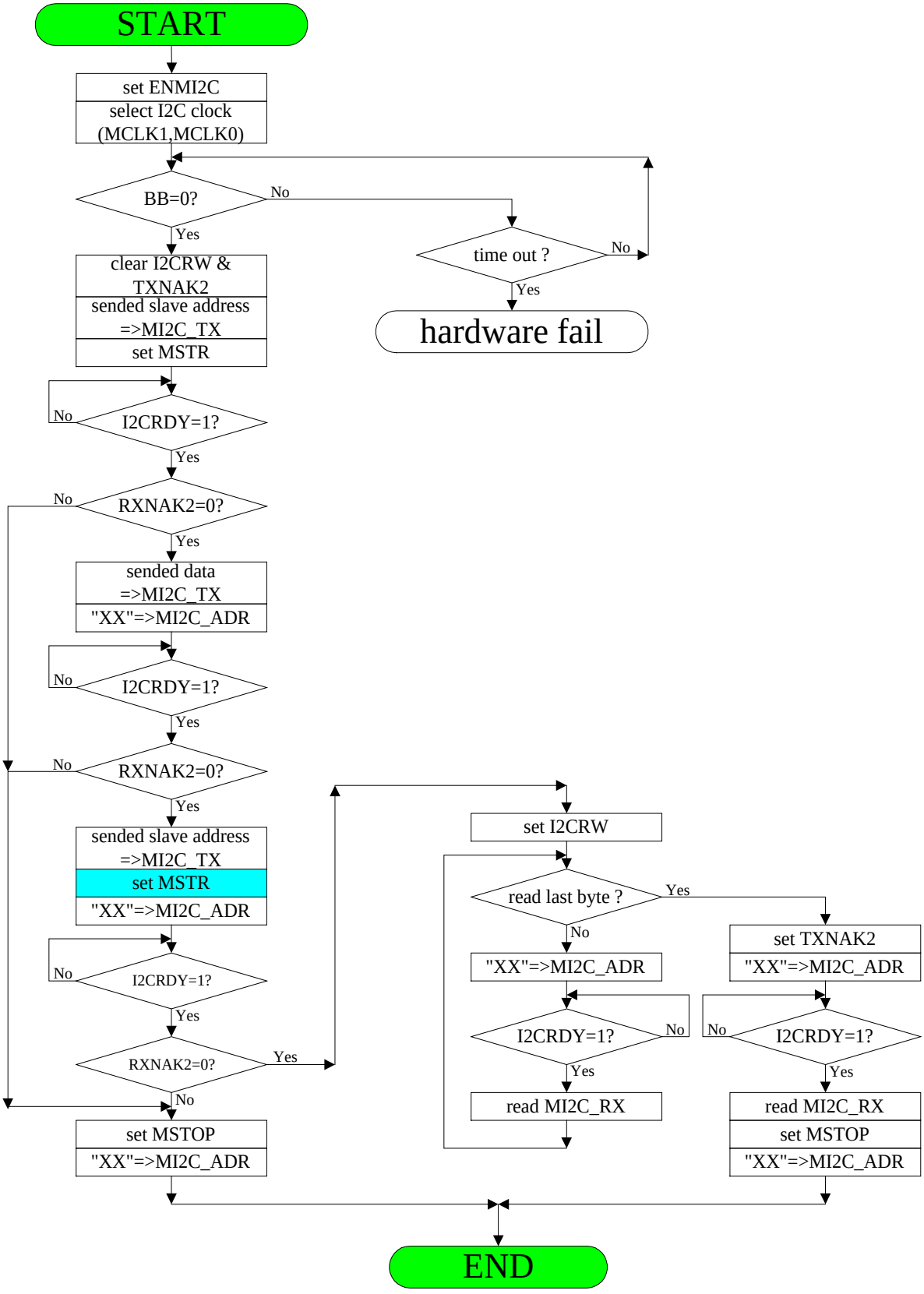
(4) Slave read mode :



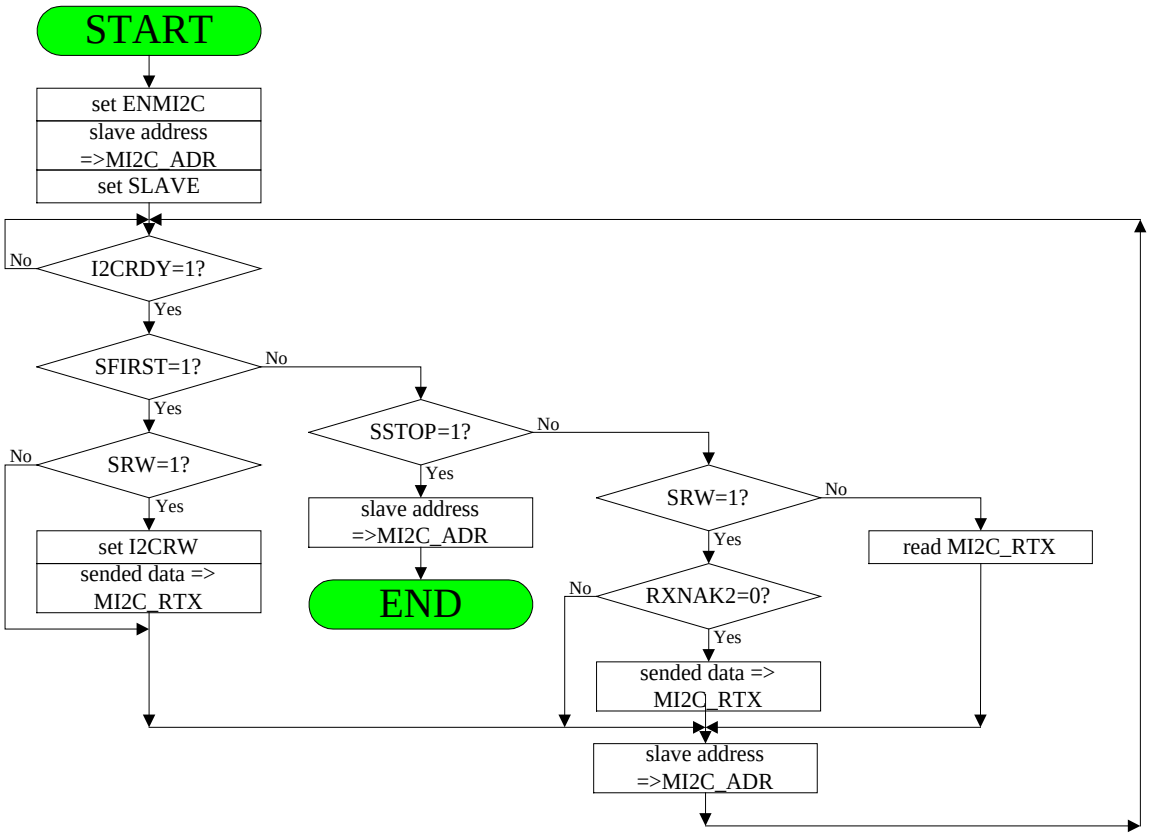
Master I2C Flow Chart



Master I2C (reSTART mode) Flow Chart



Salve I2C Flow Chart



Interrupt Control

Interrupt flag register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
INT_FLG	002Ch	R	00h	IF_DDCA	IF_MI2C	IF_DDCB	IF_SYNC	IF_IRQ2	IF_IRQ1	IF_VSO	IF_VIN
INT_FLG2	002Dh	R	00h	IF_POL	IF_OVV	IF_HCHG	IF_TM6	IF_TM5	IF_TM4	IF_TM3	IF_TM2

These interrupt sources are connected to CPU8051 /INT1

Bit Name	Description
IF_DDCA	"1" indicate 1st DDC interrupt has been triggered.
IF_DDCB	"1" indicate 2nd DDC interrupt has been triggered.
IF_MI2C	"1" indicate I2C interrupt has been triggered.
IF_SYNC	"1" indicate Hsync counter ready interrupt has been triggered.
IF_IRQ2	"1" indicate NIRQ2 interrupt has been triggered.
IF_IRQ1	"1" indicate NIRQ1 interrupt has been triggered.
IF_VSO	"1" indicate Vsync output leading edge interrupt has been triggered.
IF_VIN	"1" indicate Vsync input leading edge interrupt has been triggered.
IF_POL	"1" indicate Hsync or Vsync input polarity changed interrupt has been triggered.
IF_OVV	"1" indicate Vsync input overflow interrupt has been triggered. (Refer to Addr 10h VFQ_OVF Vsync overflow control register)
IF_HCHG	"1" indicate Hsync input period changed interrupt has been triggered. (Refer to Addr 19h H period interrupt control)
IF_TM6	"1" indicate general purpose timer 6 (NIRQ6) interrupt has been triggered.
IF_TM5	"1" indicate general purpose timer 5 (NIRQ5) interrupt has been triggered.
IF_TM4	"1" indicate general purpose timer 4 (NIRQ4) interrupt has been triggered.
IF_TM3	"1" indicate general purpose timer 3 (NIRQ3) interrupt has been triggered.
IF_TM2	"1" indicate general purpose timer 2 (NIRQ2) interrupt has been triggered.

Interrupt enable register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EN	002Ch	W	00h	IE_DDCA	IE_MI2C	IE_DDCB	IE_SYNC	IE_IRQ2	IE_IRQ1	IE_VSO	IE_VIN
INT_EN2	002Dh	W	00h	IE_POL	IE_OVV	IE_HCHG	IE_TM6	IE_TM5	IE_TM4	IE_TM3	IE_TM2

Bit Name	Description
IE_DDC	Enable DDC interrupt when this bit is set.
IE_MI2C	Enable I2C interrupt when this bit is set.
IE_SYNC	Enable Hsync ready interrupt when this bit is set.
IE_IRQ2	Enable NIRQ2 interrupt when this bit is set.
IE_IRQ1	Enable NIRQ1 interrupt when this bit is set.
IE_VSO	Enable VOUT interrupt when this bit is set.
IE_VIN	Enable VIN interrupt when this bit is set.
IE_POL	Enable POLINT interrupt when this bit is set.
IE_OVV	Enable V overflow interrupt when this bit is set.
IE_HCHG	Enable HCHG interrupt when this bit is set.
IE_ TM6	Enable general purpose timer 6 (NIRQ6) interrupt when this bit is set.
IE_ TM5	Enable general purpose timer 5 (NIRQ5) interrupt when this bit is set.
IE_ TM4	Enable general purpose timer 4 (NIRQ4) interrupt when this bit is set.
IE_ TM3	Enable general purpose timer 3 (NIRQ3) interrupt when this bit is set.
IE_ TM2	Enable general purpose timer 2 (NIRQ2) interrupt when this bit is set.

Interrupt Source Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
INT_SRC	002Eh	R	00h	POLINT	OVVINT		SYNC	IRQ2	IRQ1	VSO	VIN

Bit Name	Description
POLINT	"1": Polarity Change
OVVINT	"1": Vsync input is lower than OVVFn
SYNC	"1": Hsync detect counter is ready
IRQ2	"1": NIRQ2 has been triggered.
IRQ1	"1": NIRQ1 has been triggered.
VSO	"1": Vsync output leading edge has been triggered.
VIN	"1": Vsync input leading edge has been triggered.

Interrupt Control Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ_CON1	002Eh	W	00h	CLR_POL	CLR_OV			CLR_IRQ2	CLR_IRQ1	CLR_VSO	CLR_VIN
IRQ_CON2	002FH	W	00h					IRQ2_RF	IRQ2_EG	IRQ1_RF	IRQ1_EG

Bit Name	Description
CLR_POL	Set CLR_POL to clear polarity changed interrupt event.
CLR_OV	Set CLR_OV to clear Vsync input overflow interrupt event.
CLR_IRQ2	Set CLR_IRQ2 to clear the IRQ2 interrupt event.
CLR_IRQ1	Set CLR_IRQ1 to clear the IRQ1 interrupt event.
CLR_VSO	Clear VOUT interrupt when this bit is set.
CLR_VIN	Clear Vsync input interrupt when this bit is set.
IRQ2_EG& IRQ2_RF	IRQ2_EG=0, IRQ2_RF=x, NIRQ2 will be triggered by a low level over 1us. IRQ2_EG=1, IRQ2_RF=0, NIRQ2 will be triggered by a falling edge. IRQ2_EG=1, IRQ2_RF=1, NIRQ2 will be triggered by a rising edge.
IRQ1_EG& IRQ1_RF	IRQ1_EG=0, IRQ1_RF=x, NIRQ1 will be triggered by a low level over 1us. IRQ1_EG=1, IRQ1_RF=0, NIRQ1 will be triggered by a falling edge. IRQ1_EG=1, IRQ1_RF=1, NIRQ1 will be triggered by a rising edge.

Interrupt Control and Clear

1st DDC interface interrupt

Interrupt Condition	Clear Interrupt
Receive one byte in DDC2 mode.	Write address to DDC_AR1A (Addr 2Ah) register.
Transmit data buffer is empty in DDC2 mode.	Write address to DDC_AR1A (Addr 2Ah) register.
Received a STOP condition in DDC2 mode.	Write address to DDC_AR1A (Addr 2Ah) register.

2nd DDC interface interrupt

Interrupt Condition	Clear Interrupt
Receive one byte in DDC2 mode.	Write address to DDC_AR1B (Addr 4Ah) register.
Transmit data buffer is empty in DDC2 mode.	Write address to DDC_AR1B (Addr 4Ah) register.
Received a STOP condition in DDC2 mode.	Write address to DDC_AR1B (Addr 4Ah) register.

I2C interface interrupt

Interrupt Condition	Clear Interrupt
After transmit a byte.	Write address to MI2C_AR register.
After receive a byte.	Write address to MI2C_AR register.
Received a STOP condition when slave mode.	Write address to MI2C_AR register.

Sync Processor interrupt

Interrupt Condition	Clear Interrupt
Latch a new H frequency to HFREQ_H and HFREQ_L register every 32.768ms or 16.384ms.	Read HFREQ_H Register.

NIRQ1 pin interrupt

Interrupt Condition	Clear Interrupt
NIRQ1 has been triggered.	Write “1” to CLR_IRQ1 bit in IRQ_CON1 register then write “0” to CLR_IRQ1.

NIRQ2 pin interrupt

Interrupt Condition	Clear Interrupt
NIRQ2 has been triggered.	Write “1” to CLR_IRQ2 bit in IRQ_CON1 register then write “0” to CLR_IRQ2.

Vsync output leading edge interrupt

Interrupt Condition	Clear Interrupt
Leading edge of VOUT pin signal.	Write “1” to CLR_VSO bit in IRQ_CON1 register then write “0” to CLR_VSO.

Vsync input leading edge interrupt

Interrupt Condition	Clear Interrupt
Leading edge of VIN pin signal.	Write “1” to CLR_VIN bit in IRQ_CON1 register then write “0” to CLR_VSI.

Polarity change interrupt

Interrupt Condition	Clear Interrupt
HIN or VIN polarity has been changed.	Write “1” to CLR_POL bit in IRQ_CON1 register then write “0” to CLR_POL.

Vsync input overflow interrupt

Interrupt Condition	Clear Interrupt
VIN is lower than VFQ_OVF.	Write “1” to CLR_OV bit in IRQ_CON1 register then write “0” to CLR_OV.

Hsync input change interrupt

Interrupt Condition	Clear Interrupt
The new H_PERD is not in the old H_PERD ± H_CNT (addr 19h).	Read H_PERD (Addr 14h) to clear this interrupt and HCHG.

General purpose timer 2,3,4,5,6 interrupt

Interrupt Condition	Clear Interrupt
NIRQ2 falling/rising edge has been triggered.	Read TM2_DAT (address 57h) will clear this bit.
NIRQ2 timer is overflow (TM2_TOV=1).	Read TM2_DAT (address 57h) will clear this bit.
NIRQ3 falling/rising edge has been triggered.	Read TM3_DAT (address 59h) will clear this bit.
NIRQ3 timer is overflow (TM3_TOV=1).	Read TM3_DAT (address 59h) will clear this bit.
NIRQ4 falling/rising edge has been triggered.	Read TM4_DAT (address 5Bh) will clear this bit.
NIRQ4 timer is overflow (TM4_TOV=1).	Read TM4_DAT (address 5Bh) will clear this bit.
NIRQ5 falling/rising edge has been triggered.	Read TM5_DAT (address 5Dh) will clear this bit.
NIRQ5 timer is overflow (TM5_TOV=1).	Read TM5_DAT (address 5Dh) will clear this bit.
NIRQ6 falling/rising edge has been triggered.	Read TM6_DAT (address 5Fh) will clear this bit.
NIRQ6 timer is overflow (TM6_TOV=1).	Read TM6_DAT (address 5Fh) will clear this bit.

A/D Converter

The Analog-to-Digital Converter (ADC) is 8-bit resolution with four selectable input channels. When EN_CHn is set, PCn is configured as ADC input and PCn pull-high resistor is disabled. When CHn is set, it will reset the ADC_DA register and start converting. After the conversion is done, the ADRDY bit is set and valid data is stored in ADC_DA. The total conversion time is 12us. If program wants to make a new conversion, it writes CHn register again and it will start another conversion.

ADC Data Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_DA	001Ch	R	xxh	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
ADC_RD	001Dh	R	xxh	ADRDY							

Bit Name	Description
ADRDY	ADC data is ready to read when this bit is set.
AD7 ~ AD0	ADC data.

ADC Channel Select Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_CH	001Ch	W	00h	EN_CH3	EN_CH2	EN_CH1	EN_CH0	CH3	CH2	CH1	CH0

Bit Name	Description
EN_CH3	“1”: PC3 is configured as ADC interface. (tri-state with no I/O function). “0”: PC3 is configured as I/O port.
EN_CH2	“1”: PC2 is configured as ADC interface. (tri-state with no I/O function). “0”: PC2 is configured as I/O port.
EN_CH1	“1”: PC1 is configured as ADC interface. (tri-state with no I/O function). “0”: PC1 is configured as I/O port.
EN_CH0	“1”: PC0 is configured as ADC interface. (tri-state with no I/O function). “0”: PC0 is configured as I/O port.
CH3	Select AD3 pin to ADC convert when this bit is set.
CH2	Select AD2 pin to ADC convert when this bit is set.
CH1	Select AD1 pin to ADC convert when this bit is set.
CH0	Select AD0 pin to ADC convert when this bit is set.

Note: The EN_CHn must be set before CHn.

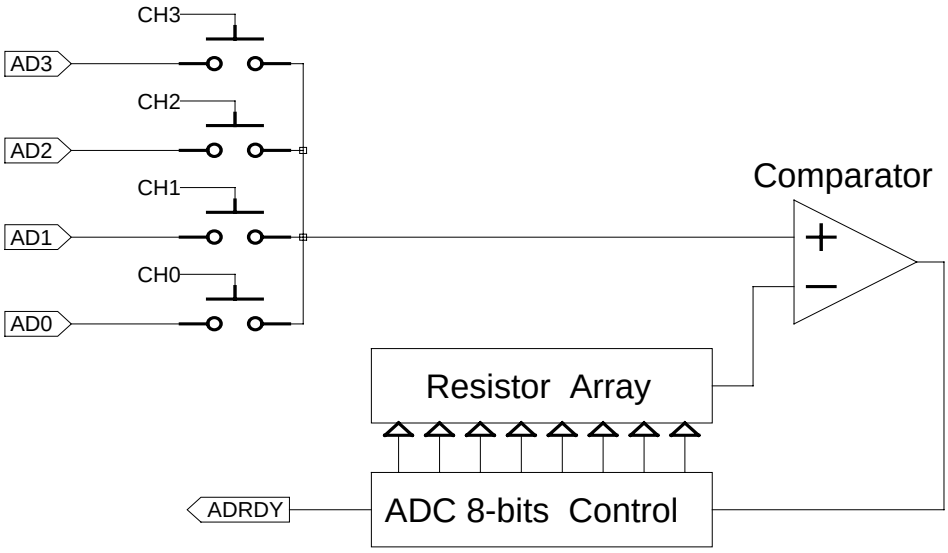
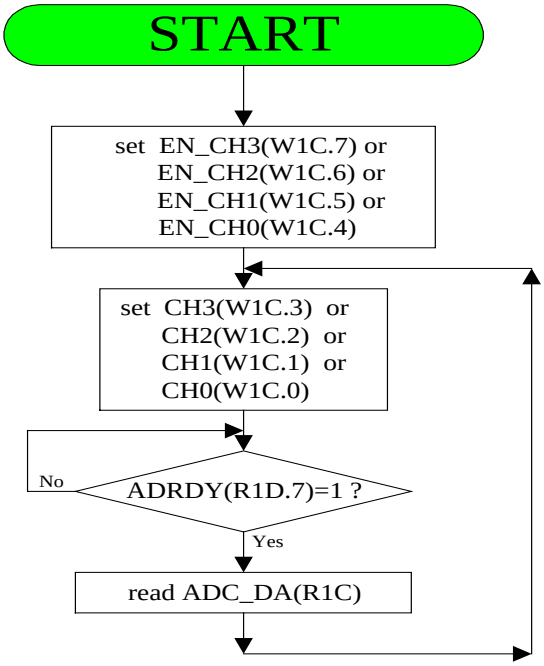


Fig. 11 Block diagram of ADC



General Purpose Timer / External Interrupt (NIRQ6,NIRQ5,NIRQ4,NIRQ3,NIRQ2)

General Purpose Timer Control Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL	0056h	W	20h	ENTM2		EN2_TOV	TM2_CK1	TM2_CK0	TM2_SEG	TM2_RF	

Bit Name	Description
ENTM2	Enable general purpose timer/external interrupt function.
EN2_TOV	Enable timer over flower interrupt (default=1) =0, IRQx is a general purpose external interrupt
TM2_CK1 TM2_CK0	Select timer clock = (0,0) : clock=64us (default) = (0,1) : clock=1us = (1,0) : clock=256us = (1,1) : clock=64ms
TM2_SEG	Enable single edge trigger
TM2_RF	Select Falling/Rising edge trigger (TM2_SEG, TM2_RF)=(0,x) : both edge trigger, rising and falling edge trigger (TM2_SEG, TM2_RF)=(1,0) : Falling edge trigger (TM2_SEG, TM2_RF)=(1,1) : Rising edge trigger

General Purpose Timer Status & Data

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_STA	0056h	R	00h	INT_TM2	TM2_HL	TM2_TOV					
TM2_DAT	0057h	R	00h	TM2_TM7	TM2_TM6	TM2_TM5	TM2_TM4	TM2_TM3	TM2_TM2	TM2_TM1	TM2_TM0

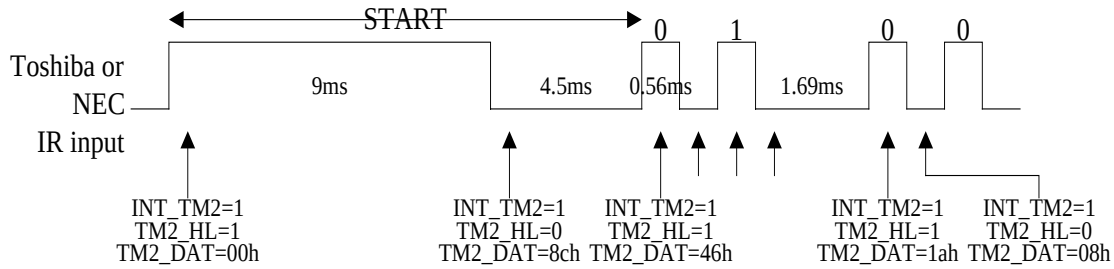
Bit Name	Description
INT_TM2	NIRQ2 edge trigger interrupt flag, H->L or L->H or overflow interrupt. Reading TM2_DAT (address 57h) will clear this bit
TM2_HL	NIRQ2 both edge trigger : =0 : NIRQ2 is now low level =1 : NIRQ2 is now high level
TM2_TOV	NIRQ2 H->L or L->H over (timer-clock*256)
TM2_DAT	NIRQ2 H->L or L->H interval = (timer-clock) * TMx_DAT_TM[7:0]

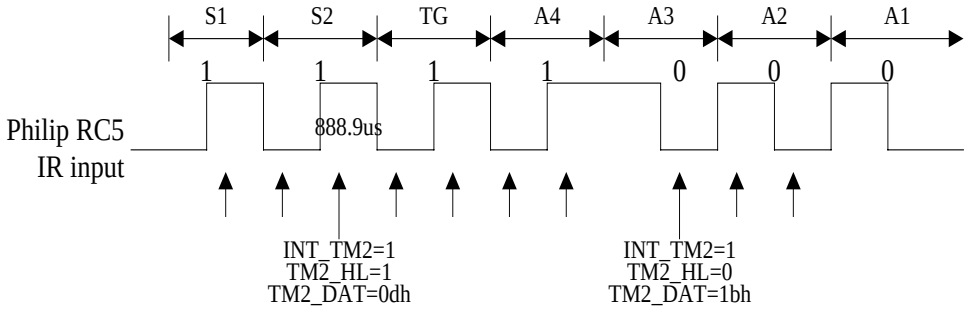
Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL	0058h	W	20h	ENTM3		EN3_TOV	TM3_CK1	TM3_CK0	TM3_SEG	TM3_RF	
TM3_STA	0058h	R	00h	INT_TM3	TM3_HL	TM3_TOV					
TM3_DAT	0059h	R	00h	TM3_TM7	TM3_TM6	TM3_TM5	TM3_TM4	TM3_TM3	TM3_TM2	TM3_TM1	TM3_TM0
TM4_CTL	005Ah	W	20h	ENTM4		EN4_TOV	TM4_CK1	TM4_CK0	TM4_SEG	TM4_RF	
TM4_STA	005Ah	R	00h	INT_TM4	TM4_HL	TM4_TOV					
TM4_DAT	005Bh	R	00h	TM4_TM7	TM4_TM6	TM4_TM5	TM4_TM4	TM4_TM3	TM4_TM2	TM4_TM1	TM4_TM0
TM5_CTL	005Ch	W	20h	ENTM5		EN5_TOV	TM5_CK1	TM5_CK0	TM5_SEG	TM5_RF	
TM5_STA	005Ch	R	00h	INT_TM5	TM5_HL	TM5_TOV					
TM5_DAT	005Dh	R	00h	TM5_TM7	TM5_TM6	TM5_TM5	TM5_TM4	TM5_TM3	TM5_TM2	TM5_TM1	TM5_TM0
TM6_CTL	005Eh	W	20h	ENTM6		EN6_TOV	TM6_CK1	TM6_CK0	TM6_SEG	TM6_RF	
TM6_STA	005Eh	R	00h	INT_TM6	TM6_HL	TM6_TOV					
TM6_DAT	005Fh	R	00h	TM6_TM7	TM6_TM6	TM6_TM5	TM6_TM4	TM6_TM3	TM6_TM2	TM6_TM1	TM6_TM0

When base clock = 64us : Detectable NIRQx min period=64us, max period=16.384ms
When base clock = 1us : Detectable NIRQx min period=1us, max period=256us
When base clock = 256us : Detectable NIRQx min period=256us, max period=65.536ms(15.3hz)
When base clock = 64ms : Detectable NIRQx min period=64ms, max period=16.384s

For example : General purpose Timer => External interrupt
Set TMx_CTL=84h, => ENTMx=1, TMx_SEG =1, TMx_RF =0/1, the others=0
Read TMx_DAT to clear interrupt, but ignore TMx_DAT data

For example : General purpose Timer => IR detector
Set TMx_CTL=A0h, => ENTMx=1, ENx_TOV=1, the others=0
=> Base Clock = 64us
=> Both falling/rising edge trigger.
Read TMx_DAT to clear interrupt, TMx_DAT: High/Low timing





Watchdog Timer

Watchdog Timer Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
WDT	001Eh	W	00h	DISWDT						WDT1	WDT0

Bit Name	Description
DISWDT	"1" : Disable Watchdog Timer. "0" : Enable Watchdog Timer.
WDT	(WDT1, WDT0)=(0,0): reset time = 1.536s (WDT1, WDT0)=(0,1): reset time = 3.072s (WDT1, WDT0)=(1,0): reset time = 48ms (WDT1, WDT0)=(1,1): reset time = 96ms

Power Saving Control

Power Saving Control Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PSC_CTL	0041h	W	00h	IRQ1_WK	IRQ2_WK	DDC_WK	H_{in}1&SOG	Vin1	Hin2	Vin2	

Bit Name	Description
IRQ1_WK	NIRQ1 falling edge trigger to wake up OSC.
IRQ2_WK	NIRQ2 falling edge trigger to wake up OSC.
DDC_WK	SCL, SDA falling edge trigger to wake up OSC.
Hin1_WK& SOG_WK	Hin1, SOG falling edge trigger to wake up OSC.
Vin1_WK	Vin1 falling edge trigger to wake up OSC.
Hin2_WK	Hin2 falling edge trigger to wake up OSC.
Vin2_WK	Vin2 falling edge trigger to wake up OSC.
Bit0	Must be 0.

It will clear all PSC_CTL trigger latch buffer when write data to the register 41H. The trigger latch buffer must be cleared before entering the power down mode. After the external trigger signal received, CPU delays 64ms and wakes up..

Function Configuration Register

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
OTH_CTL1	004Eh	W	00h	ENCLKO	SLT_UOT	ENT0T1	PWMCLK	CLK24M	CRYT24M		

Bit Name	Description
ENCLKO	Enable OSC clock output to port PB4
SLT_UOT	"1": UART ports are PA0 & PA1. "0": UART ports are PC5 & PC4.
ENT0T1	Enable the 8031 T0 and T1 source by external.
PWMCLK	"1": PWM clock is 1.5MHz. "0": PWM clock is 12MHz.
CLK24M	"1": The clock of system is same as OSCI/2 but the clock of CPU is (OSCI x 2). "0" The clock of CPU and system is same as OSCI.
CRYT24M	"1": The clock of CPU is same as OSCI but the clock of system is (OSCI/2). "0" The clock of CPU and system is same as OSCI.

Low Speed PWM to control duty cycle

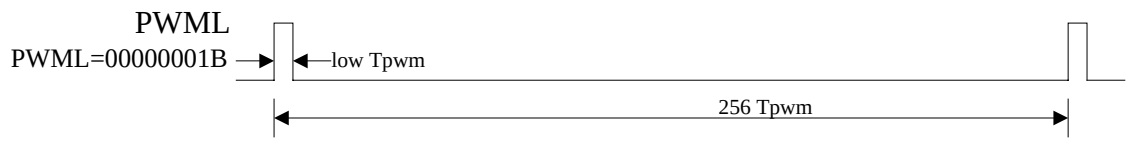
PWML : 8 bit PWM and +5/+3.3V push-pull output, shared with I/O port PE1.

8 bit PWM : 8 bit PWM determines 0/256 ~ 255/256 duty cycle.

PWM base clock=1Mhz=1us
PWM output clock=1Mhz / ((PWMLCx +1)* 256) = **256us * (PWMLCx+1)**
MAX clock=256us*1=256us= 3.90625khz
MIN clock=256us*128=65280us= 30.52hz

When PWMLC=15, PWM output clock=4.096ms=244.1hz
When PWMLC=16, PWM output clock=4.352ms=229.8hz
When PWMLC=64, PWM output clock=16.64ms=60.1hz
When PWMLC=65, PWM output clock=16.896ms=59.2hz

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PWMLCLK	0042h	W	00h	ENPWML	PWMLC6	PWMLC5	PWMLC4	PWMLC3	PWMLC2	PWMLC1	PWMLC0
PWML	0043h	R/W	00h	PWML7	PWML6	PWML5	PWML4	PWML3	PWML2	PWML1	PWML0



PWM

PWM0: 12-bit PWM and +5/3.3V push-pull output, shared with I/O.
PWM1 ~ PWM15: 8-bit PWM and +5/3.3V push-pull output, shared with I/O.
The corresponding PWM register controls the PWM duty cycle. Duty cycle range is from 0/256 to 255/256. PWM0 duty cycle range is from 0/4096 to 4095/4096.

LSB 3-bit of the PWM1~PWM15 will extend Tpwm to the frame0~7, Fig.
- 000: no Tpwm extended.
- 001: extended Tpwm to the frame 4.
- 010: extended Tpwm to the frame 2 and 6.
- 011: extended Tpwm to the frame 2, 4 and 6.
- 100: extended Tpwm to the frame 1, 3, 5 and 7.
- 101: extended Tpwm to the frame 1, 3, 4, 5 and 7.
- 110: extended Tpwm to the frame 1, 2, 3, 5, 6 and 7.
- 111: extended Tpwm to the frame 1, 2, 3, 4, 5, 6 and 7.

PWMCLK=0, Tpwm=1/12MHz. PWMCLK=1, Tpwm=1/1.5MHz. Tframe=32Tpwm.
MSB 5-bit of the PWM1~PWM15: 0/32 to 31/32 duty of the Tframe.

LSB 6-bit of the PWM0 will extend Tpwm to the frame0~63, Fig.
- 000000 : no Tpwm extended.
- 000001 : extended Tpwm to the frame 32.
- 000010 : extended Tpwm to the frame 16 and 48.
- 000100 : extended Tpwm to the frame 8, 24, 40 and 56.
- 001000 : extended Tpwm to the frame 4, 12, 20, 28, 36, 44, 52 and 60.
- 010000 : extended Tpwm to the frame 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58 and 62.
- 100000 : extended Tpwm to the frame 1, 3, 5, 7, 9, ……57, 59, 61 and 63.

PWMCLK=0, Tpwm=1/12MHz. PWMCLK=1, Tpwm=1/1.5MHz. Tframe=64Tpwm.
MSB 6-bit of the PWM0: 0/64 to 63/64 duty of the Tframe.

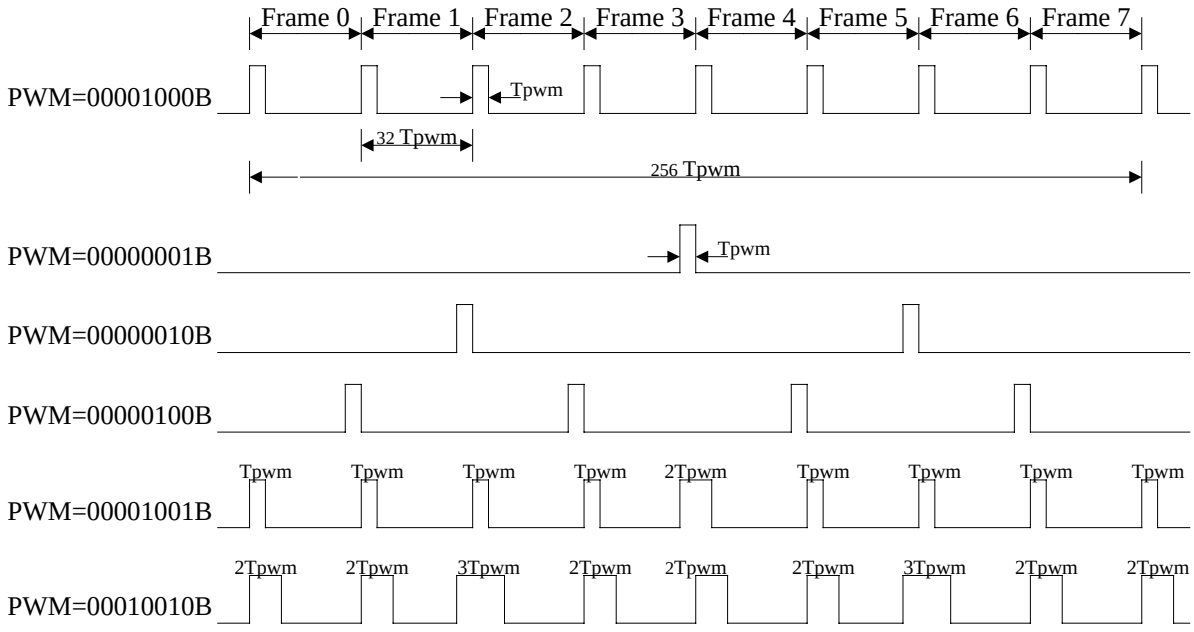


Fig. 14 PWM output waveform

PWM Registers

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0L	000Ch	R/W	00h					$PWM0_3$	$PWM0_2$	$PWM0_1$	$PWM0_0$
PWM0H	000Dh	R/W	80h	$PWM0_{11}$	$PWM0_{10}$	$PWM0_9$	$PWM0_8$	$PWM0_7$	$PWM0_6$	$PWM0_5$	$PWM0_4$
PWM1	0031h	R/W	80h	$PWM1_7$	$PWM1_6$	$PWM1_5$	$PWM1_4$	$PWM1_3$	$PWM1_2$	$PWM1_1$	$PWM1_0$
PWM2	0032h	R/W	80h	$PWM2_7$	$PWM2_6$	$PWM2_5$	$PWM2_4$	$PWM2_3$	$PWM2_2$	$PWM2_1$	$PWM2_0$
PWM3	0033h	R/W	80h	$PWM3_7$	$PWM3_6$	$PWM3_5$	$PWM3_4$	$PWM3_3$	$PWM3_2$	$PWM3_1$	$PWM3_0$
PWM4	0034h	R/W	80h	$PWM4_7$	$PWM4_6$	$PWM4_5$	$PWM4_4$	$PWM4_3$	$PWM4_2$	$PWM4_1$	$PWM4_0$
PWM5	0035h	R/W	80h	$PWM5_7$	$PWM5_6$	$PWM5_5$	$PWM5_4$	$PWM5_3$	$PWM5_2$	$PWM5_1$	$PWM5_0$
PWM6	0036h	R/W	80h	$PWM6_7$	$PWM6_6$	$PWM6_5$	$PWM6_4$	$PWM6_3$	$PWM6_2$	$PWM6_1$	$PWM6_0$
PWM7	0037h	R/W	80h	$PWM7_7$	$PWM7_6$	$PWM7_5$	$PWM7_4$	$PWM7_3$	$PWM7_2$	$PWM7_1$	$PWM7_0$
PWM8	0038h	R/W	80h	$PWM8_7$	$PWM8_6$	$PWM8_5$	$PWM8_4$	$PWM8_3$	$PWM8_2$	$PWM8_1$	$PWM8_0$
PWM9	0039h	R/W	80h	$PWM9_7$	$PWM9_6$	$PWM9_5$	$PWM9_4$	$PWM9_3$	$PWM9_2$	$PWM9_1$	$PWM9_0$
PWM10	003Ah	R/W	80h	$PWM10_7$	$PWM10_6$	$PWM10_5$	$PWM10_4$	$PWM10_3$	$PWM10_2$	$PWM10_1$	$PWM10_0$
PWM11	003Bh	R/W	80h	$PWM11_7$	$PWM11_6$	$PWM11_5$	$PWM11_4$	$PWM11_3$	$PWM11_2$	$PWM11_1$	$PWM11_0$
PWM12	003Ch	R/W	80h	$PWM12_7$	$PWM12_6$	$PWM12_5$	$PWM12_4$	$PWM12_3$	$PWM12_2$	$PWM12_1$	$PWM12_0$
PWM13	003Dh	R/W	80h	$PWM13_7$	$PWM13_6$	$PWM13_5$	$PWM13_4$	$PWM13_3$	$PWM13_2$	$PWM13_1$	$PWM13_0$
PWM14	003Eh	R/W	80h	$PWM14_7$	$PWM14_6$	$PWM14_5$	$PWM14_4$	$PWM14_3$	$PWM14_2$	$PWM14_1$	$PWM14_0$
PWM15	003Fh	R/W	80h	$PWM15_7$	$PWM15_6$	$PWM15_5$	$PWM15_4$	$PWM15_3$	$PWM15_2$	$PWM15_1$	$PWM15_0$
PWM_EN1	000Eh	W	00h	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1	EPWM0
PWM_EN2	000Fh	W	00h	EPWM15	EPWM14	EPWM13	EPWM12	EPWM11	EPWM10	EPWM9	EPWM8

Bit Name	Description
$PWMX_7$ ~ $PWMX_0$	Select duty cycle of PWM1~15 output. 00000000: duty cycle = 0 00000001: duty cycle = 1/256 00000010: duty cycle = 2/256 : 11111110: duty cycle = 254/256 11111111: duty cycle = 255/256
$PWM0_{11}$ ~ $PWM0_0$	Select duty cycle of PWM0 output. duty cycle = 0/4096 ~ 4095/4096
EPWMx	Set the corresponding EPPWMx will enable the PWM output. (x from 0 to 15)

WT61P6 Register Map:

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PA_CTRL	0000h	R/W	00h	PA7OE	PA6OE	PA5OE	PA4OE	PA3OE	PA2OE	PA1OE	PA0OE
PA_DATA	0001h	R/W	ffh	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PB_CTRL	0002h	R/W	00h		PB6OE	PB5OE	PB4OE	PB3OE	PB2OE	PB1OE	PB0OE
PB_DATA	0003h	R/W	xfh		PB6	PB5	PB4	PB3	PB2	PB1	PB0
PC_CTRL	0004h	R/W	00h	PC7OE	PC6OE	PC5OE	PC4OE	PC3OE	PC2OE	PC1OE	PC0OE
PC_DATA	0005h	R/W	ffh	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PD_CTRL	0006h	R/W	00h	PD7OE	PD7OE	PD5OE	PD4OE	PD3OE	PD2OE	PD1OE	PD0OE
PD_DATA	0007h	R/W	ffh	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PE_CTRL	0008h	R/W	00h					PE3OE	PE2OE	PE1OE	PE0OE
PE_DATA	0009h	R/W	xfh					PE3	PE2	PE1	PE0
PD_CTRL2	000Ah	W	00h	PD7HE	PD6HE	PD5HE	PD4HE	PD3HE	PD2HE	PD1HE	PD0HE
HFREQ_L	0010h	R	xxh	HLVL	HINPOL	HCHG	HFL4	HFL3	HFL2	HFL1	HFL0
HFREQ_H	0011h	R	xxh	HOVF	HFH6	HFH5	HFH4	HFH3	HFH2	HFH1	HFH0
VFREQ_L	0012h	R	xxh	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
VFREQ_H	0013h	R	xxh	VLVL	VINPOL	VOVF	VF12	VF11	VF10	VF9	VF8
H_PERD	0014h	R	xxh	HPRD7	HPRD6	HPRD5	HPRD4	HPRD3	HPRD2	HPRD1	HPRD0
HF_VL	0015h	R	00h	HFV7	HFV6	HFV5	HFV4	HFV3	HFV2	HFV1	HFV0
HF_VH	0016h	R	00h					HFV11	HFV10	HFV9	HFV8
VFQ_OVF	0010h	W	FFh	OVVF11	OVVF10	OVVF9	OVVF8	OVVF7	OVVF6	OVVF5	OVVF4
HV_CR1	0011h	W	00h	ENHOUT	ENVOUT	HOPOL	VOPOL	QUICK	SEPART	ENFREE	ENPAT
HV_CR2	0012h	W	00h	ENCLP	CLPEG	CLPPO	CLPPW1	CLPPW0	SOG	HVPASS	BYPASS
FRH_CR	0013h	W	00h			FRH5	FRH4	FRH3	FRH2	FRH1	FRH0
FRHD_CR	0014h	W	00h	FRHB4	FRHD6	FRHD5	FRHD4	FRHD3	FRHD2	FRHD1	FRHD0
FRHB_CR	0015h	W	00h	FRHB3	FRHB2	FRHB1	FRHB0	FRHW3	FRHW2	FRHW1	FRHW0
FRV_CR	0016h	W	00h	FRV7	FRV6	FRV5	FRV4	FRV3	FRV2	FRV1	FRV0
FRVD_CR	0017h	W	00h	FRVD7	FRVD6	FRVD5	FRVD4	FRVD3	FRVD2	FRVD1	FRVD0
FRVB_CR	0018h	W	00h	FRVB4	FRVB3	FRVB2	FRVB1	FRVB0	FRVW2	FRVW1	FRVW0
HPD_CHG	0019h	W	00h	HVIN2				EN_LMT	HCNT2	HCNT1	HCNT0
1/2HV_CR	001Ah	W	00h	ENH2D	ENV2D	HEDG					
ADC_DA	001Ch	R	xxh	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
ADC_CH	001Ch	W	00h	EN_CH3	EN_CH2	EN_CH1	EN_CH0	CH3	CH2	CH1	CH0
ADC_RD	001Dh	R	xxh	ADRDY							
WDT	001Eh	W	00h	DISWDT						WDT1	WDT0
I2C_STA	0020h	R	22h			BB	SFIRST	SSTOP	SRW	RXNAK2	I2CRDY
I2C_CON	0020h	W	02h	ENI2C	MCLK1	MCLK0	MSTR	MSTOP	I2CRW	TXNAK2	SLAVE
I2C_RX	0021h	R	xxh	MRX7	MRX6	MRX5	MRX4	MRX3	MRX2	MRX1	MRX0
I2C_TX	0021h	W	xxh	MTX7	MTX6	MTX5	MTX4	MTX3	MTX2	MTX1	MTX0
I2C_ADR	0022h	W	X0h	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	DLYHLD
DDCA_ST1	0024h	R	01h	ALRDYA	BBA	DDC2A	FIRSTA	STOPA	ALGRWA	MATCHA	DRXNKA
DDCA_ST2	0025h	R	00h						IN_CMDA	WR_D3A	
DDCA_CN1	0024h	W	00h	ENDDCA		DDC2A			DTXA		DTXNKA
DDCA_CN2	0025h	W	80h				RAMAH	RAMAL	CL_ADRA	CL_WD3A	WR_ENA
DDCA_RTX	0026h	R/W	FFh	DRXA7	DRXA6	DRXA5	DRXA4	DRXA3	DRXA2	DRXA1	DRXA0
DDCA_AAE	0027h	W	FFh	EN_AN7A	EN_AN6A	EN_AN5A	EN_AN4A	EN_AN3A	EN_AN2A	EN_AN1A	EN_AN0A
DDCA_AR0	0029h	W	X0h	DAR07A	DAR06A	DAR05A	DAR04A	--	--	--	ENAR0A
DDCA_AR1	002Ah	W	X0h	DAR17A	DAR16A	DAR15A	DAR14A	DAR13A	DAR12A	DAR11A	ENAR1A
DDCA_AR2	002Bh	W	X0h	DAR27A	DAR26A	DAR25A	DAR24A	DAR23A	DAR22A	DAR21A	ENAR2A
INT_FLG	002Ch	R	00h	IF_DDC	IF_MI2C	IF_RGB	IF_SYNC	IF_IRQ2	IF_IRQ1	IF_VSO	IF_VIN
INT_EN	002Ch	W	00h	IE_DDC	IE_MI2C	IE_RGB	IE_SYNC	IE_IRQ2	IE_IRQ1	IE_VSO	IE_VIN
INT_FLG2	002Dh	R	00h	IF_POL	IF_OVV	IF_HCHG	IF_TM6	IF_TM5	IF_TM4	IF_TM3	IF_TM2
INT_EN2	002Dh	W	00h	IE_POL	IE_OVV	IE_HCHG	IE_TM6	IE_TM5	IE_TM4	IE_TM3	IE_TM2
INT_SRC	002Eh	R	00h	POLINT	OVVINT	RGBRDY	SYNC	IRQ2	IRQ1	VSO	VIN
IRQ_CON1	002Eh	W	00h	CLR_POL	CLR_OV			CLR_IRQ2	CLR_IRQ1	CLR_VSO	CLR_VIN
IRQ_CON2	002FH	W	00h					IRQ2_RF	IRQ2_EG	IRQ1_RF	IRQ1_EG

Name	Addr	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0L	000Ch	R/W	00h					$PWM0_3$	$PWM0_2$	$PWM0_1$	$PWM0_0$
PWM0H	000Dh	R/W	80h	$PWM0_{11}$	$PWM0_{10}$	$PWM0_9$	$PWM0_8$	$PWM0_7$	$PWM0_6$	$PWM0_5$	$PWM0_4$
PWM1	0031h	R/W	80h	$PWM1_7$	$PWM1_6$	$PWM1_5$	$PWM1_4$	$PWM1_3$	$PWM1_2$	$PWM1_1$	$PWM1_0$
PWM2	0032h	R/W	80h	$PWM2_7$	$PWM2_6$	$PWM2_5$	$PWM2_4$	$PWM2_3$	$PWM2_2$	$PWM2_1$	$PWM2_0$
PWM3	0033h	R/W	80h	$PWM3_7$	$PWM3_6$	$PWM3_5$	$PWM3_4$	$PWM3_3$	$PWM3_2$	$PWM3_1$	$PWM3_0$
PWM4	0034h	R/W	80h	$PWM4_7$	$PWM4_6$	$PWM4_5$	$PWM4_4$	$PWM4_3$	$PWM4_2$	$PWM4_1$	$PWM4_0$
PWM5	0035h	R/W	80h	$PWM5_7$	$PWM5_6$	$PWM5_5$	$PWM5_4$	$PWM5_3$	$PWM5_2$	$PWM5_1$	$PWM5_0$
PWM6	0036h	R/W	80h	$PWM6_7$	$PWM6_6$	$PWM6_5$	$PWM6_4$	$PWM6_3$	$PWM6_2$	$PWM6_1$	$PWM6_0$
PWM7	0037h	R/W	80h	$PWM7_7$	$PWM7_6$	$PWM7_5$	$PWM7_4$	$PWM7_3$	$PWM7_2$	$PWM7_1$	$PWM7_0$
PWM8	0038h	R/W	80h	$PWM8_7$	$PWM8_6$	$PWM8_5$	$PWM8_4$	$PWM8_3$	$PWM8_2$	$PWM8_1$	$PWM8_0$
PWM9	0039h	R/W	80h	$PWM9_7$	$PWM9_6$	$PWM9_5$	$PWM9_4$	$PWM9_3$	$PWM9_2$	$PWM9_1$	$PWM9_0$
PWM10	003Ah	R/W	80h	$PWM10_7$	$PWM10_6$	$PWM10_5$	$PWM10_4$	$PWM10_3$	$PWM10_2$	$PWM10_1$	$PWM10_0$
PWM11	003Bh	R/W	80h	$PWM11_7$	$PWM11_6$	$PWM11_5$	$PWM11_4$	$PWM11_3$	$PWM11_2$	$PWM11_1$	$PWM11_0$
PWM12	003Ch	R/W	80h	$PWM12_7$	$PWM12_6$	$PWM12_5$	$PWM12_4$	$PWM12_3$	$PWM12_2$	$PWM12_1$	$PWM12_0$
PWM13	003Dh	R/W	80h	$PWM13_7$	$PWM13_6$	$PWM13_5$	$PWM13_4$	$PWM13_3$	$PWM13_2$	$PWM13_1$	$PWM13_0$
PWM14	003Eh	R/W	80h	$PWM14_7$	$PWM14_6$	$PWM14_5$	$PWM14_4$	$PWM14_3$	$PWM14_2$	$PWM14_1$	$PWM14_0$
PWM15	003Fh	R/W	80h	$PWM15_7$	$PWM15_6$	$PWM15_5$	$PWM15_4$	$PWM15_3$	$PWM15_2$	$PWM15_1$	$PWM15_0$
PWM_EN1	000Eh	W	00h	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1	EPWM0
PWM_EN2	000Fh	W	00h	EPWM15	EPWM14	EPWM13	EPWM12	EPWM11	EPWM10	EPWM9	EPWM8
PSC_CTL	0041h	W	00h	IRQ1_WK	IRQ2_WK	DDC_WK	$H_{in}1$&SOG	Vin1	Hin2	Vin2	
PWMLCLK	0042h	W	00h	ENPWML	PWMLC6	PWMLC5	PWMLC4	PWMLC3	PWMLC2	PWMLC1	PWMLC0
PWML	0043h	R/W	00h	PWML7	PWML6	PWML5	PWML4	PWML3	PWML2	PWML1	PWML0
DDCB_ST1	0044h	R	01h	ALRDYB	BBB	DDC2B	FIRSTB	STOPB	ALGRWB	MATCHB	DRXNKB
DDCB_ST2	0045h	R	00h						IN_CMDB	WR_D3B	
DDCB_CN1	0044h	W	00h	ENDDCB		DDC2B			DTXB		DTXNKB
DDCB_CN2	0045h	W	80h				RAMBH	RAMBL	CL_ADRB	CL_WD3B	WR_ENB
DDCB_RTX	0046h	R/W	FFh	DRXB7	DRXB6	DRXB5	DRXB4	DRXB3	DRXB2	DRXB1	DRXB0
DDCB_AAE	0047h	W	FFh	EN_AN7B	EN_AN6B	EN_AN5B	EN_AN4B	EN_AN3B	EN_AN2B	EN_AN1B	EN_AN0B
DDCB_AR0	0049h	W	X0h	DAR07B	DAR06B	DAR05B	DAR04B	--	--	--	ENAR0B
DDCB_AR1	004Ah	W	X0h	DAR17B	DAR16B	DAR15B	DAR14B	DAR13B	DAR12B	DAR11B	ENAR1B
DDCB_AR2	004Bh	W	X0h	DAR27B	DAR26B	DAR25B	DAR24B	DAR23B	DAR22B	DAR21B	ENAR2B
OTH_CTL1	004Eh	W	00h	ENCLKO	SLT_UOT	ENT0T1	PWMCLK	CLK24M	CRYT24M		
TM2_CTL	0056h	W	20h	ENTM2		EN2_TOV	TM2_CK1	TM2_CK0	TM2_SEG	TM2_RF	
TM2_STA	0056h	R	00h	INT_TM2	TM2_HL	TM2_TOV					
TM2_DAT	0057h	R	00h	TM2_TM7	TM2_TM6	TM2_TM5	TM2_TM4	TM2_TM3	TM2_TM2	TM2_TM1	TM2_TM0
TM3_CTL	0058h	W	20h	ENTM3		EN3_TOV	TM3_CK1	TM3_CK0	TM3_SEG	TM3_RF	
TM3_STA	0058h	R	00h	INT_TM3	TM3_HL	TM3_TOV					
TM3_DAT	0059h	R	00h	TM3_TM7	TM3_TM6	TM3_TM5	TM3_TM4	TM3_TM3	TM3_TM2	TM3_TM1	TM3_TM0
TM4_CTL	005Ah	W	20h	ENTM4		EN4_TOV	TM4_CK1	TM4_CK0	TM4_SEG	TM4_RF	
TM4_STA	005Ah	R	00h	INT_TM4	TM4_HL	TM4_TOV					
TM4_DAT	005Bh	R	00h	TM4_TM7	TM4_TM6	TM4_TM5	TM4_TM4	TM4_TM3	TM4_TM2	TM4_TM1	TM4_TM0
TM5_CTL	005Ch	W	20h	ENTM5		EN5_TOV	TM5_CK1	TM5_CK0	TM5_SEG	TM5_RF	
TM5_STA	005Ch	R	00h	INT_TM5	TM5_HL	TM5_TOV					
TM5_DAT	005Dh	R	00h	TM5_TM7	TM5_TM6	TM5_TM5	TM5_TM4	TM5_TM3	TM5_TM2	TM5_TM1	TM5_TM0
TM6_CTL	005Eh	W	20h	ENTM6		EN6_TOV	TM6_CK1	TM6_CK0	TM6_SEG	TM6_RF	
TM6_STA	005Eh	R	00h	INT_TM6	TM6_HL	TM6_TOV					
TM6_DAT	005Fh	R	00h	TM6_TM7	TM6_TM6	TM6_TM5	TM6_TM4	TM6_TM3	TM6_TM2	TM6_TM1	TM6_TM0

TARGET AC AND DC SPECIFICATION

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DC Supply Voltage (VDD)	-0.3	5.5	V
Input and output voltage with respect to Ground	-0.3	VDD+0.3	V
Storage temperature	-25	125	^{o}C
Ambient temperature with power applied	-10	85	^{o}C

D.C Characteristics (VDD=5.0V±10%, Ta=0-70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD5v}	+5v Supply Voltage		4.5	5	5.5	V
I_{VDD}	Operating Current	F_{OSC}= 12MHz, No load	--	12	30	mA
$I_{Suspend}$	Power Down Mode Current	No load	--	150	--	µA
$V_{IH,IO}$	Input High Voltage		0.7VDD	--	VDD+0.3	V
$V_{IL,IO}$	Input Low Voltage		-0.3	--	0.2VDD	V
$V_{OH,IO}$	Output High Voltage	I_{OH} = -6mA	4	4.5	VDD	V
$V_{OL,IO}$	Output Low Voltage	I_{OL} = 6mA	0	0.18	0.4	V
$V_{OL,IO}$	Output Low Voltage (PC0-PC7)	I_{OL} = 10mA	0	0.15	0.4	V
R_{PH}	Pull High Resistance		--	25	50	Kohm
$V_{IH,SYNC}$	HIN, VIN, SOG Input High Voltage (Schmitt trigger)		--	1.6	--	V
$V_{IL,SYNC}$	HIN, VIN, SOG Input Low Voltage (Schmitt trigger)		--	1.2	--	V
$I_{IL,SYNC}$	Input Leakage Current HSYNC and VSYNC pins	0V <V_{IN} < VDD	-1	--	1	µA
$V_{IH,SCL}$ $V_{IH,SDA}$	SCL, SDA Input High Voltage (Schmitt trigger)		2.8	--	VDD+0.3	V
$V_{IH,SCL}$ $V_{IH,SDA}$	SCL, SDA Input Low Voltage (Schmitt trigger)		-0.3	--	1.6	V
$V_{IH,RES}$	Reset Input High Voltage		2.8	--	VDD+0.3	V
$V_{IL,RES}$	Reset Input Low Voltage		-0.3	--	1.6	V
V_{LVD}	Low VDD Reset Voltage		2.5	2.7	2.9	V

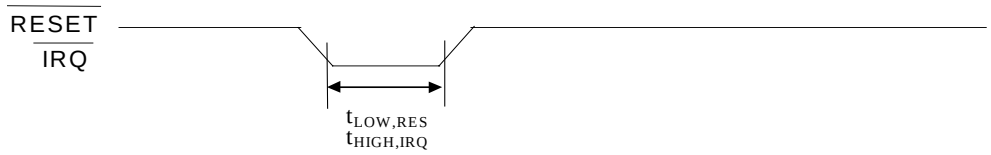
D.C Characteristics (VDD=3.3V±10%, Ta=0-70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD5v}	+5v Supply Voltage		3.0	3.3	3.6	V
I_{VDD}	Operating Current	F_{OSC}= 12MHz, No load	--	12	30	mA
$I_{Suspend}$	Power Down Mode Current	No load	--	50	--	µA
$V_{IH,IO}$	Input High Voltage		0.7VDD	--	VDD+0.3	V
$V_{IL,IO}$	Input Low Voltage		-0.3	--	0.2VDD	V
$V_{OH,IO}$	Output High Voltage	I_{OH} = -6mA	2.8		VDD	V
$V_{OL,IO}$	Output Low Voltage	I_{OL} = 6mA	0		0.4	V
$V_{OL,IO}$	Output Low Voltage (PC0-PC7)	I_{OL} = 10mA	0		0.4	V
R_{PH}	Pull High Resistance		--	25	50	Kohm
$V_{IH,SYNC}$	HIN,VIN,SOGIN Input High Voltage (Schmitt trigger)		--	1.2	--	V
$V_{IL,SYNC}$	HIN,VIN,SOG Input High Voltage(Schmitt trigger)		--	0.9	--	V
$I_{IL,SYNC}$	Input Leakage Current HSYNC and VSYNC pins	0V <V_{IN} < VDD	-1	--	1	µA
$V_{IH,SCL}$ $V_{IH,SDA}$	SCL,SDA Input High Voltage (Schmitt trigger)		2.0	--	VDD+0.3	V
$V_{IH,SCL}$ $V_{IH,SDA}$	SCL,SDA Input Low Voltage (Schmitt trigger)		-0.3	--	1.0	V
$V_{IH,RES}$	Reset Input High Voltage		2.0	--	VDD+0.3	V
$V_{IL,RES}$	Reset Input Low Voltage		-0.3	--	1.0	V
V_{LVD}	Low VDD Reset Voltage		2.5	2.7	2.9	V

A.C Characteristics (VDD=5.0V±5%, fosc=24MHz, Ta=0-70°C)

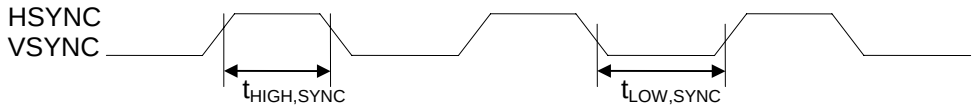
NRES and NIRQ Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{LOW,RES}$	NRES pin low pulse	83	--	--	ns
$t_{LOW,IRQ}$	NIRQ low pulse (level trigger)	83	--	--	ns



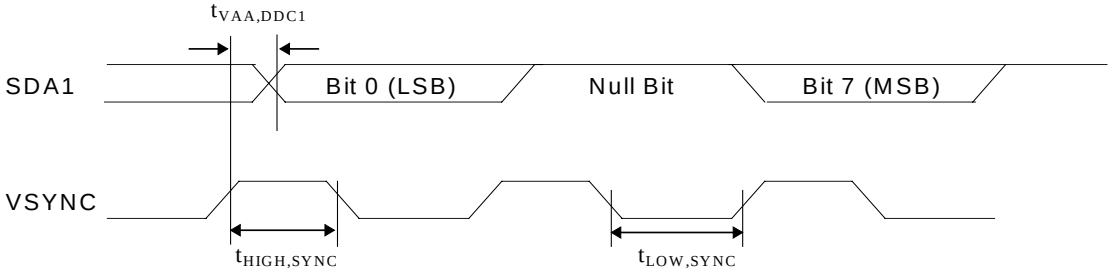
SYNC Processor Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{HIGH,SYNC}$	HSYNC and VSYNC high time	167	--	--	ns
$t_{LOW,SYNC}$	HSYNC and VSYNC low time	167	--	--	ns



DDC1 Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{VAA,DDC1}$	SDA1 output valid from VSYNC rising edge	125	--	500	ns

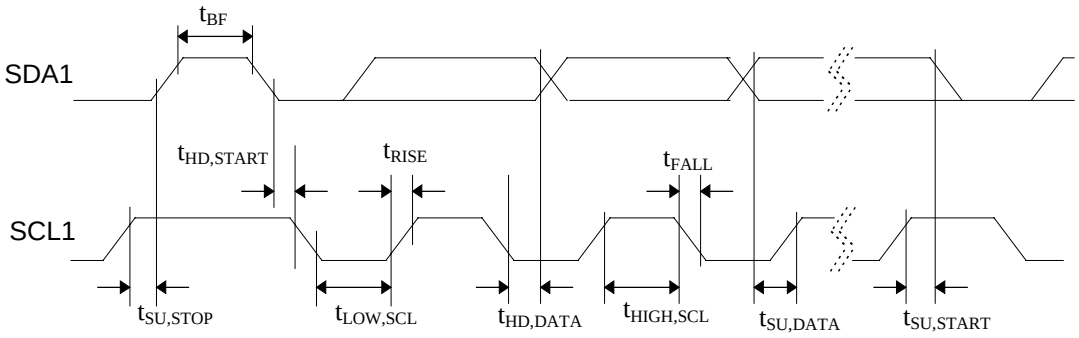


DDC2 Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL1 input clock frequency	--	--	400	kHz
t_{BF}	Bus free time	1.3	--	--	us
$t_{HD,START}$	Hold time for START condition	0.6	--	--	us
$t_{SU,START}$	Set-up time for START condition	0.6	--	--	us
$t_{HIGH,SCL}$	SCL1 clock high time	0.6	--	--	us
$t_{LOW,SCL}$	SCL1 clock low time	1.3	--	--	us
$t_{HD,DATA}$	Hold time for DATA input	0	--	--	ns
	Hold time for DATA output	--	--	--	ns
$t_{SU,DATA}$	Set-up time for DATA input	100	--	--	ns
	Set-up time for DATA output	--	--	--	ns
$t_{RISE,DDC}$	SCL1 and SDA1 rise time	--	--	300	Ns
$t_{FALL.DDC}$	SCL1 and SDA1 fall time	--	--	300	ns
$t_{SU,STOP}$	Set-up time for STOP condition	0.6	--	--	us

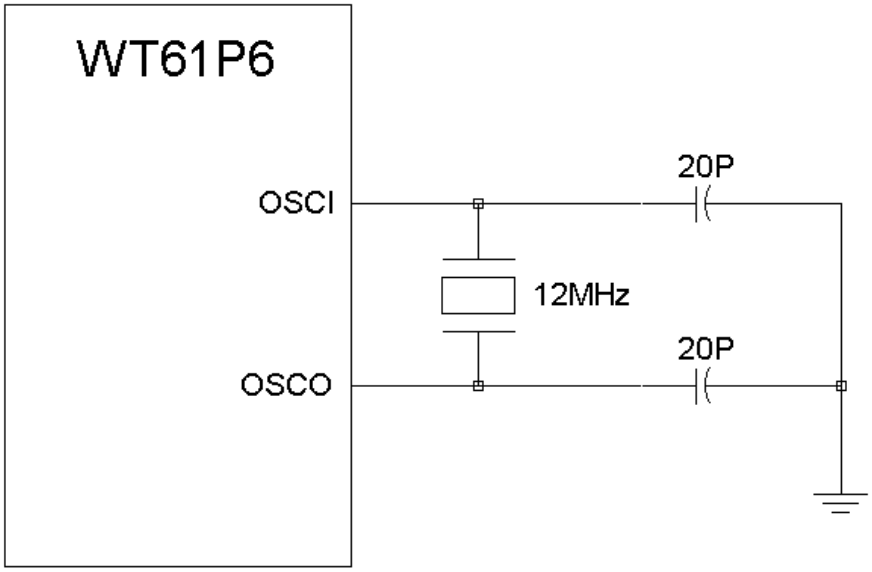
SLAVE I or II I2C Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL1 input clock frequency	0	-	100	kHz
t_{BF}	Bus free time	2	-	-	us
$t_{HD,START}$	Hold time for START condition	1	-	-	us
$t_{SU,START}$	Set-up time for START condition	1	-	-	us
$t_{HIGH,SCL}$	SCL1 clock high time	1	-	-	us
$t_{LOW,SCL}$	SCL1 clock low time	1	-	-	us
$t_{HD,DATA}$	Hold time for DATA input	0	-	-	ns
	Hold time for DATA output	167	-	-	ns
$t_{SU,DATA}$	Set-up time for DATA input	167	-	-	ns
	Set-up time for DATA output	334	-	-	ns
$t_{RISE,DDC}$	SCL1 and SDA1 rise time	-	-	1	us
$t_{FALL.DDC}$	SCL1 and SDA1 fall time	-	-	300	ns
$t_{SU,STOP}$	Set-up time for STOP condition	2	-	-	us

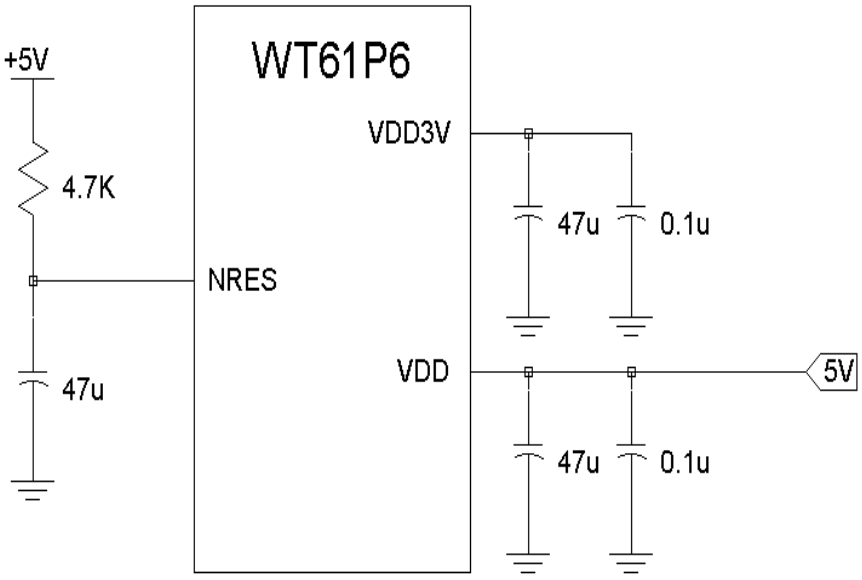


TYPICAL APPLICATION CIRCUIT

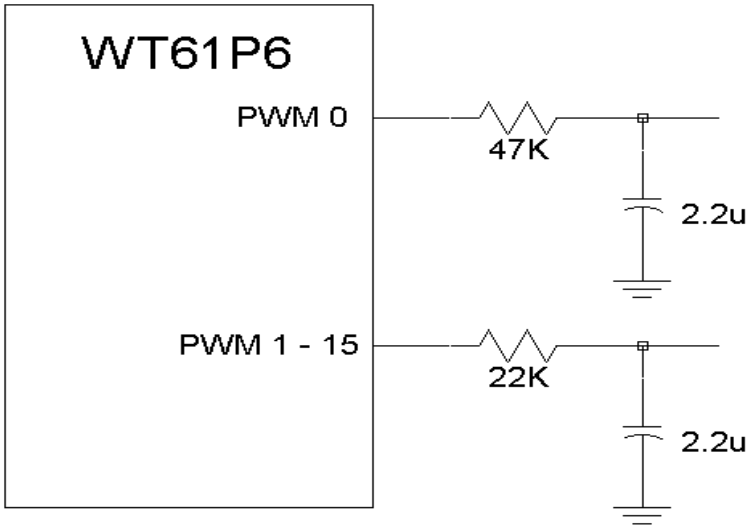
Crystal Oscillator



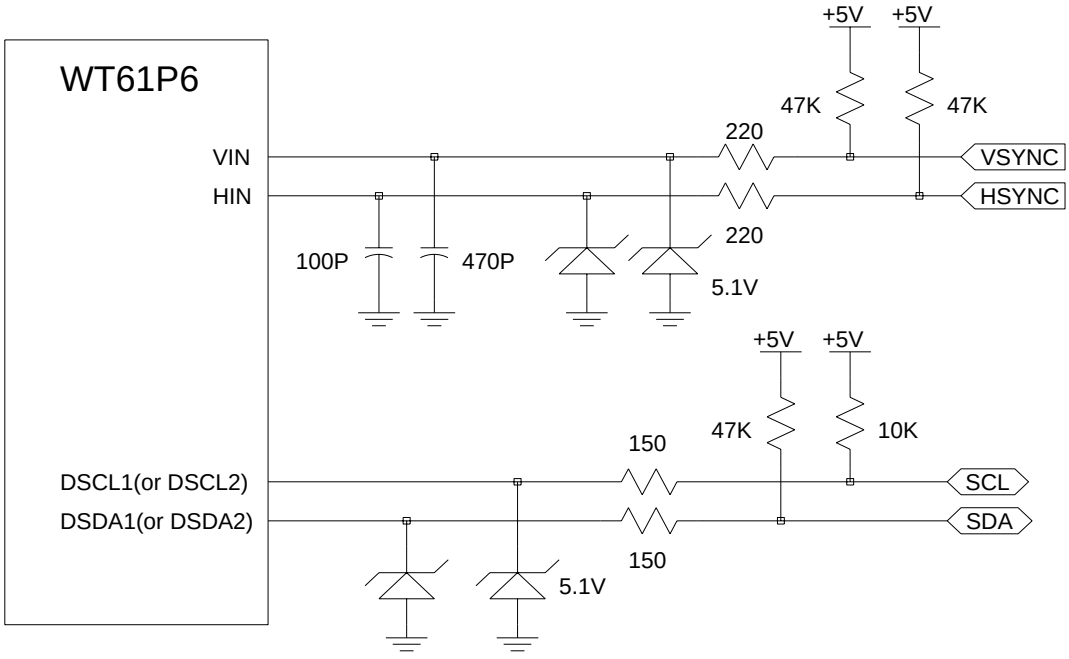
NRES Pin and 3.3V Regulator

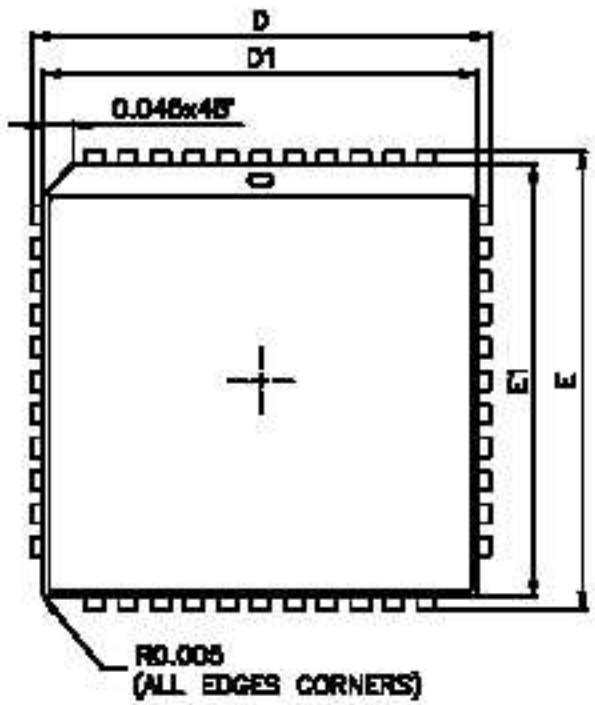


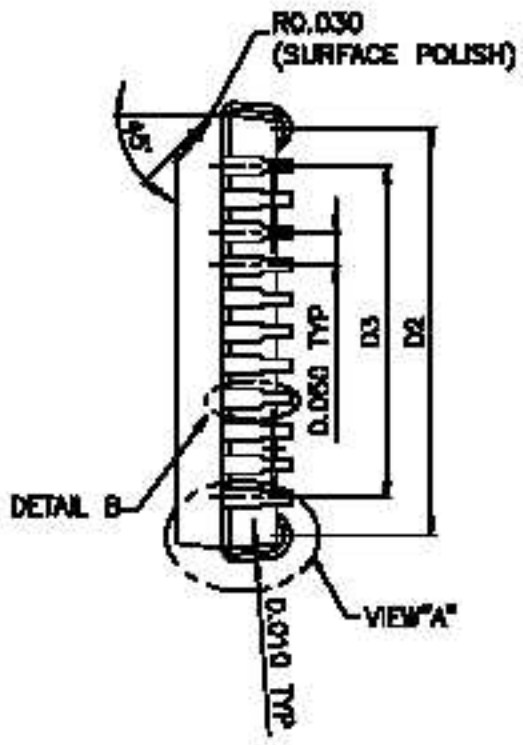
PWM Output

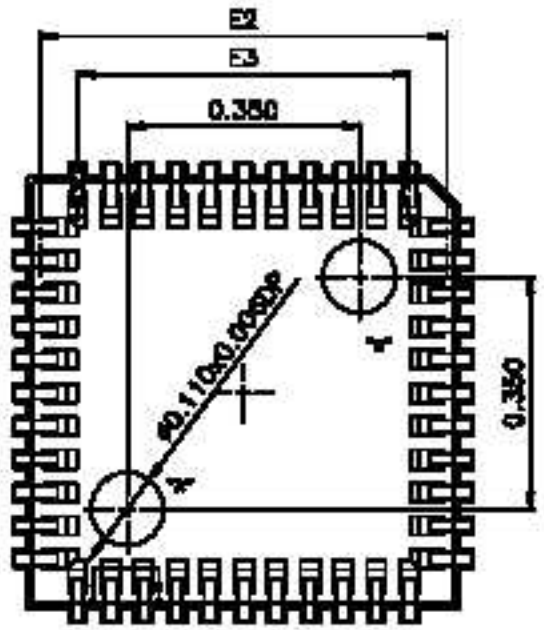


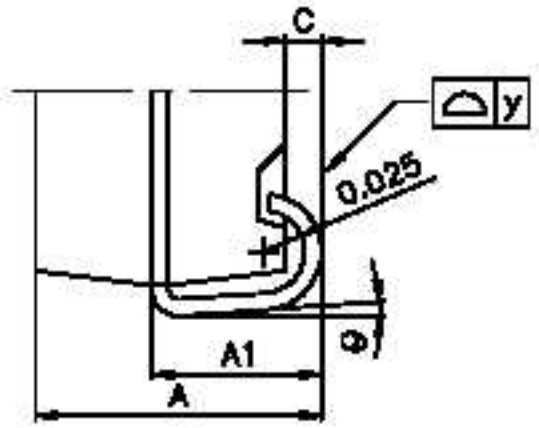
Hsync, Vsync and DDC Interface Protection



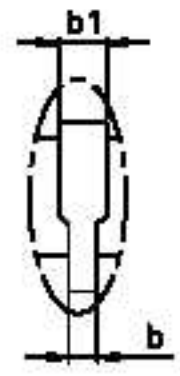




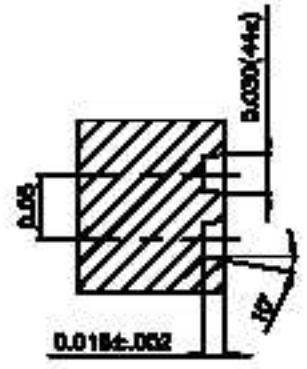




VIEW "A"



DETAIL B



Y-Y SECTION

NOTE :

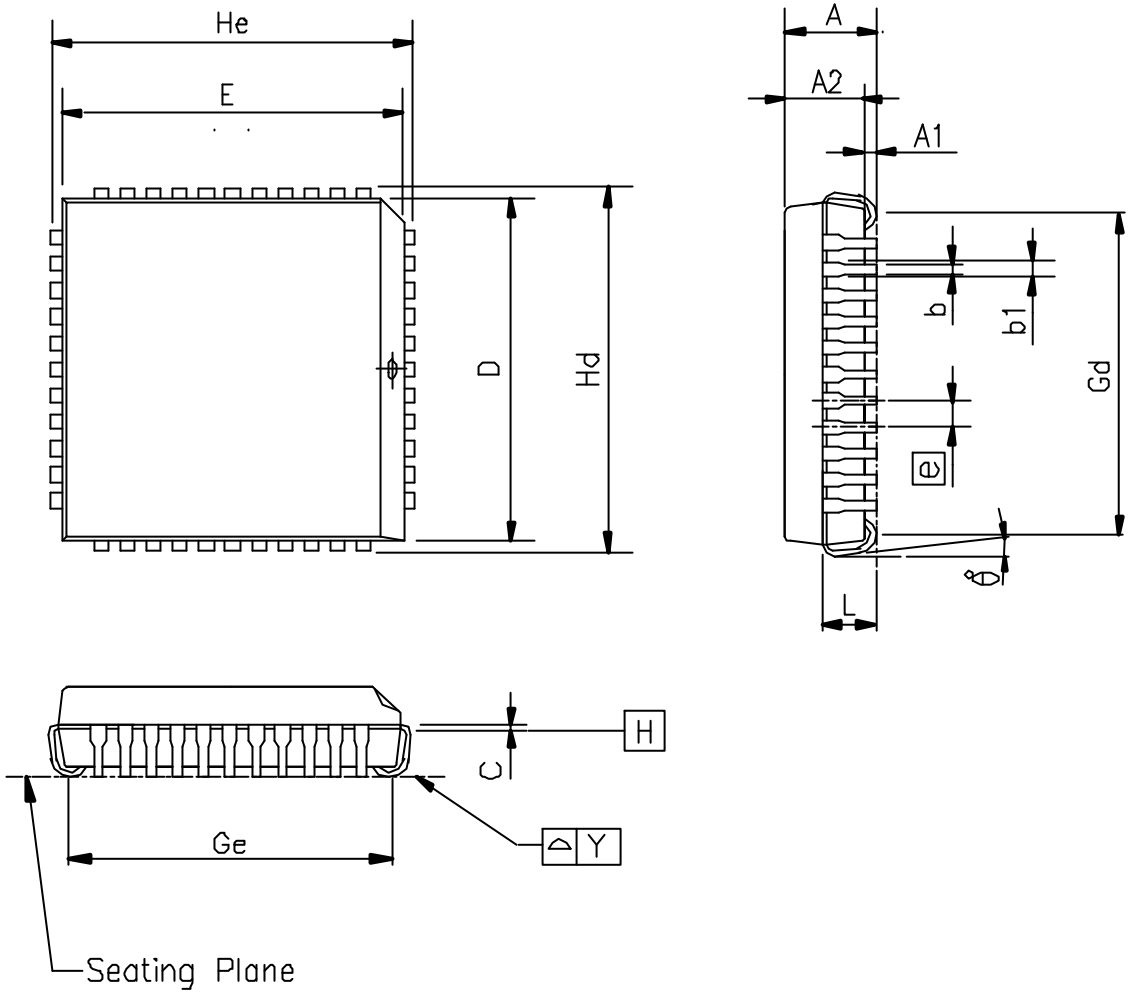
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : OLIN C151
3. DIMENSION "D1" AND "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.010"[0.25mm] TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm].
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-018-AC
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :

X : A ,B....C
Y : 1 ~ 8

NO : DENOTE MOLD SET NUMBER ____

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.27	—	4.52	0.168	—	0.178
A1	2.41	—	2.82	0.095	—	0.111
b	0.33	0.45	0.53	0.013	0.018	0.021
b1	0.66	0.71	0.81	0.026	0.028	0.032
C	0.51	—	—	0.020	—	—
D	17.40	17.53	17.65	0.685	0.690	0.695
D1	16.41	16.54	16.66	0.646	0.651	0.656
D2	15.42	15.54	15.67	0.607	0.612	0.617
D3	—	12.70	—	—	0.500	—
E	17.40	17.53	17.65	0.685	0.690	0.695
E1	16.41	16.54	16.66	0.646	0.651	0.656
E2	15.42	15.54	15.67	0.607	0.612	0.617
E3	—	12.70	—	—	0.500	—
y	0	—	0.10	0	—	0.004
θ	0°	—	6°	0°	—	6°

CUSTOMER :		LINGSEN 5-1 HSIN SHU ROAD T.E.P.Z. PINGSHAN IND., LTD. TAICHUNG, TAIWAN, R. O. C.	
APPROVED BY	DATE	TITLE: PLCC 44L PACKAGE OUTLINE DRAWING	
DESIGN BY: Kenny Hsu	04/08/26		
CHECK BY: Ken Wang	4/04/26		
APPROVAL: Paul Lin	4/04/26	DWG. NO. PO-PLCC-006	REV. 1
APPROVAL: Paul Lin	4/04/26	UNIT : INCH SCALE : 4/1 SHEET 1 OF 1	



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	0.185
A1	0.020	–	–
A2	0.145	0.150	0.155
b1	0.026	0.028	0.032
b	0.016	0.018	0.022
c	0.007	0.010	0.013
D	0.648	0.653	0.658
E	0.648	0.653	0.658
e	0.050 BSC		
Gd	0.590	0.610	0.630
Ge	0.590	0.610	0.630
Hd	0.680	0.690	0.700
He	0.680	0.690	0.700
L	0.090	0.100	0.110
Y	–	–	0.004

UNIT : INCH

* ***NOTE:***

1.JEDEC OUTLINE : MO-047 AC

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY

3.DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

超豐電子股份有限公司
GREATEK ELECTRONICS INC.

3RD ANGLE SYS	比例 SCALE:	材質 MTRL	製程 FINISH	數量 QTY
繪圖 DWN / 日期 DATE	圖名: PLASTIC CHIP CARRIER DATA SHEET 44 LEADS 0.05" LEAD SPACING SQUARE			
檢核: CHK / 日期: DATE	圖號: J1-06044-001			
核准: APPL: / 日期: DATE:	圖檔: J-044P-1		REV: 02	QTY: 1