偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT6805

Monitor On-Screen Display

Preliminary Data Sheet

REV. 1.1

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GENERAL DESCRIPTION

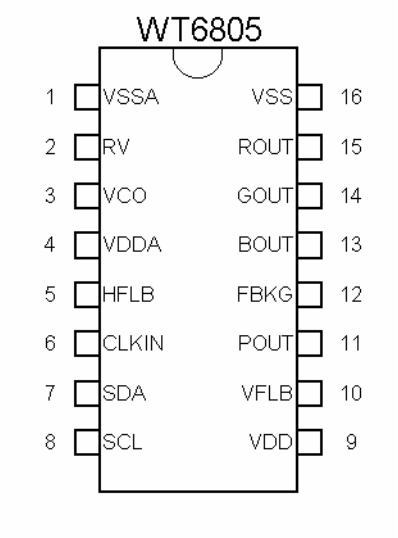
The WT6805 is an on-screen display (OSD) IC which display color symbols or characters onto monitor. With the control of microcontroller through I^2C interface, it can display characters with special effect like blinking or shadowing automatically.

FEATURES

- Programmable horizontal resolutions up to 1530 dots per line
- Horizontal frequency up to 150KHz
- On-chip PLL up to 150MHz
- Fully programmable character array of 15 rows by 30 columns
- 12x18 dot matrix per character
- 512 characters and graphic symbols ROM
- 16 multi-color fonts
- 8 user RAM font
- 8 colors per display character
- 7 colors per display character background
- 4 programmable windows
- Double character height and width control
- Programmable character height (18 to 71 lines)
- Programmable row-to-row spacing
- Programmable vertical and horizontal positioning for display screen center
- Bordering, shadowing, blinking and box effect
- Fade-in/fade-out effects
- I^2C interface with slave address $7AH
- Power supply : 5V
- Package type : 16-pin plastic DIP/SOP

PIN ASSIGNMENT AND PACKAGE TYPE

PACKAGE TYPE : PDIP-16, SOP-16



Pin No.	Pin Name	I/O	Description
1	VSSA		Analog ground.
2	RV	I	A resistor can be connected to this pin for control VCO range.
3	VCO	I/O	Loop filter of PLL.
4	VDDA		Analog power supply
5	HFLB	I	Horizontal sync input.
6	CLKIN	I	External clock input.
7	SDA	I/O	Serial data of I^2C interface.
8	SCL	I	Serial clock of I^2C interface.
9	VDD		Digital power supply
10	VFLB	I	Vertical sync input.
11	POUT	O	General purpose output pad
12	FBKG	O	Fast Blanking output. This pin controls the mixer of vedio amplifier to cutoff the video signal while displaying character or window.
13	BOUT	O	Blue color output
14	GOUT	O	Green color output
15	ROUT	O	Red color output
16	VSS		Digital ground

FUNCTIONAL DESCRIPTION

I²C Interface

This is a slave mode I²C interface. Device address is $7AH.
There are three data transmission formats for writing: Format (a), (b) and (c).

Format (a):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	ROW	A	COL	A	Data	A	•••••	P

Format (b):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	COL	A	Data	A	COL	A	•••••	P

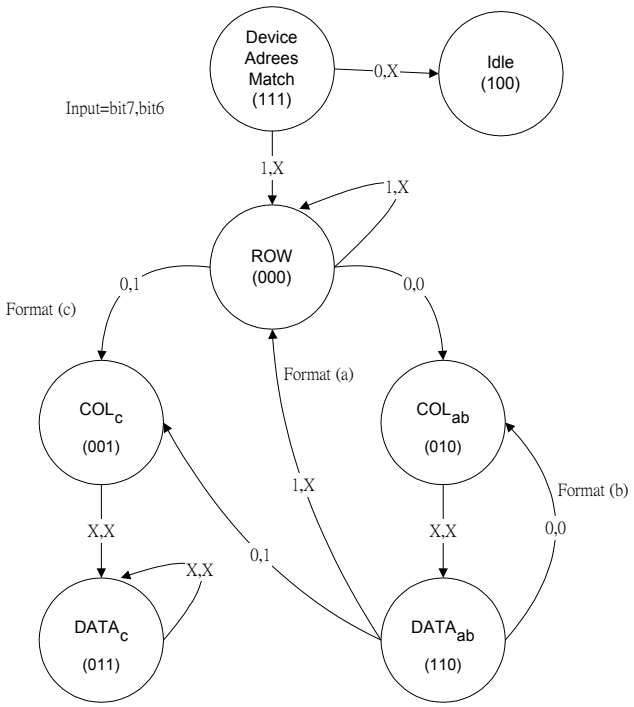
Format (c):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	Data	A	Data	A	Data	A	•••••	P

Where S = START condition
R/W = Read/Write control bit. “1” means READ operation and “0” means WRITE operation.
A = Acknowledge bit. “0” means acknowledge.
P = STOP condition
ROW = Row address byte
COL = Column address byte
Data = Data byte

Format (a) is used when write data in different row and column address.
Format (b) is used when write data in the same row.
Format (c) is suitable for writing data sequentially. The column address will increase automatically.

Format (a)→(b), Format (a)→(c), Format (b)→(a) or Format (b)→(c) is allowed. But Format (c)→(a) and Format (c)→(b) is not allowed.



Transmission Format

	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Format
Address Bytes in Display RAM (Row0~14)	Row	1	0	0	R4	R3	R2	R1	R0	a,b,c
	$Column_{a,b}$	0	0	**D8**	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	**D8**	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
Attribute Bytes in Display RAM	Row	1	0	1	R4	R3	R2	R1	R0	a,b,c
	$Column_{a,b}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	x	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
User Fonts	Row	1	1	0	R4	R3	R2	R1	R0	a,b,c
	$Column_{a,b}$	0	0	**C5**	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	**C5**	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
Control Registers (Row15~16)	Row	1	0	0	R4	R3	R2	R1	R0	a,b,c
	$Column_{a,b}$	0	0	X	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	X	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c

There are two ways to change D8 in format (c) of Row0~Row14 address byte.

- write D8 with column address.
- If the TP bit in Row16 Column3 is “1”, use data byte $FFh to toggle D8. This function can toggle D8 without restarting a new I^2C command. However, the fonts located at $0FFh and $1FFh cannot be displayed in this condition.

Example:

If TP bit is set, write “**S - 7A - 81 - 60 - 58 - 54 - FF- 07 - 09 - 01 - 06 - P”**
The operation is :
(Row1, Column0) <= $158h
(Row1, Column1) <= $154h
Toggle D8
(Row1, Column2) <= $007h
(Row1, Column3) <= $009h
(Row1, Column4) <= $001h
(Row1, Column5) <= $006h

The read format is shown as follow.

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	S	0 1 1 1 1 0 1 1	A	Data	A	Data	A	•••••	P

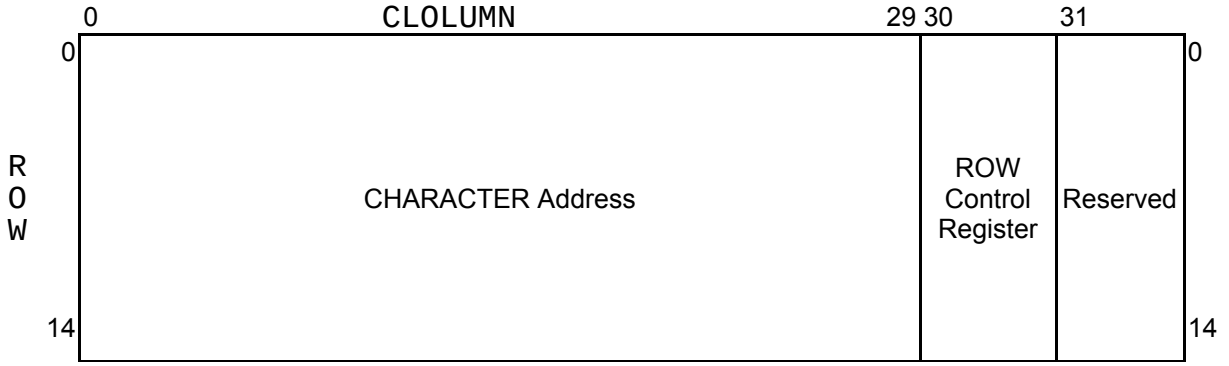
Must use write format first to set row and column address, then follows a read command.

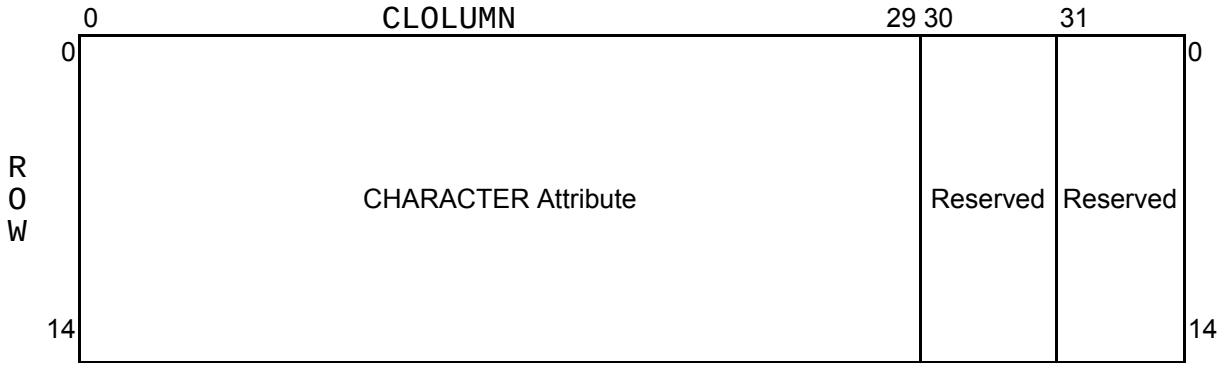
Display RAM and Row Control Register

DISPLAY RAM

The display RAM stores the data to be displayed. Address byte determines display character and attribute bytes determines character background, character color and blinking effect.

The memory location is shown as below.





Address Byte

(Row,Col)	R/W	Bit 8	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0, 0) : (14,29)	W	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA8~CA0 – 9-bit address of Character ROM.

Attribute Byte

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0, 0) : (14,29)	W	--	BG_R/ BOX2	BG_G/ BOX1	BG_B/ BOX0	BLINK	CH_R	CH_G	CH_B

BG_R, BG_G, BG_B – Background color of its corresponding character.

BG_R	BG_G	BG_B	Color
0	0	0	Background
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

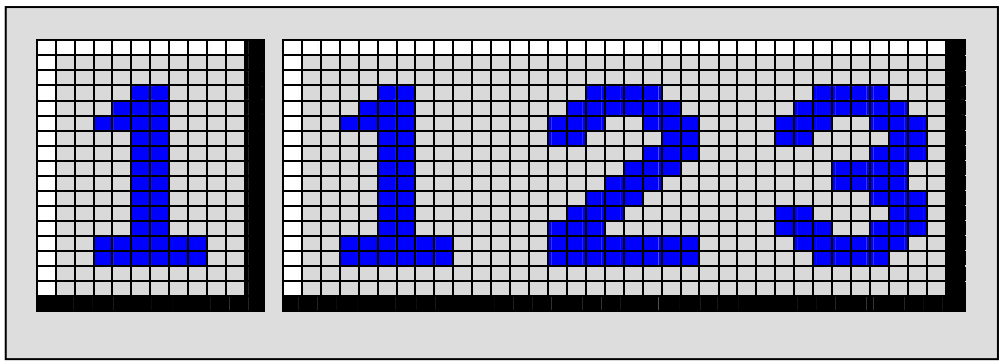
BOX2,BOX1,BOX0 – Character button box format selection of its relative character

BOX2	BOX1	BOX0	Function
0	0	0	Disabled button box.
0	0	1	End of button box.
0	1	0	Middle of button box.
0	1	1	Reserved.
1	0	0	Start depressed button box. More than one character.
1	0	1	Start depressed button box. One character only.
1	1	0	Start raised button box. More than one character.
1	1	1	Start raised button box. One character only.

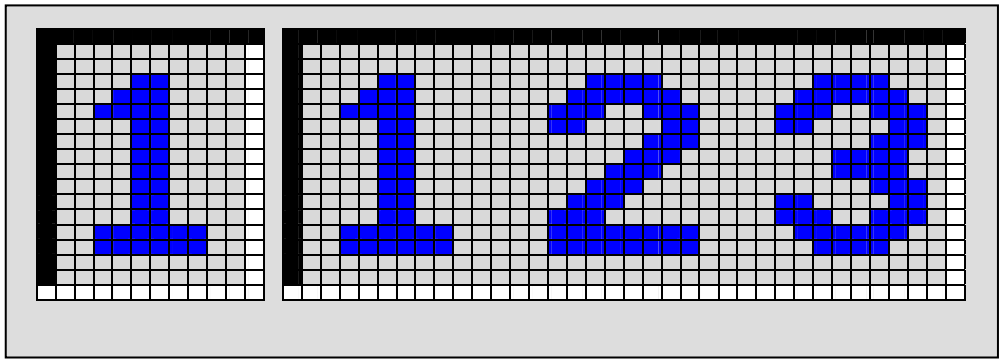
BLINK – Enable blinking effect of its corresponding character. The blinking speed is controlled by BNK1 and BNK0 bits.
CH_R, CH_G, CH_B – Color of its corresponding character.

CH_R	CH_G	CH_B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Example of button box



(BOX2-BOX0)= (1, 1, 1) (1, 1, 0) (0, 1, 0) (0, 0, 1)



(BOX2-BOX0)= (1, 0, 1) (1, 0, 0) (0, 1, 0) (0, 0, 1)

ROW Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0,30) : (14,30)	W	--	--	--	BOX	--	--	DCH	DCW

BOX – "0" : Background color attribute bits (BG_R, BG_G, BG_B) are used.
"1" : Button boxes bits (BOX2, BOX1, BOX0) are used.
DCH – Double Character height
DCW – Double Character width. The character width of even column (column 0, 2, 4, 6, ….) is doubled and the odd column will not display.

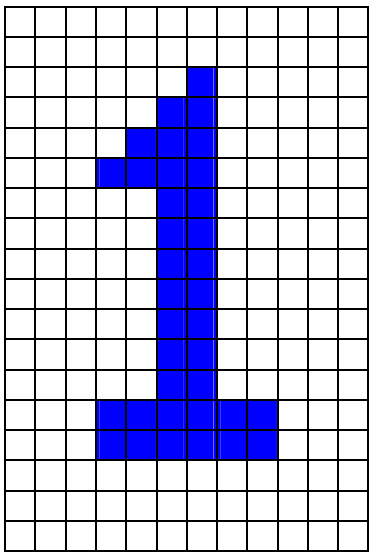
Write data into RAM must enable PLL or external clock. The I^2C interface clock frequency must less than 1/24 pixel clock frequency.

User Fonts RAM

There are 8 user fonts can be stored in the RAM. The RAM structure is shown below. Each font occupies one Row.

Row #	Column #	
	0 1 2 3 4 5 6 ... 34 35	36 37 ... 63
0 1 2 3 4 5 6 7	User Fonts RAM	Reserved

The data structure of RAM font is shown below.



	Column#	Data	Column#	Data
Line0	0	00h	1	00h
Line1	2	00h	3	00h
Line2	4	02h	5	00h
Line3	6	06h	7	00h
Line4	8	0Eh	9	00h
Line5	10	1Eh	11	00h
Line6	12	06h	13	00h
Line7	14	06h	15	00h
Line8	16	06h	17	00h
Line9	18	06h	19	00h
Line10	20	06h	21	00h
Line11	22	06h	23	00h
Line12	24	06h	25	00h
Line13	26	1Fh	27	80h
Line14	28	1Fh	29	80h
Line15	30	00h	31	00h
Line16	32	00h	33	00h
Line17	34	00h	35	00h

Window Control

Window 1 has the highest priority and window 4 is the least. If window overlapping occurs, the higher priority covers the lower and the higher priority color will take over on the overlap window area.

Window 1 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,0)	W	W1RS3	W1RS2	W1RS1	W1RS0	W1RE3	W1RE2	W1RE1	W1RE0
(15,1)	W	W1CS4	W1CS3	W1CS2	W1CS1	W1CS0	W1EN	--	W1SHD
(15,2)	W	W1CE4	W1CE3	W1CE2	W1CE1	W1CE0	W1_R	W1_G	W1_B

W1RS3~0 – Window 1 Row start address
W1RE3~0 – Window 1 Row end address
W1CS4~0 – Window 1 Column start address
W1CE4~0 – Window 1 Column end address
W1EN – Enable Window 1. Default value = 0
W1SHD – Enable the shadow effect of the window 1. Default value = 0
W1_R, W1_G, W1_B – Define the color of window 1

W1_R	W1_G	W1_B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Window 2 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,3)	W	W2RS3	W2RS2	W2RS1	W2RS0	W2RE3	W2RE2	W2RE1	W2RE0
(15,4)	W	W2CS4	W2CS3	W2CS2	W2CS1	W2CS0	W2EN	--	W2SHD
(15,5)	W	W2CE4	W2CE3	W2CE2	W2CE1	W2CE0	W2_R	W2_G	W2_B

Window 3 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,6)	W	W3RS3	W3RS2	W3RS1	W3RS0	W3RE3	W3RE2	W3RE1	W3RE0
(15,7)	W	W3CS4	W3CS3	W3CS2	W3CS1	W3CS0	W3EN	--	W3SHD
(15,8)	W	W3CE4	W3CE3	W3CE2	W3CE1	W3CE0	W3_R	W3_G	W3_B

Window 4 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,9)	W	W4RS3	W4RS2	W4RS1	W4RS0	W4RE3	W4RE2	W4RE1	W4RE0
(15,10)	W	W4CS4	W4CS3	W4CS2	W4CS1	W4CS0	W4EN	--	W4SHD
(15,11)	W	W4CE4	W4CE3	W4CE2	W4CE1	W4CE0	W4_R	W4_G	W4_B

Frame Control Register

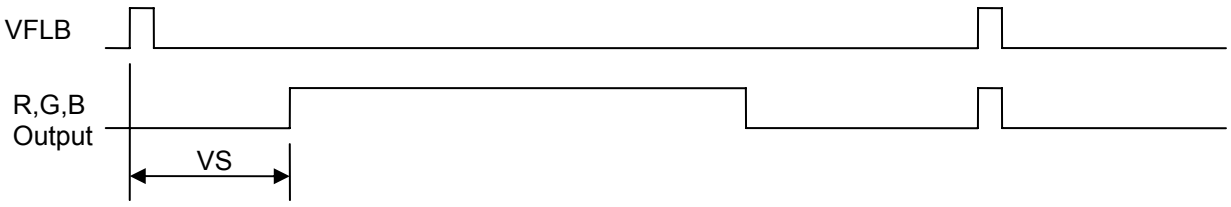
OSD Vertical Starting Position Register

This register controls the vertical displacement from top.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,12)	W	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Default Value = $04h
Minimum value = $01h

VS7~VS0 – Vertical starting position. Each step is 4 Horizontal lines.
Vertical starting position = (VS x 4)+2



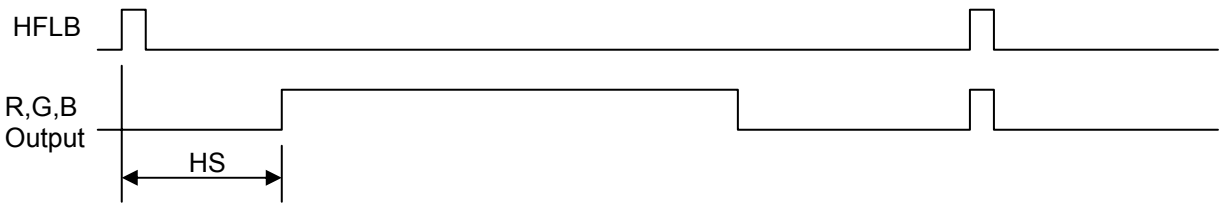
OSD Horizontal Starting Position Register

This register controls the vertical displacement from top.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,13)	W	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0

Default Value = $0Fh
Minimum value = $01h

HS7~HS0 – Horizontal starting position. Each step is 6 dots.
Horizontal starting position = (HS x 6) + 45 dot ± PLL phase error



Character Height Enlargement Register

This register enlarges the character height. The enlargement is done by repeating lines of every row.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,14)	W	--	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Default Value = $00h

CH6~CH0 – Define the enlargement of character height.

CH6	CH5	CH4	CH3	CH2	CH1	CH0	Total Lines	Repeat Line																		
								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	0	x	x	x	x	x	18																		
0	1	0	0	0	0	0	18																		
0	1	0	0	0	0	1	19									v									
0	1	0	0	0	1	0	20					v								v					
0	1	0	0	1	0	0	22			v				v				v				v			
0	1	0	1	0	0	0	26		v		v		v		v		v		v		v		v		
0	1	0	1	1	1	1	33		v	v	v	v	v	v	v	v	v	v	v	v	v	v	v		
0	1	1	0	0	0	0	34		v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	
0	1	1	0	0	0	1	35	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	
1	0	0	0	0	0	0	36	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v
1	0	1	0	0	0	1	53																		
1	1	0	0	0	0	0	54																		
1	1	1	0	0	0	0	70																		
1	1	1	0	0	0	1	71																		

Horizontal Resolution Register

This register controls the pixel clock frequency which is multiplied by HFLB input.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,15)	W	--	HR6	HR5	HR4	HR3	HR2	HR1	HR0

Default Value = $40h

HR6~HR0 – Define the Horizontal resolution (i.e. pixels per horizontal line).

Dot frequency = **{(HR[6:0]x2) + HORR}x 6 x f_{HFLB}**
where HORR is the bit0 of (Row16, Column 3) register

Row-to-Row Spacing Register

This register controls the row-to-row spacing. It adds line(s) below each row.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,16)	W	--	--	--	RSP4	RSP3	RSP2	RSP1	RSP0

Default Value = $00h

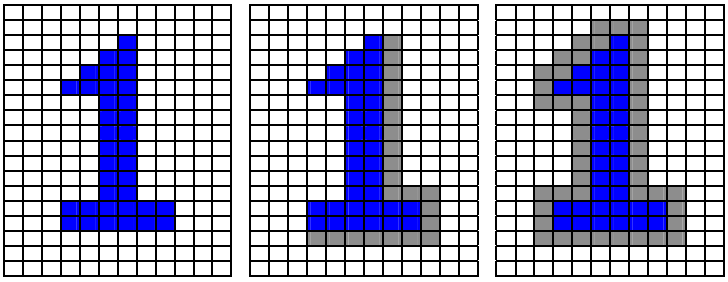
RSP4~RSP0 – Define the line(s) below each row.

Display Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,17)	W	ENOSD	BSEN	SHADW	FADE	BLEND	WINCLR	RAMCLR	FBKGC

Default Value = $00h

ENOSD – Enable OSD Display.
BSEN – Enable bordering and shadowing effect
SHADW – "1" : Shadowing.
"0" : Bordering
FADE – Fade in /Fade out Enable
BLEND – Blending in/out select when FADE bit is set.
WINCLR – Clear all window enable bits. (W1EN ~ W4EN)
RAMCLR – Clear all ADDRESS bytes, BG_R, BG_G, BG_B and BLINK bits.
FBKGC – FBKG control.
"0" : FBKG pin outputs during displaying character or window
"1" : FBKG pin outputs during displaying character only.



Normal **Shadow** **Border**

Output Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,18)	W	TRIC	FSS	--	SELVCL	HPOL	VPOL	VC1	VC0

Default Value = $FCh

TRIC – Tri-state control of ROUT, GOUT, BOUT and FBKG pin.
"1" – When OSD is disabled, these pins will drive low.
"0" – When OSD is disabled, these pins will be in high impedance state

FSS – Font size select.
"0" – 12x16 font size.
"1" – 12x18 font size.

SELVCL – Auto synchronize Hsync with Vsync.
"0" – Disable.
"1" – Enable.

HPOL – "1": Accept positive polarity of Hsync input.
"0" : Accept negative polarity of Hsync input.

VPOL – "1": Accept positive polarity of Vsync input.
"0" : Accept negative polarity of Vsync input.

VC1,VC0 – VCO control
The VCO range is depend on the resistor on Pin2.
When Pin2 connect a 6.2K resistor to ground, the VCO range is shown below.

VC1	VC0	Frequency range
0	0	12MHz ~ 28MHz
0	1	28MHz ~ 56MHz
1	0	56MHz ~ 112MHz
1	1	112MHz ~ 150MHz

Shadow and Border Effect

Shadow Color Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,19)	W	--	--	--	--	--	CS_R	CS_G	CS_B

Default Value = $00h

CS_R, CS_G, CS_B – Define the color of character shadow or border

CS_R	CS_G	CS_B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Full Screen test pattern control register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,20)	W	FSW	--	--	--	--	FSR	FSG	FSB

Default Value = $00h

FSW - Enable full screen test pattern when this bit is set. FBKG pin is forced to high to video
FSR,FSG,FSB – Define the color of full screen test pattern.

FSR	FSG	FSB	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Window Shadow Width Register

This register controls the width of window shadow.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,21)	W	WSW41	WSW40	WSW31	WSW30	WSW21	WSW20	WSW11	WSW10

Default Value = $00h

WSW41,WSW40 – Shadow width of Window 4.
WSW31,WSW30 – Shadow width of Window 3.
WSW21,WSW20 – Shadow width of Window 2.
WSW11,WSW10 – Shadow width of Window 1.
Width = (bit value x 2) + 2 dots

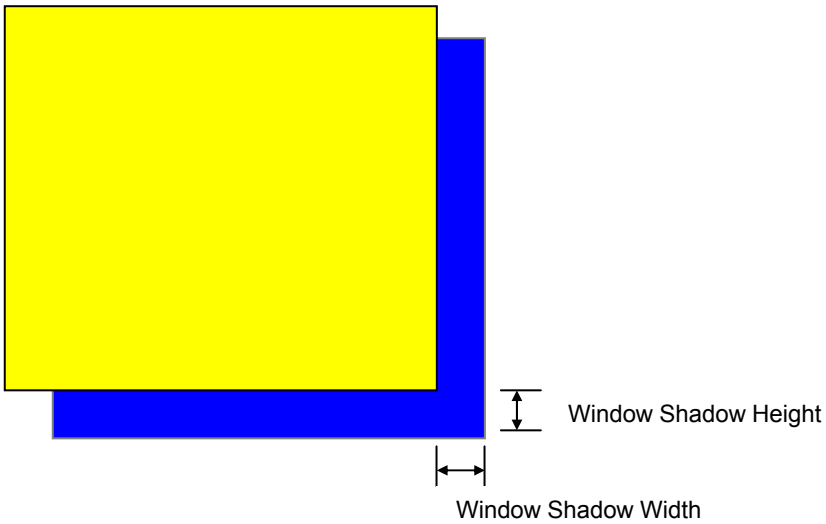
Window Shadow Height Register

This register controls the height of window shadow.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,22)	W	WSH41	WSH40	WSH31	WSH30	WSH21	WSH20	WSH11	WSH10

Default Value = $00h

WSH41,WSH40 – Shadow height of Window 4.
WSH31,WSH30 – Shadow height of Window 3.
WSH21,WSH20 – Shadow height of Window 2.
WSH11,WSH10 – Shadow height of Window 1.
Height = (bit value x 2) + 2 lines



Window Shadow Color Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(16,0)	W	--	W1SR	W1SG	W1SB	--	W2SR	W2SG	W2SB
(16,1)	W	--	W3SR	W3SG	W3SB	--	W3SR	W3SG	W3SB

Default Value = $00h

W1SR, W1SG, W1SB – Define the shadow color of window 1.
W2SR, W2SG, W2SB – Define the shadow color of window 2.
W3SR, W3SG, W3SB – Define the shadow color of window 3.
W4SR, W4SG, W4SB – Define the shadow color of window 4.

WnSR	WnSG	WnSB	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Multi-color Font Selection Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(16,2)	W	--	--	--	--	--	--	UFONT	CFONT

Default Value = $01h

UFONT – “1” : Enable user font. Address $1E8h~$1EFh is user font.
“0” : Disable multi-color font. Address $1E8h~$1EFh is single color font.

CFONT – “1” : Enable multi-color font. Address $1F0h~$1FFh is multi-color font.
“0” : Disable multi-color font. Address $1F0h~$1FFh is single color font.

Fade in/Fade out Effect

The fade-in/fade-out effect can be controlled either in horizontal direction only, vertical direction only or both direction.

Fade in/out Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(16,3)	W	DISH	DISV	FVC1	FVC0	BKS1	BKS0	TP	HORR

Default Value = $00h

DISH : Disable fade in/out horizontal direction. Increment/decrement one column per frame.

DISV : Disable fade in/out vertical direction

FVC1,FVC0 : Fade in/out vertical speed control
- 00 – When BLEND=0, increment/decrement 1 row per frame.
  When BLEND=1, it take 32 frames to finish blending effect
- 01 –When BLEND=0, increment/decrement 1 row every two frame
  When BLEND=1, it take 40 frames to finish blending effect
- 10 –When BLEND=0, increment/decrement 1 row every three frame
  When BLEND=1, it take 48 frames to finish blending effect
- 11 –When BLEND=0, increment/decrement 1 row every four frame
  When BLEND=1, it take 56 frames to finish blending effect

BKS1,BKS0 : Blinking speed select
- 00 – 32 frames on, 32 frames off
- 01 – 40 frames on, 40 frames off
- 10 – 48 frames on, 48 frames off
- 11 – 56 frames on, 56 frames off

TP : Toggle page of character ROM.
- "0" : D8 is not toggled when display RAM address data byte is $FFh of format (c)
- "1" : $FFH can toggle D8. This effects only in display RAM address of format (c) and Row0~Row14.

HORR : Extension bit of horizontal resolution. Please refer Horizontal Resolution Register.

POUT pin Control

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(16,4)	W	POC	--	--	--	PO	--	--	--

Default =00h

POC: POUT pin output control.
- "0" : POUT pin is tri-state.
- "1" : POUT pin is output.

PO: POUT pin output level when POC bit is "1".
- "0" : POUT pin outputs low.
- "1" : POUT pin outputs high.

Clock Source Selection Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(16,5)	W	ENPLL	CLKS	LCD	VREN	CPL	CD2	CD1	CD0

Default Value = $90h

ENPLL – "1" : Enable PLL.
"0" : Disable PLL.

CLKS – Clock select.
"0" : Pixel clock comes from PLL.
"1" : Pixel clock comes from CLKIN pin, i.e. use external clock. This function is for LCD monitor.

LCD – LCD or CRT monitor application select.
"0" : For CRT monitor.
"1" : For LCD monitor.

VREN – VCO resistor enable.
"0" : Turn off internal resistor.
"1" : Turn on internal resistor.

CPL – Control the polarity of CLKIN pin.
If CPL=0, no change of CLKIN polarity.
If CPL=1, reverse the polarity of CLKIN.

CD2~CD0 –
When CLKS=1, CD2~CD0 select the pixel clock delay time from CLKIN pin.

CD[2:0]	Delay Time
000	No delay.
001	Delay 2ns.
010	Delay 4ns.
011	Delay 6ns.
100	Delay 8ns.
101	Delay 10ns.
110	Delay 12ns.
111	Delay 14ns.

Reset

There are two reset sources in WT6805.
(1) Low VDD reset
When VDD lower than 2.6V, a reset will be generated.
(2) Software reset
Write register(16,31) will reset the IC just like power on reset.

Device ID

MCU can identify the ID of WT6805. The ID is $65h when read following register. This function can let MCU know the OSD IC is from Weltrend or not.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,31)	R	0	1	1	0	0	1	0	1

TEST Mode

This register is for factory test only, Must keep $00h in normal operation.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,31)	W	--	--	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0

Default $00h

Register Map

(Row,Col)	R/W	Initial Value	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,0)	W	b'xxxxxxxx	W1RS3	W1RS2	W1RS1	W1RS0	W1RE3	W1RE2	W1RE1	W1RE0
(15,1)	W	b'xxxxx0x0	W1CS4	W1CS3	W1CS2	W1CS1	W1CS0	W1EN	--	W1SHD
(15,2)	W	b'xxxxxxxx	W1CE4	W1CE3	W1CE2	W1CE1	W1CE0	W1_R	W1_G	W1_B
(15,3)	W	b'xxxxxxxx	W2RS3	W2RS2	W2RS1	W2RS0	W2RE3	W2RE2	W2RE1	W2RE0
(15,4)	W	b'xxxxx0x0	W2CS4	W2CS3	W2CS2	W2CS1	W2CS0	W2EN	--	W2SHD
(15,5)	W	b'xxxxxxxx	W2CE4	W2CE3	W2CE2	W2CE1	W2CE0	W2_R	W2_G	W2_B
(15,6)	W	b'xxxxxxxx	W3RS3	W3RS2	W3RS1	W3RS0	W3RE3	W3RE2	W3RE1	W3RE0
(15,7)	W	b'xxxxx0x0	W3CS4	W3CS3	W3CS2	W3CS1	W3CS0	W3EN	--	W3SHD
(15,8)	W	b'xxxxxxxx	W3CE4	W3CE3	W3CE2	W3CE1	W3CE0	W3_R	W3_G	W3_B
(15,9)	W	b'xxxxxxxx	W4RS3	W4RS2	W4RS1	W4RS0	W4RE3	W4RE2	W4RE1	W4RE0
(15,10)	W	b'xxxxx0x0	W4CS4	W4CS3	W4CS2	W4CS1	W4CS0	W4EN	--	W4SHD
(15,11)	W	b'xxxxxxxx	W4CE4	W4CE3	W4CE2	W4CE1	W4CE0	W4_R	W4_G	W4_B
(15,12)	W	b'00000100	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
(15,13)	W	b'00001111	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
(15,14)	W	b'x0000000	--	CH6	CH5	CH4	CH3	CH2	CH1	CH0
(15,15)	W	b'x0000100	--	HR6	HR5	HR4	HR3	HR2	HR1	HR0
(15,16)	W	b'xxx00000	--	--	--	RSP4	RSP3	RSP2	RSP1	RSP0
(15,17)	W	b'00000000	ENOSD	BSEN	SHADW	FADE	BLEND	WINCLR	RAMCLR	FBKGC
(15,18)	W	b'11x11100	TRIC	FSS	--	SELVCL	HPOL	VPOL	VCO1	VCO0
(15,19)	W	b'xxxxx000	--	--	--	--	--	CS_R	CS_G	CS_B
(15,20)	W	b'0xxxx000	FSW	--	--	--	--	FSR	FSG	FSB
(15,21)	W	b'xxxxxxxx	WSW41	WSW40	WSW31	WSW30	WSW21	WSW20	WSW11	WSW10
(15,22)	W	b'xxxxxxxx	WSH41	WSH40	WSH31	WSH30	WSH21	WSH20	WSH11	WSH10
(15,31)	W	b'xx000000	--	--	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
(16,0)	W	b'x000x000	--	W1SR	W1SG	W1SB	--	W2SR	W2SG	W2SB
(16,1)	W	b'x000x000	--	W3SR	W3SG	W3SB	--	W3SR	W3SG	W3SB
(16,2)	W	b'xxxxxx01	--	--	--	--	--	--	UFONT	CFONT
(16,3)	W	b'000000x0	DISH	DISV	FVC1	FVC0	BKS1	BKS0	TP	HORR
(16,4)	W	b'0xxx0xxx	POC	--	--	--	PO	--	--	--
(16,5)	W	b'10010000	ENPLL	CLKS	LCD	VREN	CPL	CD2	CD1	CD0
(15,31)	R	b'01100101	0	1	1	0	0	1	0	1

Electrical Characteristics

D.C Characteristics (VDD=5.0V±5%, Ta=0-70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75	5	5.25	V
$V_{IH,I2C}$	SDA and SCL Input High Voltage		$0.7V_{DD}$	--	V_{DD}+0.3	V
$V_{IL,I2C}$	SDA and SCL Input Low Voltage		-0.3	--	$0.3V_{DD}$	V
$V_{IH,FLB}$	HFLB and VFLB Input High Voltage		2.0	--	V_{DD}+0.3	V
$V_{IL,FLB}$	HFLB and VFLB Input Low Voltage		-0.3	--	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -6mA	4	--	V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 6mA	0	--	0.4	V
I_{IL}	Input Leakage Current	0V <V_{IN} < V_{DD}	-10	--	10	μA
I_{DD}	Operating Current	Dot rate=100MHz, no load	--	TBD	25	mA
I_{STB}	Standby Current	Disable PLL	--	0.1	1	mA
V_{RESET}	Low V_{DD} reset voltage		2.4	2.6	2.8	V

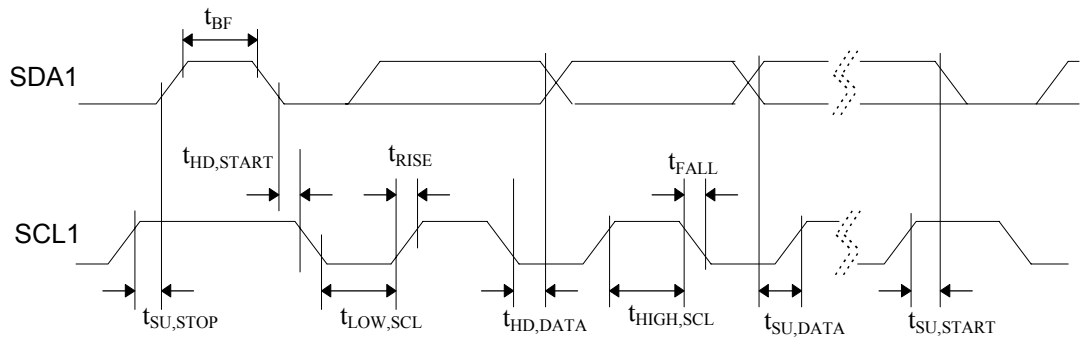
A.C Characteristics (VDD=5.0V, Ta=0-70°C)

R,G,B and FBKG pins

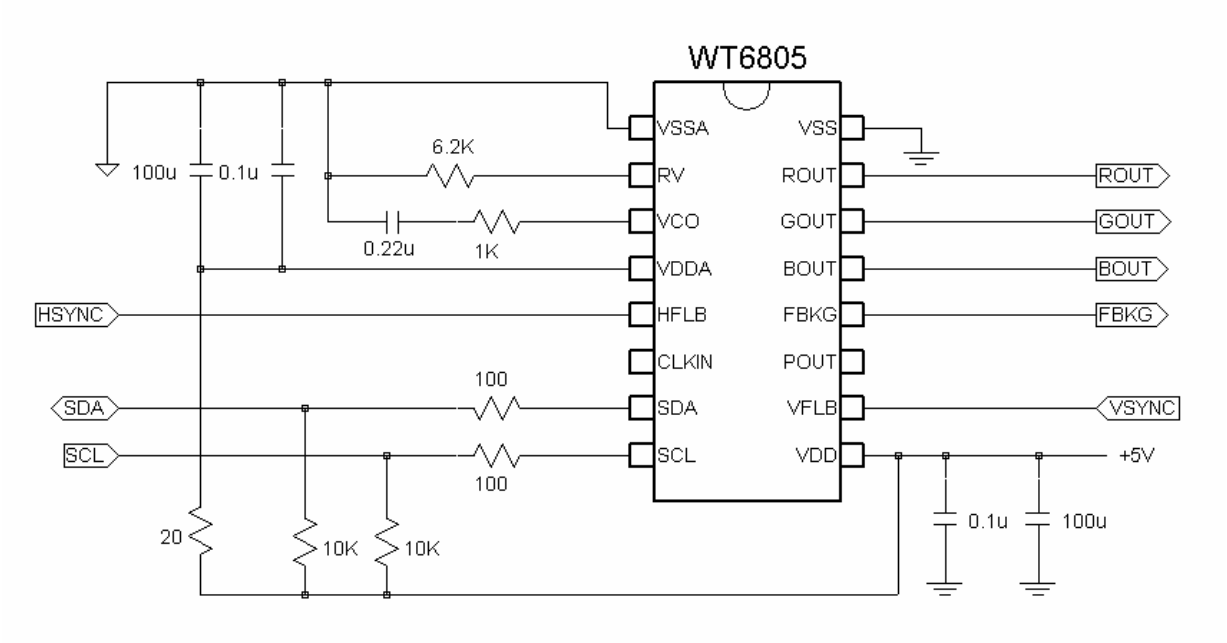
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{RISE}	Rise time (ROUT,GOUT,BOUT and FBKG pins)	Cload=30pF	-	2	3.5	ns
T_{FALL}	Fall time (ROUT,GOUT,BOUT and FBKG pins)	Cload=30pF	-	2	3.5	ns
F_{HFLB}	HFLB Input Frequency		10	-	150K	Hz
F_{VFLB}	VFLB Input Frequency		4	-	2047	H lines
F_{PLL}	PLL Frequency		6	-	150	MHz

I2C Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL input clock frequency	0	-	100	kHz
t_{BF}	Bus free time	2	-	-	us
$t_{HD,START}$	Hold time for START condition	1	-	-	us
$t_{SU,START}$	Set-up time for START condition	1	-	-	us
$t_{HIGH,SCL}$	SCL clock high time	1	-	-	us
$t_{LOW,SCL}$	SCL clock low time	1	-	-	us
$t_{HD,DATA}$	Hold time for DATA input	0	-	-	ns
	Hold time for DATA output	80	-	-	ns
$t_{SU,DATA}$	Set-up time for DATA input	20	-	-	ns
	Set-up time for DATA output	100	-	-	ns
$t_{RISE,I2C}$	SCL and SDA rise time	-	-	1	us
$t_{FALL,I2C}$	SCL and SDA fall time	-	-	300	ns
$t_{SU,STOP}$	Set-up time for STOP condition	1	-	-	us



TYPICAL APPLICATION CIRCUIT



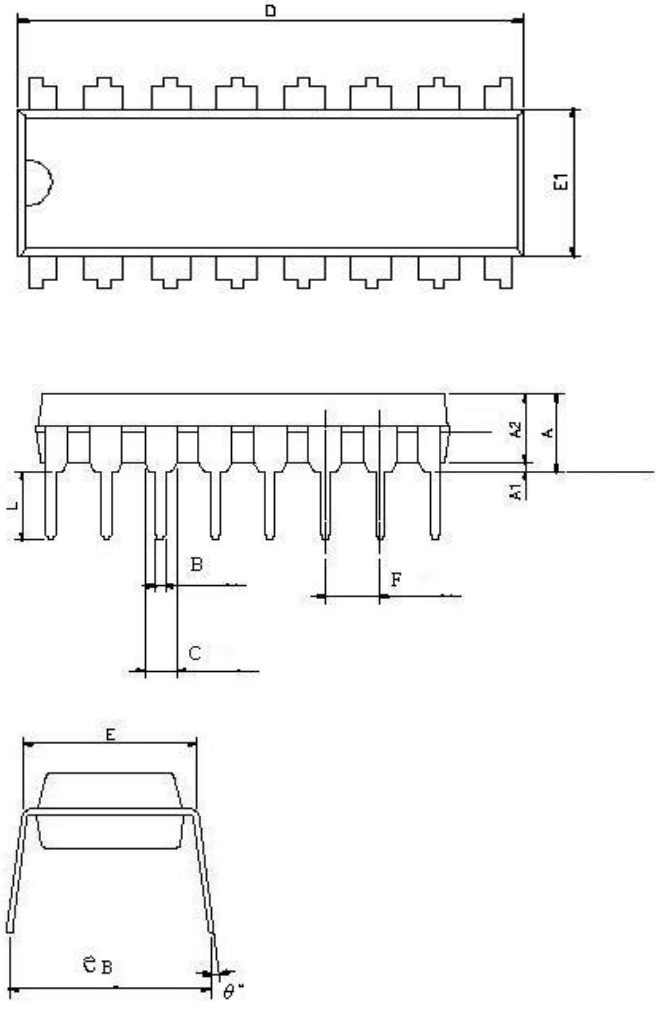
The circuit above is for reference only. Component value may vary in different system application.

PACKAGE OUTLINE

PDIP 16-pin package

Package type：16 Pin DIP 300mil

UNIT : INCH



SYMBOLS	MIN	NOR	MAX
A			0.210
A1	0.015		
A2	0.125	0.130	0.135
B		0.018	
C		0.060	
D	0.735	0.755	0.775
E		0.300 BSC	
E1	0.245	0.250	0.255
F		0.100	
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15