WT7161R
Multi-Mode Flyback PWM Controller

Product Spec.

Rev. 0.7

August 2022

Disclaimers

Right to make change –
This document provides technical information for user. Weltrend Semiconductor, Inc. reserves the right to make change without further notice to any products herein.

Table of Contents

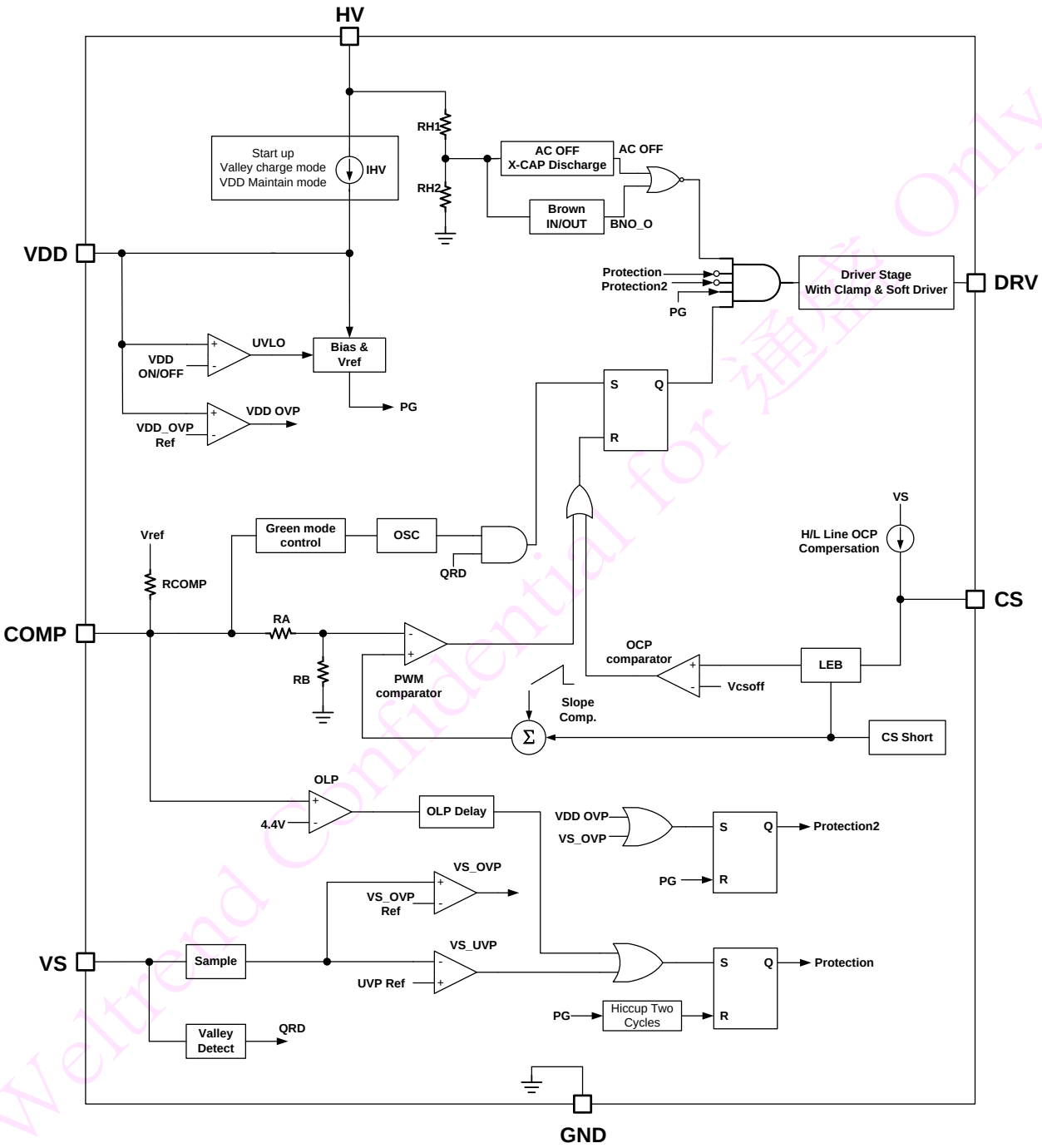
1. General Description

The WT7161R is a high performance multi-mode (CCM/Valley Switching) Flyback PWM controller. It is specifically designed to work with USB PD controller to provide a total solution for USB PD or a programmable power adapter. It minimizes the components counts and is available in a SOP-8 package. The controller operates in continuous Current Mode (CCM) during heavy load and operates in discontinuous conduction mode with valley switching during light load. The WT7161R helps to improve the overall efficiency and optimize the product performance. The controller provides with important protection features, such as Brown In/Out, Vo UVP, VDD OVP, OLP, OCP and Output Short Circuit Protection.

2. Features

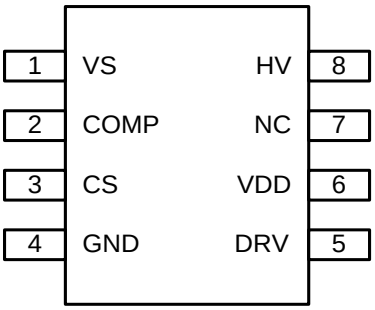
- No Load Power Consumption < 30mW
- 700V Ultra HV Start-up Current
- Ultra HV Valley Charge Mode (VCM) for Wide Output Voltage Operation
- Optimized for Wide Output Voltage
  - OCP Compensation with Adjustable Line Compensation
  - Adaptive Green Mode Control
  - No External VDD Linear Regulator Circuit
  - Only One VDD Auxiliary Winding
- CCM/DCM/Valley-Switching Multi-Mode Operation
- DRV pin with Soft Driver to Reduce EMI Noise
- Built-in X-Cap Discharge Function
- Internal Soft-Start Function
- Protection:
  - Brown In/Out Protection on HV Pin
  - Output Under Voltage Protection (VS_UVP)
  - Output Over Voltage Protection (VS_OVP)
  - VDD Over Voltage Protection (VDD_OVP)
  - Open Loop Protection (OLP) when Feedback Loop Open
  - Over Current Protection (OCP)
  - Internal Over Temperature Protection
  - CS Pin Open/Short Protection
- Green Package: 8-pin SOP

3. Block Diagram



4. Pin Configuration

8-pin SOP



4.1 Pin Description

Pin Number SOP8	Pin Name	Description
1	VS	This pin connects to a voltage divider between an auxiliary winding and detects the core demagnetization to have the controller operated at the valley switching for DCM. This pin provides the output over-voltage and under-voltage detection.
2	COMP	This pin connects to a Photo-coupler collector and adjusts the peak current set point. By a resistor between VDD and COMP pin, the brown in/out detect thresholds can be changed.
3	CS	The current sense pin monitors and control the primary peak current.
4	GND	Ground
5	DRV	This pin drives the gate of external MOSFET switch.
6	VDD	This pin is connected to an external auxiliary voltage and supplies the controller.
7	NC	
8	HV	Connect this pin to Line/ Neutral of AC main voltage through a resistor and two diodes to provide the startup current for the controller. The HV pin also protects the converter when the input voltage lowers than the BNO level.

5. Function Description

The WT7161R is a high performance multi-mode (CCM/Valley Switching) Flyback PWM controller. It is specifically designed to work with the USB PD controller or programmable power adapter controller, to provide a total solution. For the wide output voltage application, the WT7161R features many new innovations, including UHV valley tracking charge mode, adaptive OCP compensation and adaptive green mode control. Its major features are described as below.

5.1 Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The WT7161R is implemented with a high-voltage startup circuit for fast start-up functions and reduce power dissipations, as shown in Fig. 5.1. At startup, the high-voltage current source sinks current from AC Line and Neutral to provide startup current and charge the capacitor C1 which connected to VDD. At the startup transient, the HV current will charge VDD capacitor until this VDD voltage reaches the UVLO (ON) threshold. As VDD trips UVLO (OFF), HV pin will recharge VDD capacitor till VDD voltage rise back to UVLO (ON) again. The resistor RHV connected in series with HV pin is recommended in the range between 100Ω and 510Ω. Besides, recommended that the VDD capacitor C1 connected with VDD pin is in the range from 22μF to 47μF. It is important to note that it is not allowed to connect HV pin to any dc voltage. (e.g.: directly to bulk capacitor)

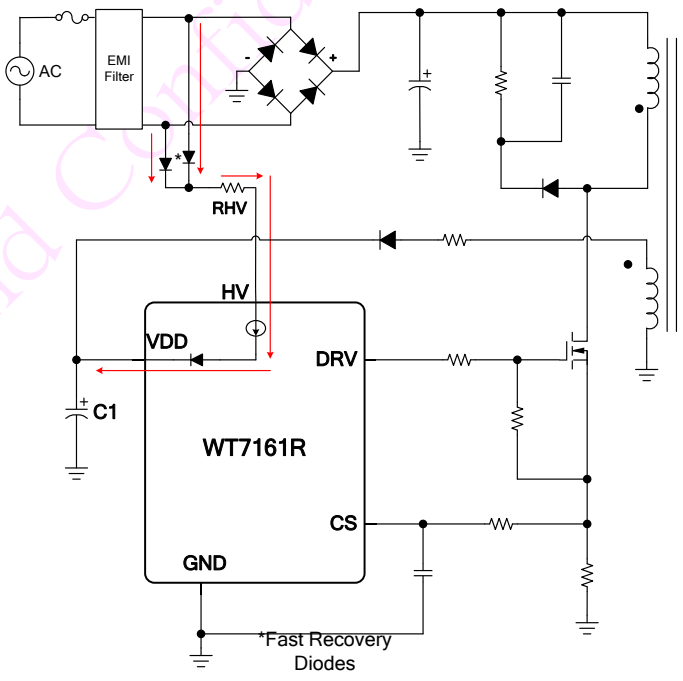


Fig. 5.1

5.2 Brown In/Out Protection and Setting

The WT7161R features brown in/out protection on HV pin. When HV pin voltage (VHV) goes above brown-in threshold (BNI) and VDD > VDD_BNO (13.5V), the controller can start immediately. Otherwise, the controller actually starts the next time VDD reaches UVLO (ON), as shown in Fig. 5.2. When VHV goes below brown out threshold (BNO) for more than a de-bounce time, the controller will stop switching. The WT7161R has four brown in/out detect thresholds, which set by a resistor between VDD and COMP pin. The setting table 5.1 is shown as below.

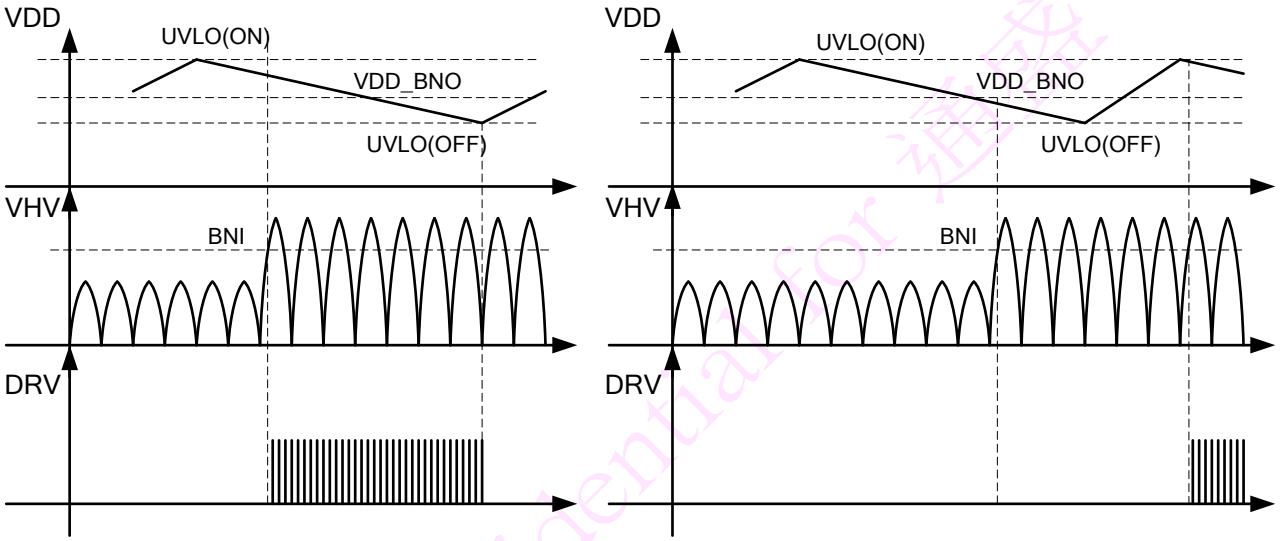


Fig. 5.2

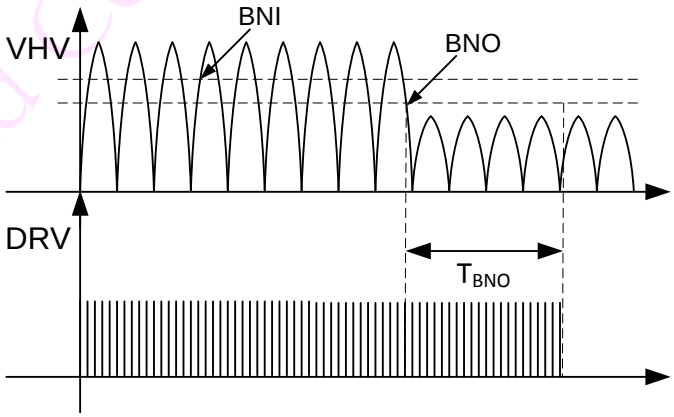


Fig. 5.3

Table 5.1

BNI / BNO	VDD to COMP Resistance (Tolerance<±1%)
160 / 144 V_{rms}	2MΩ
140 / 126 V_{rms}	3.9MΩ
70 / 63 V_{rms}	8MΩ
80 / 72 V_{rms}	NC

5.3 HV Valley Charge Mode & VDD Maintain Mode

For wide VOUT range application, the WT7161R provides the HV pin valley charge mode (VCM). When VDD voltage is below the VDD_VCM (OFF) and HV voltage is below ON threshold (near the valley region), HV valley charge mode will be enabled. The HV VCM will supply current to keep the VDD voltage between VDD_VCM (ON) and VDD_VCM (OFF). Therefore, the WT7161R can reduce additional VDD LDO regulator circuits to have a better total BOM cost.

The VDD maintain mode can also turn on and turn off the HV current to maintain the VDD voltage no matter how high the HV voltage is. However, the HV current will be limited to 4mA (Typical) to protect the HV device.

5.4 HV X-Cap Discharge Function

In general, a discharging resistor is placed across X-capacitor to meet safety requirement. This component requires to be discharged in less than 1 second after AC line is disconnected. To eliminate the significant power loss from this discharging resistor, the IC applies the patent technology to discharge X-Cap's energy through HV current source when AC line is disconnected. By applying this technology, the system can easily pass the safety test without discharging resistor. When the X-Cap discharge function is enabled, the DRV will be off to stop the switching of power circuit. The IC will restart after the four VDD hiccup cycles.

5.5 Multi-Mode Operation for High Efficiency

The WT7161R is a high performance multi-mode (CCM/Valley Switching) Flyback PWM controller. The controller could operate in CCM and DCM with valley switching. As the load decreases, the controller enters green mode with valley switching. At zero load or very light load conditions (V_{COMP} < Burst mode voltage), the DRV pin of the WT7161R will be disabled immediately under such condition, enhancing power saving. The WT7161R helps to improve the overall efficiency and optimize the product performance.

5.6 Open Loop Protection (OLP)

The WT7161R has an open loop protection function. An internal circuit detects the V_{COMP} level, when the V_{COMP} is larger than an OLP threshold level and continues over OLP delay time, the protection will be activated and then turn off the DRV output to stop the switching of power circuit. The IC will restart after two VDD hiccup cycles.

5.7 Gate Clamp/Soft Driving

Driver output is clamped by an internal clamping circuit to prevent from undesired over-voltage gate signals to reduce the current consumption of the controller. The WT7161R also has soft driving function to minimize EMI.

5.8 Output OVP and UVP on VS Pin

The WT7161R provides the OVP and UVP multi-protection by using VS pin, as shown in Fig. 5.5. It samples the auxiliary winding voltage via the divided resistors after a blanking time when DRV off. The auxiliary winding voltage is reflected to secondary winding and therefore the voltage on the VS pin is proportional to the output voltage. The sampling voltage level, VS1, is used for OVP and UVP. If VS1 exceeds the 3.5V, the VS OVP circuit switches the power MOSFET off. If VS1 declines below 0.375V for over the 25ms, the UVP protection will be activated to turn off the DRV and protect the circuit from damage due to output short condition. The UVP will be disabled when IC enter the burst mode operation. The equation of VS1 is shown as below:

$$VS1 = VAUX \times \frac{R2}{R1+R2} = Vout \times \frac{Naux}{Ns} \times \frac{R2}{R1+R2}$$

$$R2 = \frac{R1}{\frac{Vout_{\_OVP}}{3.5} \times \frac{Naux}{Ns} - 1}$$

Where Naux is the turns of VDD winding, Ns is the turns of secondary winding.

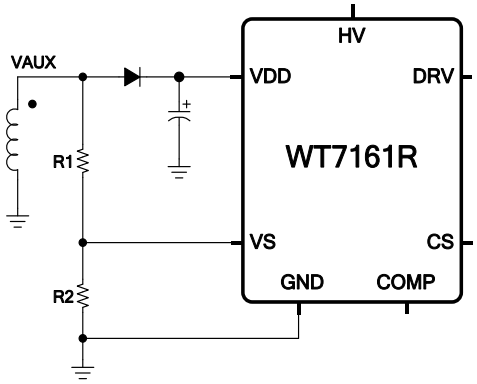


Fig. 5.4

5.9 Over Current Compensation

To compensate over current protection under different input voltage, an offset voltage is added to the CS signal by an internal current source, IOCP and an external resistor, Rcs, in series between the sense resistor, RS, and the CS pin, as shown in Fig. 5.5. Different values of resistors in series with the CS pin may adjust the amount of compensation. The value of IOCP depends on the clamping current, IVS, of VS pin when the MOSFET is turned on. The clamping current is proportional to the input voltage. The relationship between IOCP and IVS is shown as Fig. 5.6. The equation of IVS and R1 are decreased as:

$$IVS = \frac{V_{AUX}}{R1} = \frac{Vin \times N_{AUX} / N_P}{R1}$$

The WT7161R also could adjust down the current limit (Vcsoff) if it detects a lower output voltage by detect the VS pin voltage.

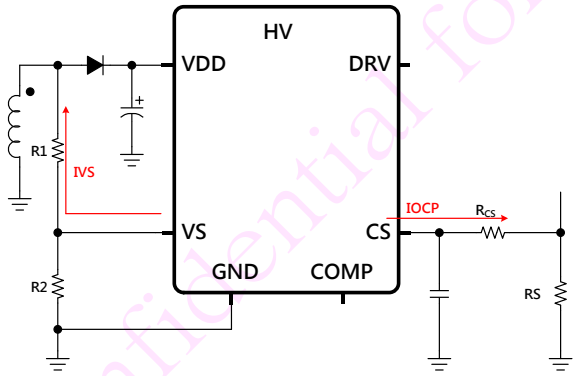


Fig. 5.5

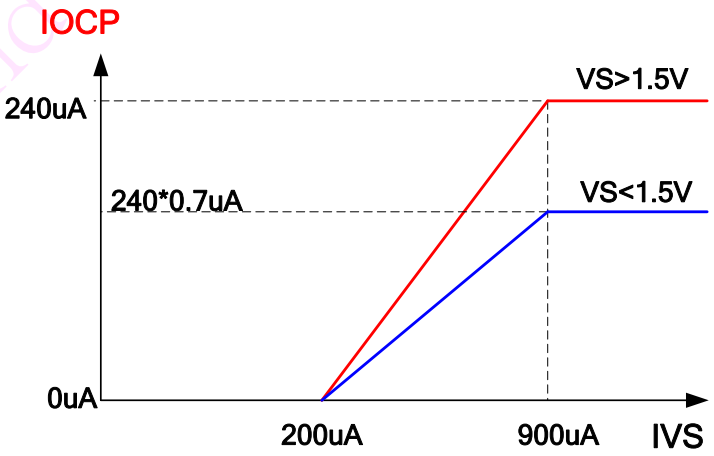


Fig. 5.6

Table 5.2

VCS_OFF_1	5-20V OCP	VS>0.7	0.66V
VCS_OFF_2	3V OCP	VS<0.7	0.60V

5.10 Adaptive Green Mode Control

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency at light load. Fig. 5.7 shows the characteristics of the switching frequency vs. the COMP pin voltage (V_{COMP}). The system stability is different for wide range VOUT range application. The WT7161R would adjust green mode curve automatically to ensure the system stability for different VOUT operation. When VS pin voltage < 1.5V, the green mode curve period will be increased to improve system stability for lower output voltage, as shown in Fig. 5.7.

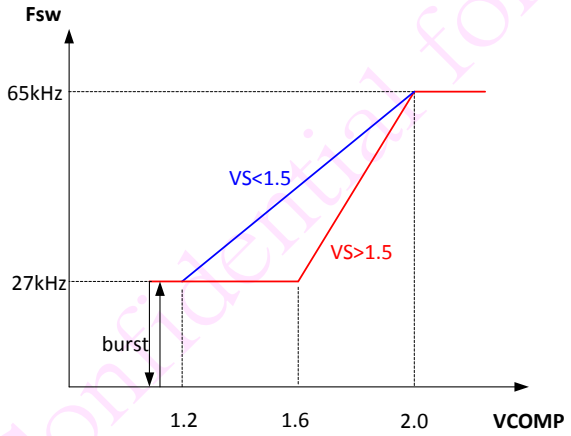


Fig. 5.7

5.11 CS Pin Short Protection

The WT7161R also provides CS pin short protection to protect system. When CS pin is short to GND or the CS signal is not detected, DRV will be turned off after a delay time and system will be shutdown. By the way, the CCM operation will be disabled in the CS short protection to reduce the voltage stress on the power MOSFET. It is recommended that the ratio of the input voltage, the current sense resistor and the transformer must be limited by the following equation:

$$\frac{Vin \times RS}{Lp} > 25000$$

Where Vin is the input voltage, RS is the current sense resistor; LP is the primary magnetizing inductance of the transformer. By the way, the CCM operation will be disabled in the CS short protection to reduce the voltage stress on the power MOSFET.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
HV Pin	-0.3	700	V
VDD to GND	-0.3	41	V
DRV to GND	-0.3	Internal clamp	V
VS, COMP, CS,	-0.3	6.5	V
VS (Transient Time ≦1μs)	-1	6.5	V
Power Dissipation, SOP-8 at Ambient Temperature = 85℃		0.25	W
Junction Temperature		150	℃
Lead Temperature (Soldering, 10 sec.)		260	℃
Storage Temperature Range	-65	150	℃
MM ESD (except HV Pin)	300		V
HBD ESD (except HV Pin)	3		kV
MM ESD (HV Pin)	300		V
HBD ESD (HV Pin)	1		kV

Note: Maximum ratings applied to the device are individual stress limit value. Stresses above those listed may cause permanent damage and reliability may be affected.

6.2 Recommended Operating Parameters

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
AC Input Voltage Range	Vac		63		264	Vrms
V_{DD} Capacitor	C_{VDD}		22		47	μF
HV Pin Resistor	R_{HV}		100		510	Ω
COMP Pin Capacitor	C_{COMP}		1		10	nF
Operating Junction Temperature	T_J		-40		125	℃

Notes:

- Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
- The small signal components should be placed to IC pin as possible.

- It is essential to connect VDD pin with a SMD ceramic capacitor (0.1 μF~1.0 μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.

6.3 Thermal Resistance

Package	Parameter		Min.	Typ.	Max.	Units
8-pin SOP	θ_{JA}	Thermal Resistance (Junction to Air)		150		°C /W
	θ_{JC}	Thermal Resistance (Junction to Case)		39		°C /W

6.4 Protection Type Table

Protection	WT7161R
VDD OVP	Auto
VS OVP	Auto
OLP	Auto (Hiccup Two Cycles)
VS UVP	Auto (Hiccup Two Cycles)
CS Pin Short Protection	Auto

6.5 DC Electrical Characteristics

(VDD=15V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High Voltage Startup (HV PIN)						
HV Startup Current	IHV_ST_0	HV=100V, VDD=0V		1		mA
HV Startup Current	IHV_ST_1	HV=100V, VDD=15V		2.7		mA
HV Pin Brown IN Threshold	VHV_BNI	VCC to COMP=NC	105	113	121	V_{DC}
HV Pin Brown OUT Threshold	VHV_BNO	VCC to COMP=NC	95	102	109	V_{DC}
Brown OUT De-bounce Time	TBNO_OUT	(Note1)		64		ms
X-Cap Discharge De-bounce Time	THV_DIS	(Note1)		64		ms

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage (VDD PIN)						
VDD Turn-on Threshold	VDD_ON		16	17	18	V
VDD Turn-off Threshold	VDD_OFF		6.5	7	7.5	V
Operating Current	IVDD_0	COMP=0V		500		μA
Operating Current	IVDD_3	DRV=1nF, COMP=3V, VS=2V		2.0		mA
HV Valley Charge Mode ON	VDD_VCM_ON	(Note1)		10		V
HV Valley Charge Mode OFF	VDD_VCM_OFF	(Note1)		12		V
VDD Maintain Mode ON Level	VDD_Main	(Note1)		8.0		V
VDD Maintain Mode OFF Level	VDD_Main_OFF	(Note1)		11		V
Power Down Reset Level (PDR)	VDD_PDR	Latch Reset Level (Note1)		6.3		V
VDD OVP	VDD_OVP		37.5	39	40.5	V
VDD OVP De_bounce Time				4		cycle
Protection Current_Auto	IPROT_A			320		μA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Loop Compensation (COMP PIN)						
COMP Open Level	V_{COMP}_OPEN		5	5.3	5.6	V
Open Loop Trip Threshold	VOLP		4.2	4.4	4.6	V
COMP Short Current	ICOMP_0V		170	200	230	μA
AV For CS/COMP		RA/RB, (Note1)		3		
Burst ON Threshold	Burst_ON			1.1		V
Burst Hys.	Burst_Hys			0.1		V
Open Loop Delay Time	TOLP	after start-up		80		ms

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Internal Oscillator						
CCM Switching Frequency	FS_CCM	V_{COMP}=3V	62	65	68	kHz
CCM Jitter Range	FJITTER	V_{COMP}=3V		±5.2		kHz
Green Mode Frequency	FGREEN		22	27		kHz
Maximum Duty	DMAX	(Note1)	70	75	80	%

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Current Sense (CS PIN)						
CS OFF Threshold,	VCS_OFF	VS>0.7	0.64	0.66	0.68	V
Slope Compensation	VSLOPE	0% to 75% (Note1)		300		mV
Leading Edge Blanking	TLEB	For OCP		350		ns
Soft Start	TSS1	(Note1)		5		ms

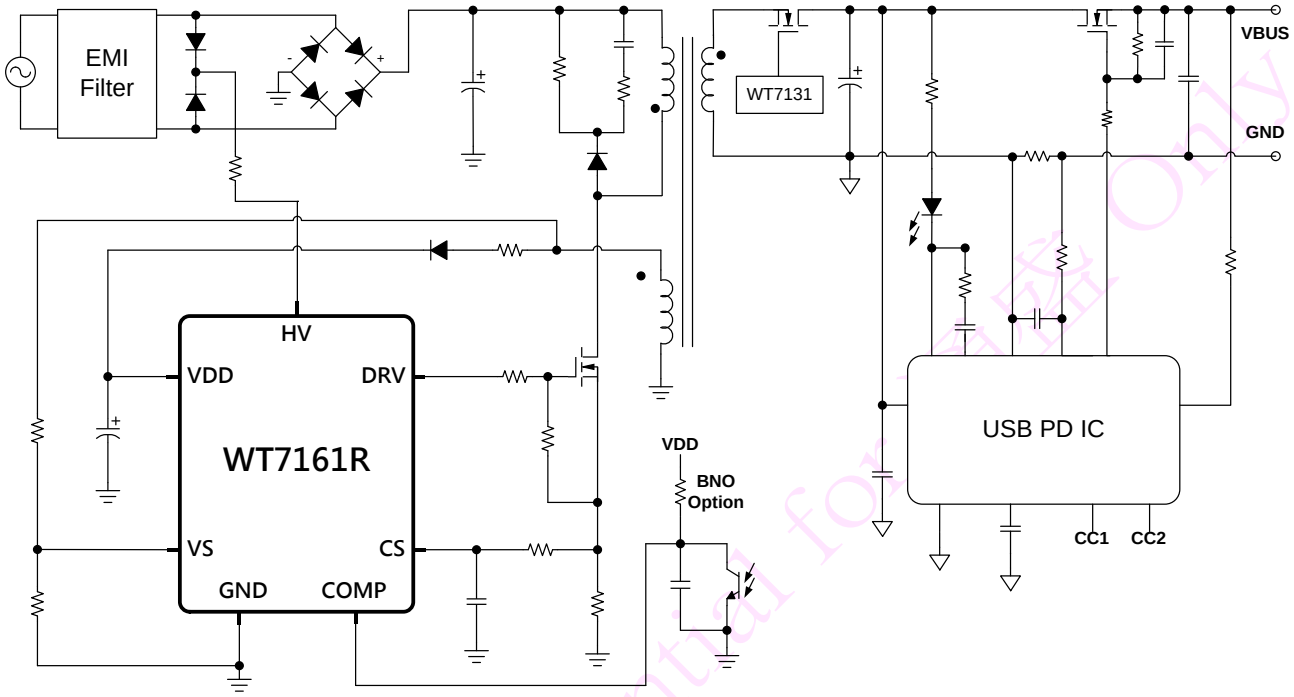
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
MOSFET Driver (DRV PIN)						
DRV High Level	VOH	RL=1 kΩ	9.5		VDD	V
DRV Low Level	VOL	Io=40mA	0		1	V
DRV Clamp Level	VOC			11		V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Valley Switching (VS PIN)						
VS OVP Threshold	VS_OVP			3.5		V
VS_UVP Detection	VS_UVP		0.34	0.375	0.42	V
VS_UVP Delay Time		(Note1)		25		ms
Time Out	TO	(Note1)		15		µs
		@CS short		100		µs

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Internal Thermal Shutdown						
Thermal shutdown temperature	T_{SD_L}	(Note1)		150		℃
Thermal shutdown hysteresis	T_{SD_H}	(Note1)		10		℃

Note 1. Guaranteed by design.

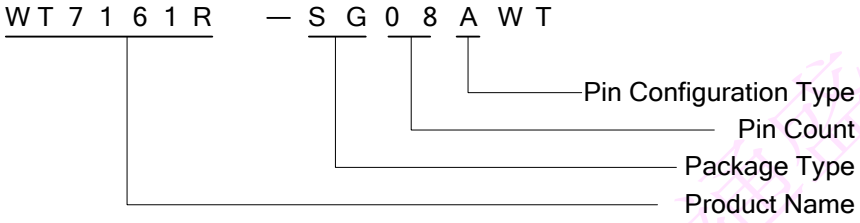
7. Simplified Application Circuit



8. Ordering Information

Part Number	Package Type	Ordering Number	Tapping (EA/Reel)
WT7161R	SOP-8	WT7161R-SG08AWT	4000

Example



Top Marking

8-pin SOP Top Marking

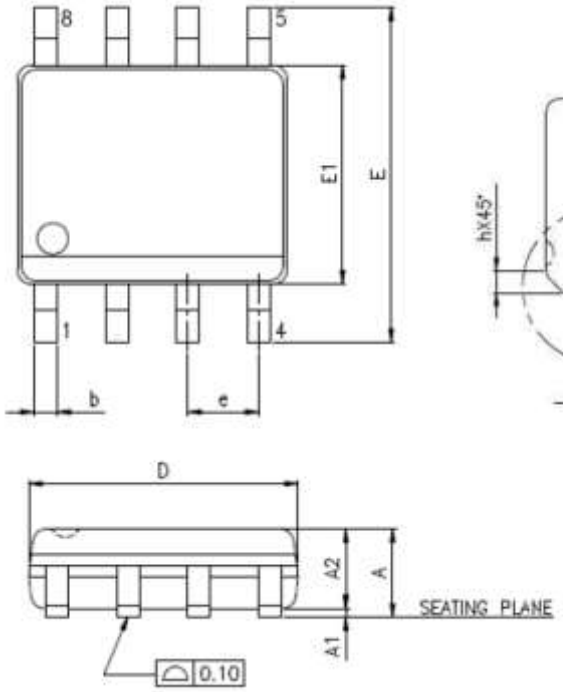
□: Date Code

X: Production Tracking Code

9. Package Information

9.1 Package Dimensions

8-pin SOP



All dimensions shown in mm

SYMBOL	MIN.	MAX.
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

Notes:

1. JEDEC outline: MS-012 AA REV.F
2. Dimension “D” does not include mold flash, protrusions or gate burrs mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

10. Revision History

Version	History	Date
0.1	Initial issue	August 2018
0.2	Update DC Electrical Characteristics	September 2018
0.3	Update Part Number	October 2018
0.4	Update DC Electrical Characteristics	February 2019
0.5	Update CH1, CH2, CH5.1, CH5.11, and CH7 (Application Circuit)	July 2020
0.6	Update CH2, CH5.8, CH6.5, and CH7 (Application Circuit)	December 2021
0.7	Update CH2, CH5.9, CH5.10 ,CH6.1, CH6.2 and CH6.5	August 2022